Impact of Mechanical Stress on the Electrical Stability of Flexible a-Si TFTs

by

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Abstract

The development of functional flexible electronics is essential to enable applications such as conformal medical imagers, wearable health monitoring systems, and flexible light-weight displays. Intensive research on thin-film transistors (TFTs) is being conducted with the goal of producing high-performance devices for improved backplane electronics. However, there are many challenges regarding the performance of devices fabricated at low temperatures that are compatible with flexible plastic substrates. Prior work has reported on the change in TFT characteristics due to mechanical strain, with especially extensive data on the effect of strain on field-effect mobility. This thesis investigates the effect of gate-bias stress and elastic strain on the long-term stability of flexible low-temperature hydrogenated amorphous silicon (a-Si:H) TFTs, as the topic has yet to be explored systematically.

An emphasis was placed on bias-stress measurements over time in order to obtain information on the physical mechanisms of instability. Drain current was measured over various intervals of time to track the degradation of devices due to metastability, and results were then compared across devices of various sizes under tensile, compressive, and zero strain. Transfer characteristics of the TFTs were also measured under the different conditions, to allow for extraction of parameters that would provide insight into the instability mechanisms. In addition to parameter extraction, the degradation and recovery of TFT output current was quantitatively compared for various bias-stress times across the different levels of strain. Finally, the instability mechanisms are modelled with a Markov system to further examine the effect of strain on long-term TFT operation.

From the analysis of results, it was found that shallow charge trapping in the dielectric is the main mechanism of instability for short bias stress times, and did not seem to

be greatly affected by strain. For longer bias stress times of over 10000 seconds, defect creation in the a-Si:H becomes a more significant contributor to instability. Both tension and compression increased defect creation compared to TFTs with zero applied strain. Compression appeared to cause the greatest increase in the rate of defect formation, likely by weakening Si-Si bonds in the a-Si:H. Tension appeared to cause a less significant increase, possibly due to a strengthening of some proportion of the Si-Si bonds caused by the slight elongation of bond length or because the applied tension relieves intrinsic compressive stress in a-Si:H film. A longer conduction path and greater dielectric area appears to increase the bias-stress and strain-related effects. Therefore reducing device size should increase the reliability of flexible TFTs.

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Dedication

For the pursuit of knowledge.

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Chapter 1

Introduction

1.1 Applications of flexible TFTs

Flexible large-area electronics are an area of increasing research interest, and offer a wealth of potential applications. Flexible films have the inherent advantage of being lightweight and immune to shattering, making them well-suited for implementation in portable devices. Flexibility also provides new freedoms in terms of design by enabling the development of conformal or flexible displays and sensors. Examples of applications under development include contact-lens displays [5]; hemispherical imaging arrays that allow for wide-angle viewing [6]; wearable health monitors; as well as flexible electronic readers [7].

A common component to both display and imaging applications is the thin-film transistor (TFT). TFTs are used in active-matrix backplanes, which allow for highly responsive and precise control of the arrays of lighting or sensor elements that form display or imaging screens. A cross-section of a typical active-matrix organic light-emitting diode (AMOLED) display panel is shown in Figure 1.1. Each lighting unit in the array, or pixel, is typically

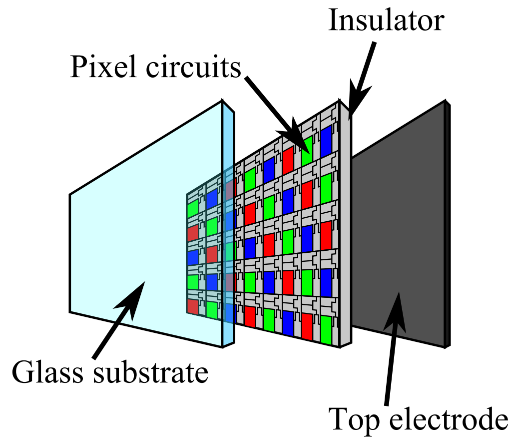

Figure 1.1: Exploded cross-section of an AMOLED display panel

comprised of a red, a green and a blue subpixel. Each subpixel contains an OLED and a pixel circuit with TFTs to control the OLED. By varying the intensity of each subpixels' output, their combined output is capable of rendering a range of colours at various brightness.

A simple 2-transistor circuit that can be used to control a subpixel of a display is illustrated in Figure 1.2. First, a signal is applied across a horizontal row of subpixels, turning on the switch TFT (S-TFT). The row is then ready to receive video signals from the vertical lines. The vertical lines program each OLED in the activated row by applying a voltage to the gate of the drive TFT (D-TFT), which delivers the necessary current for the OLED to emit light at the required intensity. The S-TFTs are then switched off for the row, isolating the OLEDs from the vertical lines. Voltage at the gate of the D-TFT is maintained by charge stored on capacitor C_S, holding the OLED output at the required level. The S-TFTs in the next row are then switched on, and the above procedure repeats until the rest of the screen is programmed.

The components and functionality of a sensor panel are similar to those of the display

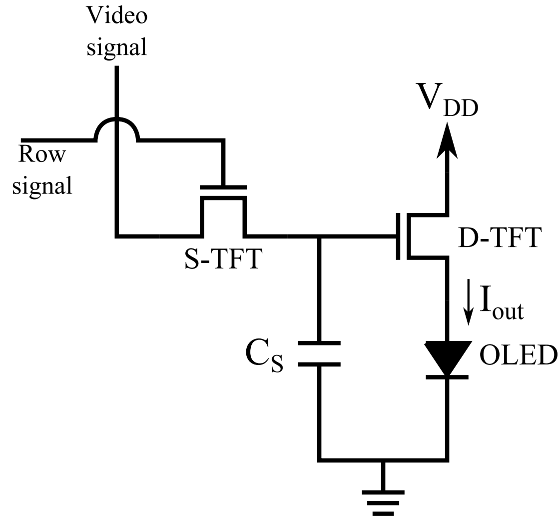

Figure 1.2: 2-T pixel circuit

panel described above. If the OLEDs are replaced with photodiodes, each pixel becomes a sensor that converts incident light into electrical signals that can be recorded, capturing the image.

1.2 Advantages of amorphous silicon

Researchers have demonstrated functional flexible TFTs fabricated from a variety of materials. The research documented in this thesis focusses on hydrogenated amorphous silicon (a-Si:H) TFTs, as they offer several key advantages. Firstly, a-Si:H TFTs are currently in widespread commercial production, most notably for application in flat-screen display panels. Flexible a-Si:H TFTs can be produced by the same processes, which facilitates adoption of the technology by industry as there is no need for investment in novel fabrication equipment. Existing knowledge can be applied towards the development of flexible a-Si:H TFTs as they are based on a relatively mature technology.

There are several other advantages with a-Si:H with respect to fabrication. It can be deposited uniformly over large substrates, making it ideally suited for large-area electronics. Large substrates are desirable as not only can larger panel sizes be produced, an increasing number of panels can be cut from a single substrate for efficient large-volume production. The fabrication of a-Si:H TFTs is also possible at relatively low temperatures such as 120C, enabling the use of inexpensive, flexible plastic substrates which typically have glass-transition temperatures in the range of 80 °C to 150 °C [8].

Another advantage is that a-Si:H can be finely patterned by photolithography. Although TFTs in most commercial display applications have minimum feature sizes on the order of tens of micrometers, the limit of the technology is below the submicron level. Being an amorphous material, a-Si:H forms good interfaces with a variety of materials. This is significant as interface properties, especially between the semiconductor channel and gate dielectric of a TFT, are important determinators of device performance. This also allows for flexibility in terms of processing and selection of materials for TFT substrates and device layers.

Although organic TFTs may be simple and cheap to fabricate as well [9], amorphous silicon has a relatively high mobility compared to organic materials. Figure 1.3 shows a comparison of the mobility of a-Si:H with other TFT materials. Crystalline and polycrystalline silicon can offer higher mobility but also require high temperature processes which would damage flexible plastic substrates or additional unconventional process steps. At about $1\ \mathrm{cm^2/V \cdot s}$, the electron mobility of amorphous silicon is more than sufficient for display applications [10]. High mobility is necessary for good current driving ability, which allows a large amount of current to be controlled by a device with small area. This is important for applications such as the drive TFT shown previously in Figure 1.2, as a smaller device size minimizes the area of the pixel circuit. More space is then available for

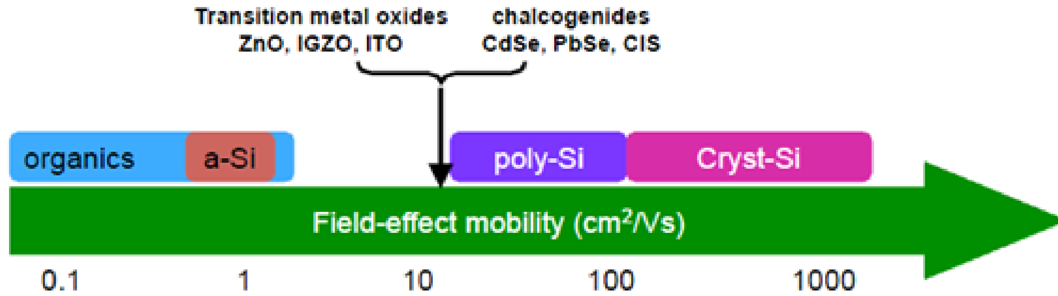

Figure 1.3: Comparison of mobility for various TFT materials

a larger OLED which results in a higher resolution display.

1.3 Motivation

A major challenge of developing flexible displays and sensors with amorphous silicon is electrical metastability. The electrical characteristics of a-Si:H TFTs, such as threshold voltage, gradually shift over time when a gate bias is applied. The metastability leads to a degradation in the operation of TFT circuits and limits the device lifetime. Taking the pixel circuit in Figure 1.2 as an example, metastability is present in the TFTs controlling the output current of the OLEDs and causes the current to decrease over time. This phenomenon leads to a decrease in the brightness of the pixels, and eventually causes the display to become perceptibly dimmer.

In order to advance flexible a-Si:H TFT technology, it is necessary to gain a better understanding of the shift mechanisms under the influence of applied mechanical strain. Such knowledge could then be applied at the device level to design more robust flexible TFTs. Alternately, systems can be designed to compensate for instability using knowledge of the

long-term device behaviour. The effects of applied strain, occurring when a flexible device is bent, on the physical mechanisms of instability are not well characterized. Hence, it is the goal of the research presented in this thesis to investigate the impact of simultaneous electrical and mechanical stress on the behaviour of flexible a-Si:H TFTs.

Chapter 2

Background on a-Si:H TFTs

2.1 Properties of amorphous silicon

Over a short range of a few interatomic distances, the structure of amorphous silicon closely resembles that of crystalline silicon, with valence and conduction bands formed from the splitting of the sp3 hybrid orbitals in tetrahedrally bonded silicon. Therefore both the amorphous and crystalline phases have similar overall electronic structure, with band gaps of about 1.7 eV and 1.1 eV respectively [10]. The disordered structure of amorphous silicon becomes apparent over longer ranges, and influences its electronic properties in various ways. The variation in bond lengths and angles in amorphous silicon form broad band tails at the conduction and valence bands instead of the clearly defined band edges in crystalline silicon. Amorphous silicon also contains coordination defects as shown in Figure 2.1, which can lead to electronic states deep within the mobility gap. Such defects can occur in the a-Si:H bulk, but are also common at the semiconductor-dielectric interface. The conduction and valence bands, band tails and deep defect states in amorphous silicon

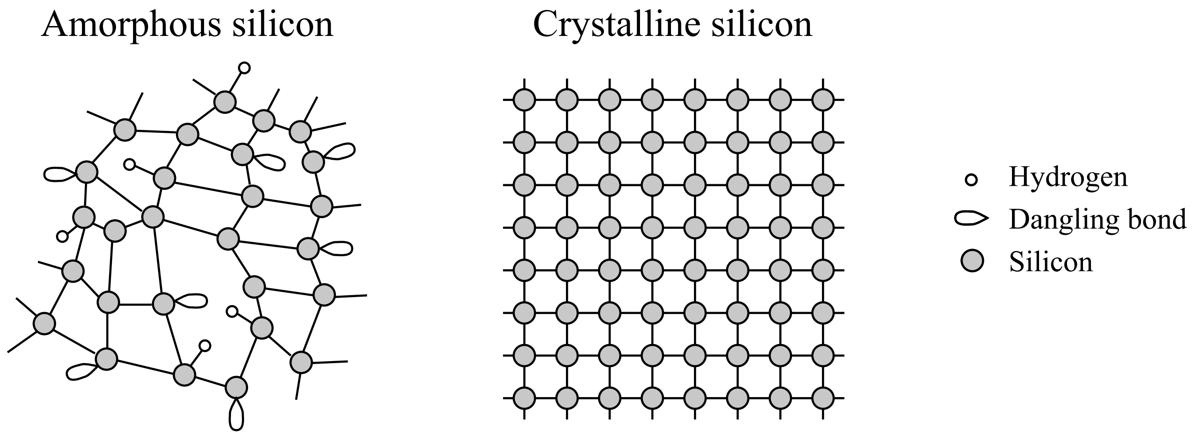

Figure 2.1: Structure of amorphous vs. crystalline silicon

are described by the distribution of the density of states $N(E)$ as illustrated in Figure 2.2.

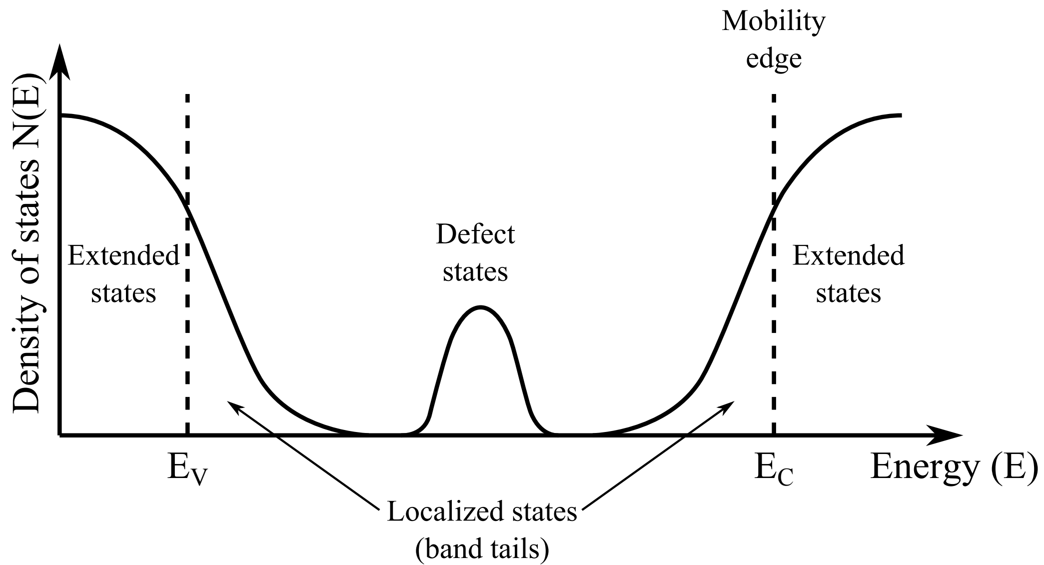

Figure 2.2: Density of states in amorphous silicon

The band tails in amorphous silicon consist of localized states and are separated from

the extended states in the conduction band by the mobility edge. The localized states are defined as such as carriers in the states are confined to a small volume of the material and do not contribute to conduction at T = 0 K [11]. The localized states in the upper half of the mobility gap act as acceptor-like states which are neutral when empty and negatively charged when filled with an electron. The localized states closer to the valence band act as donor-like states that a positively charged when empty and neutral when filled with an electron. The density of states (DOS) in the band tails are given by exponential equations as a function of energy [10]:

$$\begin{aligned} g_A(E) &= g_{nt} \exp\left(\frac{E - E_C}{E_{nt}}\right) \\ g_D(E) &= g_{pt} \exp\left(\frac{E_V - E}{E_{pt}}\right) \end{aligned} \tag{2.1}$$

$g_A(E)$ and $g_D(E)$ are the density of acceptor-like and donor-like states respectively. g_{nt} and g_{pt} are the DOS at E_C and E_V for the tail states as shown in Figure 2.2. $E_{nt} = kT_{nt}$ and $E_{pt} = kT_{pt}$ are defined as the characteristic slopes of the conduction and valence band tails, with k being the Boltzmann constant, and characteristic temperatures of T_{nt} and T_{pt}.

Conduction in a-Si:H mainly occurs through a combination of movement of carriers through the extended states and hopping in the localized states [12]. The conductivity in the extended states is given by

$$\sigma = \sigma_0 \exp^{\frac{E_F - E_C}{kT}} \tag{2.2}$$

$$= q\mu_{band} n_{band} \tag{2.3}$$

where n_{band} is the extended states and μ_{band} is the mobility in the extended states. Therefore $n_{band} = N_b \exp((E_F - E_C)/kT)$ with $N_b = \sigma_0 / q\mu_{band}$. In the conduction band, $\sigma_0 \approx 350\ \Omega^{-1} \cdot \mathrm{cm}^{-1}$ and the band mobility $\mu_{band} \approx 13\ \mathrm{cm}^2/\mathrm{V} \cdot \mathrm{s}$ [11]. The Fermi energy is dependent on the DOS distribution and is ~ 0.6 meV below E_C at room temperature [10].

E_F is slightly closer to the conduction band as the valence band tail is wider than the conduction band tail. In state-of-the-art a-Si:H, hopping in the deep states around E_F is an insignificant mechanism of conduction as there is a low density of defects ($10^{15} - 10^{16}$ cm^{-3}) due to hydrogen passivation [13]. However, the deep defect states influence the behaviour of a-Si TFTs by acting as traps for carriers.

The band mobility is much higher for electrons than holes in a-Si:H, and consequently TFTs for most practical applications are n-type. μ_{band} is significantly limited by scattering in disordered material, as evident in comparing $\mu_{band} \approx 13$ cm^2/V $\cdot$ s for electrons in a-Si:H whereas the room temperature mobility of c-Si is $\sim$1000 cm^2/V $\cdot$ s. Scattering increases with the amount of disorder in the material which causes μ_{band} to vary with mechanical strain [10].

Consequently, the conductivity is also affected by strain. Strain can change the level of disorder in the material (i.e. by slightly altering bond lengths and angles), which affects the width of the distribution of tail states. The change in the charge distribution in the localized states leads to a slight shift in the Fermi level. For n-type material, compression lowers conductivity while the opposite is true for tension as shown in Figure 2.3. Similar

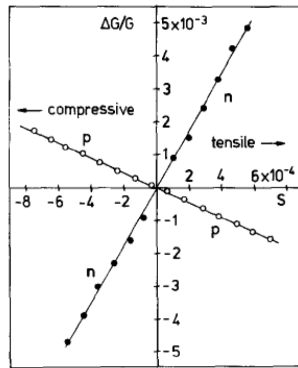

Figure 2.3: Conductance of doped TFTs vs. strain [1]

behaviour can be expected for n-type TFTs, and has been observed in previous experiments [14, 15].

2.2 Device structure

The TFTs used in this study featured an inverted, staggered structure. This structure is commonly used in the production of TFTs for research and commercial purposes due to several benefits [9]. Various TFT structures are shown in Figure 2.4. With the inverted

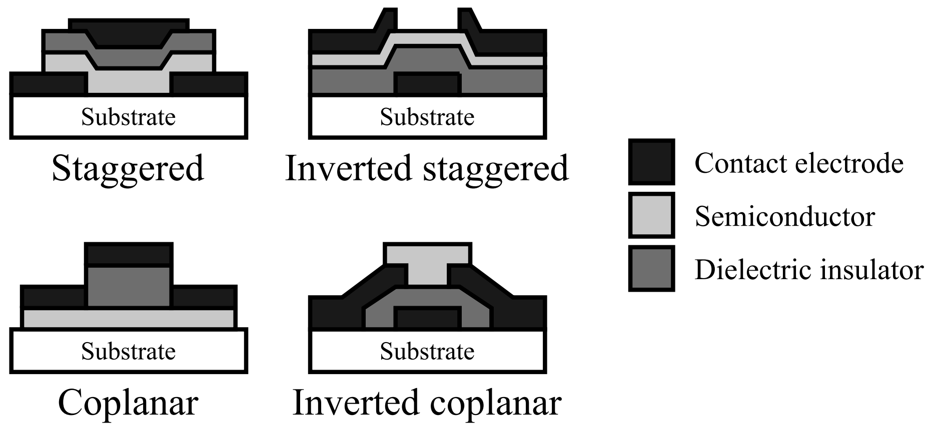

Figure 2.4: Various TFT structures

structure, also known as a bottom-gate TFT, the gate dielectric is deposited before the semiconductor channel of the device. The dielectric and semiconductor layers are conventionally deposited by plasma-enhanced chemical vapour deposition (PECVD). With a non-inverted top-gate structure, where the semiconductor layer is deposited first, the plasma used for depositing the dielectric can damage the semiconductor near the interface of the two materials. This process may lead to poor device performance as TFT operation relies on the formation of an accumulated electron channel close to the interface. Therefore,

the inverted structure is more likely to produce TFTs with good characteristics.

The coplanar structure arranges the gate, source and drain on the same side of the semiconductor, which creates a conduction channel that is closer to the ideal structure assumed by most TFT models [16]. However, offsets between the edge of the gate and the source/drain will lead to a high series resistance which degrades the performance of the device. This is not a problem with the staggered structure as it includes some overlap between the source/drain and gate, which creates a relatively large contact area.

A cross-section diagram of a typical device used in this study is shown in Figure 2.5. A 250 μm-thick polyethylene naphthalate (PEN) film was used as a substrate to allow for

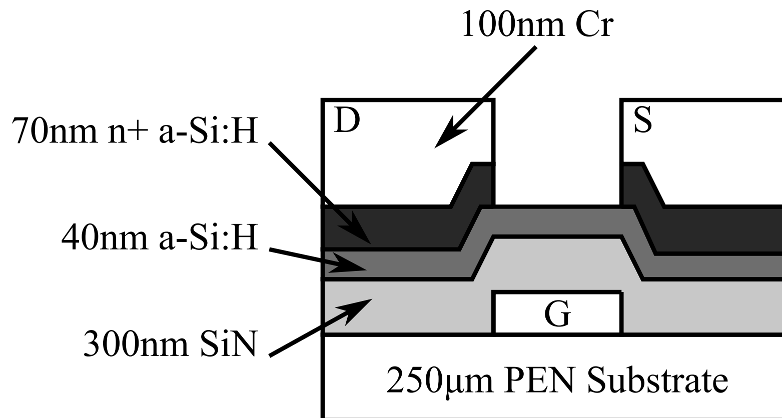

Figure 2.5: TFT cross-section

flexibility. The TFTs were fabricated with a 4-mask back-channel-etch (BCE) process with a maximum temperature of 150 °C. First, the gate metal layer is patterned from 100 nm of Cr sputtered onto the substrate. Next, the gate dielectric layer is deposited by PECVD of a 300 nm-thick layer of a-SiNx:H, followed by 40 nm of a-Si:H forming the semiconductor channel, and 70 nm of n+ doped nc-Si:H for low-resistance source/drain contacts. The top metal layer is deposited by sputtering 100 nm of Cr. The drain and source contacts

are then patterned by etching down to the a-Si:H layer. Lastly, an encapsulation layer of 300 nm a-SiNx:H was deposited on top of the samples.

2.3 TFT operation

The operation of a typical n-type, accumulation-mode TFT is illustrated by Figure 2.6 and the energy band diagrams in Figure 2.7. The device is off without applied bias to the gate.

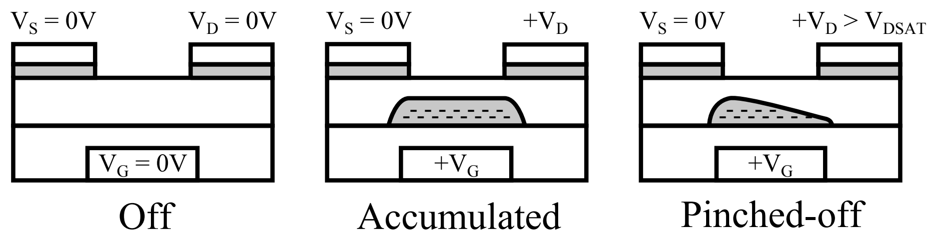

Figure 2.6: TFT in operation

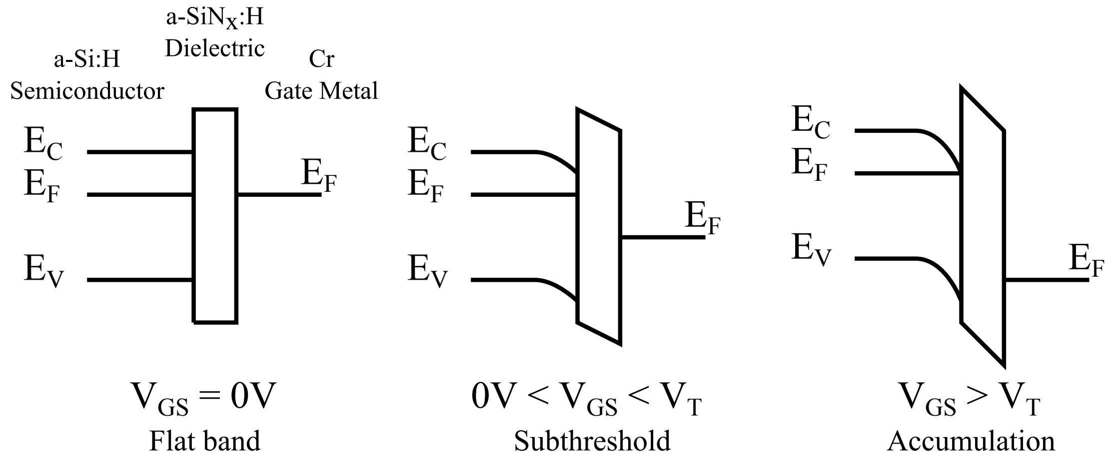

Figure 2.7: Energy band diagram for the gate of a TFT

When V_{GS} is increased, the Fermi level moves towards the conduction band and electrons

accumulate near the gate to form a channel for conduction. The n+ doped material at the source and drain also contribute mobile carriers to help form the channel. When V_{DS} is subsequently increased, a drain-source current is generated. The TFT essentially acts as a resistor, with I_{DS} increasing linearly with V_{DS}. Further increasing V_{DS} will eventually cause the accumulation at the drain to decrease due to the lower potential difference from the gate, leading to a pinched-off channel as shown in Figure 2.6. This causes the device current to saturate at a maximum value.

2.3.1 Above threshold

The above-threshold characteristics of the TFTs can be described by a model developed by P. Servati [17]. This model was chosen as it accounts for parasitic elements such as contact resistance and provides information on the physical properties of the devices. According to this model, the above-threshold drain-source current is described as

$$I_{DS} = \frac{\mu_{eff}}{\alpha} \zeta C_i^{\alpha-1} \frac{W}{L_{eff}} \left[(V'_{GS} - V_T)^\alpha - (V'_{GD} - V_T)^\alpha \right] \tag{2.4}$$

where μ_{eff} is the effective mobility, C_i the gate capacitance which was measured to be approximately 20 nF/cm^2, W is the device width, L$_{eff}$ is the effective length, and V_T is the threshold voltage. V'_{GS} and V'_{DS} are the terminal voltages with contact resistance taken into account:

$$V'_{GS} = V_{GS} - I_{DS} R_S \text{ and } V'_{DS} = V_{DS} - I_{DS}(R_S + R_D) \tag{2.5}$$

ζ is related to the properties of the a-Si:H material and is given by:

$$\zeta = \frac{(q\epsilon\alpha v_{th} n_o)^{1-\alpha/2}}{\alpha - 1} \tag{2.6}$$

where n_o is an arbitrary normalizing number for the density of carriers in the a-Si:H. Setting it as 10^{16} makes it close to the value of $1/(q\epsilon v_{th})^{1/2}$ and allows ζ to be simplified into an

expression that is only dependent on α:

$$\zeta \approx \frac{(10^{16}\alpha)^{1-\alpha/2}}{\alpha - 1} \tag{2.7}$$

The power parameter α is given by $2V_{nt}/v_{th}$ where $E_{nt} = qV_{nt}$ gives the characteristic slope of the conduction band tail as in Equation 2.1. v_{th} is the thermal voltage (25.8 mV at 300 K).

In the linear region of operation, $V'_{DS} << V'_{GS}$ and the following can be derived from Equations 2.4 and 2.5:

$$I_{DS,lin} = \frac{\mu_{eff}}{\alpha}\zeta C_i^{\alpha-1}\frac{W}{L_{eff}}\left(V_{GS} - V_T - 0.5V_{DS}\right)^{\alpha-1}\left(V_{DS} - R_{DS}I_{DS}\right) \tag{2.8}$$

where it is assumed that $R_S = R_D = R_{DS}/2$.

In the saturation region of operation (neglecting non-idealities such as the channel length modulation effect for simplicity)

$$I_{DS,sat} = \frac{\mu_{eff}}{\alpha}\zeta C_i^{\alpha-1}\frac{W}{L_{eff}}\gamma_{sat}\left(V'_{GS} - V_T\right)^{\alpha} \tag{2.9}$$

where $\gamma_{sat} = 1 - (1 - \alpha_{sat})^{\alpha})$ with α_{sat} being a saturation parameter related to the drain-source voltage at which pinch-off occurs. Most practical applications employ TFTs biased in the saturation region due to the higher output current, and also because I_{DS} becomes a sole function of the overdrive voltage $(V_{GS} - V_T)$ and independent of V_{DS}, giving the device a high output impedance.

2.3.2 Subthreshold

In the subthreshold region of operation, the TFT current increases exponentially with increasing V_{GS}, allowing the device to turn on rapidly. The drain current is defined as [18]

$$I_{DS,sub} = I_{sub0}\frac{W}{L}\exp\left(\frac{V_{GS} - V_{TS}}{S_f}\right) \tag{2.10}$$

where V_{TS} denotes the onset of the subthreshold region from the off state, such that the equation holds for $V_{TS} < V_{GS} < V_T$. S_f is the subthreshold slope that is obtained graphically from the plot of $log(I_{DS})$ versus V_{GS} as shown in Figure 2.8. At low V_{GS},

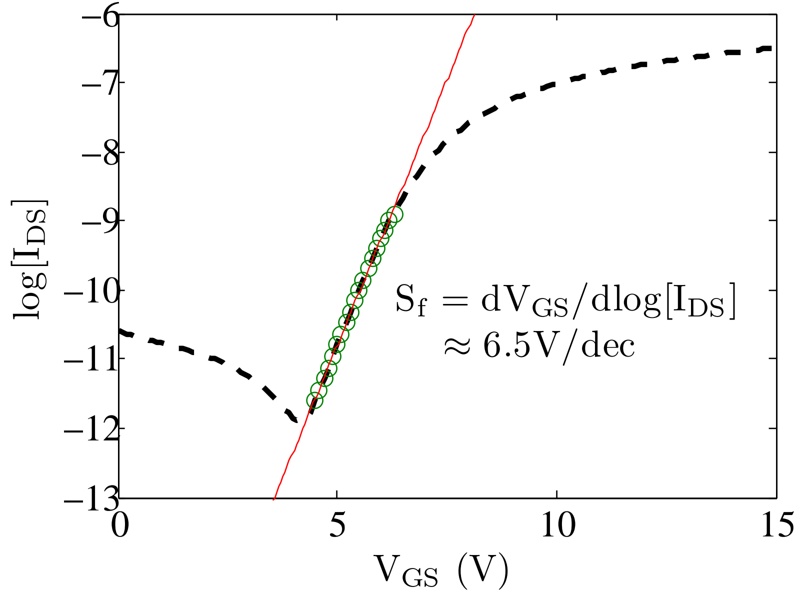

Figure 2.8: Example of subthreshold slope (S_f) extraction

electrons begin to accumulate in a thin layer at the top interface of the channel, leading to the small subthreshold current. As the Fermi level is near mid-gap in this mode of operation, most of the induced carriers go to the deep states caused by defects in the bulk and interface of a-Si:H. Therefore, the subthreshold slope is correlated to the density of deep states.

2.4 Metastability

As mentioned in Section 1.3, a-Si:H TFTs exhibit metastable behaviour under prolonged bias stress. Although there is some uncertainty about the exact physical mechanisms of instability, various studies agree that a simultaneous combination of charge trapping in the a-SiNx:H dielectric and defect state creation in a-Si:H is responsible for threshold voltage shift in TFTs [19]. In previous studies regarding TFTs with a-SiNx:H dielectric, charge trapping has been shown to be the main contributor to V_T shift at high gate voltage bias while defect creation is more significant with lower bias stress [20]. However, the dominant mechanism at a given bias voltage can vary depending on device processing conditions; charge trapping has been reported to be dominant in devices with V_{GS} of ~100 V [2] or as low as 10 V [21]. In order to determine which mechanism is dominant, it is necessary to measure the V_T shift behaviour of devices and see whether they match the kinetics of charge trapping versus defect state creation processes.

2.4.1 Charge trapping

When a TFT is biased in accumulation, electrons can become trapped in the dielectric. Figure 2.9 illustrates the various possible trapping processes. Direct tunnelling from the valence band, Fowler-Nordheim injection, and trap-assisted injection (1-3) occur only at high electric fields and are negligible for normal TFT operation. For the TFTs used in this study, the most likely mechanism is the tunnelling of electrons from the conduction band and from filled conduction band tail states to trap states in the a-SiNx:H (5). After a certain amount of time under bias stress, trap states in the dielectric can become filled to a depth where it may become favourable for electrons to hop from occupied shallow states to deeper traps in the dielectric (6) instead. Conduction in the gate-dielectric (6)

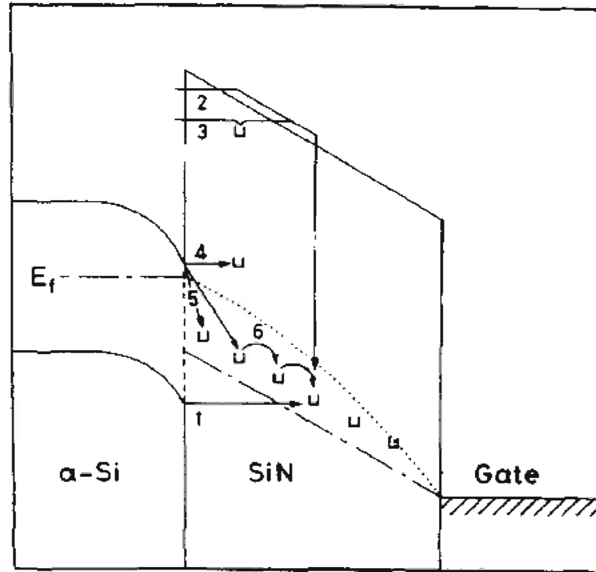

Figure 2.9: Charge trapping mechanisms [2]

is a temperature-dependent process and appears to become significant only above room temperature, so it may not be applicable to the devices in this study. However, it is necessary to look at the temperature dependence of bias-stress measurements in order to rule out this mechanism.

Figure 2.10 shows an energy band diagram of the trapping mechanism under positive bias. Electrons can randomly tunnel into trap states at an energy E_T in the a-SiNx:H. When the TFT is at zero bias, electrons that have tunnelled into the dielectric can easily return to the a-Si:H as E_T is above E_F of the a-Si:H. This is because there is a high density of states available above the Fermi energy of the semiconductor, due to the conduction band tail. Under positive bias, E_T past a certain depth in the dielectric dips below E_F of the a-Si:H. Electrons in these trap states are then unable to return to the a-Si:H until the bias is removed, as there are virtually no unfilled states below E_F in the semiconductor.

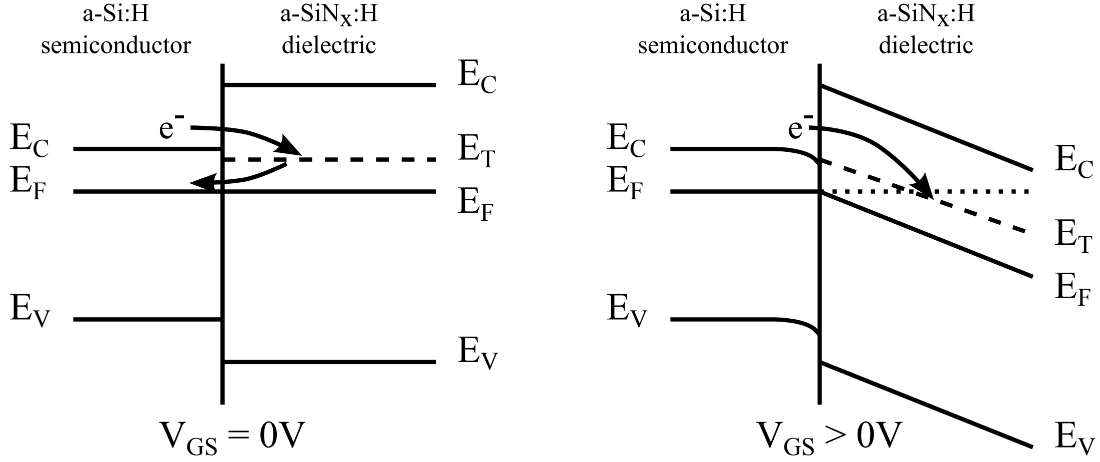

Figure 2.10: Energy band diagram of charge trapping mechanism

The charge trapping process described above results in a parallel shift of transfer characteristics, with no changes in the subthreshold slope. V_T shift through this mechanism has a low temperature dependence and a logarithmic time dependence given by [22]:

$$\Delta V_T = r_d log[1 + \frac{t}{t_0}] \tag{2.11}$$

r_d depends on the density of traps N_t in the dielectric and t_0 is a time constant which can include a temperature-dependent supply function.

An alternative model exists for this charge trapping process [21]. It is assumed that the trap energy level remains constant throughout the dielectric, and therefore the tunnelling of electrons is unaffected by trap depth. In reality, it is more likely for electrons to tunnel into traps nearer to the interface. Hence this model introduces a capture cross-section term, $S(x)$, that decreases exponentially with distance x into the dielectric and is given by

$$S(x) = S_0 \exp[-ax] \tag{2.12}$$

where a is a decay parameter dependent on the electron tunnelling effective mass, barrier height, and electric field. The concentration of filled trap states in the a-SiNx:H at depth

x and bias stress time t changes according to the following equation:

$$\frac{dn_{tr}(x,t)}{dt} = S(x)\vec{v}[n_t[N_{tr} - n_{tr}(x,t)] - n_{empty}(x)n_{tr}(x,t)] \quad (2.13)$$

where n_t is the density of trapped electrons in conduction band tail near the interface, $\vec{v}$ is the thermal velocity of electrons, and n_{empty} is the concentration of empty trap states at distance x.

Integrating n_{tr} through the thickness d of the dielectric gives the total trapped charge and hence the V_T shift is expressed as

$$\Delta V_T(t) = \frac{q}{C_i}\int_{x=0}^{d} n_{tr}(x,t)dx \quad (2.14)$$

$$\Delta V_T(t) \approx \frac{qN_{tr}}{aC_i}\ln(\frac{t}{t_0}) \quad (2.15)$$

where

$$t_0 = \frac{1}{S_0\vec{v}n_t}\exp(ax_0) \quad (2.16)$$

The equation can also be further developed to consider a Gaussian distribution of trap states instead of a single trap energy.

Another model for charge trapping proposes a multiple-trapping mechanism. Electrons from the a-Si:H conduction band become localized in a broad distribution of conduction band tail states that exist at the semiconductor-dielectric interface. The electrons initially hop or inject directly into lower energy interfacial states or to shallow traps in the a-SiNx:H. Over longer bias stress times, larger electric fields and/or higher temperatures, these states become filled and the electrons are emitted back to the a-Si:H conduction band tail states and/or move to deeper traps in the dielectric. The mix of trapping events and movement between traps results in a power-law time dependence instead of a logarithmic time dependence [23, 24]. The V_T shift is modelled by a stretched exponential equation

[25]:

$$\Delta V_T = \Delta V_0 \left[1 - \exp\left[-\left(\frac{t_{ST}}{\tau}\right)^{\beta}\right]\right] \tag{2.17}$$

where ΔV_0 is the approximate effective voltage drop across the insulator, t_{ST} is the bias stress time, and $\tau = \tau_0 \exp(E_\tau/kT)$ is the characteristic trapping time of carriers where the thermal activation energy is $E_a = E_\tau \beta$ with β being the stretched-exponential exponent. E_τ is the average effective energy barrier that electrons have to overcome when tunnelling from the a-Si:H to the dielectric, and τ_0 is thermal prefactor for emission over the barrier. β and τ are independent of bias voltage unlike ΔV_0.

2.4.2 Defect creation

Although defect creation in a-Si:H is not fully understood, two possible mechanisms have been proposed. It is inferred that the defect creation process begins with the breaking of Si-H bonds, releasing H atoms which then collide and form a bound, paired hydrogen complex (SiHHSi) as well as dangling bonds. This reaction is illustrated in Figure 2.11a. A second

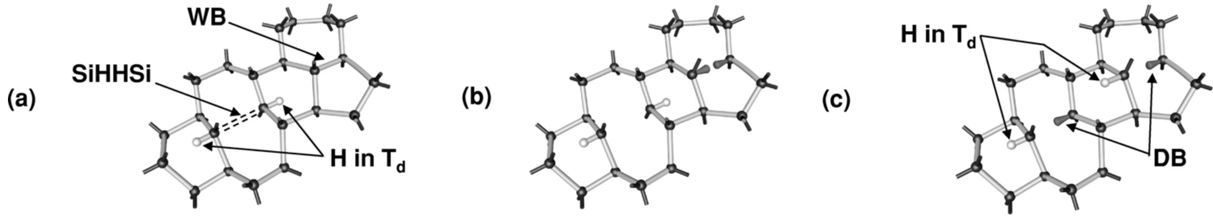

Figure 2.11: Localized defect creation process [3]

mechanism involves the breaking of weak Si-Si bonds that are in close proximity to SiHHSi complexes. The hydrogen atoms subsequently rearrange to leave dangling bonds close to the hydrogen atoms (SiHdb), as shown in Figure 2.11b-c, which stabilizes the dangling

bonds. The second process, and therefore Si-Si bond breaking, is the rate limiting step for defect creation [26].

Figure 2.12 shows an energy band diagram of the defect creation process under electron

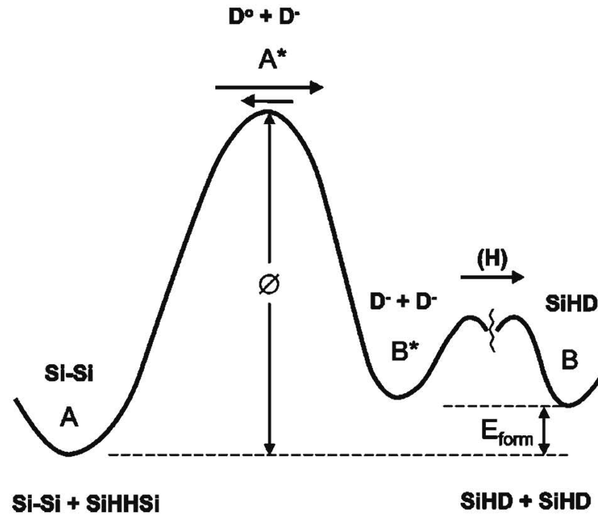

Figure 2.12: Energy diagram of defect creation [3]

accumulation. The initial Si-Si bond is at energy A. The breaking of the bond forms a D0 and a D- state as the bond becomes occupied by only a single electron. This is described as the intermediate state A*. The dangling bonds then stabilize to state B. B* is an additional intermediate state for a backward reaction where both dangling bonds become negatively charged. This state is possible due to disorder in a-Si:H causing an exponential distribution of energy barrier heights $\varnothing$, so a backwards reaction can occur for the lower range of barrier heights. The barrier height $\varnothing$ primarily determines the rate of defect creation, while the total amount of defect creation is mainly dependent on the energy difference E_{form} between the initial and final states [3].

From studies of a-Si:H TFTs deposited under a range of deposition conditions to vary

the intrinsic stress, compressive stress in the a-Si:H results in a shortening of Si-Si bonds, which reduces the energy required to break the bonds [27]. Conversely, the Si-Si bond strengthens with increasing bond length distortion up to 1 Å [28]. However, some groups have speculated that sufficiently high tension can weaken Si-Si bonds and increase the rate of defect creation as well [29, 30].

The energy of the created defects can vary depending on the conditions of dangling bond formation. The dangling bonds can also be charged (e.g. by capturing an electron). The density distribution of defect states is shown in Figure 2.13. Defect states formed

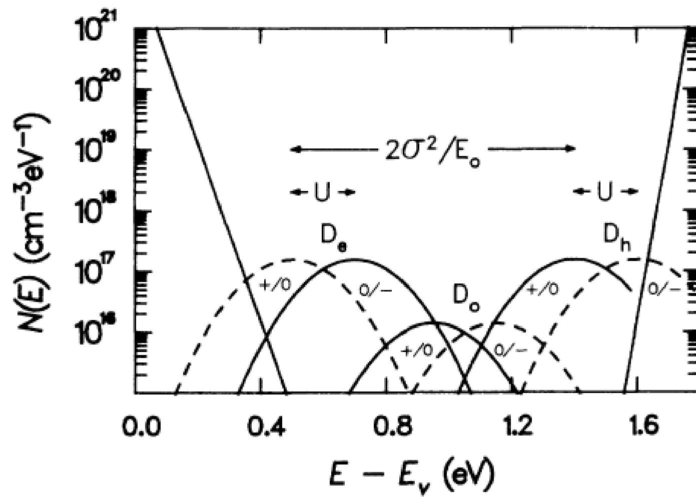

Figure 2.13: Density distribution of defect states [4]

under positive bias with electron accumulation (De) have energy levels in the lower half of the a-Si:H bandgap. Defects formed under negative bias with hole accumulation (Dh) have energy levels in the upper half of the bandgap. De states are initially formed as dangling bonds which have captured an electron (D-) as described previously, while Dh states start out as positively charged dangling bonds (D+). However, the defects can subsequently

transition to different charge states. Some D0 states are formed as well, but are relatively low in density. The various energies of the defect states are exponential distributions due to the disorder in a-Si:H.

It has been experimentally shown that moving the Fermi energy affects the distribution and density of states. Raising the Fermi energy towards the conduction band by applying a positive bias stress increases the density of De states. A higher density of De states results in a positive shift of electron threshold voltage. The electron subthreshold slope is unaffected while the hole subtheshold slope is degraded. Conversely, negative bias stress which moves the Fermi energy closer to the valence band causes an increase in Dh states. This causes positive electron V_T shift as well, but also degrades the electron subtheshold slope [4].

The V_T shift due to defect creation can be simply modelled by a stretched-exponential equation [31]

$$\Delta V_T(t) = (V_{GS} - V_{T0}) \left[1 - \exp\left[-\left(\frac{t}{\tau} \right)^{\beta} \right] \right] \tag{2.18}$$

where V_{T0} is the initial threshold voltage, and τ and β are characteristic parameters for defect creation during bias stress. According to this equation, the V_T shift has a power-law time dependence.

An improved and more complex model has also been presented which gives a stretched-hyperbola equation for the V_T shift [27]:

$$\Delta V_T(E_{th}) = V_0 \left(1 - \frac{1}{1 + \exp\left[\frac{E_{th} - E_A}{kT_0} \right]^{1/\epsilon}} \right) \tag{2.19}$$

where $E_{th} = kTln(vt)$ is the thermalisation energy, such that after a time t at temperature kT, all defect creation sites with energy barriers less than E_{th} will have converted to defects.

V_0 is the initial overdrive voltage, E_A is the typical energy barrier for defect creation under a given level of electron accumulation and kT_0 is the characteristic slope of the exponential distribution of barriers. $\epsilon = \alpha - 1$ where α is obtained from the slope of V_T shift over $(V_{GS} - V_{T0})$.

2.4.3 Relaxation

Relaxation is primarily due to charge detrapping, from electrons simply back-tunnelling to a-Si:H. Shallow trap states in the nitride close to the dielectric interface are more likely to detrap reversibly, unlike deeper states.

Defect removal occurs through a different process than simply the reverse of defect creation. Instead of the annealing of broken Si-Si bonds, defect removal is dependent on the breaking of Si-H bonds. The released hydrogen atoms then passivate dangling bond defects, and could occur locally like with defect creation process and also after long-range diffusion [3, 26]. Time scales for defect annealing are much longer than is relevant for our experiment at room temperature. Therefore the primary mechanism of relaxation is charge detrapping.

Chapter 3

Experiment

3.1 Prior work

The effect of mechanical strain on flexible a-Si:H TFTs has long been a subject of research interest. Initial studies focussed on determining failure mechanisms and the maximum level of strain devices could tolerate. It was found that TFTs tended to fail due to cracking under tension and by delamination and buckling of the device layers under compression [32]. The maximum amount of strain that can be applied without device failure is dependent on the mechanical properties of the substrate, device geometry, deposition conditions and thicknesses of the TFT layers, but was found to be ~0.5% tensile and ~2% compressive strain for a-Si:H TFTs on polyimide film [33].

There has also been much investigation on the electrical behaviour of TFTs with applied strain below the failure limit. Many groups have measured the transfer characteristics of TFTs strained to various levels of tension and compression. It has been found that the electron field effect mobility increases with tension [34] and decreases with compression

[35], with a linear dependence on the applied strain. The sensitivity of the mobility to the change in strain has been described as

$$M_{\epsilon}(\mu) = \frac{\Delta\mu}{\mu \cdot \epsilon} \tag{3.1}$$

where ϵ is the applied strain. Sensitivity values ranging from $\sim$ 22 to $\sim$ 26 have been reported for a-Si:H TFTs on polyimide film [29]. The mobility changed instantly with the application of strain, then remained stable while being held under strain for 40 hours [36]. However, the sensitivity gradually decreased from 23.6 to 11.1 with multiple strain load cycles which suggests that prolonged strain may have caused long-term changes in device characteristics. Threshold voltage, subthreshold swing and Ioff showed monotonic trends with respect to time when a sequence of random levels of strain was applied, which indicated that the results were also affected by bias-stress-induced instability [29]. The influence of uniaxial applied strain on device characteristics was found to be strongest when the strain was oriented in parallel to the drain-source current [14]. The effect of strain on bias-stress instability of flexible TFTs has been studied to some extent as well. Threshold voltage shift over 2h with constant gate voltage bias stress was found to be greater under tension than without strain [30].

The cause of the aforementioned shifts in device characteristics has mainly been attributed to strain-induced changes in the a-Si:H material. Strain changes the characteristic slope of the conduction band tail as discussed in Section 2.1, which may have led to the observed changes in mobility [15, 37]. The increased instability with tension was speculated to be due to the weakening of Si-Si bonds under strain, leading to increased creation of dangling bonds [30]. This hypothesis was confirmed with atomic force microscopy (AFM) and micro-Raman spectra of the top side of back-channel-etched a-Si:H TFTs after bending. The long-range structure of the a-Si:H was deformed by applied tension, but the

short-range structure remained about the same. An interpretation of this phenomenon is that the applied strain causes a redistribution of traps from localized states to deep states, leading to changes in V_T, field-effect mobility and subthreshold swing [37].

3.2 Approach

The goal of this study is to further investigate electrical bias-stress instability in mechanically strained a-Si:H TFTs, as the topic has yet to be explored systematically. The study also aims to determine whether strain affects the magnitude and rate of the physical mechanisms which cause threshold voltage shift. Hence, an emphasis was placed on bias-stress measurements over time. Drain current was measured over various intervals of time to track the degradation of devices due to metastability, and results were then compared across different levels of strain.

In previous studies of TFT behaviour under mechanical strain, parameters such as threshold voltage and field-effect mobility were often extracted from linear extrapolation of transfer characteristics, based on an ideal square-law model for TFT operation [16]. However, this method of extraction results in a threshold voltage that is sensitive to series resistance and dependent on mobility. The field-effect mobility also increases gradually with increasing V_{GS}, which introduces uncertainty when selecting data points for linear extrapolation and introduces error into the extracted parameters [38]. The drain current in a-Si:H TFTs may also have a power parameter that is different from the ideal square-law model which assumes a value of 2 [16].

A general method for threshold voltage extraction in non-crystalline MOSFETs which circumvents the above difficulties has been presented [39]. However, the extraction is based on devices biased in the saturation region of operation. Although TFTs are usually

biased in saturation for most practical applications, a pinched-off channel complicates the collection of data for the purpose of studying bias-stress instability. As there is a large variation of the overdrive voltage along the channel, TFTs biased in saturation show a non-uniform V_T shift along the length of the device [40].

In this study, the above-threshold characteristics of the TFTs were extracted using a procedure based on the compact model developed by P. Servati [41], which was presented in Section 2.3.1. This model was chosen as it accounts for parasitic elements such as contact resistance, allows for extraction of a non-ideal power parameter, and defines parameters such as an effective mobility which provides information on the physical properties of the a-Si:H channel.

3.3 Measurement procedure

First, the transfer characteristics for various TFTs were measured by applying a drain voltage of 0.1 V and sweeping the gate voltage from 0 V to 20 V. Initial device characteristics extracted from the linear region of operation showed an Ion/Ioff ratio of greater than 10^5, threshold voltage of around 4 V, transconductance of about 50 pA/mV, and subthreshold swing of 0.7 V/dec. The devices showed a high degree of uniformity across the wafer; variation of the above parameters was within about 5% across the TFTs measured.

Uniaxial tensile strain was then applied to several devices, with the strain oriented parallel to the drain-to-source current path. Transfer characteristics were measured for comparison with data obtained when the device was unstrained. Individual devices were then subjected to bias stress for various durations of time by applying a constant gate voltage of 20 V and monitoring the drain current with a 0.1 V drain voltage applied. Separate TFTs were monitored for bias stress times of 100 s, 1000 s and 10000 s.

After the 100 s and 1000 s bias stress tests, the gate voltage was set to 0 V and the device was allowed to recover. The drain current was monitored with a very low duty cycle pulsed measurement. At various intervals, the drain current was measured by applying a 20 V pulse to the gate while the drain voltage remained held at 0.1 V. The pulse width was set to 1 s, with off intervals of up to 300 s. The pulse width was chosen to be long enough to eliminate transient fluctuations in the measured current due to charging of parasitic capacitances, but also short enough to minimize further aging of the device, which could hinder recovery.

For the 10000 s bias stress measurement, transfer characteristics with $V_{DS} = 0.1$ V and 1 V over $V_{GS} = 0$ V to 20 V were also measured at 1000 s intervals during the bias stress time. To track TFT recovery, transfer characteristics were measured approximately 30 hours after the bias stress was removed from the devices.

The above measurements were then repeated with a separate group of TFTs that were put under uniaxial compressive strain. All measurements were also repeated with a group of TFTs that were not subjected to any mechanical stress, as a reference for comparison with the strained cases.

3.4 Testbench

Tensile and compressive strain was applied to the TFTs by bending samples to convex and concave curves of known radii. The exact amount of strain in the channel of each TFT is difficult to determine as the samples consist of many layers of different materials patterned to various geometries. However, the strain can be calculated by modelling the bent device as the simplified structure shown in Figure 3.1. This model treats the various device layers as a single uniform film with Young's modulus Y_f, sitting on one surface of the

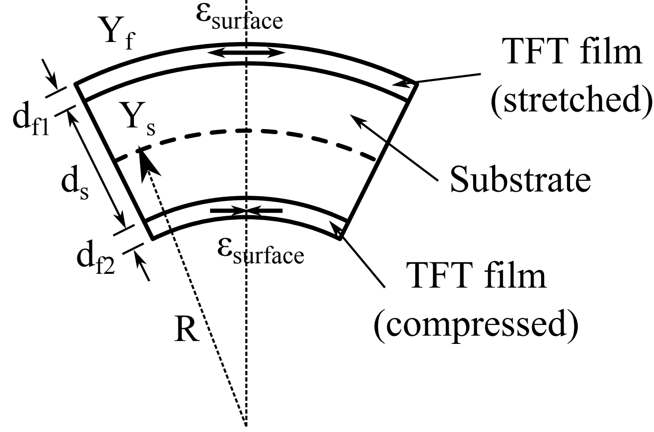

Figure 3.1: Model for surface strain calculation

substrate with thickness d_s and Young's modulus Y_s. For applied tension and compression respectively, the TFTs are represented as either a layer of thickness d_{f1} on the outside of the bend or as a layer of thickness d_{f2} on the inside. The strain on the TFT film surface can then be estimated by the following equation [33]:

$$\epsilon_{\text{surface}} = \left(\frac{1}{R} \pm \frac{1}{R_0}\right) \frac{d_s + d_{f1} + d_{f2}}{2} \cdot \frac{\chi({\eta_1}^2 + {\eta_2}^2) + 2(\chi\eta_1 + \chi\eta_1\eta_2 + \eta_2) + 1}{\chi(\eta_1 + \eta_2)^2 + (\eta_1 + \eta_2)(1 + \chi) + 1} \tag{3.2}$$

where $\chi = Y_f/Y_s$, $\eta_1 = d_{f1}/d_s$ and $\eta_2 = d_{f2}/d_s$. R_0 is the initial radius of the sample, with the plus and minus signs representing applied bending opposite to or with the built-in curvature. In the samples used in this experiment, the deposition conditions of the device layers were carefully chosen to minimize the internal film stresses. Accordingly, the samples were fairly flat. Therefore it is assumed that the internal film stresses are negligible compared to externally applied forces, allowing the R_0 term in the equation to be ignored.

The estimated values of strain for the various radii are listed in Table 3.1. Values were calculated using $Y_f = 200$ GPa [33], $Y_f = 6.1$ GPa [6] and film thicknesses as described in Section 2.2.

Table 3.1: Calculated values of strain

Bending radius (mm)	Tensile strain (%)	Compressive strain (%)
38	0.3	0.3
32	0.4	0.4
22	0.6	0.5
16	0.9	0.7
11	1.2	1.0
6	2.2	1.8
4	3.5	2.8

Metal support structures for each bending radius were created to hold the TFTs under constant strain during measurement. Samples with dimensions of approximately 1.5 cm by 1.5 cm containing multiple devices were positioned and attached to the curved surfaces of the structures such that the applied strain was aligned along the drain-to-source current path of the TFTs. The structures were then placed into a probe station and the devices were measured directly as shown in Figure 3.2.

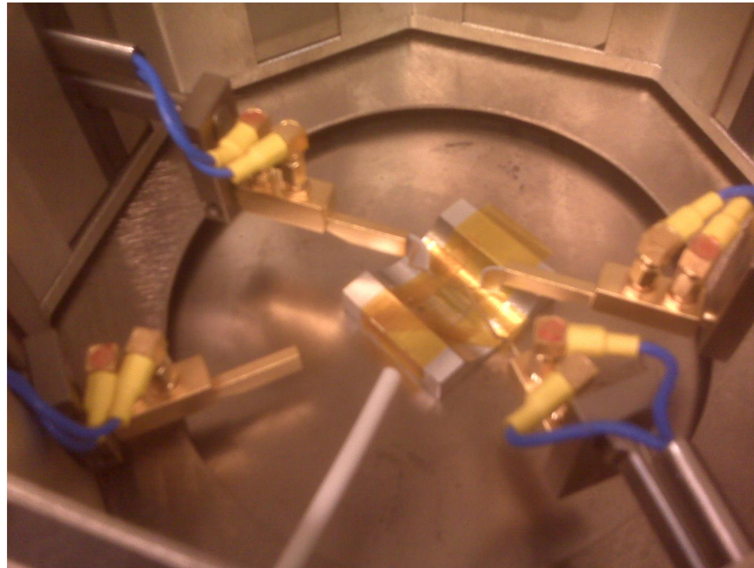

Figure 3.2: TFT sample mounted on strain testbench

Chapter 4

Results

4.1 TFT parameters and bias stress

The above-threshold characteristics of the TFTs were extracted using a procedure based on the model presented in Section 2. TFTs were biased in the linear region of operation, with a gate voltage of 20 V. The threshold voltage, power parameter, contact resistance, and effective mobility were extracted from transfer characteristics measured every 1000 s for a total time of 10000 s.

From Equation 2.8 and assuming negligible contact resistance effects, the linear transconductance can be derived as

$$g_{m,lin} = \frac{\mathrm{d}I_{DS,lin}}{\mathrm{d}V_{GS}} = \frac{\mu_{eff}}{\alpha}\zeta C_i^{\alpha-1}\frac{W}{L_{eff}}(\alpha-1)\left(V_{GS}-V_T-0.5V_{DS}\right)^{\alpha-2}V_{DS} \tag{4.1}$$

Dividing the drain-source current by this yields

$$\frac{I_{DS,lin}}{g_{m,lin}} = \frac{\left(V_{GS}-V_T-0.5V_{DS}\right)}{\alpha-1} \tag{4.2}$$

Therefore, by plotting $I_{DS,lin}/g_{m,lin}$ versus V_{GS} and fitting a line to the linear region, initial values for α and V_T can be extracted from the slope and x-intercept. The values of α and V_T were then further refined through curve-fitting to the measured I_{DS} versus V_{GS} data. This is necessary to improve the accuracy of α as the initial values assume R_{DS} is negligible. The error in α compared to the initial value can be estimated as [17]

$$\Delta\alpha_{\text{lin}} \approx -k_o(\alpha - 1) \tag{4.3}$$

where

$$k_o = \frac{R_{DS} W \mu_{\text{eff}} \zeta C_i^{\alpha-1}}{L_{\text{eff}}(V_{GS0} - V_T)^{\alpha-1}} \tag{4.4}$$

with V_{GS0} being the highest value of V_{GS} where the plot of $I_{DS,lin}/g_{mlin}$ remains linear (i.e. unaffected by R_{DS}). Thus the value of α should be slightly higher than the initial value when RDS is considered.

Using the fitted values for α, V_T was further refined by determining the intercept of $I_{DS}^{1/(\alpha-1)}$ versus V_{GS}. The new values of α and V_T were then used in Equation 2.8, and further fitting was conducted to refine R_{DS}. Depending on whether R_{DS} was raised or lowered, the value of alpha was adjusted accordingly. This process was then iterated to improve the accuracy of the extracted parameters. Figure 4.1 compares the measured drain-source current with values calculated from parameters obtained through fitting. Note that the fitting only applies to the linear region of operation and therefore deviates from the measured values at lower values of V_{GS}.

The values for R_{DS}, α, V_T, and μ_{eff} are plotted with respect to the applied strain in Figures 4.2a to 4.2d. The data was extracted from devices with zero applied strain and at the maximum levels of tension and compression without visible damage to the TFTs (roughly 1% strain). However, further study is required to rule out the presence of any micro-cracking which could affect the measured characteristics.

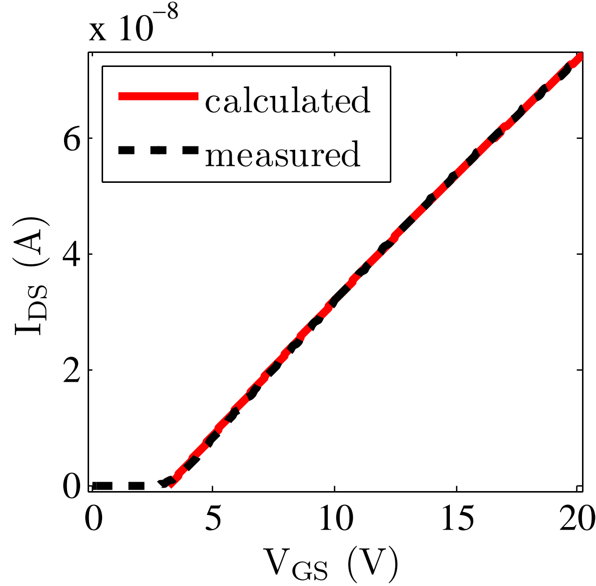

Figure 4.1: An example of measured vs. simulated I_{DS} vs. V_{GS}

The extracted parameters are plotted as a function of total bias stress time in Figures 4.3 to 4.8. In addition to the above-threshold parameters, the subthreshold swing was also extracted from the transfer characteristics.

R_{DS} seems to be unaffected by the level of applied tension used in the experiment. However, R_{DS} decreases with compression in Figure 4.2a. This could be due to the closing of pre-existing micro-cracks and/or a decrease in contact resistance as the TFT layers at the drain and source are compressed [42]. From Figure 4.3, R_{DS} drops steeply with bias stress over the first 1000 s for the unstrained and compression cases, then remains fairly stable for the rest of the 10000 s. Under tension, R_{DS} continues to decrease until 3000 s, then remains roughly constant. The overall change for tension is similar to the unstrained case. The greatest decrease occurs for compression. However, the decrease in extracted R_{DS} over bias stress time may be due to the lowering of the drain-source current

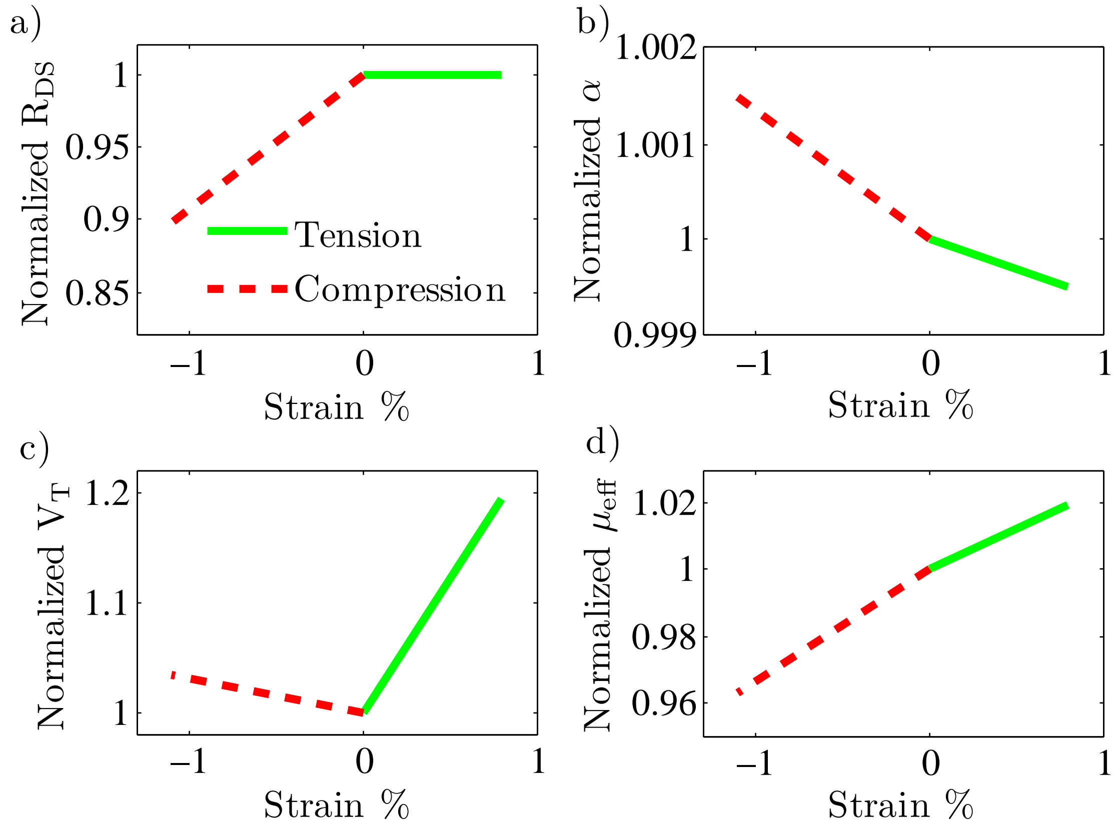

Figure 4.2: Normalized R_{DS}, α, V_T and μ_{eff} vs. strain

with increasing V_T shift as V_{GS} is held constant for the measurement. The degradation in the transfer characteristic due to series resistance becomes less apparent with lower I_{DS}, leading to a lower value of R_{DS} when extracted by curve-fitting. It is necessary to do a more accurate R_{DS} extraction by measuring and comparing devices with a greater variation in channel length. Also, a higher value of V_{GS} or constant-current measurements could be used to obtain data with a smaller ratio of change in overdrive voltage.

Figure 4.2b shows that α increases with compression and decreases with tension. As defined in Section 2.3.1, α is directly proportional to the characteristic slope E_{nt} of the

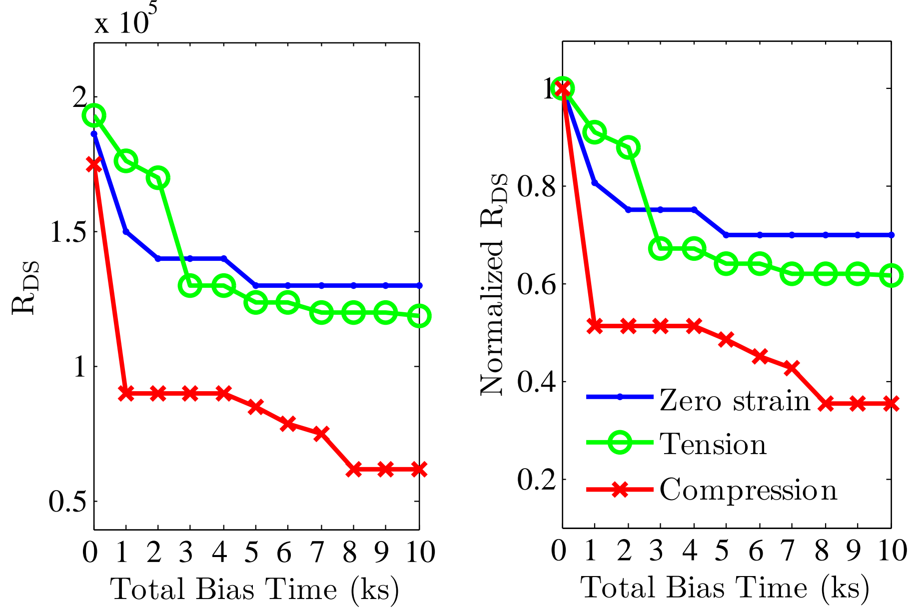

Figure 4.3: R_{DS} and normalized R_{DS} vs. total bias stress time

conduction band tail. The data indicates that the conduction band tail widens with compression and narrows for tension, which agrees with findings by previous groups [34]. Figure 4.4 shows that α remains roughly constant with increasing bias stress time, but with a slight increase over the first 1000 s for the unstrained and compression cases. The fairly constant values for α show that the distribution of localized states near the conduction band do not change significantly during the bias stress experiment. This result is expected as positive bias stress should mainly create defect states at energies below mid-gap according to the defect pool model discussed in Section 2.4.2.

The values of α obtained from curve-fitting vary much less with respect to bias time than the roughly extracted values obtained initially from Equation 4.2. This is because the fitting process considers the R_{DS} parameter, which decreases under bias stress over time as shown in Figure 4.3. The decreasing value of R_{DS} essentially absorbs the change seen in

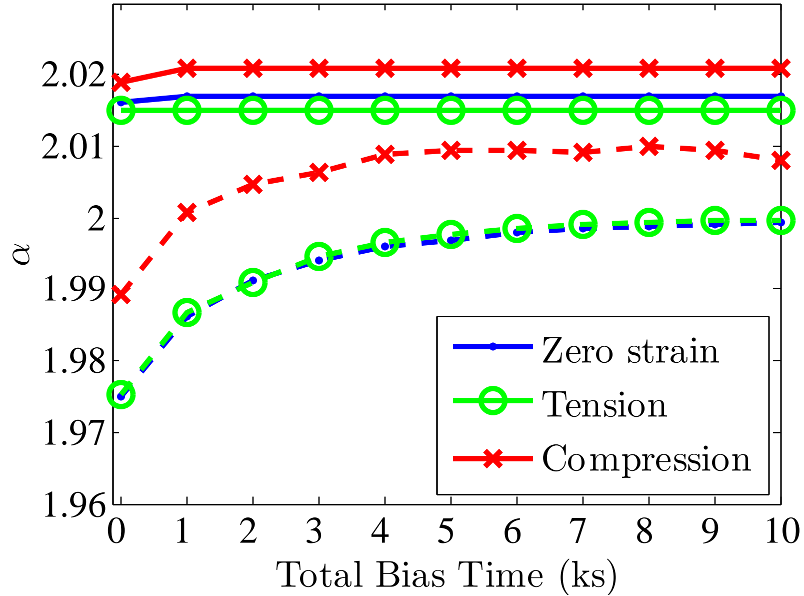

Figure 4.4: α vs. total bias stress time (initial values are plotted with dashed lines)

the initial α. The slight increase in α over the first 1000 s of bias stress for the unstrained and compression cases is most likely an artefact of extraction caused by this correlation.

Figure 4.2c shows that V_T increases slightly with both applied tension and compression, and with a somewhat more pronounced effect for tension. Figure 4.5 shows the V_T shift over 10000 s bias stress time for the various cases of applied strain. The V_T shift over long-term bias stress is highest for compression, which is in accordance with the hypothesis of increased defect creation under compression due to bond breaking as discussed in Section 2.4.2. Although the V_T increased slightly with the initial application of tension, the magnitude of shift under bias stress is slightly lower for TFTs under tension than for unstrained TFTs. This could be a sign of decreased defect creation due to the slight elongation and strengthening of Si-Si bonds. Alternately, the tension could be relieving some of the intrinsic compressive stress in the a-Si:H film, leading to the same effect.

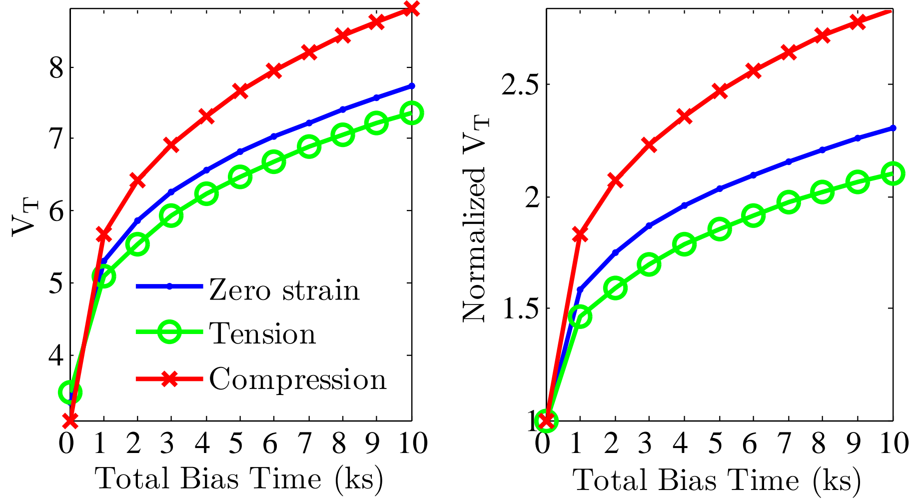

Figure 4.5: V_T and normalized V_T vs. total bias stress time

Figure 4.2d indicates that μ_{eff} decreases with compression, and increases with tension. This corresponds to the trends in field-effect mobility previously reported by multiple groups [15, 30]. The plot of μ_{eff} versus bias stress time in Figure 4.6 shows a faster rate of decrease under tension and compression, while μ_{eff} for the unstrained case remains relatively constant. Both types of strain result in lower final values of μ_{eff} than for zero applied strain, with the lowest value for compression. This may again indicate increased defect state creation over bias stress time for both strained cases, with a greater impact with compression than tension. Greater disorder is induced by increased bond-breaking in the a-Si:H and increases the scattering of electrons, thus lowering the effective mobility. From the derivation of the model equations, μ_{eff} is defined as

$$\mu_{eff} = \mu_{band} \frac{N_{fi}}{N_{ti}^{\frac{\alpha}{2}}} N_o^{\left[\frac{\alpha}{2}-1\right]} \tag{4.5}$$

where N_{fi} and N_{ti} are respectively the concentrations of free and trapped electrons in the a-Si:H with no band bending. N_o and α are as previously defined. α was determined to be

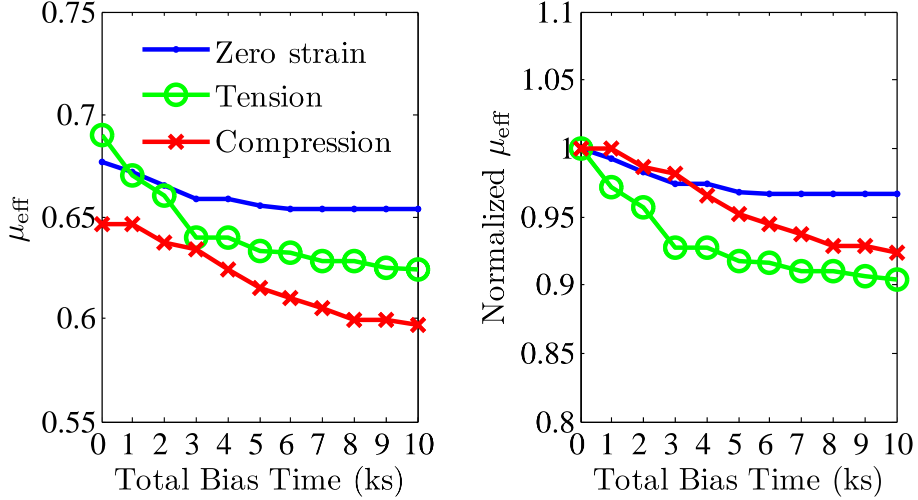

Figure 4.6: μ_{eff} and normalized μ_{eff} vs. total bias stress time

roughly constant. u_{band} decreases with the level of disorder in the material which agrees with the data and above explanation. The decrease in μ_{eff} can be further accelerated by an increase in the ratio of trapped versus free carriers, due to increased trapping in either the a-Si:H or a-SiNx:H.

Figure 4.7 shows semi-log plots of transfer characteristics under various strain conditions. The direction of the arrows indicate data taken at increasing lengths of bias stress time, up to a total of 10000 s. From Figure 4.8, the subthreshold swing S_f seems to improve slightly over the bias stress time. There is only a slight difference between all the strain cases, and the variation may not be statistically significant. The general decrease in S_f reinforces that no upper bandgap defect states (Dh) are being created with positive bias stress. The change in S_f could also be an artefact of the extraction. A gradual decrease in I_{off} with bias stress was apparent for TFTs under compression or zero strain as seen in Figure 4.7, which could lead to lower extracted values of S_f. A lower I_{off} could suggest an increased density of trapped charge in the dielectric which would hinder electron accu-

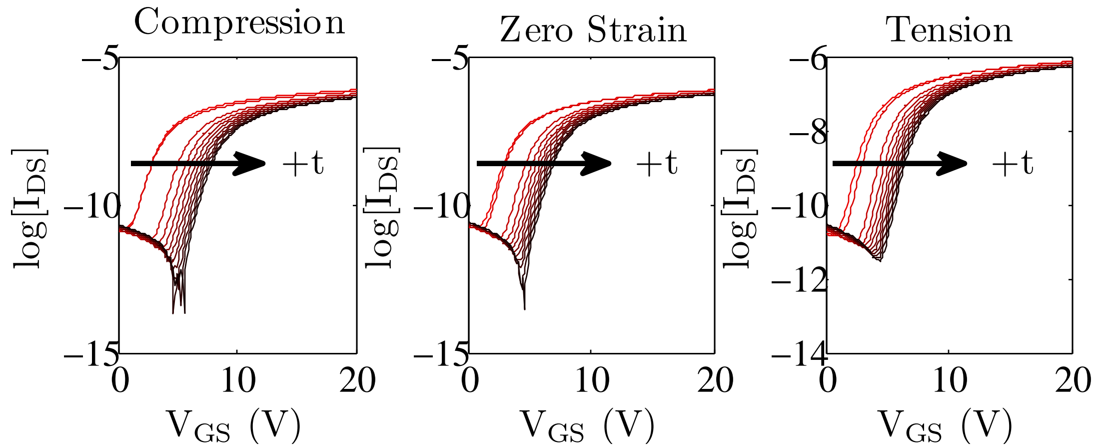

Figure 4.7: Data for S_f extraction

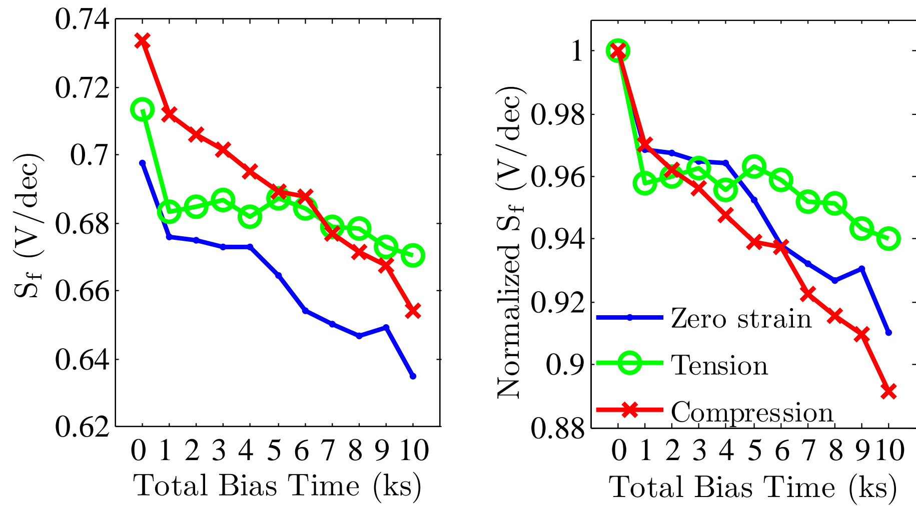

Figure 4.8: S_f and normalized S_f vs. total bias stress time

mulation at low bias. Therefore strain may increase charge injection to the a-SiNx:H with prolonged bias stress.

4.2 Bias stress degradation and recovery

Figure 4.9 shows a sample of experimental data obtained from a bias stress and recovery

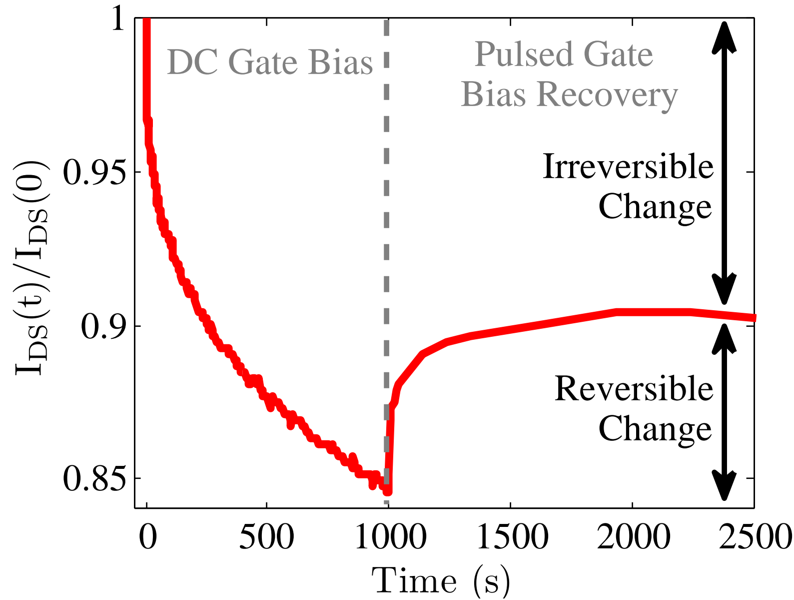

Figure 4.9: Example of bias stress degradation and recovery data

measurement as described in Section 3.3. The drain current shows the percentage of degradation over time while a constant gate bias is applied. For all measurements, devices were kept in the linear region of operation, such that the TFT drain-source current would remain approximately linearly proportional to $V_{GS} - V_T$. The devices exhibited excellent uniformity and a constant gate bias of 20 V was used in all measurements, with a low drain voltage of 0.1 V.

From curve fitting to the model equations in Section 4.1, R_{DS} was determined to be on the order of 10^5 Ω at maximum, while measured values of I_{DS} were on the order of 10^{-8} A. Therefore $V_{DS} >> R_{DS}I_{DS}$ and it can be assumed that the influence from contact

resistance is insignificant. The parameter alpha was found to be roughly equal to 2, and remained fairly constant over bias stress time. Therefore, the TFT current for linear operation from Equation 2.8 can be simplified as:

$$I_{DS,lin} = \mu_{eff} C_i \frac{W}{L_{eff}} (V_{GS} - V_T) V_{DS} \tag{4.6}$$

The change in the normalized drain current can then be used to determine the V_T shift of a given device by the following relation:

$$\Delta V_T = \left[1 - \frac{I_{DS,lin}(t) g_{m0}}{I_{DS,lin}(0) g_m} \right] (V_{GS} - V_{T0}) \tag{4.7}$$

The gate bias is removed after 1000 s in the example shown in Figure 4.9, and the drain current is shown to partially recover. The current rises rapidly once the bias is removed, then quickly settles to a maximum value that stays fairly constant for several hours. The proportion of the current that is recovered can be considered an indicator of a 'reversible' shift in V_T, while the amount of current not recovered essentially marks a permanent change in terms of practical device operation [43].

The exact physical origins of the instability in V_T are not revealed by the measurement data. Figure 4.10 shows a log-log plot of V_T shift over 1000 s of bias stress time for TFTs under different strain conditions. The data after ∼200 s of bias stress follows a power-law time dependence, as it appears roughly linear on the plot. As explained in Section 2.4, this could be due to defect creation and/or charge trapping into multiple states with subsequent redistribution. The non-linearity near the beginning of the bias stress time suggests that a different mechanism of charge trapping is dominant at small time scales. The data also shows a slight decrease near the end of the bias stress period. This is likely due to the change in overdrive voltage ($V_{GS} - V_T$) caused by the increase in V_T over time. Therefore it is recommended that further measurements be taken using a higher value of V_{GS} or with constant-current bias stress.

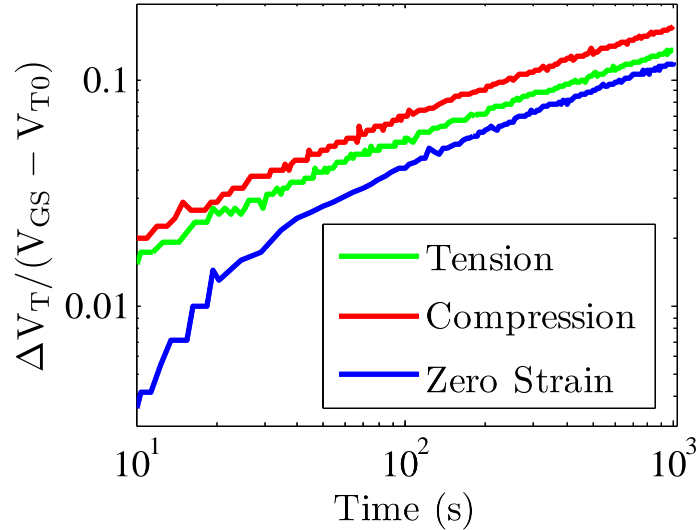

Figure 4.10: Log-log plot of normalized V_T shift over 1000 s bias stress

However, it is possible to characterize the proportion of V_T shift as reversible or irreversible by examining the recovery of the stressed TFTs. It has been established that V_T shift is due to charge trapping either into the gate dielectric or into defects created within the semiconductor channel while the device is under bias stress. The trapped charges can be classified as being in reversible or 'fast' states that readily trap and detrap carriers to the extended conduction states, or in irreversible 'slow' states that do not easily release the trapped charges. Fast states include shallow traps in the gate dielectric close to the top interface and defect states in the semiconductor channel with low energy barrier height. Slow states include traps deep in the dielectric which have a lower probability of carrier tunnelling, and defect states in the a-Si:H with a high energy barrier to formation.

Figure 4.11 shows measurement results for devices subjected to 100 s of applied electrical bias stress. The devices appeared to degrade about the same amount for the unstrained TFTs and the TFTs under tension or compression. The amount of current and magnitude

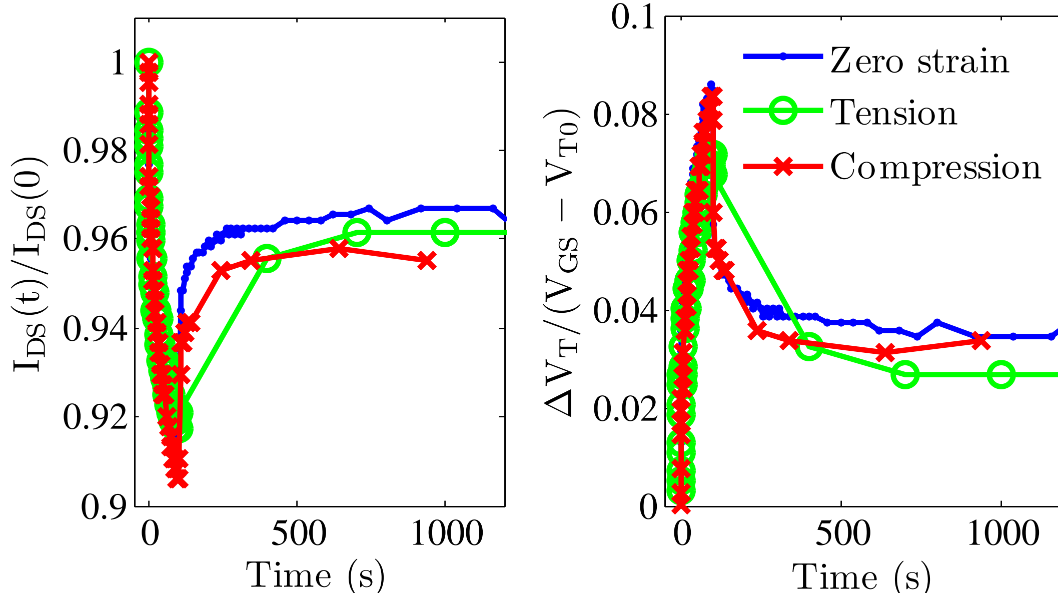

Figure 4.11: Normalized I_{DS} and normalized V_T shift for 100 s bias stress and recovery

of V_T shift recovered after removing the bias stress was almost identical for all three cases as well.

After 1000 s of bias stress time, Figure 4.12 shows that the devices under tension degraded a similar amount as unstrained devices, while TFTs under compressive strain showed greater degradation in comparison. The proportion of V_T shift recovered after the bias stress period was again similar for all three cases, but was slightly lower for the strained cases than for unstrained by a difference or roughly 10%. The percentage of reversible V_T shift for each test case is summarized in Table 4.2.

Figure 4.13 shows the current degradation and V_T shift for devices measured in 1000 s intervals for a total bias time of 10000 s. The brief interruptions allowed transfer characteristics to be measured between the intervals. Again, the current degradation and V_T shift were notably more significant for devices under compressive strain than for tension

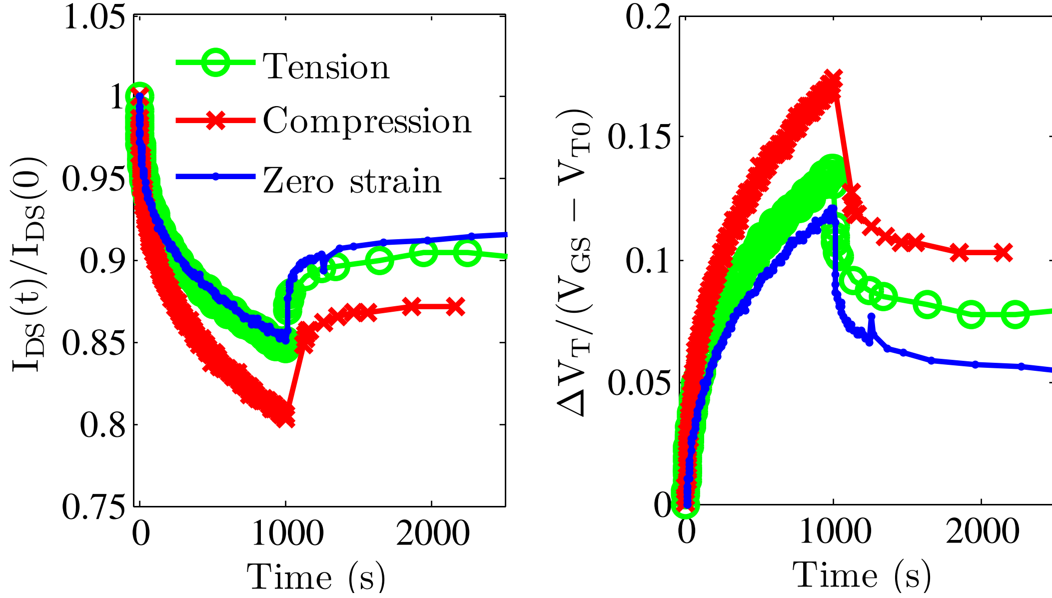

Figure 4.12: Normalized I_{DS} and normalized V_T shift for 1000 s bias stress and recovery

or zero strain. This trend corresponds with the plot of V_T shift derived earlier through curve-fitting of the transfer characteristics.

Table 4.1 and 4.2 summarize the magnitude of V_T shift and recovery observed for the

Table 4.1: Percent threshold voltage shift

Bias time (s)	Unstrained	Tension	Compression
100	8.6	7.1	8.3
1000	12	14	17
10000	27	24	35

various bias stress times and strain conditions. At shorter bias times, the percentages of degradation were roughly the same for the various strain cases. However, the amount of V_T shift for devices under compression becomes much greater with longer bias stress time

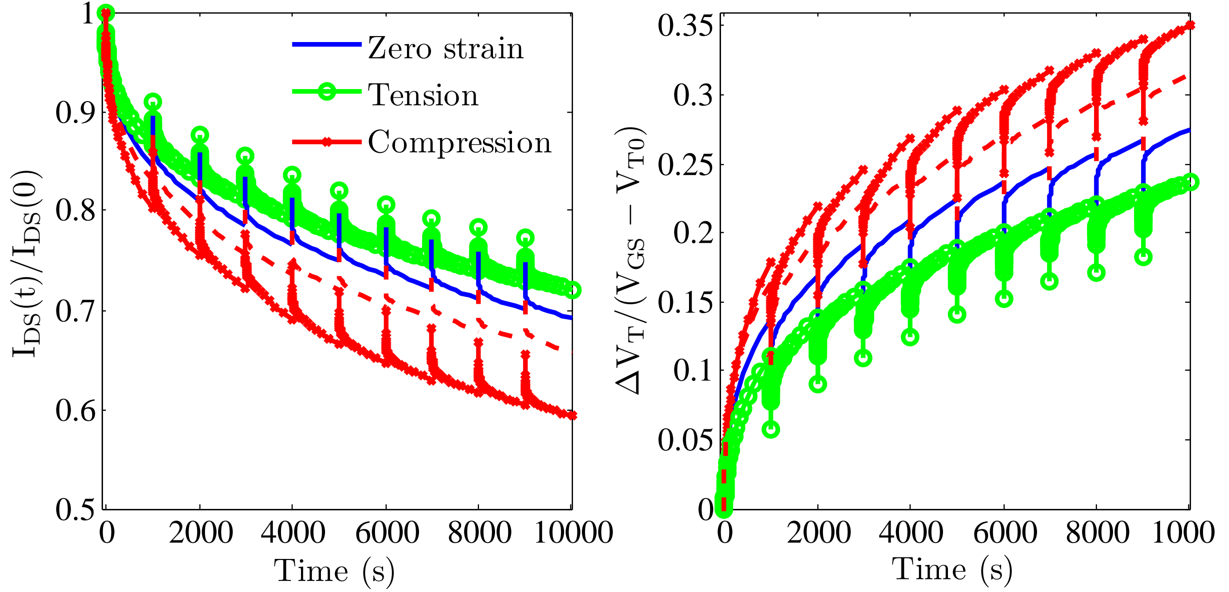

Figure 4.13: Normalized I_{DS} and V_T shift for 10000 s bias stress and recovery; dotted line is for a device with W/L = 200/8 instead of 200/16

Table 4.2: Percent of threshold voltage shift recovered

Bias time (s)	Unstrained	Tension	Compression
100	60	63	63
1000	54	44	41

when compared to devices under tension or zero strain. Overall, devices under tension seemed to have the same or slightly lower instability than the unstrained TFTs. The data suggests that strain does not affect TFT instability for low bias stress times of ∼100 s, but becomes more significant with longer times. Compressive strain seems to cause increased V_T shift while tension slightly decreases V_T shift over long bias stress times.

The recovery data indicates that for low bias times, the TFT instability is mostly

reversible. The large magnitude of recovery points towards shallow charge trapping rather than defect creation as the main mechanism of instability at 100 s and 1000 s [43]. The percentage of recovery is significantly higher for the 100 s stress case than compared to the 1000 s case, which suggests that irreversible changes such as deep a-SiNx:H trapping and a-Si:H defect creation gradually become the dominant instability mechanisms over longer bias stress times.

The 100 s data shows a slightly greater amount of recovery for TFTs in tension and compression than for zero strain. It is unclear if this signifies that strain increases shallow charge trapping in the nitride, which is the main mechanism of instability at lower stress times. Since only a small amount of instability was observed during conditions in which charge trapping was dominant, the experiment should be repeated with higher bias stress such that trapping becomes the main mechanism of instability. Subsequently, TFTs should be observed for longer bias stress times to see if strain has an effect on charge trapping.

The trend in V_T recovery is reversed at 1000 s, with the strained devices showing lower recovery than for the unstrained devices. As discussed previously, both compression and tension can increase the rate of defect creation by weakening Si-Si bonds. This corresponds to the lower recovery for the strained cases at longer bias stress times when irreversible changes become more apparent. The recovery is slightly higher for tension than for compression, possibly because of intrinsic compressive stress in a-Si:H film cancelling out some of the applied tension and causing a slightly lower rate of defect creation. Tension can also strengthen some proportion of Si-Si bonds in the a-Si:H, as discussed in Section 2.4.2.

In addition, Figure 4.13 shows that the normalized V_T shift was lower for devices with a shorter channel length. As the devices were similar in all other regards, the trends discussed above are likely due to the material properties of the a-Si channel and gate dielectric as anticipated. The longer conduction path and greater dielectric area increases

the degradation and strain-related effects for the longer devices. The differences observed in TFT behaviour under various strain and bias stress time are unlikely to originate from the drain/source contacts or metal traces as these are constant across the TFTs tested since the devices share a common width. However, it is recommended that a greater number of devices with larger variation in channel length be measured to confirm this trend and to verify that the results are statistically significant.

4.3 Modelling of trapping

The charge trapping into fast reversible and slow irreversible states as described in the previous section can be modelled as a Markov system as shown in Figure 4.14 [44]. It is assumed that holes do not have significant influence due to their low mobility in a-Si [10], and only electrons are considered as carriers. State 1 represents fast trap states and State 2 represents slow trap states, with $n_1(t)$ and $n_2(t)$ being the number of trapped electrons in each state at time t. The total number of electrons in the system is $N(t)$. The number of free electrons in the conduction band is given by $N(t) - n_1(t) - n_2(t)$. r_{ij} are constants that represent the rate at which carriers pass from State i to State j. It is assumed that there is a negligible rate of detrapping from the slow states.

The system can be expressed as the following set of rate equations:

$$\begin{aligned} \frac{dn_1(t)}{dt} &= (r_{01})[N(t) - n_1(t) - n_2(t)] + (-r_{10} - r_{12})n_1(t) \\ \frac{dn_2(t)}{dt} &= (r_{02})[N(t) - n_1(t) - n_2(t)] + (r_{12})n_1(t) \end{aligned} \tag{4.8}$$

It can be assumed the rate of free carriers becoming trapped in fast traps is much greater than the rate of carriers moving from fast traps to slow traps, as hopping from shallow to deep traps in the dielectric is unlikely at the relatively low bias stress times, V_{GS} and

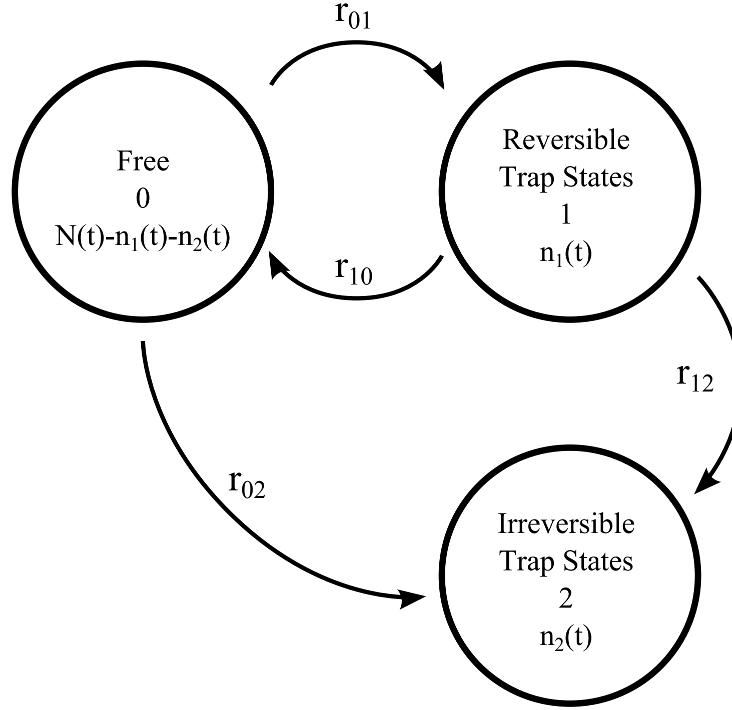

Figure 4.14: Markov model of trapping

temperature used in this experiment [25]. Therefore it is assumed that r_{12} is very small, and the equations can be simplified. Letting $\alpha = r_{01}$, $\beta = r_{10}$ and $\gamma = r_{02}$, the equations can be expressed as:

$$\frac{d\vec{n}(t)}{dt} = \begin{bmatrix} -\alpha - \beta & -\alpha \\ -\gamma & -\gamma \end{bmatrix} \vec{n}(t) + \begin{bmatrix} \alpha \\ \gamma \end{bmatrix} N(t) \tag{4.9}$$

where

$$\vec{n}(t) = \begin{bmatrix} n_1(t) \\ n_2(t) \end{bmatrix}$$

It is assumed there are no trapped charges initially and $n_1(0) = n_2(0) = 0$. Since a constant gate voltage bias stress is used, $N(t) = [(V_{GS} - V_{T0})C_i/q]u(t)$ where $u(t)$ is the

unit step function. Solving the system for $n_1(t)$ and $n_2(t)$, the total V_T shift can then be obtained from the total amount of trapped charge:

$$\begin{aligned}\Delta V_T(t) &= \frac{q}{C_i}[n_1(t)+n_2(t)] \\ &= (V_{GS}-V_{T0})[1-(1-\varphi)e^{\lambda_1 t}-\varphi e^{\lambda_2 t}]\end{aligned} \tag{4.10}$$

where $2\lambda_1 = -p+q$, $2\lambda_2 = -p-q$ and $2\varphi = (p-2\beta+q)/q$, with $p = \alpha+\beta+\gamma$ and $q = \sqrt{p^2-4\beta\gamma}$. For $\lambda_1 >> \lambda_2$, the λ_1 and λ_2 coefficients are related to the rates of fast and slow trapping respectively, while φ a factor indicating the proportion of slow versus fast trapping [44].

It is possible to solve for the rates of reversible and irreversible trapping by extracting λ_1, λ_2 and φ from the measured data. Using the first-order Taylor series approximation of the exponential terms in Equation 4.10, the change in ΔV_T for fast time scales of $t \approx 1/\lambda_1$ is approximately $-(V_{GS}-V_{T0})(1-\varphi)\lambda_1$. For long time scales where $t \approx 1/\lambda_2$, the tangent line to ΔV_T has a slope of approximately $-(V_{GS}-V_{T0})\varphi\lambda_2$ and a y-intercept of $(V_{GS}-V_{T0})(1-\varphi)$. Figure 4.15 illustrates the graphical extraction process.

The calculated threshold voltage shift over 10000 s of bias stress time from Figure 4.13 was used. For the fast time scale fitting, the g_m measured before each measurement interval was used in the calculation of V_T shift. Otherwise, the g_m from the end of each interval was used. Also, each 1000 s measurement interval is considered independently from the last, i.e. n(0) = 0 is assumed at the beginning of each interval. The rates of trapping into each state are plotted in the following figures. Normalized values have also been plotted in order to compare the relative rate of change of the parameters.

The magnitudes of r_{01} and r_{10} which are associated with fast trapping and detrapping are much higher than the rate of slow trapping, r_{02}, as would be expected by definition. There is not much change in r_{01} and r_{10} over bias stress time except for the beginning of

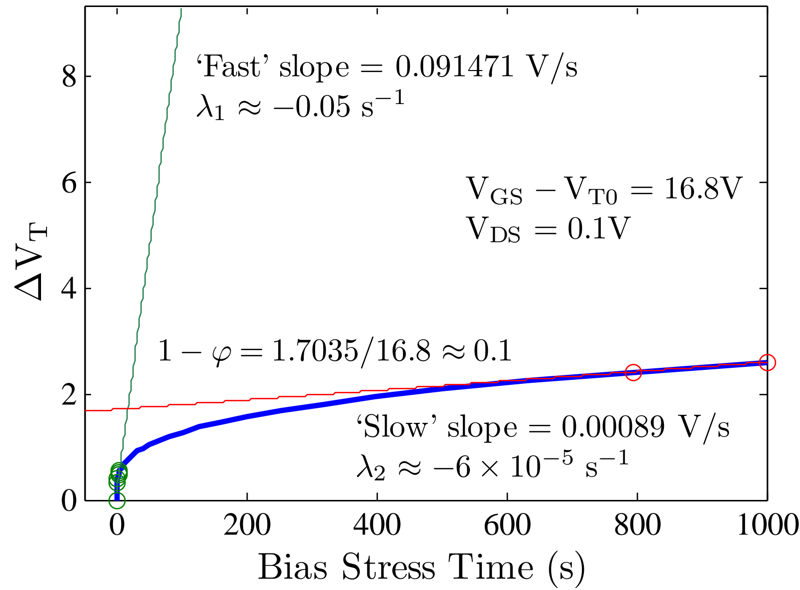

Figure 4.15: Sample calculation of λ_1, λ_2 and φ from measured V_T shift

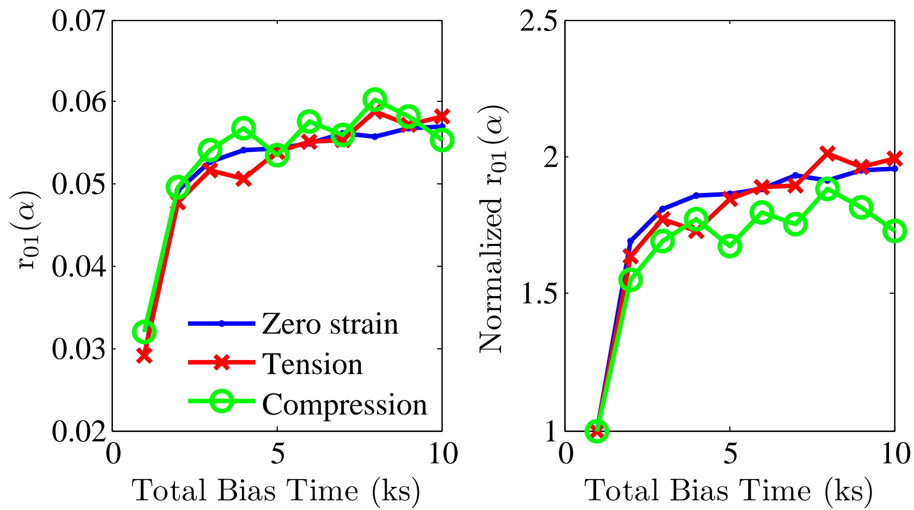

Figure 4.16: Values and normalized values for r_{01}

the measurement, since the charge trapping occurs at a fast time scale. The slight increase after 1000 s could be interpreted as due to the number of fast traps from the ongoing defect

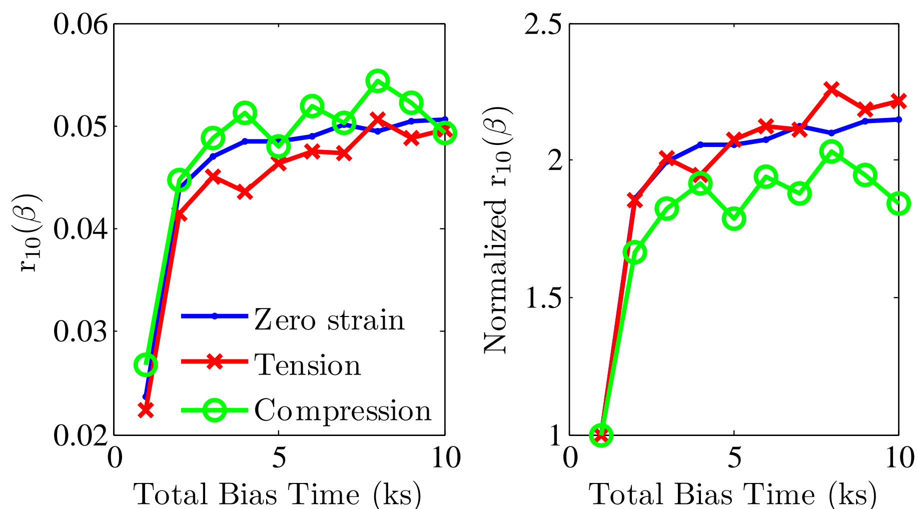

Figure 4.17: Values and normalized values for r_{10}

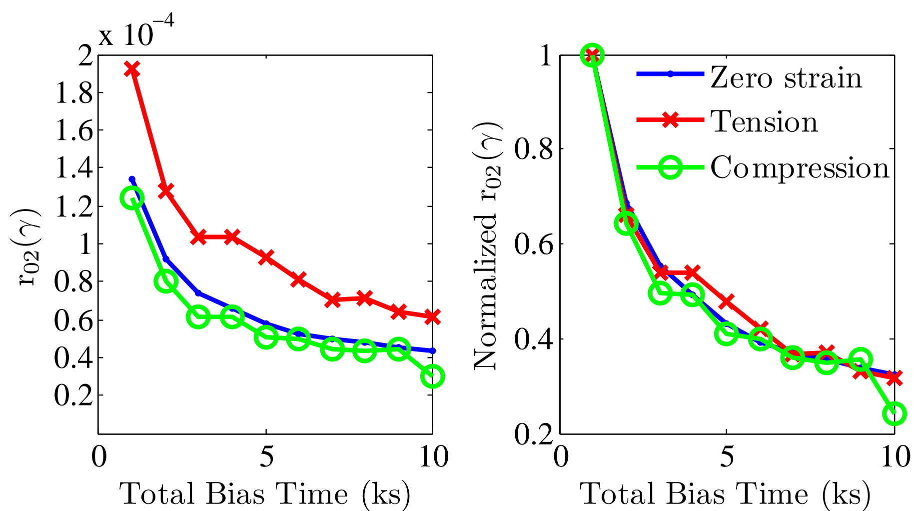

Figure 4.18: Values and normalized values for r_{02}

creation (e.g. states with barrier heights in the low end of the gaussian distribution).

From Figures 4.16 and 4.17, r_{01} is similar in magnitude but higher than r_{10}, indicating net trapping into reversible states over the bias stress time, i.e. some of the fast states are

not being reversed over the course of the measurement. This is probably because there was only a very small delay between measurements, preventing a full recovery. The difference and normalized difference between r_{01} and r_{10} is plotted in Figure 4.19. The magnitude

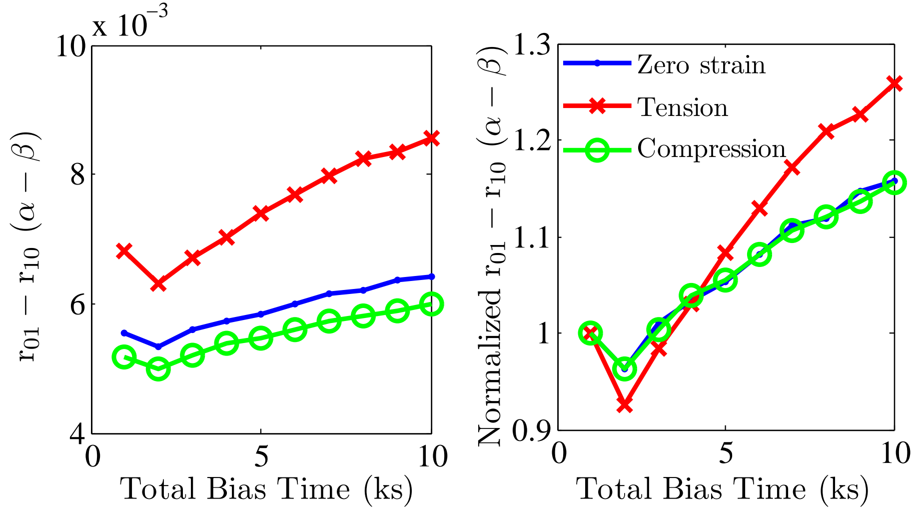

Figure 4.19: Values and normalized values for $r_{01} - r_{10}$

of $r_{01} - r_{10}$ is greatest with TFTs in compression and lower for zero strain and tension. From the normalized plot, the increase is also greater over time for compression than for the other cases. This could likewise be attributed to the slight increase of fast defect states with compression.

Figure 4.18 shows that r_{02} is greatest in magnitude for the compression case, and lower for tension and zero strain. The normalized plot shows that the rate of defect creation is similar between all cases, with a slight decrease for the tension case near the end of the 10000 s. These trends match the previous observations that irreversible defect creation is greatest with compression, and lower with zero strain, with tension possibly decreasing the rate of defect creation even further. The values of r_{02} decrease over bias stress time, indicating that the rate of defect creation gradually saturates as weak bonds are converted

into defects and eventually reach an equilibrium.

Chapter 5

Conclusions

Several conclusions have been made regarding the effect of mechanical strain on TFT electrical instability.

Although both charge trapping and defect creation occur simultaneously, each mechanism of instability appears to dominate at different bias stress times. Charge trapping in the a-SiNx:H close to the semiconductor-dielectric interface is the main contributing mechanism to TFT instability at short bias stress times of about 100 s. Defect creation becomes more significant at longer bias stress times of over 10000 s. TFT performance was not observed to be significantly impacted by strain at short bias stress times, suggesting that the rate of dielectric charge trapping is unaffected by strain. This is supported by bias stress and recovery data and also parameters obtained from a Markov model for V_T shift. However, only a small amount of instability was observed during conditions in which charge trapping was dominant. The experiment should be repeated with higher bias stress such that trapping becomes the main mechanism of instability. Subsequently, TFTs should be observed for longer bias stress times to see if strain has an effect. Strain appears

to have a more significant impact on the rate of defect creation in a-Si:H over long-term bias stress. Both tension and compression increased defect creation compared to TFTs with zero applied strain, according to the extracted values of μ_{eff} and V_T recovery data at longer bias stress times. Parameters extracted from the Markov model and the higher degradation seen in bias stress measurements indicate that compression increases the defect formation rate the most, likely by weakening Si-Si bonds. Tension appears to cause a less significant increase in the defect creation rate. This could be due to a strengthening of some proportion of the Si-Si bonds due to slight elongation of bond length or because the applied tension relieves intrinsic compressive stress in a-Si:H film.

From measurement of TFTs with different channel lengths, a longer conduction path and greater dielectric area appears to increase the bias-stress and strain-related effects. Therefore smaller devices should be less affected by strain and bias stress.

It is recommended that more accurate TFT parameter extraction be done in future by measuring a greater number of devices with larger variation in channel length, in order to verify that the results are statistically significant. Data should also be collected for higher gate voltage biases and constant-current measurements. Further study is also recommended to rule out the presence of any micro-cracking.

References

[1] M. Heintze and W. E. Spear, "The effects of linear strain on the electronic-properties of glow-discharge amorphous-silicon," *Journal of Non-Crystalline Solids*, vol. 77-8, pp. 495–498, DEC 1985 1985. PT: J; PN: Part 1; TC: 9; UT: WOS:A1985AXX2200109.

[2] M. J. Powell, "Charge trapping instabilities in amorphous silicon-silicon nitride thin-film transistors," *Applied Physics Letters*, vol. 43, pp. 597–599, 1983 1983. PT: J; TC: 176; UT: WOS:A1983RG78000030.

[3] M. J. Powell, S. C. Deane, and R. B. Wehrspohn, "Microscopic mechanisms for creation and removal of metastable dangling bonds in hydrogenated amorphous silicon," *Physical Review B*, vol. 66, p. 155212, OCT 15 2002 2002. PT: J; TC: 15; UT: WOS:000179080800077.

[4] M. J. Powell, C. Vanberkel, A. R. Franklin, S. C. Deane, and W. I. Milne, "Defect pool in amorphous-silicon thin-film transistors," *Physical Review B*, vol. 45, pp. 4160–4170, FEB 15 1992 1992. PT: J; TC: 160; UT: WOS:A1992HF82800024.

[5] S. A. Stauth and B. A. Parviz, "Self-assembled single-crystal silicon circuits on plastic," *Proceedings of the National Academy of Sciences of the United States of*

America, vol. 103, pp. 13922–13927, SEP 19 2006 2006. PT: J; TC: 64; UT: WOS:000240746600006.

[6] *Flexible electronics materials and applications.* New York: Springer, 2009. ID: vtug4154693; Includes bibliographical references and index.

[7] D. R. Allee, S. Venugopal, R. Krishna, K. Kaftanoglu, M. A. Quevedo-Lopez, S. Gowrisanker, A. E. Avendano-Bolivar, H. N. Alshareef, and B. Gnade, *Flexible CMOS and Electrophoretic Displays.* 2009 2009. PT: B; CT: 47th Annual Symposium of the Society-for-Information-Display; CY: MAY 31-JUN 05, 2009; CL: San Antonio, TX; SP: Soc Informat Display; TC: 0; UT: WOS:000272997600196.

[8] A. Sazonov, M. Meitine, D. Stryakhilev, and A. Nathan, "Low-temperature materials and thin-film transistors for electronics on flexible substrates," *Semiconductors*, vol. 40, pp. 959–967, AUG 2006. PT: J; UT: WOS:000239563600015.

[9] C. R. Kagan and P. Andry, *Thin-film transistors.* New York: Marcel Dekker, 2003.

[10] R. A. Street, *Hydrogenated amorphous silicon.* Cambridge: Cambridge University Press, 1991.

[11] N. F. N. Mott, *Electronic Processes in Non-Crystalline Materials.* Oxford : Clarendon Press, 1979; Oxford : New York: Clarendon Press ; Oxford University Press, 1979. Bibliography: P.(548)-582; Bibliography: p. [548]-582. ; Includes index.; ID: dedupmrg71166394.

[12] D. Monroe, "Hopping in exponential band tails," *Physical Review Letters*, vol. 54, pp. 146–149, 1985 1985. PT: J; TC: 322; UT: WOS:A1985TZ40200016.

[13] *Thin film resistive sensors.* Bristol: Institute of Physics Publishing, 1992. ID: vtug1170523; Includes bibliographical references and index.

[14] P. Servati and A. Nathan, "Orientation-dependent strain tolerance of amorphous silicon transistors and pixel circuits for elastic organic light-emitting diode displays," *Applied Physics Letters*, vol. 86, p. 033504, JAN 17 2005. PT: J; UT: ISI:000226864600083.

[15] H. Gleskova, P. I. Hsu, Z. Xi, J. C. Sturm, Z. Suo, and S. Wagner, "Field-effect mobility of amorphous silicon thin-film transistors under strain," *Journal of Non-Crystalline Solids*, vol. 338, pp. 732–735, JUN 15 2004. PT: J; CT: 20th International Conference on Amorphous and Microcrystalline Semiconductors; CY: AUG 25-29, 2003; CL: Campos do Jordao, BRAZIL; UT: ISI:000222219000164.

[16] D. Hong, G. Yerubandi, H. Q. Chiang, M. C. Spiegelberg, and J. F. Wager, "Electrical modeling of thin-film transistors," *Critical Reviews in Solid State and Materials Sciences*, vol. 33, pp. 101–132, APR-JUN 2008. PT: J; UT: WOS:000256917300001.

[17] P. Servati, D. Striakhilev, and A. Nathan, "Above-threshold parameter extraction and modeling for amorphous silicon thin-film transistors," *IEEE Transactions on Electron Devices*, vol. 50, pp. 2227–2235, NOV 2003. PT: J; UT: WOS:000186083800007.

[18] A. Nathan, P. Servati, and K. S. Karim, "Tft circuit integration in a-si : H technology," *2002 23rd International Conference on Microelectronics, Vols 1 and 2, Proceedings*, pp. 115–124, 2002 2002. PT: S; CT: 23rd International Conference on Micorelectronics; CY: MAY 12-15, 2002; CL: NISH, YUGOSLAVIA; SP: Yugoslavia IEEE Sect, ED/SSC Chapter; IEEE Electron Devices Soc; IEEE Solid State Circuits Soc; TC: 0; UT: WOS:000176359700017.

[19] A. R. Merticaru, A. J. Mouthaan, and F. G. Kuper, "Determination of the contribution of defect creation and charge trapping to the degradation of a-si : H/sin tfts at room temperature and low voltages," *Journal of Non-Crystalline Solids*, vol. 352, pp. 3849–3853, OCT 1 2006 2006. PT: J; TC: 0; UT: WOS:000241098800014.

[20] C. Vanberkel and M. J. Powell, "Resolution of amorphous-silicon thin-film transistor instability mechanisms using ambipolar transistors," *Applied Physics Letters*, vol. 51, pp. 1094–1096, OCT 5 1987 1987. PT: J; TC: 107; UT: WOS:A1987K198600016.

[21] A. A. Fomani and A. Nathan, "Metastability mechanisms in thin film transistors quantitatively resolved using post-stress relaxation of threshold voltage," *Journal of Applied Physics*, vol. 109, p. 084521, APR 15 2011. PT: J; UT: WOS:000290047000219.

[22] A. V. Ferrisprabhu, "Charge-transfer by direct tunneling in thin-oxide memory transistors," *IEEE Transactions on Electron Devices*, vol. 24, pp. 524–530, 1977 1977. PT: J; TC: 20; UT: WOS:A1977DE30200004.

[23] D. Monroe, "Hopping in exponential band tails," *Phys. Rev. Lett.*, vol. 54, pp. 146–149, Jan 1985.

[24] F. W. Schmidlin, "Theory of trap-controlled transient photoconduction," *Phys. Rev. B*, vol. 16, pp. 2362–2385, Sep 1977.

[25] F. LIBSCH and J. KANICKI, "Bias-stress-induced stretched-exponential time-dependence of charge injection and trapping in amorphous thin-film transistors," *Applied Physics Letters*, vol. 62, pp. 1286–1288, MAR 15 1993. PT: J; UT: WOS:A1993KR57400039.

[26] A. J. Flewitt, S. Lin, W. I. Milne, R. B. Wehrspohn, and M. J. Powell, "Mechanisms for defect creation and removal in hydrogenated and deuterated amorphous silicon studied

using thin film transistors," *Amorphous and Polycrystalline Thin-Film Silicon Science and Technology 2006*, vol. 910, pp. 449–460, 2007 2007. PT: S; CT: Symposium on Amorphous and Polycrystalline Thin-Film Silicon Science and Technology held at the 2006 MRS Spring Meeting; CY: APR 18-21, 2006; CL: San Francisco, CA; SP: Mat Res Soc; TC: 0; UT: WOS:000245670700064.

[27] R. Wehrspohn, S. Deane, I. French, I. Gale, J. Hewett, M. Powell, and J. Robertson, "Relative importance of the si-si bond and si-h bond for the stability of amorphous silicon thin film transistors," *Journal of Applied Physics*, vol. 87, pp. 144–154, JAN 1 2000. PT: J; UT: WOS:000084244300021.

[28] C. VANDEWALLE and N. NICKEL, "Energetics of bond-centered hydrogen in strained si-si bonds," *Physical Review B*, vol. 51, pp. 2636–2639, JAN 15 1995. PT: J; UT: WOS:A1995QF33900087.

[29] H. Gleskova and S. Wagner, "Electrical response to uniaxial tensile strain of a-si : H tfts fabricated on polyimide foils," *Journal of Non-Crystalline Solids*, vol. 354, pp. 2627–2631, MAY 1 2008. PT: J; CT: 22nd International Conference on Amorphous and Nanocrystalline Semiconductors; CY: AUG 19-24, 2007; CL: Breckenridge, CO; UT: ISI:000256500400123.

[30] S. H. Won, J. K. Chung, C. B. Lee, H. C. Nam, J. H. Hur, and J. Jang, "Effect of mechanical and electrical stresses on the performance of an a-si : H tft on plastic substrate," *Journal of the Electrochemical Society*, vol. 151, pp. G167–G170, MAR 2004 2004. PT: J; TC: 30; UT: WOS:000188943800056.

[31] W. B. Jackson, “Role of band-tail carriers in metastable defect formation and annealing in hydrogenated amorphous-silicon,” *Physical Review B*, vol. 41, pp. 1059–1075, JAN 15 1990 1990. PT: J; TC: 68; UT: WOS:A1990CJ62400021.

[32] J. HUTCHINSON and Z. SUO, “Mixed-mode cracking in layered materials rid b-1221-2008 rid b-1067-2008,” *Advances in Applied Mechanics, Vol 29*, vol. 29, pp. 63–191, 1992. PT: J; UT: WOS:A1992BZ96U00002.

[33] H. Gleskova, S. Wagner, and Z. Suo, “Failure resistance of amorphous silicon transistors under extreme in-plane strain,” *Applied Physics Letters*, vol. 75, pp. 3011–3013, NOV 8 1999. PT: J; UT: ISI:000083483900047.

[34] H. Gleskova, S. Wagner, W. Soboyejo, and Z. Suo, “Electrical response of amorphous silicon thin-film transistors under mechanical strain rid b-1067-2008,” *Journal of Applied Physics*, vol. 92, pp. 6224–6229, NOV 15 2002. PT: J; UT: WOS:000178987200100.

[35] H. Gleskova and S. Wagner, “Electron mobility in amorphous silicon thin-film transistors under compressive strain,” *Applied Physics Letters*, vol. 79, pp. 3347–3349, NOV 12 2001. PT: J; UT: ISI:000172046800045.

[36] H. Gleskova, S. Wagner, W. Soboyejo, and Z. Suo, “Effects of mechanical strain on amorphous silicon thin-film transistors,” *Amorphous and Heterogeneous Silicon-Based Films-2002*, vol. 715, pp. 667–677, 2002. PT: S; CT: Symposium on Amorphous and Heterogeneous Silicon-Based Films held at the 2002 MRS Spring Meeting; CY: APR 02-05, 2002; CL: SAN FRANCISCO, CA; UT: ISI:000179162400096.

[37] M.-H. Lee, S.-T. Chang, Y.-C. Wu, M. Tang, and C.-Y. Lin, “Mechanical bending cycles of hydrogenated amorphous silicon layer on plastic substrate by plasma-enhanced

chemical vapor deposition for use in flexible displays," *Japanese Journal of Applied Physics*, vol. 48, p. 021301, FEB 2009. PT: J; UT: WOS:000264955900039.

[38] D. K. Schroder, *Semiconductor material and device characterization.* Piscataway, NJ : Hoboken, N.J.: IEEE Press ; Wiley, 2006. ID: vtug3978570; Includes bibliographical references and index.

[39] A. Ortiz-Conde, F. J. G. Sanchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent mosfet threshold voltage extraction methods," *Microelectronics Reliability*, vol. 42, pp. 583–596, APR-MAY 2002 2002. PT: J; TC: 74; UT: WOS:000176465800011.

[40] Z. Tang, M. S. Park, S. H. Jin, and C. R. Wie, "Drain bias dependent bias temperature stress instability in a-si:h tft," *Solid-State Electronics*, vol. 53, pp. 225–233, FEB 2009 2009. PT: J; TC: 8; UT: WOS:000263596100021.

[41] P. Servati, *Experimental characterization and parameter extraction for amorphous silicon thin-film transistors.* Waterloo, Ont.: Dept. of Electrical and Computer Engineering, University of Waterloo, 2002. ID: vtug3327857; Includes bibliographical references (leaves 18-19).

[42] M. C. Wang, T. C. Chang, P.-T. Liu, S. W. Tsao, and J. R. Chen, "Analysis of parasitic resistance and channel sheet conductance of a-si : H tft under mechanical bending," *Electrochemical and Solid State Letters*, vol. 10, no. 3, pp. J49–J51, 2007. PT: J; UT: WOS:000243583700041.

[43] A. Salleo, F. Endicott, and R. Street, "Reversible and irreversible trapping at room temperature in poly(thiophene) thin-film transistors," *Applied Physics Letters*, vol. 86, p. 263505, JUN 27 2005. PT: J; UT: WOS:000230090000069.

[44] S. Sambandan, L. Zhu, D. Striakhilev, P. Servati, and A. Nathan, “Markov model for threshold-voltage shift in amorphous silicon tfts for variable gate bias,” *IEEE Electron Device Letters*, vol. 26, pp. 375–377, JUN 2005. PT: J; UT: WOS:000229522000011.