Energy Efficient Techniques For Algorithmic Analog-To-Digital Converters

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Analog-to-digital converters (ADCs) are key design blocks in state-of-art image, capacitive, and biomedical sensing applications. In these sensing applications, algorithmic ADCs are the preferred choice due to their high resolution and low area advantages. Algorithmic ADCs are based on the same operating principle as that of pipelined ADCs. Unlike pipelined ADCs where the residue is transferred to the next stage, an N-bit algorithmic ADC utilizes the same hardware N-times for each bit of resolution. Due to the cyclic nature of algorithmic ADCs, many of the low power techniques applicable to pipelined ADCs cannot be directly applied to algorithmic ADCs. Consequently, compared to those of pipelined ADCs, the traditional implementations of algorithmic ADCs are power inefficient.

This thesis presents two novel energy efficient techniques for algorithmic ADCs. The first technique modifies the capacitors' arrangement of a conventional flip-around configuration and amplifier sharing technique, resulting in a low power and low area design solution. The other technique is based on the unit multiplying-digital-to-analog-converter approach. The proposed approach exploits the power saving advantages of capacitor-shared technique and capacitor-scaled technique. It is shown that, compared to conventional techniques, the proposed techniques reduce the power consumption of algorithmic ADCs by more than 85%.

To verify the effectiveness of such approaches, two prototype chips, a 10-bit 5 MS/s and a 12-bit 10 MS/s ADCs, are implemented in a 130-nm CMOS process. Detailed design considerations are discussed as well as the simulation and measurement results. According to the simulation results, both designs achieve figures-of-merit of approximately 60 fJ/step, making them some of the most power efficient ADCs to date.

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Dedication

In loving memory of my grandparents
Mr. and Mrs. Abdul Hai

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List of Symbols and Abbreviations

β	Feedback factor
τ	Time constant
C_{pi}	Input Parasitic Capacitance
C_{po}	Output Parasitic Capacitance
f_{3dB}	OTA's closed loop bandwidth
f_{in}	Input signal frequency
f_s	Sampling frequency
f_T	Unity gain frequency
n_f	Noise factor of the circuit
$\Sigma\Delta$ ADC	Sigma Delta Analog to Digital Converter
A_v	OTA DC gain
ADC	Analog-to-Digital Converter
C_f	Feedback Capacitor
C_s	Sampling Capacitor
CMOS	Complementary Metal Oxide Semiconductor
CS	Capacitor-shared
CSFA	Capacitor-shared flip-around
CSR	Capacitor-shared regular
DAC	Digital-to-Analog Converter
dB	Decibels
DNL	Differential Non-linearity
DR	Dynamic Range
DSP	Digital Signal Processing
ECG	Electrocardiogram
EEG	Electroencephalogram
ENOB	Effective Number of Bits
EOG	Electrooculogram
ERBW	Effective Resolution Bandwidth
FAOS	Flip-around and OTA-shared configuration
FF	Flip-flop
FFT	Fast Fourier Transform
FOM	Figure of Merit
I	Number of pipelined stages

INL	Integral Non-linearity
K	Current resolved bit or Current evaluation phase
k	Boltzman's constant
LSB	Least Significant Bit
M	Stage resolution [bits]
MDAC	Multiplying Digital-to-Analog Converter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
N	ADC number of bits
OTA	Operational Transconductance Amplifier
S/H	Sample and Hold
SAR	Successive Approximation Register
SC	Switched Capacitor
SFDR	Spurious Free Dynamic Range
SNDR	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SR	Set-Reset
T	absolute temperature
TFA	Traditional flip-around configuration
THD	Total Harmonic Distortion
TR	Traditional regular
U-MDAC	Unit-Multiplying Digital-to-Analog Converter
V_{FS}	Full scale voltage
V_{LSB}	Least Significant Bit Voltage
V_t	Threshold voltage

Chapter 1

Introduction

Analog-to-digital converters (ADCs) are ubiquitous wherever analog signals are processed, stored, or transported in a digital form. For example, in the music industry, ADCs are used to convert the voice into digital format so that it is processed, compressed, or stored. ADCs are also an integral part of wireless communication systems, disk drives, audio and video communications, radar, sonar, camcorders, cellular phones, touch-screens, displays, and other analog/digital mixed-signal applications. Typically, such applications determine the architecture of the embedded ADCs and their performance to satisfy the needs of the overall system.

1.1 ADCs for Imaging, Biomedical, and Capacitive Sensing Applications

During the last decade, there has been an increasing demand for digital signal processing (DSP) of images and other sensor based data requiring low speed and moderate resolutions, while consuming a very low power. General imaging, biomedical imaging and capacitive touch sensing applications are perhaps the most rapidly growing ones [1–14].

The most common ADC architectures for these sensing applications are successive-approximation register (SAR) [15–19], single-slope (SS) [20–22], sigma-delta ($\Sigma\Delta$) [6, 23–25], and algorithmic or cyclic [2, 3, 26] ADCs. Although SAR ADCs are easy to use, they require a digital-to-analog converter (DAC) in a column, whose area is unacceptably large

for consumer electronics. Other commonly used ADCs in sensing applications are single-slope and $\Sigma\Delta$ ADCs. Single-slope ADCs need 2^N clock cycles for an N-bit conversion, requiring very fast clock signals leading to a high power consumption in high-speed imaging and sensing applications. Whereas in many sensing applications, $\Sigma\Delta$ ADCs are typically avoided due to the complexity of the $\Sigma\Delta$ modulators and the following decimation filters [3, 27]. Although algorithmic ADCs require a less silicon area than SAR ADCs [2, 28, 29], algorithmic ADCs typical implementations necessitate accurate amplifiers, resulting in a higher power consumption. Also, algorithmic ADCs have a comparable or faster operation speed than SAR ADCs [2, 15].

1.2 Motivation

The power consumption of an ADC has a significant effect on the overall power budget of a sensor acquisition system. Among the different ADC architectures in sensing applications, algorithmic ADCs are the preferred choice [2, 13, 28, 30]. Although algorithmic ADCs are, inherently, area efficient due to the fact that in a typical N-bit algorithmic ADC, the hardware is reused N times, once for each bit of resolution, they are relatively power inefficient, compared to that of other ADC architectures.

Algorithmic ADCs are based on the same operating principle as that of pipelined ADCs, which have greatly benefited from the interstage scaling [31]. The concept of interstage scaling stems from the fact that the noise, accuracy, and settling time requirements are relaxed as the signal travels to the later stages in the pipeline. Therefore, the operational transconductance amplifier (OTA) gain and capacitors can be scaled along the pipeline such that lower-power OTAs can be utilized. In addition to low-power OTAs, various other low power techniques have been developed to reduce the power consumption of pipelined ADCs. Among them, the switched-OTA, the OTA-shared, and capacitor-shared techniques exhibit the most promise. The switched-OTA [32, 33] takes advantage of the fact that each OTA is idle for one of the clock phases, and hence, can be switched off to conserve power. OTA-shared technique [34, 35] saves power by using the same OTA for two successive stages. Capacitor-shared technique in pipelined ADCs [36–38] depends on the fact that in near optimally scaled pipelined ADCs, the unit capacitors in each stage are scaled by the interstage gain, and the feedback capacitor of one stage is equal to the total input capacitance of the following stage. Consequently, the feedback capacitor of one stage

can be reused as the input capacitor of the following stage, thereby reducing the OTA's capacitive load and its power requirements.

Due to the cyclic nature of algorithmic ADCs, many of these conventional low power techniques cannot be utilized in typical implementations of algorithmic ADCs. However, algorithmic ADCs still offer other advantages over pipelined counterparts, including as low area [39], ease of calibration [40], and capacitor mismatch insensitivity at the expense of multiple conversion cycles per bit [41, 42].

The objective of this thesis is to introduce some novel low power techniques for designing algorithmic ADCs. These techniques are verified by designing prototype ADCs.

1.3 Thesis Organization

The thesis comprises of five chapters. Chapter 2 is a review of some background material for ADCs in general, and algorithmic ADCs in particular. The algorithmic architecture, its implementation techniques, and sources of errors are explored, and the low power techniques of pipelined ADCs are discussed. The chapter is concluded with the examination of recent energy efficient techniques for algorithmic ADCs. Chapter 3 presents two proposed power efficient techniques for algorithmic ADCs. The proposed technique exploits the OTA-shared, the switched-OTA, the capacitor-shared, and the capacitor-scaled techniques to achieve a low-power data conversion. The details of two experimental ADCs are provided in Chapter 4. The design details for the circuits are described, along with the simulation and measurement results. In Chapter 5, conclusions are drawn and some future work is suggested.

Chapter 2

Background

2.1 Analog-to-Digital Conversion Overview

An ADC is a device that converts a continuous-time analog signal into a series of corresponding digital codes. Each code is a quantized version of the analog signal at the corresponding time instant.

There are two main types of ADCs: Nyquist-rate ADCs and over-sampled ADCs. The term, Nyquist-rate, is derived from the Nyquist theorem, which states that the sample rate must be greater than twice the bandwidth of the signal to preserve all the signal information. Usually, Nyquist-rate converters operate close to the Nyquist-rate, and rely on analog circuits for anti-aliasing and reconstruction filters. In addition, ADCs can be operated at much higher sampling rates than those determined by the Nyquist-rate, and increase the output's SNR by filtering out the quantization noise that is not in the signal bandwidth. These ADCs are called over-sampled ADCs.

Among the different ADC architectures, flash ADCs are known to be the fastest quantizers of an analog signal. However, for high resolutions, flash ADCs require a large number of comparators, thereby occupying a large chip area and consuming high power. A possible way to reduce the power consumption in an ADC is to split the conversion process into identical low resolution stages, working concurrently in a pipelined fashion. Each stage samples the analog signal, coarsely quantizes it, and transfers the residue (the unconverted part of the signal) to the next stage. Once the residue is sampled by the next stage, the sampling process is repeated. This pipelined approach increases the throughput and

reduces the number of comparators at the cost of an increased latency. An alternative approach to the pipelined scheme is algorithmic conversion. In an algorithmic ADC, rather than transferring the residue to the next stage, the residue is fed back to the same stage. By performing the data conversion in algorithmic or cyclic fashion, the conversion speed is traded off with the die area [43].

In this chapter, the architectural details of algorithmic and pipelined ADCs are explored, and the sources of errors in algorithmic ADCs are discussed. The last part of the chapter focusses on the low power aspects of pipelined and algorithmic ADCs.

2.2 Architectural Details of Pipelined and Algorithmic ADCs

In this section, architectural details of pipelined and algorithmic ADCs are investigated. The implementation details of a generic stage, as well as the discussion of sources of errors are introduced.

2.2.1 Pipelined ADCs

A typical pipelined ADC, consisting of I cascaded stages with each stage resolving M-bits, is depicted in Figure 2.1. The input of each stage is the output of the previous stage, except for the first stage for which the input signal is the analog input, V_{in}. In each stage, there is a sample-and-hold (S/H), sub-ADC, DAC, summing block and gain block. All the stages operate in the same fashion, except for the last stage which is simply a flash converter.

At each stage, the analog signal is first sampled and held. This sampled signal is converted to its digital equivalent by using the flash sub-ADC, and then it is converted back to an analog value by using a DAC. The analog signal from the DAC is subtracted from the original held input signal to generate the residue voltage. This voltage is amplified by 2^M to generate an output voltage range equivalent to the input voltage range. This allows the use of same or similar hardware for each stage.

The residue voltage is sampled by the next stage in the next clock cycle, and the same operation is repeated. When the second stage samples the residue of the first stage, the

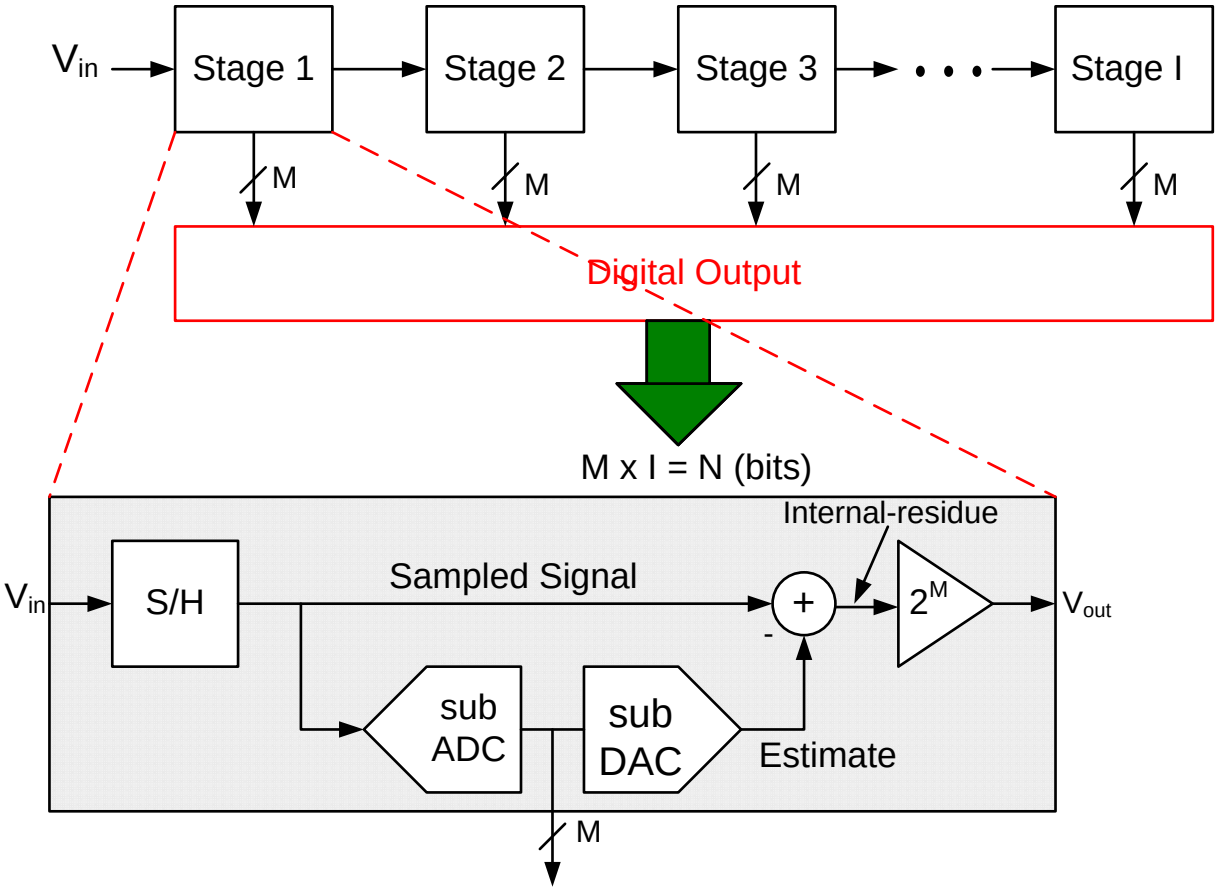


Figure 2.1: M-bit/stage pipelined ADC.

first stage is free to sample the analog input again. Consequently, a new analog sample can be taken at each clock cycle.

During each clock period, each pipelined stage resolves M-bits[1] that are digitally combined after I-cycles to generate an N-bit ($= M \times I$) digital code. This process is described in Figure 2.2. Three stages are shown where the first two stages are the 1.5-bit/stage (described in Section 2.2.2.1) and the last stage is a 2-bit flash. The delay elements are represented as D. The output bits of stage 1 passes through the two delay elements, until the data bits are available from the remaining stages. Then, at the end, all these bits are combined in the manner as illustrated in Figure 2.2.

[1]Assuming all stages resolve the same number of bits.

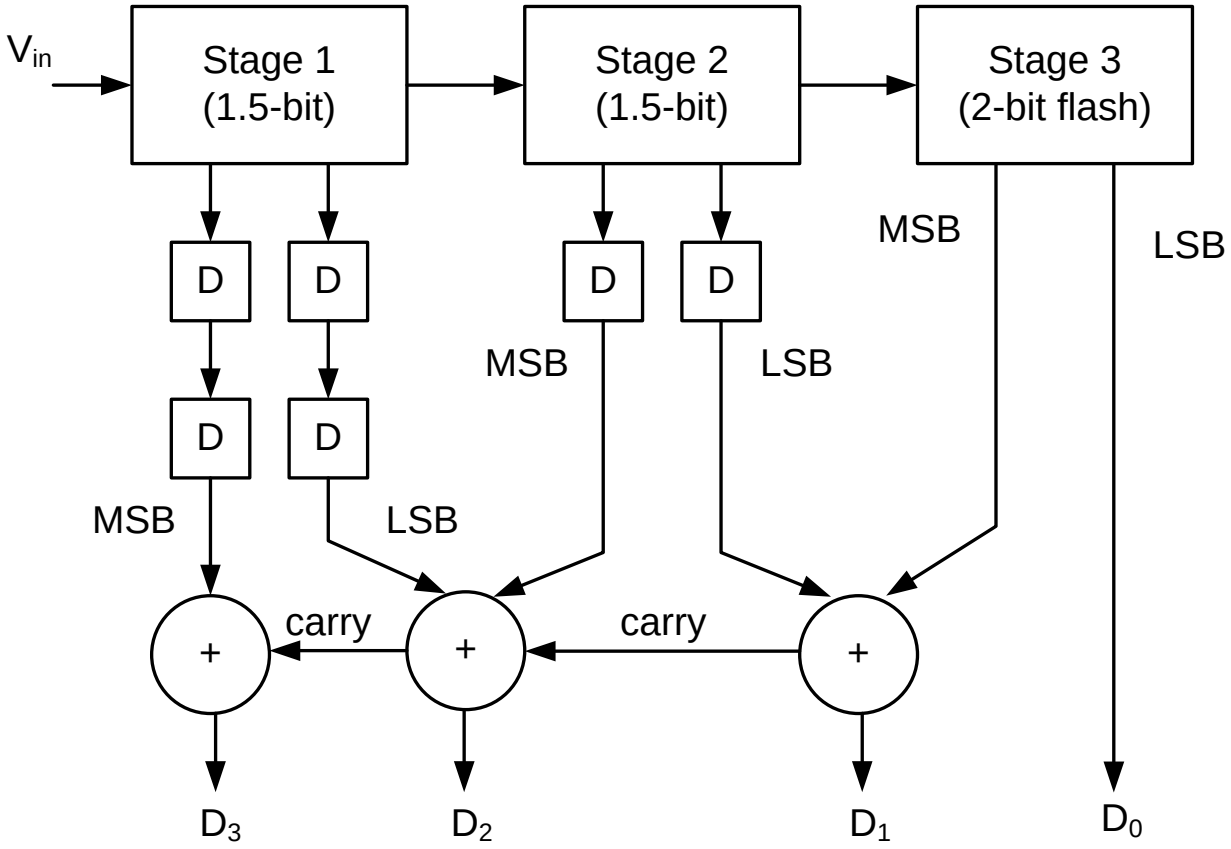


Figure 2.2: Digital alignment of pipelined output bits. Here D are the delay elements.

2.2.2 Algorithmic ADCs

The operation of algorithmic ADCs is established on the same operating principle of pipelined ADCs. In pipelined ADCs, the residue is propagated to the next stage, whereas in algorithmic ADCs, the residue voltage is fed back to the same stage, by trading speed with die area.

The primary task of an algorithmic stage is to sample the signal from the previous cycle, generate the analog residue voltage for the next cycle, and produce the digital output bits. A generic algorithmic stage, resolving M-bits, is shown in Figure 2.3. The stage consists of an S/H, a sub-ADC, a DAC, a summing block, and a gain block.

In the first cycle, $V_{S/H}(1) = V_{in}$. The sampled signal is compared to the reference voltage to generate the most significant bit (MSB). The sub-DAC generates an analog estimate of the ADC output, and the DAC output is subtracted from the held signal to generate the analog residue voltage. A precise gain of 2^M brings the residue signal swing

back to the full-scale reference level. This residue voltage is propagated to the next cycle such that

$$V_{S/H}(K+1) = 2^M \cdot V_{S/H}(K) \pm V_{ref} \tag{2.1}$$

where K is the current evaluation phase. This process continues until all the bits are generated. In the next sampling cycle, the stage again samples the V_{in}, and the same conversion process occurs again.

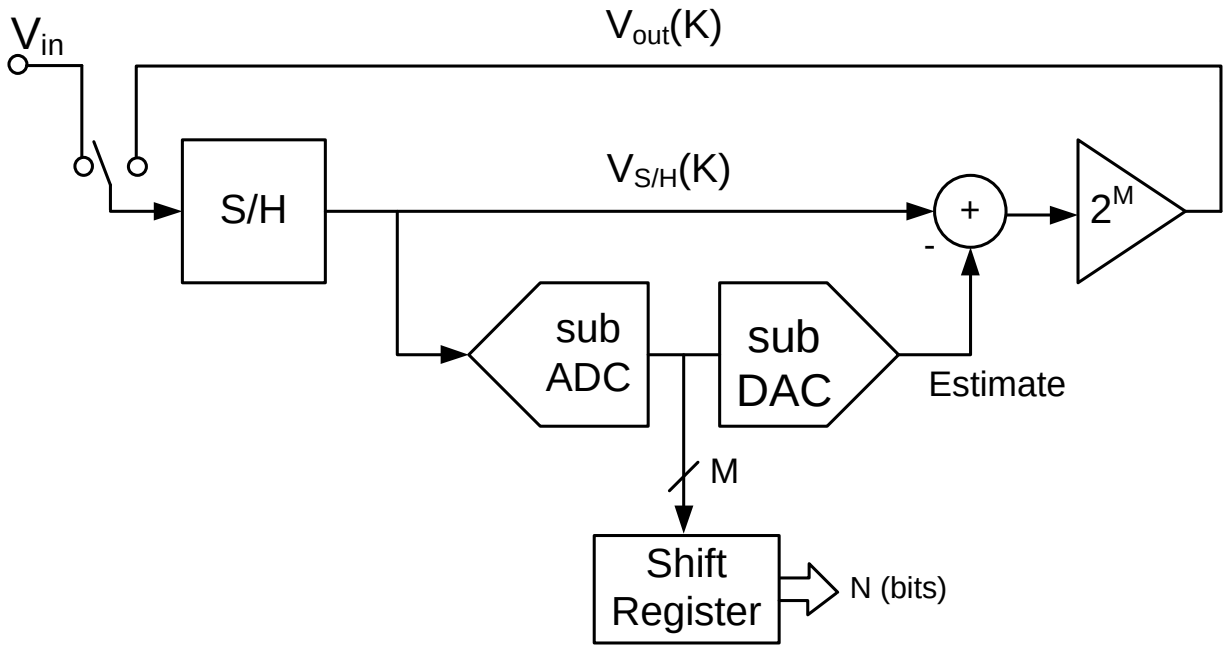


Figure 2.3: Algorithmic ADC architecture.

For a 1-bit case, where M=1, the circuit operates in the following manner. The sampled signal, V_{in}, which ranges from $-V_{ref}$ to V_{ref}, is quantized by the sub-ADC. The sub-ADC's output is then fed to the DAC to generate the analog estimate of the input signal. The estimate is then subtracted from the sampled signal to generate the internal residue voltage. The residue voltage is amplified by a gain of two such that the voltage is centered around zero. Then, this internal residue is sampled by the next cycle.

The resulting transfer characteristic of a 1-bit/stage is shown in Figure 2.4. b_K is the output bit, generated by the sub-ADC. The discontinuity at zero occurs when the comparator switches its decision from $b_K = 0$ to $b_K = 1$.

To generate the transfer function, the output of the DAC is either $-V_{ref}/2$ or $+V_{ref}/2$,

corresponding to the input codes of 1 and 0, respectively. So, the output voltage becomes

$$V_{out} = 2V_{in} \pm V_{ref} \tag{2.2}$$

which is the key function performed by an algorithmic stage. This function is referred to as the residue. Since the residue range of the algorithmic stage is the same as that of its input range, due to the gain of two, the residue is sampled during the next cycle without any further processing.

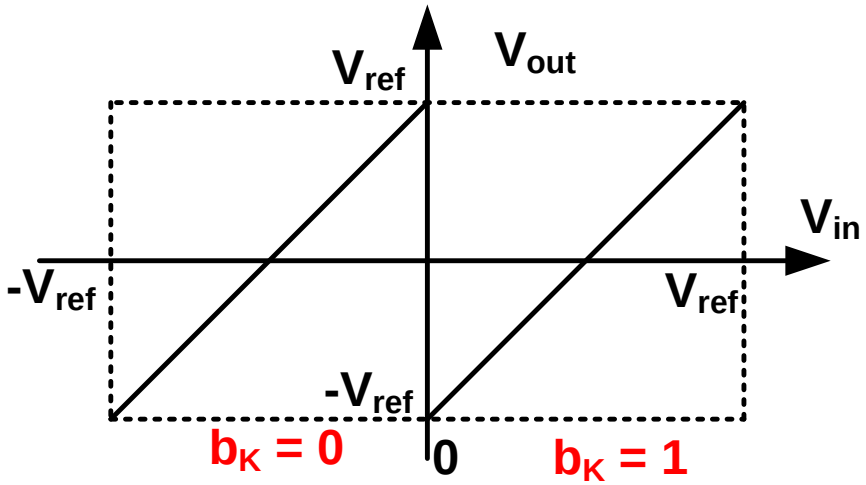


Figure 2.4: Transfer characteristics of a 1-bit pipelined stage.

2.2.2.1 Effects of offsets on the residue

Offsets in the comparators, which are in the sub-ADCs, shift the point, where the transition from one segment of the transfer function to the other segment occurs. Shifting the transition point can lead to missing codes.

Figure 2.5 demonstrates the residue of a 1-bit algorithmic stage with a comparator offset. The transition from one segment to the other segment occurs at a positive input voltage. As a result, the input to the next cycle is more than the value of V_{ref}. If the offset is large enough, it leads to missing codes in the ADC's output.

One way to get around the problem of comparator offsets is to use digital error correction. Most digital error correction techniques are based on the use of redundancy. One of the most popular digital error correction techniques is the 1.5-bit/stage structure [44] [31].

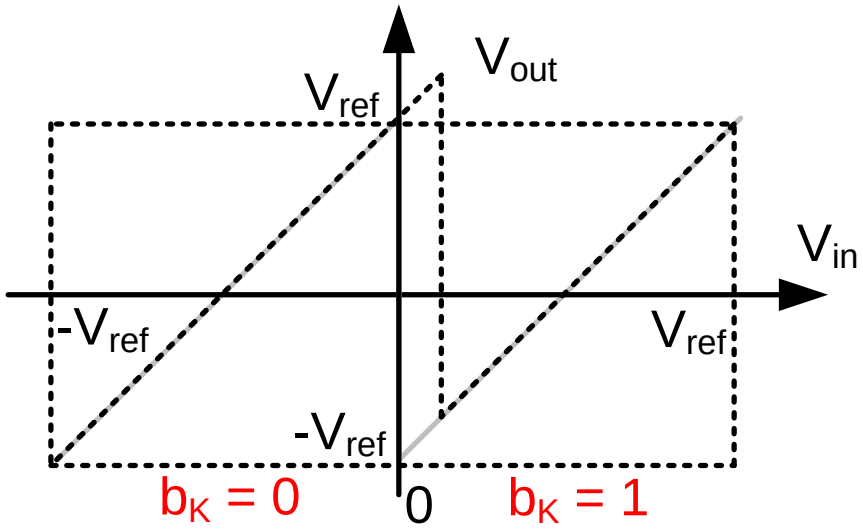


Figure 2.5: Transfer function of the 1-bit pipelined stage with an offset.

The flowchart of the redundant sign digit (RSD) algorithmic ADC is shown in Figure 2.6.

Figure 2.7(a) reflects the residue plot of the ideal 1.5-bit/stage. There are two transition points: at $+V_{ref}/4$ and $-V_{ref}/4$. The input range is now divided into three segments. In the 1.5 bit/stage implementation, a digital set of {-1, 0, 1} corresponding to a set of digital codes of 00, 01 and 10, respectively, are used. Here -1 represents $V_{in} < -V_{ref}/4$, 0 represents $-V_{ref}/4 \leq V_{in} \leq V_{ref}/4$, and +1 represents $V_{in} > V_{ref}/4$.

An important property of the 1.5-bit/stage is that it can tolerate $\pm V_{ref}/4$ comparator offsets. As a result, the errors caused by these comparator offsets can be corrected in the digital domain. The residue plots of the 1.5-bit/stage with comparator offsets of $+V_{ref}/4$ and $-V_{ref}/4$ are shown in Figure 2.7(b) and (c), respectively. In both cases, it is evident that, the residue voltages still fall within the desired output range of $\pm V_{ref}$. Provided the residue voltage remains within the input range of the following stage, the residue voltage can be successfully resolved by the following cycle.

2.2.3 Switched capacitor realization of the algorithmic stage

There are many ways to implement an pipelined/algorithmic stage [45–47]. However, the switched-capacitor (SC) approach is currently the most popular technique for the implementation. SC circuits depends on the ratios of the capacitor and not on the absolute

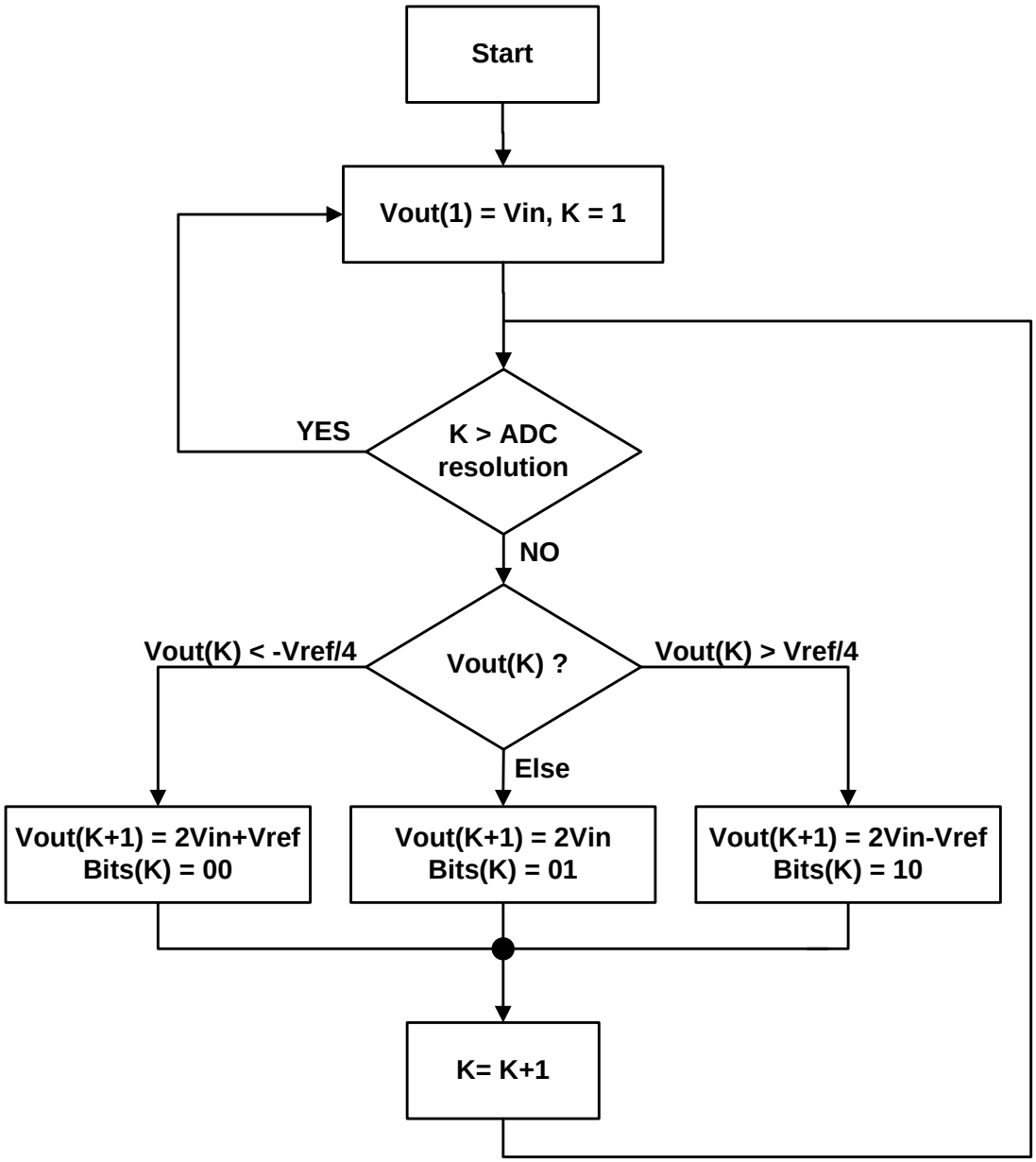


Figure 2.6: Flow chart of an RSD algorithmic ADC.

values of these capacitors. Therefore, SC circuits are very well suited to use within the integrated circuits.

A typical implementation of an algorithmic ADC is shown in Figure 2.8. Here, the algorithmic ADC operates with a two-phase clock: a sample phase, ϕ_s, and an evaluation phase, ϕ_e. During the first sampling phase, ϕ_{in} is active to sample V_{in} on C_s, while all the

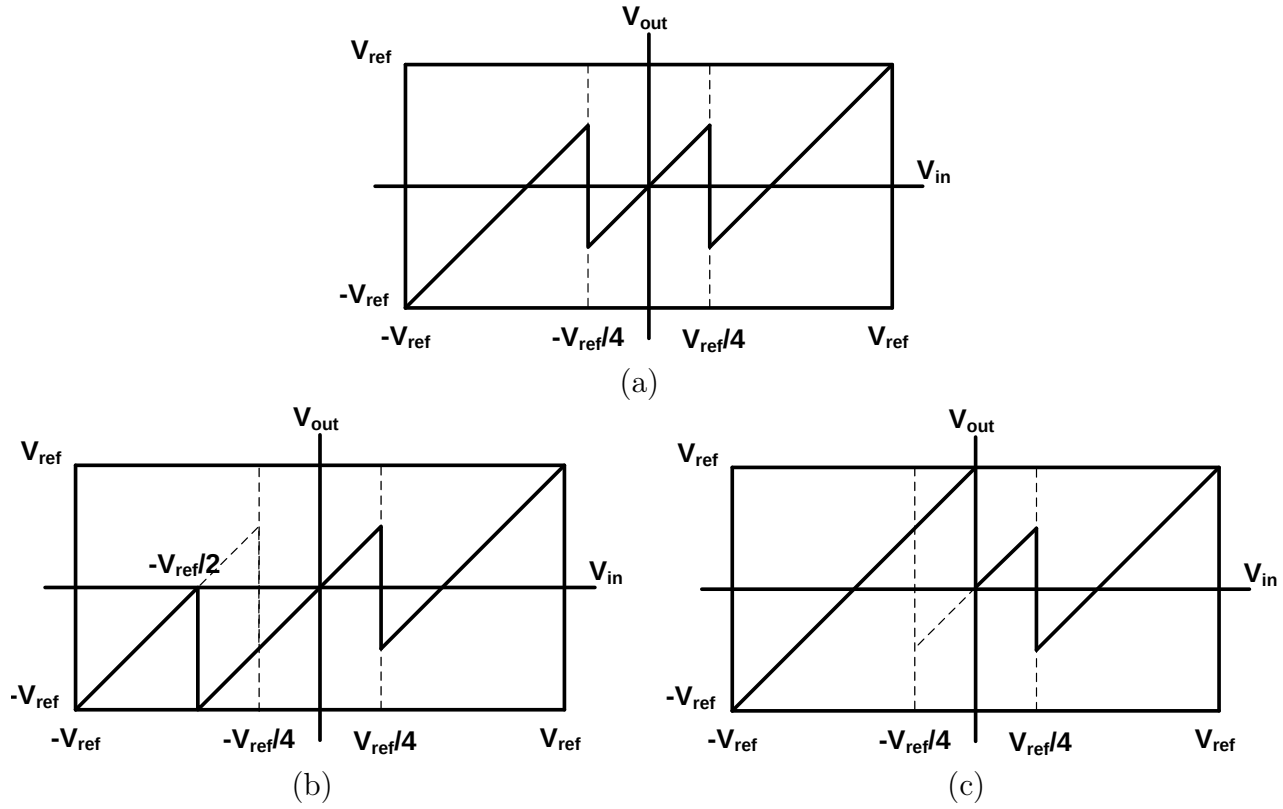
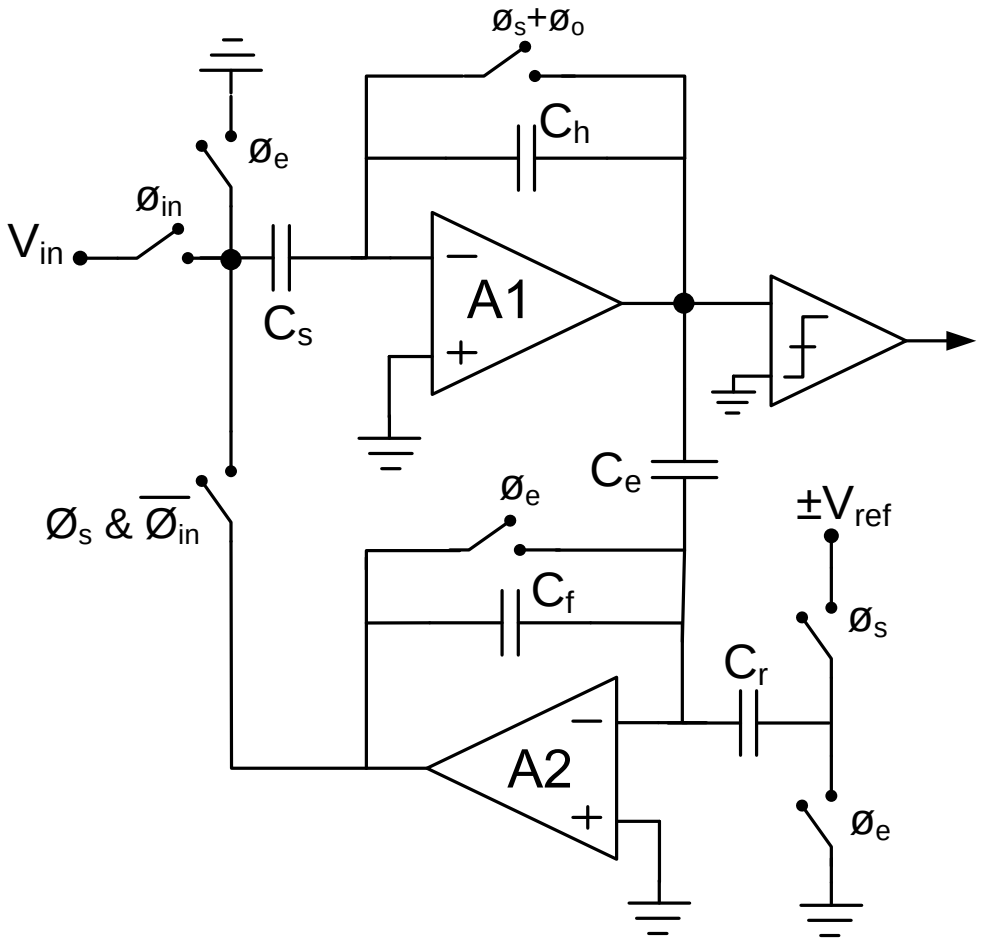
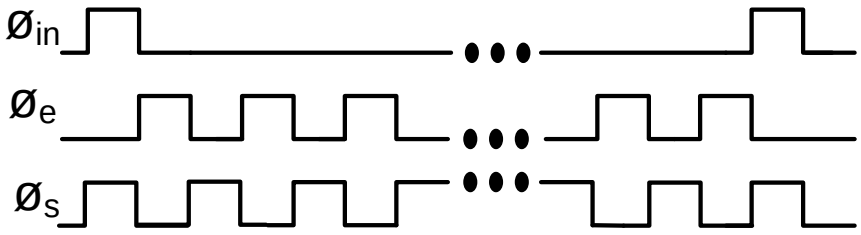


Figure 2.7: Residue plot of the 1.5 bit/stage: (a) the ideal case with zero offset, (b) one extreme case with the offset of the lower comparator at $-V_{ref}/2$, and (c) the other extreme case with the offset of the lower comparator at 0.

other capacitors are reset. All the capacitors are equal in size, except C_e, which is twice the size of the others.



(a)



(b)

Figure 2.8: Single-ended SC implementation of the conventional two-stage algorithmic ADC: (a) Schematics and (b) Clocks.

The ADC consists of two stages: the first stage, consisting of C_s, C_h, and A_1, is used as a sample-and-hold-amplifier (SHA) and the second stage, consisting of C_e, C_f, C_r and A_2 is used to generate the residue. The SHA has two principal roles: sample the analog input, V_{in}, and sample the residue generated by the second stage, before transferring the sample back to the input of the second stage. During the first cycle, V_{in} is sampled on C_s. During ϕ_e, A1 transfers the charge from C_s to C_h where the sample is held. The held signal is compared by the comparator to generate the MSB. Simultaneously, the held signal is sampled on C_e. The charge stored on C_e is given as

$$Q_{\phi_e} = C_e \cdot V_{in} \tag{2.3}$$

Then, during ϕ_s, the charge on C_e is injected into the OTA loop to generate $2V_{in}$ at the output. At the same time, based on the comparator output, C_r is connected to $\mp V_{ref}$ to generat the residue, expressed as

$$V_{out}(K+1) = \frac{C_e}{C_f} \cdot V_{out}(K) - b_K \cdot \frac{C_r}{C_f} V_{ref} \tag{2.4}$$

where $V_{out}(K)$ is the residue generated in the K^{th} evaluation phase, and $V_{out}(0) = V_{in}$. $b_K = \pm 1$ is the comparator output. Since $C_e = 2C$ and C_f=C_r=C, (2.4) is written as,

$$V_{out}(K+1) = 2V_{out}(K) - b_K \cdot V_{ref} \tag{2.5}$$

Therefore,

$$V_{out}(K+1) = \begin{cases} 2V_{out}(K) - V_{ref} & \text{if } V_{out}(K) > V_{ref}/4 \\ 2V_{out}(K) & \text{if } -V_{ref}/4 \leq V_{out}(K) \geq V_{ref}/4 \\ 2V_{out}(K) + V_{ref} & \text{if } V_{out}(K) < -V_{ref}/4 \end{cases} \tag{2.6}$$

The SHA samples this residue voltage on C_s and holds it for the second stage to generate the next residue. This residue generation and sampling process continues until all the bits are generated. Then, the stage takes the next input sample and the conversion process starts again. Therefore, for a two-phase clocking scheme, an N-bit ADC requires 2N clock phases to perform an N-bit data conversion.

The effective number of bits, ENOB, of the 1.5-bit/stage architecture is calculated,

where the V_{LSB} is given as

$$V_{LSB} \cong \frac{V_{FS}}{3} \tag{2.7}$$

because there are three decision levels. The quantization noise is expressed as

$$\overline{v}_{qns} = \frac{V_{FS}}{3\sqrt{12}} \tag{2.8}$$

For a sinusoidal input signal, the SNR is calculated as [43]

$$SNR = 20\log_{10}\left(\frac{V_{FS}}{2\sqrt{2}} \cdot \frac{3\sqrt{12}}{V_{FS}}\right) = 11.3 \text{ (dB)} \tag{2.9}$$

Therefore, the ENOB is mathematically represented as

$$ENOB = \frac{SNR(dB) - 1.76}{6.02} = 1.58 \text{ (Bits)} \tag{2.10}$$

This is why the stage is called the 1.5-bit/stage.

The concept of the 1.5-bit/stage technique can be extended to higher resolutions per stage. For example, a 2.8-bit/stage resolves 2-bits of information from the input signal, whereas the extra 0.8-bit information is adopted to correct the comparator errors. In the 2.8 bit/stage the gain of the stage is four compared to the gain of two in an 1.5-bit/stage. This is carried out to restore the residue to full-scale. The residue plot of a 2.8-bit stage is shown in Figure 2.9.

The 2.8-bit/stage implementation can be extended to higher bits per stage by providing an interstage gain of 2^M, where M is the stage resolution. Higher resolutions per stage means a lower total number of clock phases for a given ADC resolution.

In summary, the combination of SC techniques and the 1.5-bit/stage concept, provides an excellent approach to implement high-speed, high-resolution ADCs. The use of the 1.5-bit/stage implies that comparator offsets of $\pm V_{ref}/4$ can be tolerated, leading to the possibility of very high-resolution ADCs. However, there are many other sources of errors in pipelined and algorithmic ADCs. These sources of errors are analyzed next.

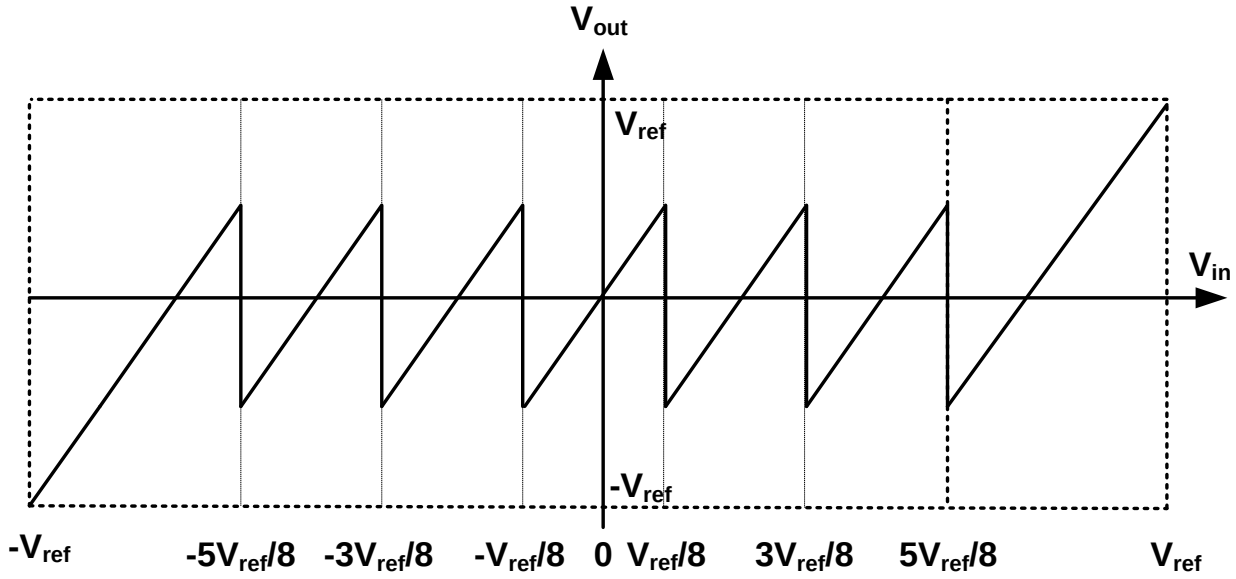


Figure 2.9: Residue plot of the 2.8-bit/stage.

2.2.4 Sources of errors in the pipelined/algorithmic stages

There are many error sources (other than comparator offsets) that have historically limited the performance of pipelined and algorithmic ADCs. These error sources are divided into two categories: noise, which varies from sample to sample, and systematic errors, which do not vary from sample to sample. The typical sources of errors in a pipelined/algorithmic stage are:

- Switching errors; caused by the non-idealities of the switches
- Matching errors; incurred from capacitor and device mismatches
- Gain errors; due to imperfect OTAs
- Noise; from switch resistances and OTAs

2.2.4.1 Switching errors

In SC implementations, MOS transistors are used as switches. The requirement of these switches are that they do not introduce any offsets, meet settling time constraints, and have a low OFF state leakage. However, these switches, being imperfect, cause clock-feedthrough and charge-injection errors, and exhibit non-linear on-resistance.

MOSFETs have capacitive coupling between the gate and the junctions. These capacitances couple the clock signal into the signal path. This phenomenon causes an error called, the clock feed-through error. The coupling is proportional to the size of the transistor, but this error is independent of the input signal. In a 0.18 μm technology, an NMOS switch of size 5μm/0.18μm charging a 100 fF capacitor at 100 MHz, leads to a clock-feedthrough charge of about 5%. With technology scaling, this coupling generally decreases, and can be canceled by using a fully differential topology

Charge injection is another mechanism that distorts the signal. When an ON MOS transistor is turned OFF, the charges in the channel at that moment are pushed to the drain and source terminals. For the aforementioned NMOS switch, a 1V input signal causes an error voltage of approximately -30 mV. This negative injected charge is signal dependant. A number of techniques have been reported, including the use of transmission gates and dummy switches to deal with this problem [48].

Another signal dependant issue of the MOS switches is the non-linear on-resistance. A MOSFET's on-resistance depends on V_{gs}, where V_s varies with the input signal. For the previous switch previous and a signal ranging from 0 to 1 V, the on-resistance ranges between 100 Ω and 1.15 kΩ. This non-linear on-resistance leads to a signal dependant settling time. The nonlinearity of the switch resistance can be improved by the use of CMOS transmission gates. However, in high resolutions, the transmission gates do not give enough linearity, and another technique, called bootstrapping is commonly used [44, 49].

In summary, switches have numerous problems, and the design techniques discussed above have been developed to avoid the errors caused by them. Consequently, errors due to MOS switches do not lead to significant problems.

2.2.4.2 Matching

Due to process variations, nominally identical components do not match in practical circuit realizations. Often, these component mismatches limit the attainable resolution of pipelined ADCs. For pipelined ADCs, implemented in CMOS processes, the most significant mismatches are capacitor mismatches and MOSFET mismatches.

The capacitor matching accuracy is usually limited by the lithography and subsequent processing steps. Modern CMOS processes offer Metal-Insulator-Metal (MIM) capacitors, which, if carefully designed in the layout, match to 0.01-0.1% accuracy [50]. However, capacitor mismatches decrease with increased capacitor size. The standard deviation of

the fractional matching error between two adjacent square capacitors is commonly modeled as [51]

$$\sigma_{\frac{\Delta C}{C}} = \frac{A_c}{\sqrt{W \cdot L}}$$

where W and L are the width and length of the capacitor. The value of A_c is a technology dependent parameter.

In SC pipelined/algorithmic ADCs, the capacitors are employed to set the gain of each stage. For the residue voltage, $V_{out} = V_{in}\left(\frac{C_1+C_2}{C_1}\right)$, C_1 and C_2 are set nominally equal to obtain a gain of two. Assume $C_1 = C \pm \Delta C$ and $C_2 = C \mp \Delta C$. Therefore, the residue voltage becomes

$$\begin{aligned} V_{out} &= \left(\frac{C \pm \Delta C + C \mp \Delta C}{C \pm \Delta C}\right) V_{in} \\ &= \left(\frac{2C}{C \pm \Delta C}\right) V_{in} \\ &\cong 2\left(1 \mp \frac{\Delta C}{C}\right) V_{in} \end{aligned} \tag{2.11}$$

The impact of the errors caused by capacitor mismatch can be seen in Figure 2.10. Due to such a mismatch, there are discontinuities in the residue plot which give rise to missing codes.

For a full scale input, V_{out} must not deviate from the ideal value by more than a half LSB. However, for an N-bit ADC, the capacitor matching must be accurate to the number of bits remaining to be resolved or N-K+1 for a half LSB accuracy, such that

$$\frac{\Delta C}{C} < 2^{-(N-K+1)} \tag{2.12}$$

Consequently, a 10-bit part resolving the first bit must match to effectively 0.1% accuracy. In summary, for high-resolutions, tight capacitor matching must be achieved. Increasing the capacitor area increases the capacitor matching, however increasing the area is impractical in many cases. In this case, digital calibration is used [52–54] .

2.2.4.3 Gain errors

An OTA is the most important building block in SC implementations of pipelined ADCs. Since the DC gain of an OTA is finite, a gain error is introduced in the residue transfer

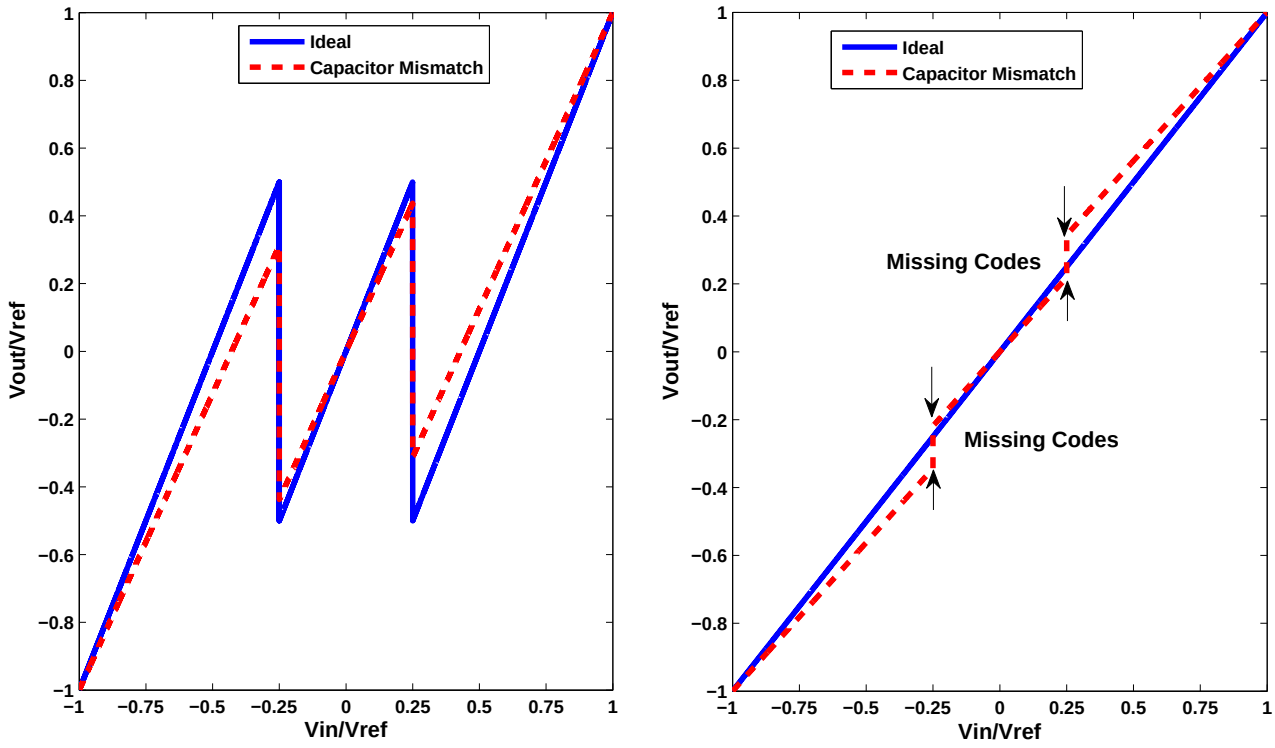


Figure 2.10: Residue plot showing the impact of the capacitor mismatch: (a) Residue plot of the first stage with capacitor mismatch and (b) Reconstructed output for the ramp input.

function, as shown in Figure 2.11, where t is the required settling time, and τ is the time constant of the closed loop system.

The relationship between an OTA's DC gain and the ADC's resolution is derived here. If the open-loop DC gain of an OTA is A_v, then the closed-loop gain, G, of the OTA is given by solving

$$G = \frac{A_v}{1 + A_v \cdot \beta} \tag{2.13}$$

where β is the feedback factor. If M is the stage resolution, then β of an M-bit flip-around stage (explained in Section 2.3.2) is given as

$$\beta = \frac{1}{2^M} \tag{2.14}$$

If the OTA DC open-loop gain is infinite, then the ideal closed-loop gain should be $1/\beta$.

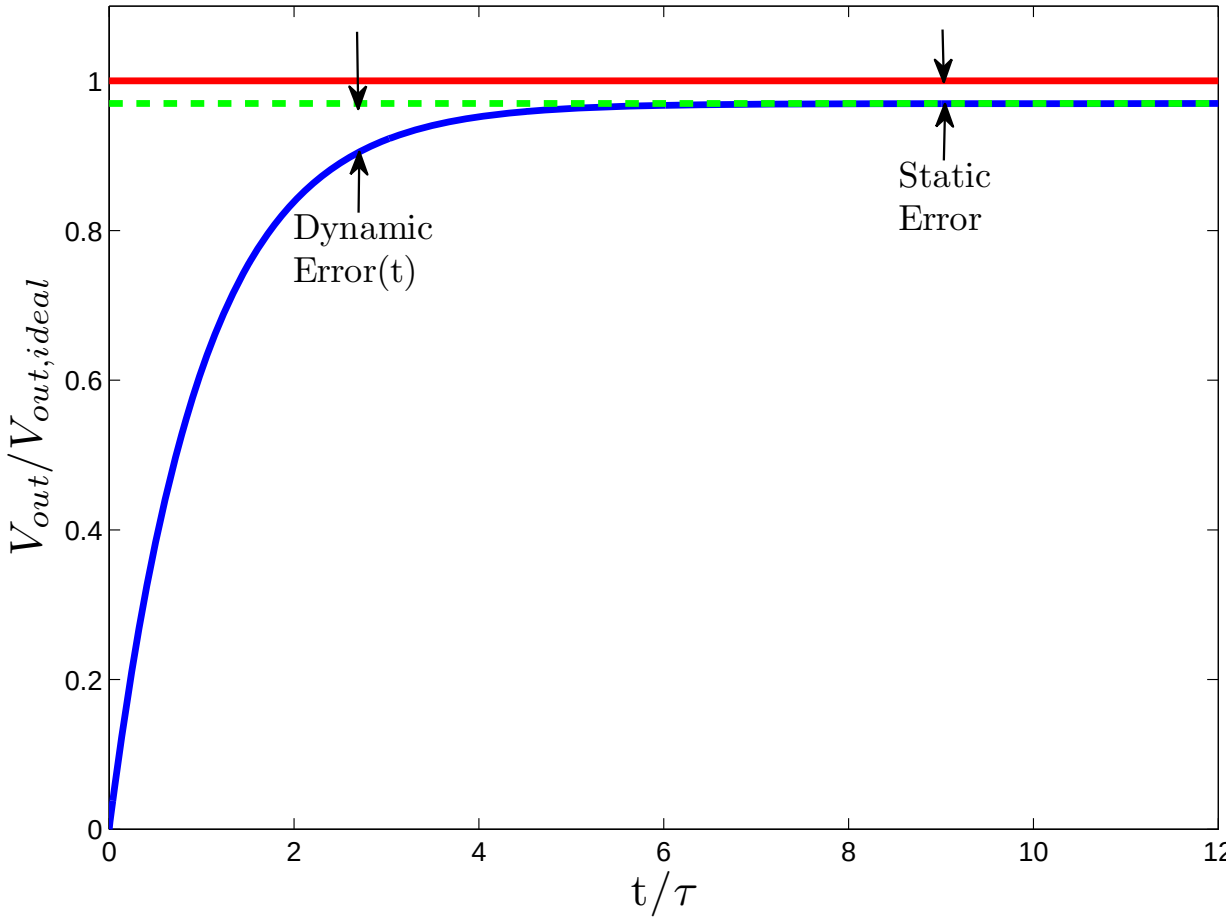


Figure 2.11: Settling time and gain error due to the imperfect OTA.

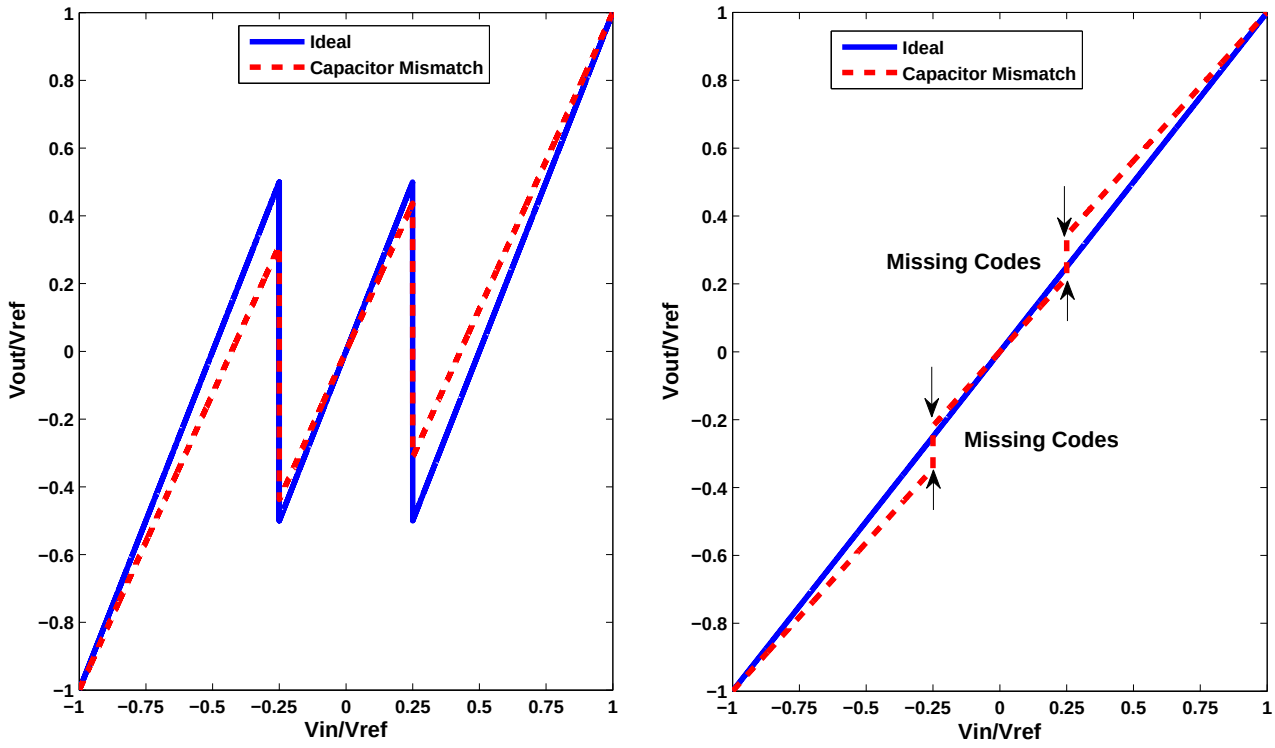
However, due to the finite A_v, the gain error is

$$\begin{aligned}\frac{G_{ideal}-G}{G_{ideal}} &= \frac{1/\beta - A_v/(1+A_v\cdot\beta)}{1/\beta} \\ &= \frac{1}{1+A_v\cdot\beta}\end{aligned} \tag{2.15}$$

If $A_v \cdot \beta \gg 1$, then the gain error of the interstage amplifier is given as

$$\left|\frac{\Delta G}{G}\right| \approx \frac{1}{A_v\cdot\beta} \tag{2.16}$$

The impact of the errors caused by a low DC gain OTA is illustrated in Figure 2.12. Due to the gain errors, discontinuities in the residue plot result in missing codes.



(a) (b)

Figure 2.12: Residue plot showing the impact of the gain errors: (a) Residue plot of the first stage with OTA's gain and (b) Reconstructed output for the ramp input.

A common requirement is that the error should be less than the maximum quantization error, that is, 0.5 LSB. Accordingly, for an N-bit algorithmic ADC currently resolving Kth-bit, the gain error is given as

$$\left|\frac{\Delta G}{G}\right| < \frac{1}{2^{(N-K+1)}}$$
$$A_v \cdot \beta > 2^{(N-K+1)} \tag{2.17}$$

Consequently, for a 12-bit algorithmic ADC resolving 1 bit in each cycle, the amplifier loop gain must be higher than 72 dB.

OTAs also have a finite bandwidth such that an OTA necessitates a finite amount of time to settle to the final value shown in Figure 2.11. The OTA's bandwidth is dictated by the settling accuracy requirements of the closed-loop system.

For a half LSB settling accuracy, the time constant, τ, of a single pole OTA, is computed

by [55]

$$\tau < \frac{t}{(N - K + 1) \cdot \ln 2} \tag{2.18}$$

The settling time of an N-bit algorithmic ADC, requiring N-clock phases, is given as

$$t = \frac{1}{N \cdot f_s} \tag{2.19}$$

where f_s is the sampling frequency. Hence, by combining (2.18) and (2.19), the OTA's closed-loop bandwidth is given as

$$f_{3dB} = f_T \cdot \beta > \left(\frac{N \cdot (N - K + 1) \cdot f_s \cdot \ln 2}{2\pi} \right) \tag{2.20}$$

Equation (2.20) shows that increasing the ADC's resolution, sampling frequency, and stage resolution increases the OTA's bandwidth requirements. For a f_s = 10 MS/s conversion rate, the OTA's closed loop bandwidth of a N = 12-bit algorithmic ADC with the stage resolution of K = 1-bit must be higher than approximately 160 MHz.

2.2.4.4 Noise

Error sources can be classified into two broad categories of noise and systematic errors. Noise varies from sample to sample, whereas systematic errors do not. This distinction has a significant impact. Systematic errors are commonly fixed with calibration, leaving only the noise as a limiting factor.

There are many kinds of noise, including shot noise, flicker noise, and thermal noise. Shot noise does not exist in typical MOS devices, but they can appear in deep sub-micron devices that exhibit significant gate leakage [56]. Flicker noise is reduced by increasing the sizes of the input transistors, and using PMOS transistors rather than NMOS transistors. However, thermal noise is a fundamental noise inside any conductor and is the dominant noise in sampled data systems.

In a SC circuit, the thermal noise of a switch is filtered by a single pole low-pass filter created by the resistance of the switch and the sampling capacitor. Therefore, the rms noise voltage sampled on the capacitor is given as [48]

$$\sqrt{\overline{e_N^2}} = \sqrt{\frac{kT}{C}} \tag{2.21}$$

where k is Boltzman's constant, T is the absolute temperature and C is the sampling capacitor size.

In algorithmic ADCs, the total input referred noise is proportional to the weighted sum of the reciprocals of the sampling capacitors. For an M-bit stage with equal sized sampling capacitors C_s, in each stage, the input referred noise is shown as [31]

$$\overline{v}_{n,in}^2 \propto \frac{kT}{C_s}\left[1 + \frac{1}{2^{2M}} + \frac{1}{2^{4M}} + \cdots\right] \tag{2.22}$$

In the case of pipelined ADCs, having scaled sampling capacitors (i.e., they get smaller in successive stages), the noise increases in the later stages, leading to a higher input referred noise.

2.3 Low Power Techniques for Pipelined ADCs

In embedded pipelined ADCs, reducing the power consumption has been the major focus of recent research. Pipelined ADCs are a cascade of low resolution stages that include OTAs and comparators. At each stage, the majority of power is consumed in OTAs [57, 58]. Their power consumption is determined by the load capacitance they drive. Consequently, a designer can minimize the power dissipation by addressing the load capacitance of the OTAs, how the OTAs are used, and the design of the OTAs.

2.3.1 Architectural level design

Historically, pipelined ADCs use I identical stages, where each stage resolves M = N/I bits. A straight forward approach is to employ 1-bit/stage [59]. However, as seen from (**??**), the noise contributions from the later stages are greatly reduced by the interstage gains of the preceding stages. By exploiting this fact, the later stages can be scaled down to save power, while minimally degrading the SNR [31]. By scaling the later stages, the power can be optimized, based on the number of bits converted in each stage.

The precision requirements of each stage depend on how many bits need to be resolved after that stage. Therefore, the precision requirements decrease along the pipeline. Consequently, the later stages can have reduced analog design complexity (lower OTA's gain and

bandwidth and smaller capacitors). Therefore, scaling the capacitors and OTAs in later stages, as shown in Figure 2.13, leads to a low power and area efficient design.

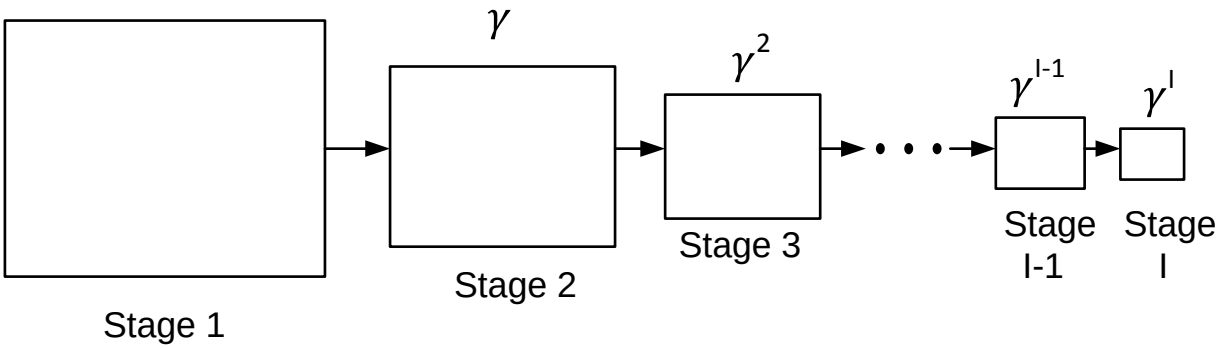


Figure 2.13: Scaling of the pipelined stages by the scaling factor γ.

A relationship between the pipelined ADC power dissipation and interstage scaling has been reported in [31]. A more detailed analysis is described in Appendix Section A.2. In the analysis, a taper factor (x) is chosen to determine the optimal scaling factor between stages. The scaling factor is related to the taper factor (x) by

$$\gamma = 2^{-Mx} \tag{2.23}$$

where M is the stage resolution. The relationship between the taper factor and normalized power dissipation is plotted in Figure 2.14 for different values of M. From the plots, it is evident that the optimal scaling factor is approximately equal to the reciprocal of the interstage gain of the pipelined stage. As shown in Appendix Section A.2, for M=1, a power savings of 70% can be achieved by using the optimal scaling factor.

As portrayed in Figure 2.15, increasing the stage resolution, ideally, results in further power savings. Increasing the number of bits allows greater capacitor scaling in the later stages, resulting in a significant power savings. On the other hand, multi-bits/stage significantly increase the number of comparators and digital overhead required. Therefore, the optimum stage resolution is still an open matter for research.

Based on the previous discussion, pipelined ADCs, designed for low power, are designed with an interstage scaling equal to the interstage gain. Typically, the number of bits converted per stage is higher for higher resolutions and lower for lower resolutions ADCs.

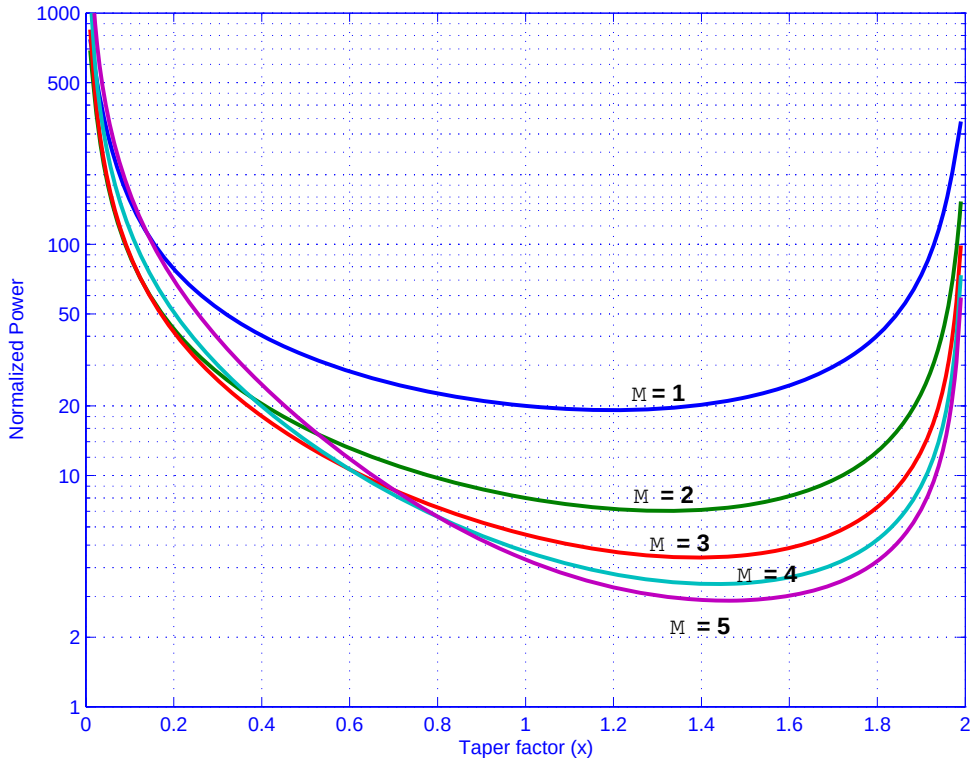


Figure 2.14: Normalized power versus the scaling factor.

2.3.2 Stage level design

At each stage, the dominant source of power dissipation is an OTA. It must be used efficiently, and the design of an OTA must be power efficient.

A traditional regular pipelined stage is implemented as shown in Figure 2.16(a). The load capacitance, C_L, consists of the sampling capacitor of the next stage and the parasitic capacitance loading the OTA. The stage works by sampling the input into 2^M unit capacitors and moving the charge into a single unit capacitor for an overall gain of 2^M. Note that, in an optimally scaled pipelined, the total input capacitance of the following stage is equal to the unit capacitance of the current stage.

An alternative approach for attaining the gain of 2^M is the flip-around technique in Figure 2.16(b). Similar to traditional pipelined stages, the input signal is sampled on 2^M unit capacitors. Then, to achieve the gain of 2^M, the charge on 2^M-1 unit capacitors is transferred to the remaining unit capacitor. Note that the sampling capacitor of the next stage is still equal to the unit capacitance. The benefit of this approach, to typical low

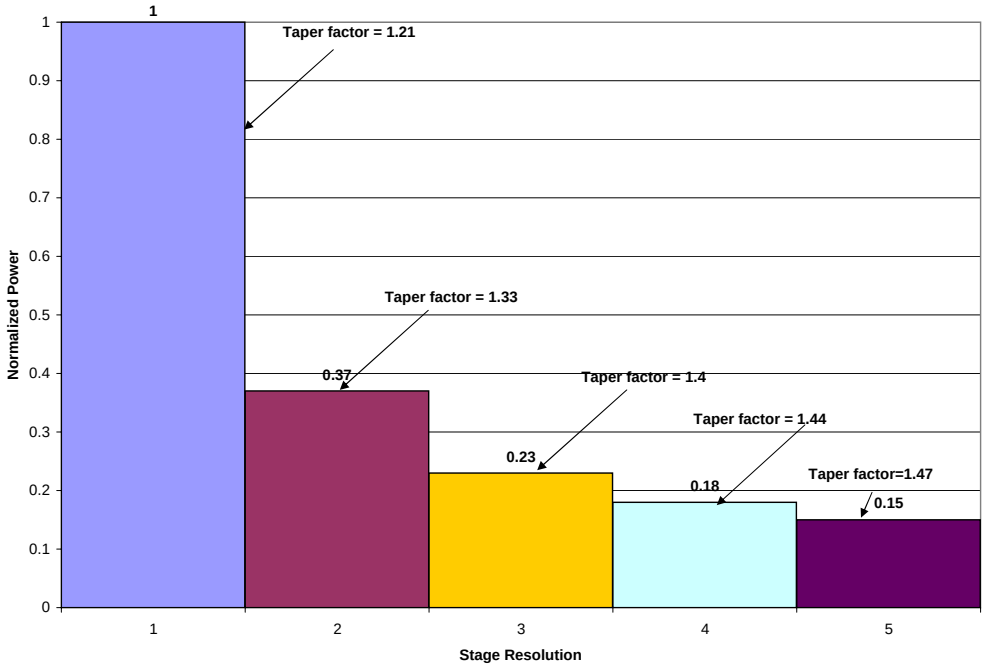


Figure 2.15: Normalized power versus the stage resolution. Here optimum taper factor of each stage resolution is used.

values of M (M=1, M=2), is a significant improvement in the feedback factor. For M=1, the feedback factor is increased from 1/3 to 1/2 in an ideal circuit. The improved feedback factor can be exploited to increase the speed or the power dissipation is reduced to maintain the desired speed. Consequently, for all pipelined ADCs, based on the 1-bit/stage, the flip-around architecture is the preferred choice.

The second approach to minimize the power within the stage is to utilize the OTA in a more efficient manner. Note that in typical implementations, during the sampling phase, the OTA is idle. This leads to the development of the switched-OTA (SO) technique [32,37], the OTA-shared technique [35, 60], and the double-sampling (DS) technique [61, 62].

For the switched-OTA technique in Figure 2.17, the OTAs are switched off during the sampling phase, ϕ_1, thereby reducing the overall power consumption. Also, the switch at the output of the OTA is removed. A drawback of this approach is that an additional turn-on time is needed, when the OTA is switched back ON from the OFF state.

Another low power design technique is based on the principle of OTA sharing. Here, one OTA serves as the residue amplifier for two different stages during two different clock phases. Therefore, the number of total OTAs are reduced by half, saving both area and

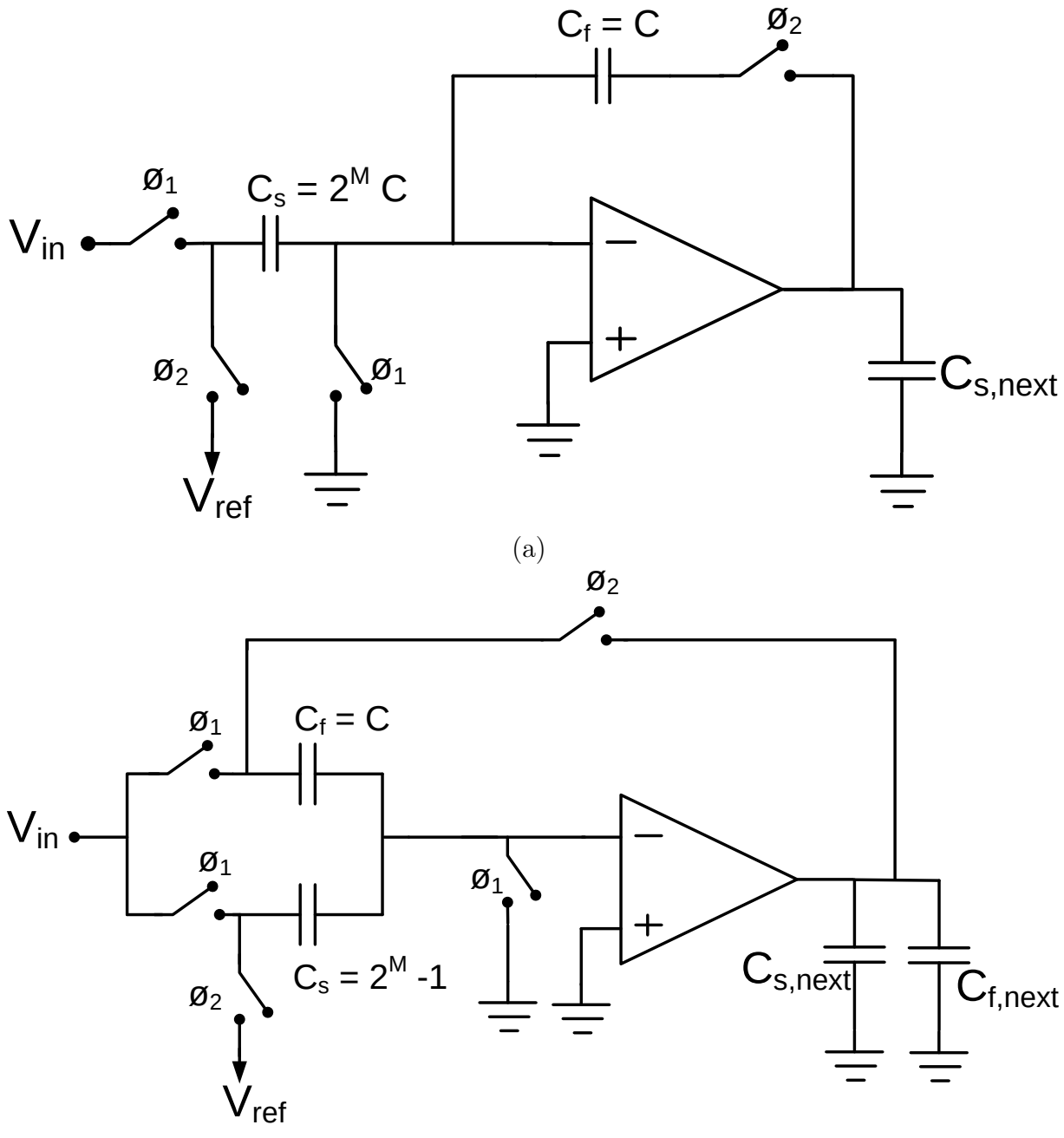


Figure 2.16: Traditional regular and flip-around configuration pipelined stage: (a) traditional regular (TR) pipelined stage and (b) traditional flip-around (TFA) pipelined stage.

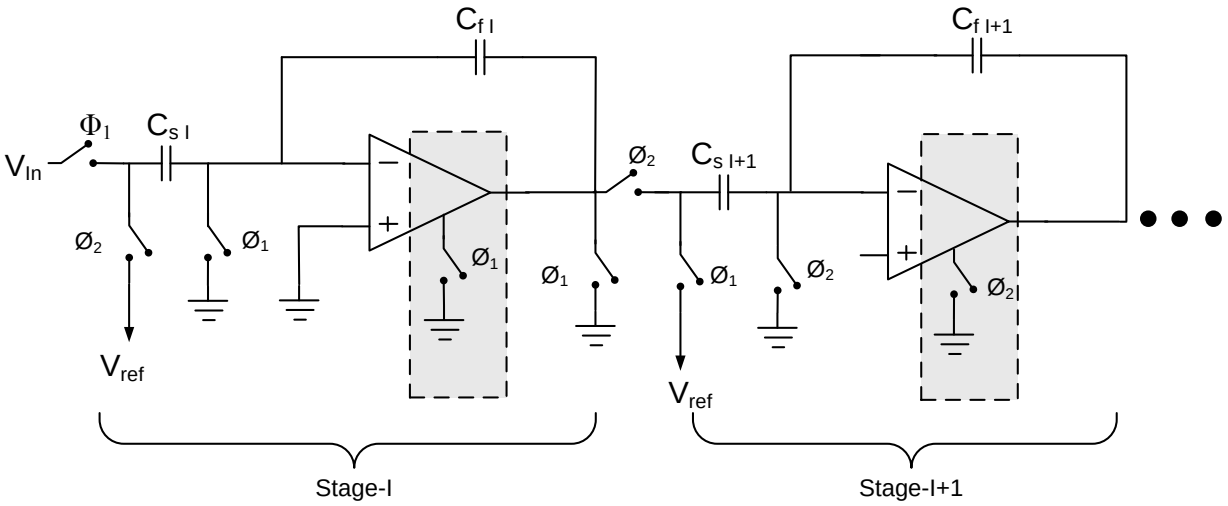


Figure 2.17: Switched-OTA (SO) technique.

power. Figure 2.18 indicates the OTA is shared between two time interleaved stages, whereas in Figure 2.19, the OTA is shared by the consecutive stages.

As mentioned that an OTA is used for only half of the clock cycles, hence, effectively, sampling rates can be doubled and the OTA is utilized in both the clock phases [63], as shown in Figure 2.20. Alternatively, the DS technique facilitates halving the clock frequency, thereby minimizing the power consumption. It is observed that during phase ϕ_1, $C_{s_{odd}}$ samples the input signal. During ϕ_2, $C_{s_{odd}}$ transfers its charge to C_{f_i}, and $C_{s_{even}}$ samples the input, and so on. In other words, the output is updated during both phases such that the operation speed is twice as fast as that of the conventional single sampling stage.

In summary, since the dominant source of power consumption in an individual stage is the OTA, most of the techniques, discussed at the stage level, are used to decrease the number of OTAs by sharing them or to switch them OFF. In addition, the flip-around technique is employed for almost all the low resolution stages due to its power dissipation being lower than that of the regular gain technique.

2.3.3 Circuit level design

Once the number of bits/stage, interstage gain and overall structure of the individual stages is determined, the circuits within the stage must be designed for low power. Within each stage, the key components are DACs, comparators, and OTA. The DAC is inherently

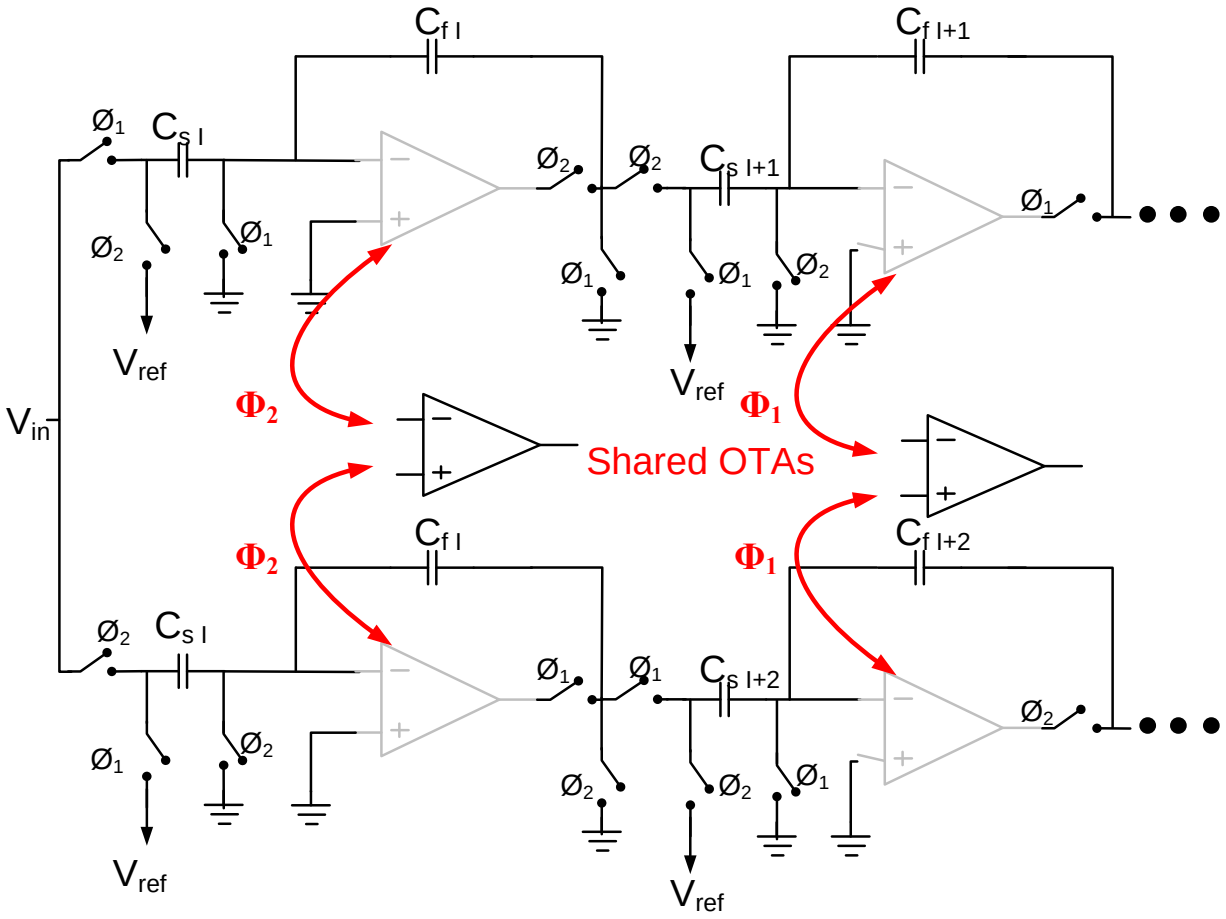


Figure 2.18: Concept of OTA-shared technique across two parallel channels.

low power, and dynamic comparators are commonly used due to their minimum power consumption. This leaves the OTA as the major source of power dissipation within each stage. Consequently, a number of researchers have focused on lowering the power of the OTAs in pipelined ADCs [64–67].

An OTA, in SC pipelined ADCs, has two tasks: to accurately transport the signal charge from one capacitor to another capacitor without leaking the signal charge to the parasitic capacitors and to act as a buffer such that the voltage on the capacitors can be sampled without affecting the charge on the capacitors. Historically, high gain wide bandwidth OTAs have been used to perform the two aforementioned tasks. These amplifiers are class-A and dissipate a significant amount of power. Recently researchers have looked at other amplifier architectures based on the class-B operation for low power. For example, comparators have been used as OTAs [64], and an even simpler approach is to employ a

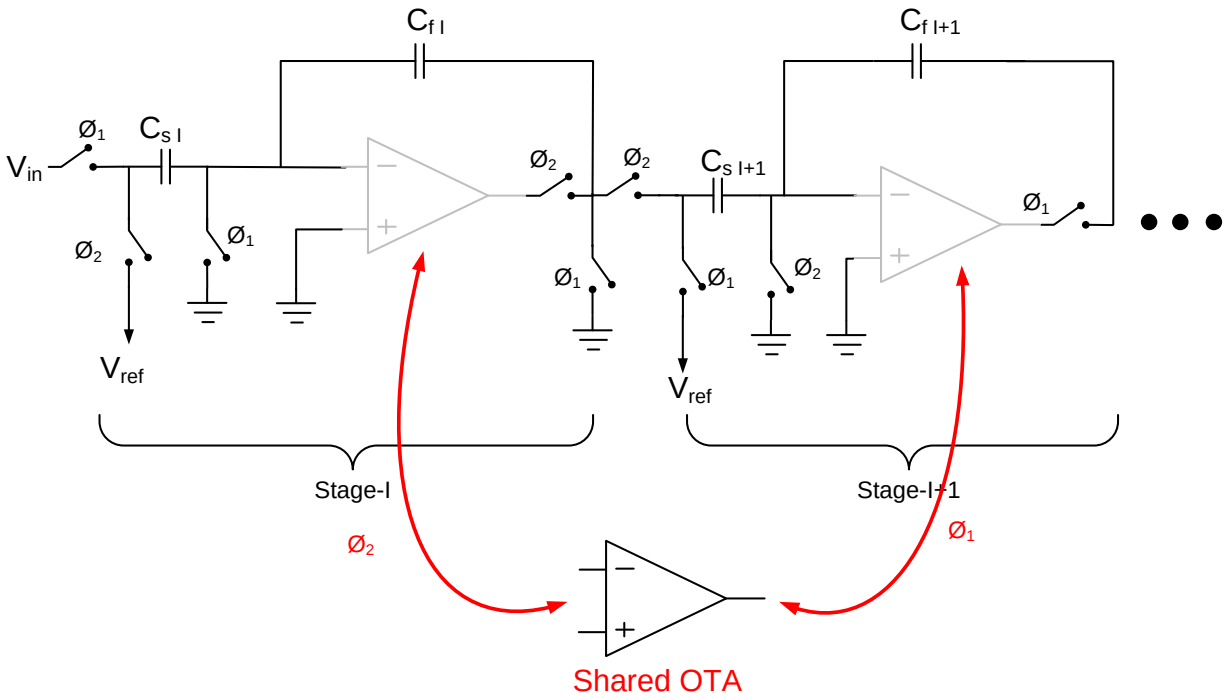


Figure 2.19: Concept of OTA-shared technique between two cascaded stages.

zero crossing based detector [65]. By using wide bandwidth and low gain OTAs, significant power savings can be achieved and the resulting errors are corrected in the digital domain [66, 67]. This low power OTA design remains an area of active research interest.

In summary, the low power design techniques for pipelined ADCs are discussed. It is found that the low power techniques for pipelined ADCs can be efficiently used at the architectural, system, and circuit levels.

2.4 Overview of Recent Energy Efficient Techniques for Algorithmic ADCs

Due to the cyclic nature of algorithmic ADCs, many of these conventional low power techniques for pipelined ADCs cannot be utilized in typical implementations of algorithmic ADCs. However, a variety of ways of modifying the conventional algorithmic ADC to reduce the ADC's power consumption are reported in the literature [1, 13, 46, 55, 68–71]. Such techniques can be broadly classified into three categories:

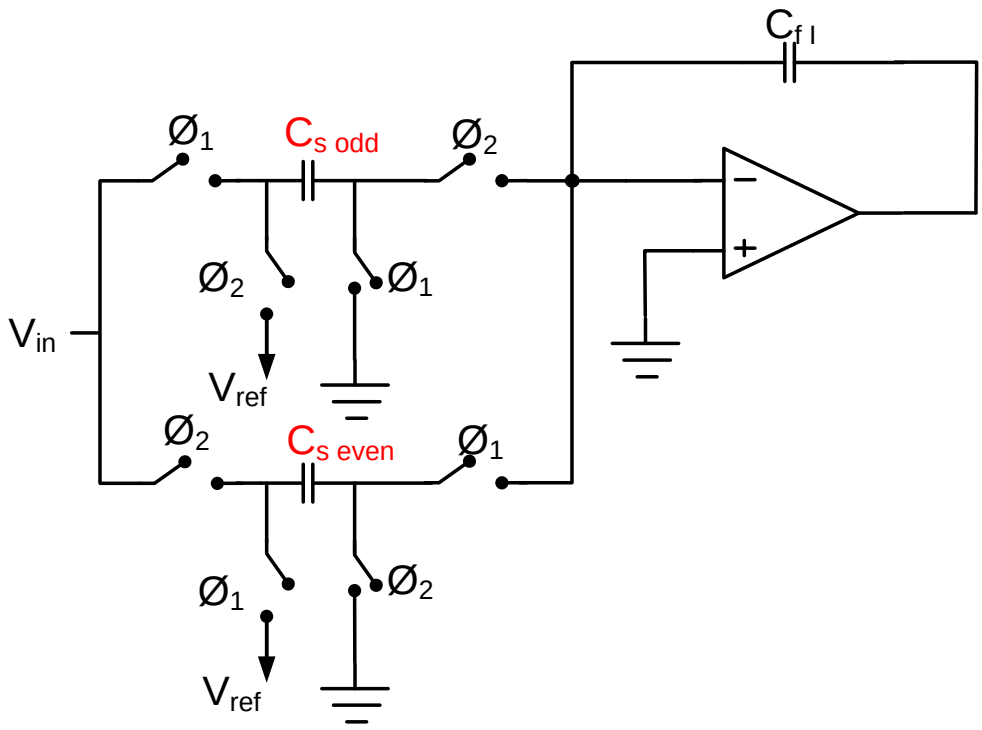


Figure 2.20: Double sampling (DS) technique.

- flip-around configuration and OTA-shared technique
- bias and clock phase scaling
- capacitor-shared technique

2.4.1 Flip-around configuration and OTA-shared technique

The most straightforward low power configurations utilize the flip-around configuration and OTA-shared techniques [13, 46, 59, 68]. The former technique reduces the load capacitance of the OTA and the latter technique cuts the number of OTAs to one. A single-ended flip-around configuration and OTA-shared SC algorithmic ADC is displayed in Figure 2.21. The ADC requires only two sets of capacitors $\{C_1, C_2\}$ and $\{C_3, C_4\}$, an OTA, and switches. During ϕ_{in}, the input signal, V_{in} is sampled on C_1 and C_2. Then, during ϕ_e, C_1 is connected to the DAC reference and C_2 is connected around the OTA to generate the residue. The residue is sampled by C_3 and C_4. To generate the next residue, the roles of

C_3 and C_4 are exchanged with C_1 and C_2, respectively, during ϕ_o. This residue generating and sampling process continues for N-phases until all the N-bits are resolved.

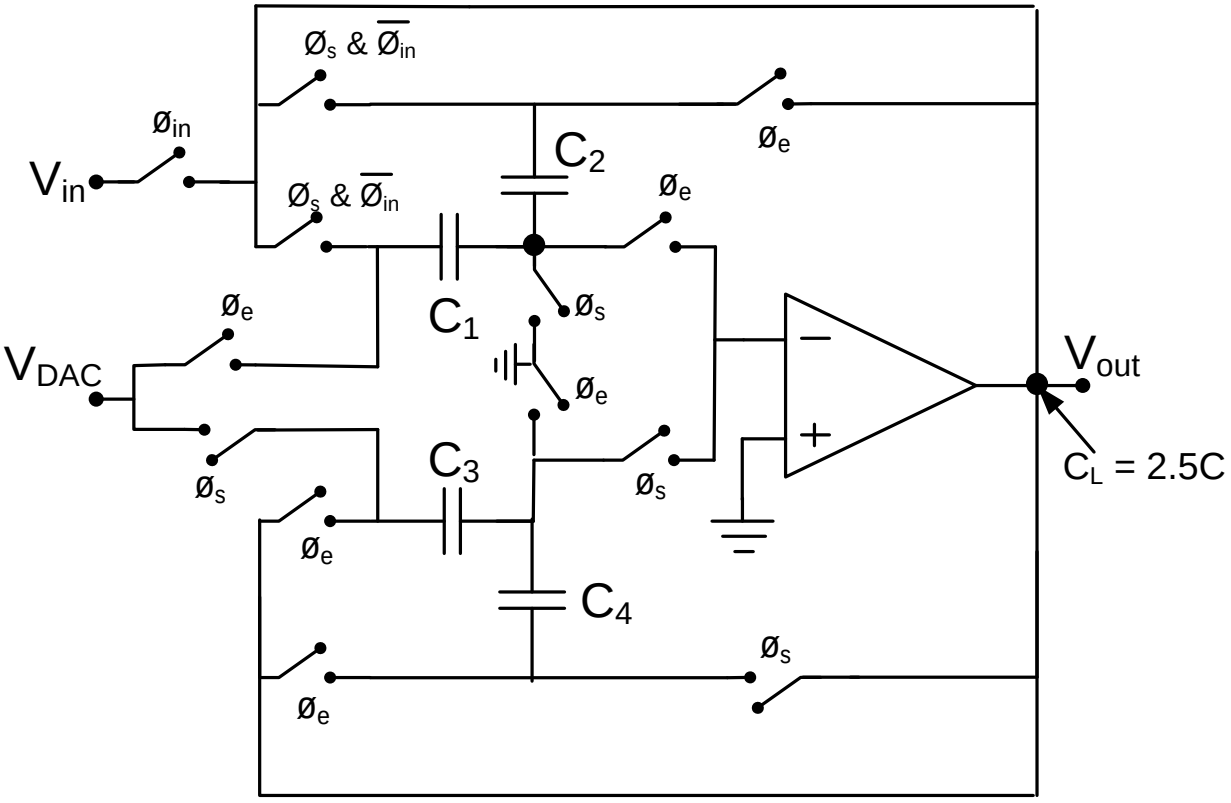


Figure 2.21: Single-ended SC implementation of a flip-around configuration and OTA-shared algorithmic ADC.

The combination of the flip-around configuration and OTA-shared scheme significantly reduces the power consumption of algorithmic ADCs. As listed in Table 2.1, OTA-shared technique reduces the conversion time from 2N in the conventional case to N clock phases due to the lack of an explicit sample and hold phase. The flip-around configuration reduces the power consumption of conventional ones by 50% due to its improved feedback factor and reduced load capacitance. Due to their significant energy savings, the flip-around configuration and OTA-shared technique is used in almost all algorithmic ADCs.

2.4.2 Bias and clock phase scaling

In an algorithmic ADC, the OTA is the most power hungry block. The power consumption of an OTA depends on its settling time requirements. During the residue evaluation phase,

Table 2.1: Comparing power and conversion time of the different techniques for an N-bit ADC.

Technique	Normalized Power (P_N)	Conversion Time (T_c)	Energy ($E = P_N \times T_c$)
Conventional	1	1	1
Flip-around	0.5	1	0.5
OTA-shared	1	0.5	0.5
Flip-around and OTA-shared	0.5	0.5	0.25
Phase scaling	1	0.5	0.5
Scaling first 4 cycles	1	0.75	0.75
Bias current scaling	0.5	1	0.5
Scaling first 4 cycles	0.75	1	0.75

the required settling time of an OTA is based on the number of unresolved bits after the current bit. Consequently, after each bit conversion, the OTA settling time requirements are relaxed and can be traded off for power savings [55, 69].

For a single pole OTA, from (2.18), the settling time requirement of the OTA is written as

$$T_{set} = \frac{(N + 1 - K) \cdot \ln 2 \cdot C_L}{\beta \cdot g_m} \tag{2.24}$$

where K is the current bit being resolved beginning with the MSB. Therefore, during each bit conversion, the OTA's settling time requirements are relaxed by a factor of $\frac{(N-K+1)}{(N-K)}$ as the K bits are resolved. Thus, this relaxation can be exploited by either scaling the clock phases or slowing down the OTA by reducing its bias current.

2.4.2.1 Non-uniform clocking

In traditional implementations of algorithmic ADCs, the conversion time allotted to each bit is equal to the conversion time of the MSB, irrespective of the bit's weight. Equation (2.24) reveals that the settling time requirement decreases as more bits are resolved. For example, a 10-bit ADC theoretically requires 10,9,8...1 time units for each data conversion, compared to ten time units for each phase in the conventional scheme. Therefore, to exploit the relaxed settling requirements, a possible technique is to scale the clock phases according to the accuracy requirements of each conversion step [55].

As shown in Figure 2.22, after the MSB conversion, for a 10-bit ADC, the minimum settling time is reduced by 10% in each step. Therefore, the clock phases can be reduced by 10% for each successive step. Consequently, the conversion time can ideally be reduced by a factor of $\frac{N+1}{2N}$ compared to that of uniform clocking. However, due to jitter and slewing considerations, only the first few clock phases of the ADC are scaled in practice [55], leading to a lower power savings than expected.

For a given sampling frequency, the reduced conversion time is traded for lower. As a result, a power reduction as high as 50%, is achieved by using non-uniform clocking. Unfortunately, to generate the non-uniform clock phases, a phase-locked-loop (PLL) or a delay-locked-loop (DLL) is required. This PLL or DLL increases the area and power consumption of the overall ADC.

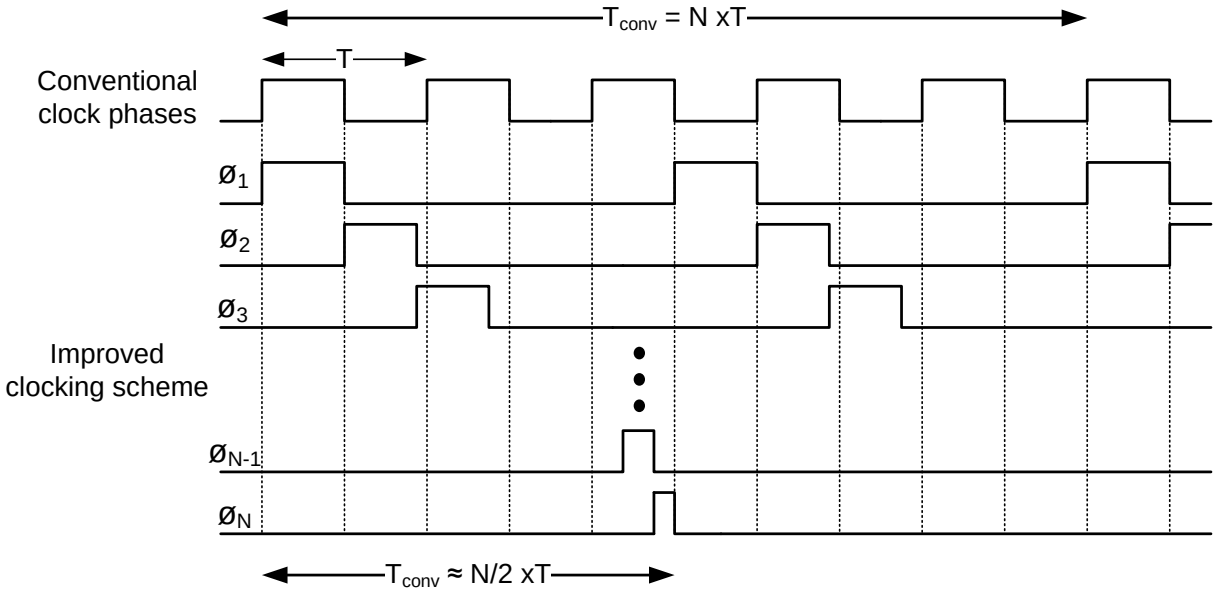


Figure 2.22: Non-uniform clocking scheme of an N-bit algorithmic ADC.

2.4.2.2 Dynamic biasing technique

Another way to exploit the reduced settling time requirements of an MDAC is to adaptively scale transconductance, g_m, of the input transistors by reducing the bias current in each successive cycle, decreasing the overall power consumption [69]. A possible implementation scheme for dynamic biasing, shown in Figure 2.23, consists of N mirrored transistors, where N is the ADC resolution. During each cycle, gate of one of the mirror NMOS is disconnected

from the bias node and connected to the ground. Therefore, in each cycle, the bias current is scaled, reducing the excess power dissipation.

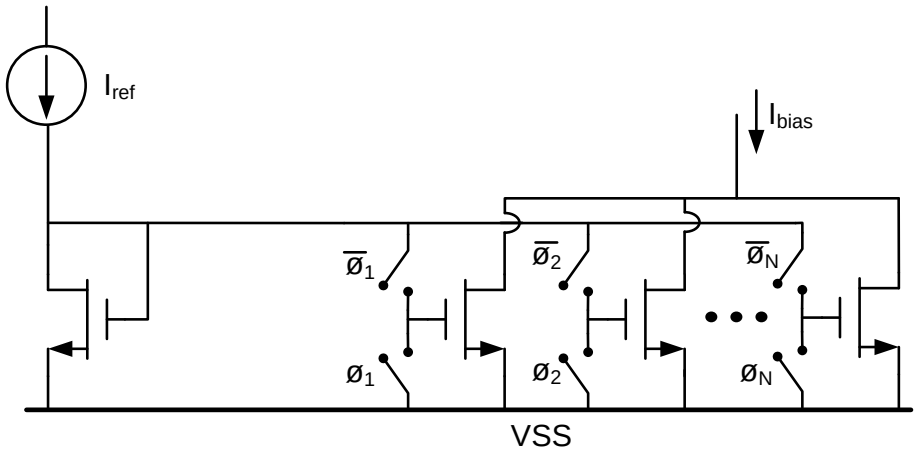


Figure 2.23: Dynamic current scaling scheme of an N-bit algorithmic ADC.

The step response of a single pole OTA is written as

$$V_{ofinal} = V_{in}\left(1 - e^{-\frac{t}{\tau}}\right) \tag{2.25}$$

where V_{ofinal} is the final output, V_{in} is the input step, t is the settling time and τ is the time constant. Also, the output current, $i = C\frac{dV}{dt}$, during linear settling, the OTA's output current is represented as

$$i_o(t) = C_L \cdot \frac{dV_o(t)}{dt} = \frac{C_L \cdot V_{ofinal}}{\tau} e^{-\frac{t}{\tau}} \tag{2.26}$$

Since the maximum current $|i_o|_{\max}$ flows at t=0, $|i_o|_{\max}$ is expressed as

$$|i_o|_{\max} = \frac{C_L \cdot V_{ofinal}}{\tau} \tag{2.27}$$

If $|i_o|_{\max} > I_{bias}$, then slewing occurs and the slew rate, SR, is expressed by

$$SR = \frac{I_{bias}}{C_L} \tag{2.28}$$

Assuming the total settling time consists of slewing time and linear settling time, for $I_{bias} < \frac{C_L \cdot V_{ofinal}}{\tau}$, the OTA's settling time requirement increases by lowering the bias cur-

rent. Consequently, the bias current scaling is advantageous only if C_L can also be scaled for all the cycles.

2.4.2.3 Summary

The aforementioned scaling techniques can be combined with the flip-around configuration and OTA-shared technique to reduce the overall power consumption as summarized in Table 2.2, where P_N is the average power consumed by an N-bit ADC, T_c is the time taken by an N-bit ADC to complete one data conversion and E is the energy consumed by the ADC.

Table 2.2: Combining flip-around configuration and OTA-shared technique with phase and bias current scaling for an N-bit ADC.

Technique	Utilizing flip-around configuration and OTA-shared		
	P_N	T_c	E
Phase scaling	0.5	0.25	0.125
Scaling first 4 cycles	0.5	0.375	0.188
Bias current scaling	0.25	0.5	0.125
Scaling first 4 cycles	0.375	0.5	0.188

For the practical case of scaling only the first four cycles, non-uniform clocking reduces the conversion time by 75%, whereas the bias current scaling reduces the power consumption by 75%. Hence, both non-uniform scaling and the bias current yield the same improvement in energy efficiency, more than 80% of that of conventional implementation. However, phase scaling is more challenging to implement due to the need for a DLL or PLL, which increases the overall power consumption and design complexity.

2.4.3 Capacitor-shared techniques

As already mentioned in Section 2.3.3, reducing the OTA's power consumption reduces the overall power consumption of the ADC. According to (2.24), for a given settling time,

$$g_m \propto C_L \tag{2.29}$$

In a well-designed circuit, g_m is proportional to the power consumption, and the power consumption is linearly proportional to the load capacitance. Hence, reducing the load capacitance reduces the ADC's power consumption.

One possible technique for load reduction is to utilize the capacitor-shared technique commonly used in pipelined ADCs [34,37,38]. The capacitor-shared technique is based on the observation that, when pipelined ADCs are scaled for minimum power, the capacitors in each stage are scaled by the interstage gain, and the feedback capacitor of one stage becomes equal to the total input capacitance of the following stage. As a result, the feedback capacitor of one stage can be reused as the input capacitor for the following stage to reduce the OTA's capacitive load, and further reduce the power requirements of pipelined ADCs.

Capacitor-shared technique can be applied to algorithmic ADCs by partitioning the sampling and feedback capacitors into two equal sized capacitors,C_{1a},C_{1b} and C_{2a},C_{2b}, evident in Figure2.24(a) [70]. During the sampling and generation of the first residue, the operation is identical to the algorithmic ADC, described in Figure 2.21. At this point, the residue is held by C_{2a} and C_{2b} . In the next phase, C_{2a} is connected to the DAC reference, while the other capacitor C_{2b} remains connected in the feedback. Figure 2.24(c) conveys that the residue is then sampled by the other set of capacitors, C_{1a},C_{1b}. In the following phase, the two sets of capacitors swap roles as depicted in Figure 2.24(d). Such techniques reduce the load capacitance by 50%, and the capacitor area by 50%, compared to that of the flip-around scheme. However, due to scaling of the capacitors, the input referred thermal noise increases. Therefore, the load capacitance must be increased by almost 1.5 times to compensate for the SNR degradation. Nevertheless, the power savings can be significant, and consequently, the concept of capacitor-shared technique can be implemented in a variety of different ways.

2.4.3.1 2-cap-shared technique

A simple low-area low-power capacitor-shared technique has been presented [1]. As shown in Figure 2.25, for the single-ended case, this technique utilizes only two capacitors. During the evaluation phase, the feedback capacitor, C_2, is charged to the desired output voltage shown in Figure 2.25(a). However there is no explicit sampling capacitor for the next cycle. In order to perform the next conversion, an extra set of capacitors is needed. This is accomplished by arranging the MDAC as a SHA. Figure 2.25(b) demonstrates that the

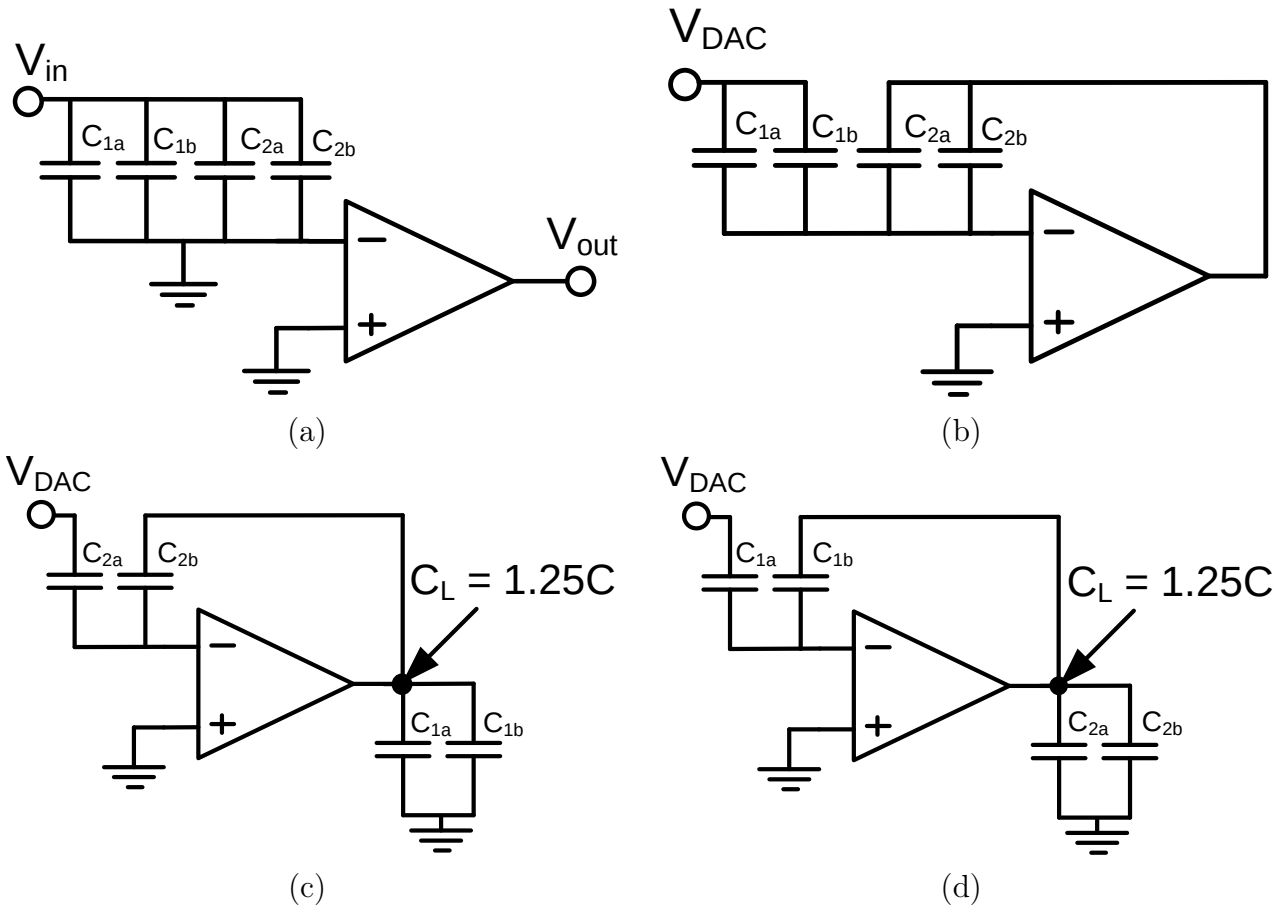


Figure 2.24: Capacitor-shared technique: (a) sampling, (b) 1st evaluation phase, (c) 2nd evaluation phase, and (d) 3rd evaluation phase.

plates of C_1 are disconnected from the DAC reference and the OTA's input, and connected to the OTA's output and OTA's input common mode, respectively. This technique reduces of the flip-around implementation by 50%, but requires an additional clock phase. Here, the load capacitance is reduced by 60% compared to that of the flip-around technique and 80%, compared to that of the conventional implementation. However, the required extra phase makes it 50% slower than the flip-around configuration and OTA-shared implementation. These results are summarized in Table 2.3.

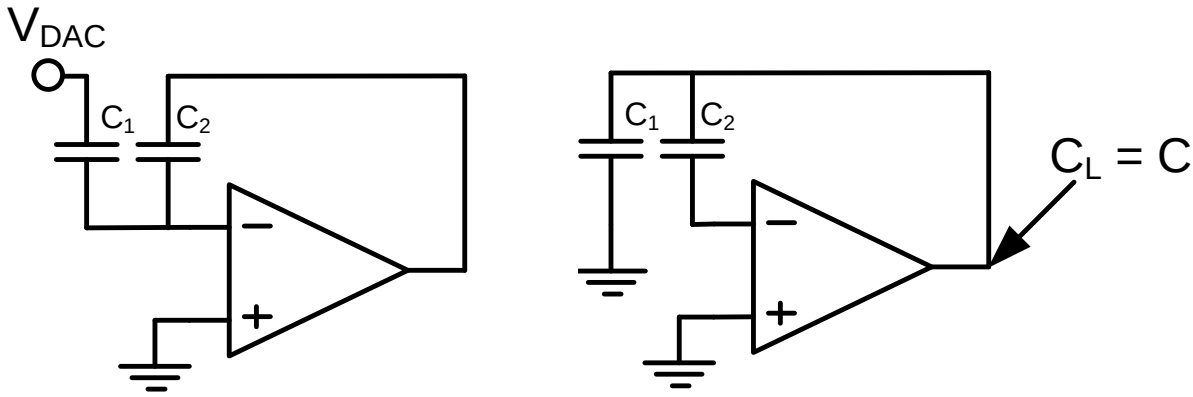


Figure 2.25: 2-cap-shared technique: (a) 1st evaluation phase and (b) sampling capacitor charging phase.

Table 2.3: Combining flip-around configuration and OTA-shared technique with the capacitor-shared techniques for an N-bit ADC.

Technique	Utilizing flip-around configuration and OTA-shared		
	P_N	T_c	E
Capacitor-shared	0.375	0.5	0.188
2-cap shared	0.2	1	0.2

2.5 Figures-of-Merit for ADCs

In this section, low power limits of sampling-based ADCs are discussed. Also, different figures-of-merit (FOM) for ADCs are presented, along with the FOM comparison of pipelined and algorithmic ADCs.

2.5.1 Low power limit of ADCs

Fundamentally, all ADCs must sample the analog signal, and the accuracy of the sampled signal must be enough to meet the SNR requirement. In practical circuits, the analog signal is sampled on the capacitor, along with the thermal noise. By increasing the capacitor size, the relative SNR is improved. Therefore, the sampling capacitor should be sized for the desired SNR. Then, the power required to charge the sampling capacitor at the required rate limits the minimum power dissipation. This minimum sampling power, as derived in

(A-29), is determined as

$$P_s = 12kT \cdot f_s \cdot 2^{2N} \tag{2.30}$$

This equation states that the power consumption in an ADC is proportional to the resolution squared and the sampling frequency. Note that (2.30) is technology independent and sets the lower bound for any sampling-based ADC.

2.5.2 ADCs' FOM

ADCs are designed for a wide range of sample rates and resolutions. Consequently, direct comparison of the power dissipation of various ADCs is difficult. As a result, a variety of different FOMs have been proposed.

The ideal FOM weighs the desirable and undesirable factors in such a manner that the tradeoff among different factors can be done in a relatively neutral fashion. For ADCs, the signal bandwidth (typically half the sampling frequency) and the resolution are desirable features, whereas the power dissipation is undesirable. One of the most popular FOM is attributed to Walden [72] and is defined as

$$FOM_1 = \frac{P}{\min(f_s, 2 \cdot ERBW) \cdot 2^{ENOB}} \tag{2.31}$$

where the nominal units are the pJ/conversion-step, $ENOB$ is the effective number of bits, f_s is the conversion rate at which the ADC is running, and $ERBW$ is the effective resolution bandwidth. The FOM_1 is a direct measure of the parameters depending what designers want and not want in an ADC.

In light of the fundamental power dissipation of ADC, derived in (2.30), FOM does not give weight to the SNR and power tradeoff. As a result, a thermal noise based FOM is commonly used such that

$$FOM_2 = \frac{P}{\min(f_s, 2 \cdot ERBW) \cdot 2^{2ENOB}} \tag{2.32}$$

where the nominal units are the pJ/conversion-step squared. However, this assumption is pessimistic for real designs, as not all building blocks of the ADC, such as comparators and digital clocks, are thermal noise limited.

2.5.3 Recent progress in low power pipelined and algorithmic ADCs

Recently, researchers have attempted to reduce the power consumption of ADCs. Many researchers aimed at increasing the resolution and sampling rates of the ADCs. Figure 2.26 is a plot FOM of recently published pipelined and algorithmic ADCs and the year of publication. There is a trend towards energy efficient ADCs. This is also evident in the

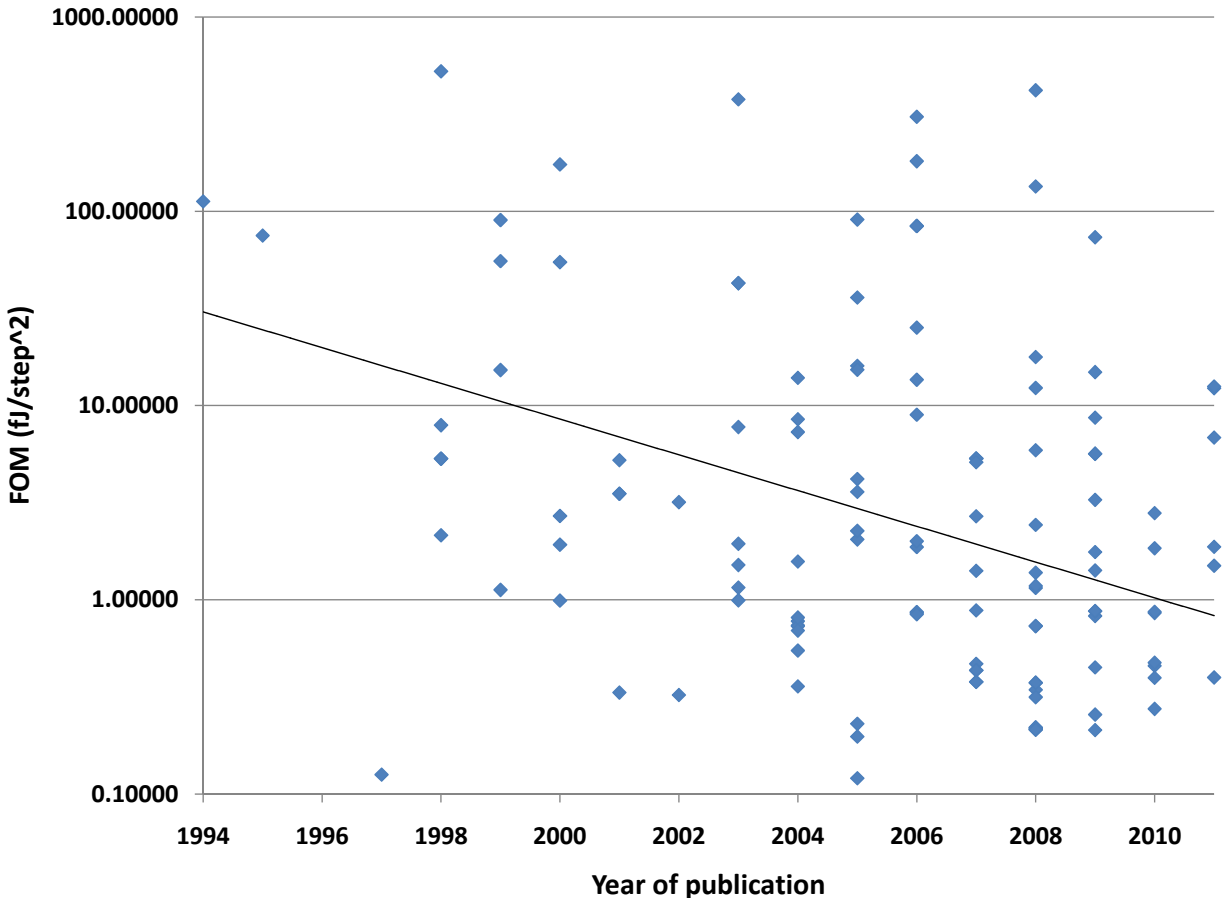


Figure 2.26: FOM_2 versus year of publication for pipelined and algorithmic ADCs.

energy consumption, in terms of mW/MHz, which is plotted in relation to the ENOB in Figure 2.27.

2.5.4 Comparison of the FOM of algorithmic and pipelined ADCs

As already mentioned at the beginning of this section that due to the cyclic nature of algorithmic ADCs, many of these conventional low power techniques for pipelined ADCs

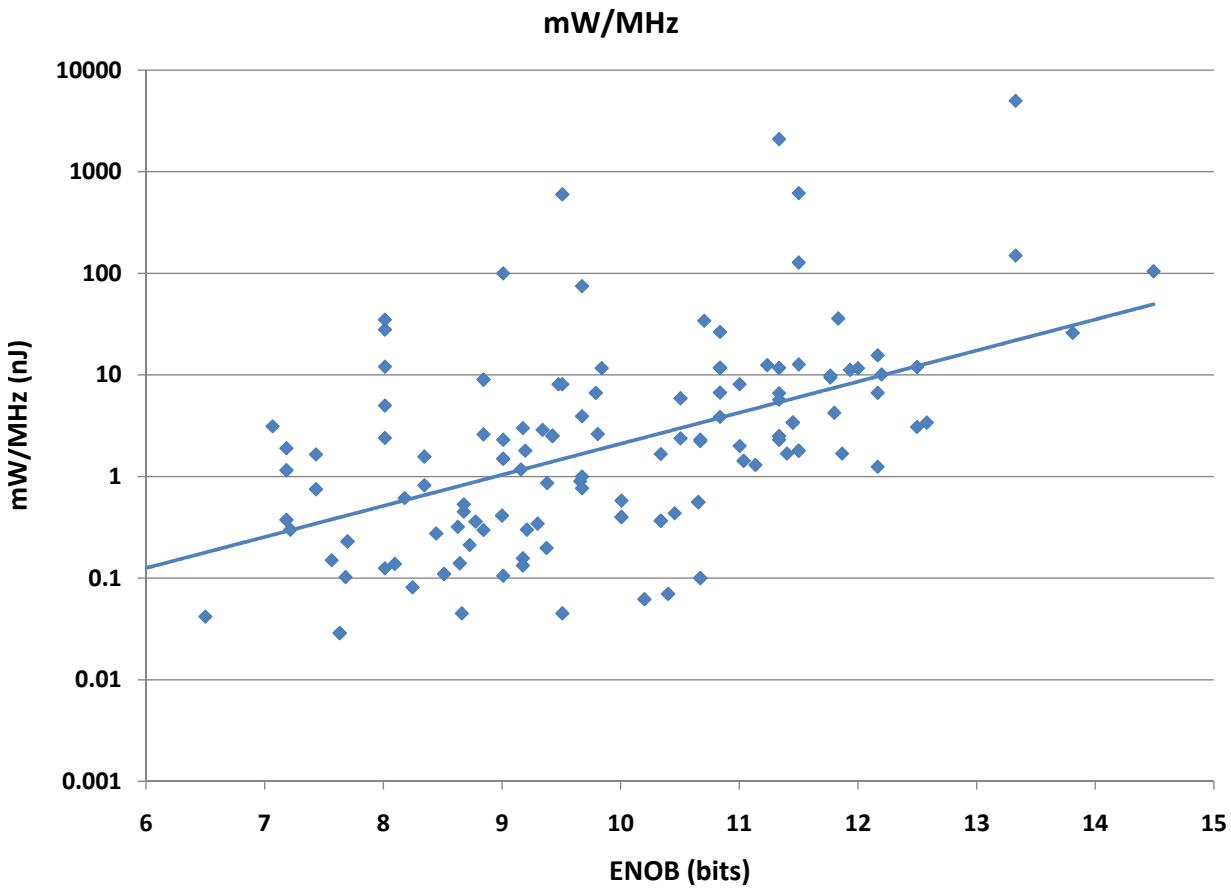


Figure 2.27: mW/MHz versus the ENOB of published pipelined and algorithmic ADCs.

cannot be utilized in typical implementations of algorithmic ADCs. Consequently, when compared to pipelined ADCs, traditional algorithmic ADCs have lagged in terms of energy efficiency. Figure 2.28 illustrates the FOM_1 of recently reported algorithmic and pipelined ADCs. It can be seen that algorithmic ADCs' FOMs fall behind the pipelined ADCs' FOMs for any given year of publication.

2.6 Summary

This chapter focuses on the architectural details of algorithmic ADCs in general and their low power techniques in particular. There is a growing trend towards energy efficient ADCs, but compared to pipelined ADCs, algorithmic ADCs are lagging behind in energy efficiency. The fundamental reason behind is the cyclic nature of the algorithmic ADCs

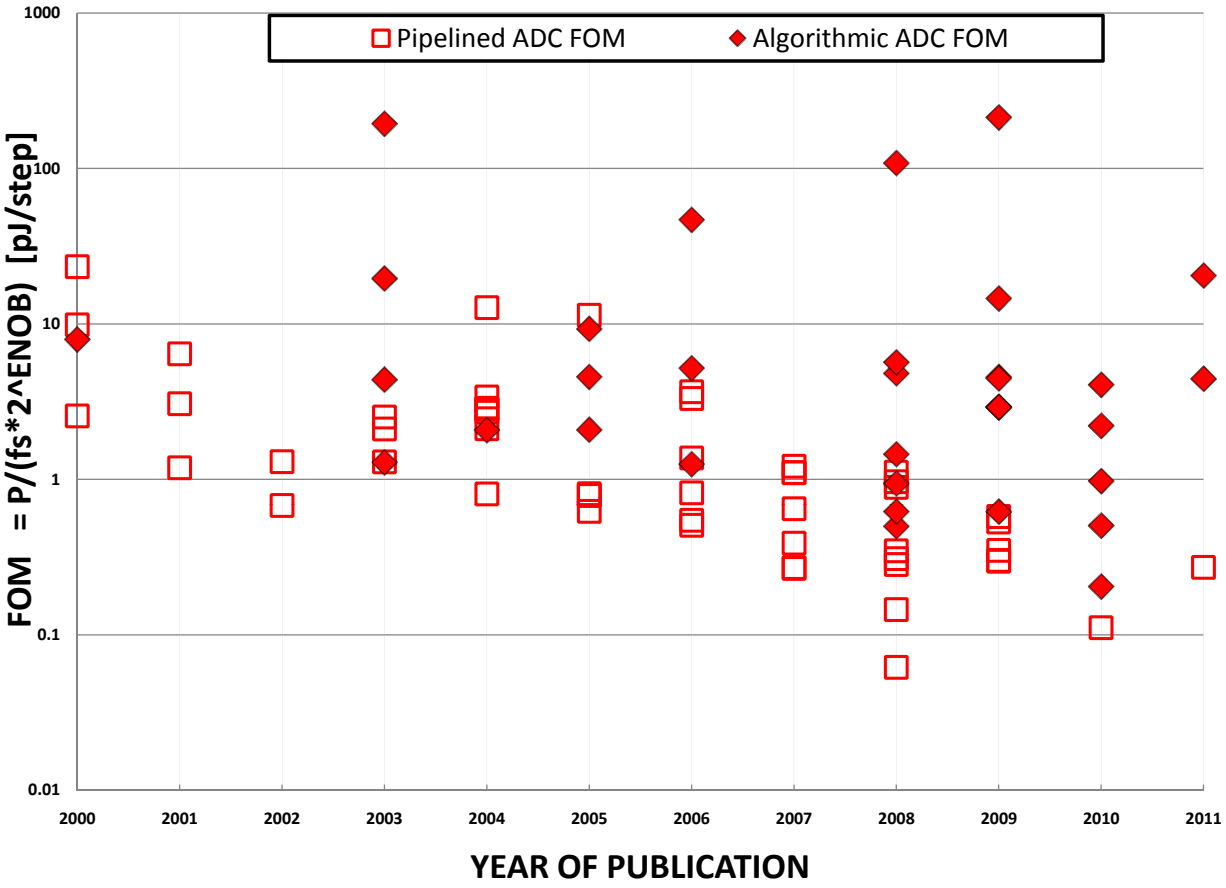


Figure 2.28: Comparison of the FOMs of recently published algorithmic and pipelined ADCs.

and their inability to utilize interstage scaling. It is evident that there is enough room for improvements in the energy efficiency of algorithmic ADCs.

Chapter 3

Power Reduction In Algorithmic ADCs With The Capacitor-shared And The Capacitor-scaled Techniques

3.1 Overview

Algorithmic ADCs are an attractive choice for image sensing and capacitive sensing applications [1, 13]. There is a continuous demand for lower power algorithmic ADCs for these applications. This chapter describes the proposed low power capacitor-shared and capacitor-scaled techniques for algorithmic ADCs, and the power estimates of the proposed techniques. Also, a thermal noise analysis and low power limits are shown for the techniques proposed in this thesis. They are based on a 3-cap-shared technique and a combined capacitor-shared and capacitor-scaled technique.

3.2 Proposed 3-Cap-Shared Technique for Algorithmic ADCs

As already mentioned in Section 2.4.1, the flip-around configuration and OTA-shared technique is the most popular SC implementation scheme of an algorithmic ADC. In the proposed 3-cap-shared technique, a modification of the capacitor arrangements of the flip-

around configuration is presented. This modification results in a considerable reduction of the OTA's load capacitance and the capacitors' area.

3.2.1 Proposed approach

In the flip-around configuration and OTA-shared scheme, described in Sec.2.4, a total of four capacitors are required to perform the conversion: two capacitors to generate the residue and two to sample the residue, as shown in Figure 3.1. The arrangement of C_1 and C_2 generate the residue voltage, which is sampled on C_3 and C_4. Also, the same residue voltage is held across the feedback capacitor, C_2. Therefore, three capacitors hold the residue voltage at the end of the evaluation phase.

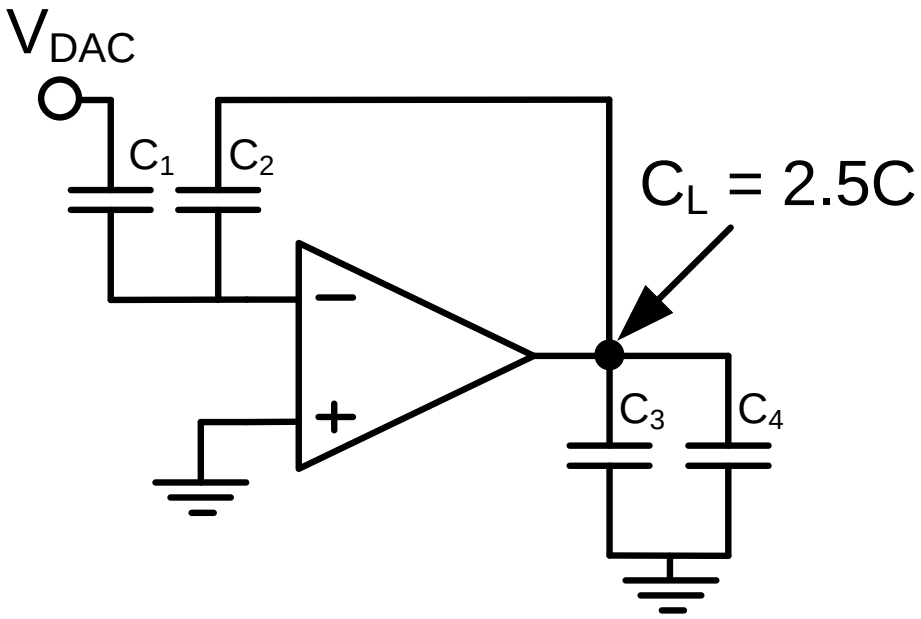
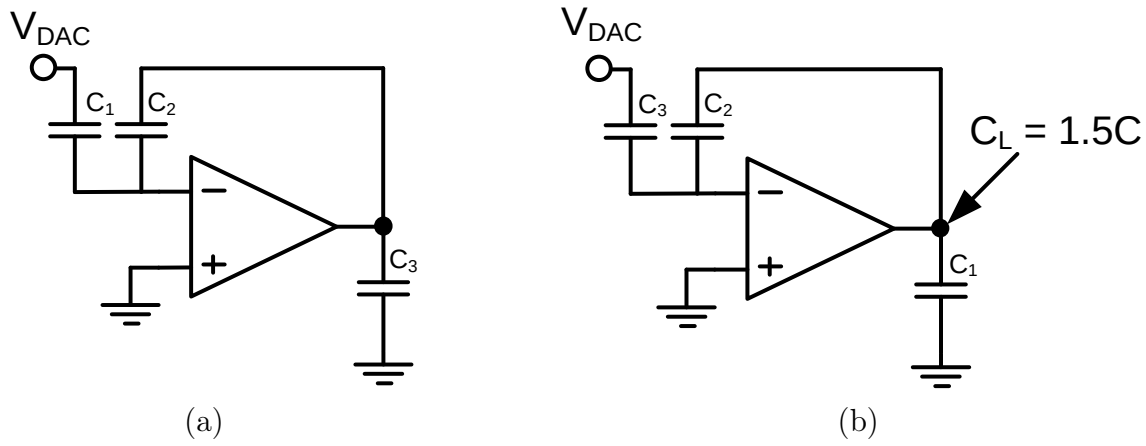


Figure 3.1: Evaluation phase of the flip-around configuration and OTA shared stage.

Since only two capacitors are required to generate the residue, only two capacitors are needed to sample the signal from the previous cycle. As a result, one capacitor at the output can be removed without affecting the overall operation of the algorithmic ADC. By assuming C_4 is removed, the next conversion is performed by keeping C_2 connected to the feedback during the entire conversion process, whereas C_1 and C_3 swap roles during the alternate phases, as depicted in the Figure 3.2(b). This residue generation continues



(a) (b)

Figure 3.2: 3-cap-shared technique: (a) 1st evaluation phase and (b) 2nd evaluation phase.

for N-phases to generate N-bits. The 3-cap-shared arrangement reduces the load capacitance from 2.5C to 1.5C (40%) compared to the flip-around configuration and OTA-shared technique.

3.2.2 Improved 3-cap-shared approach

The explicit load capacitance, C_3 or C_1, contributes about two-thirds to the overall load capacitance (Figure 3.2). A further load reduction can be achieved by arranging the capacitors such that C_3 is removed and C_2 is divided into two equal sized capacitors C_{2a},C_{2b}, providing the two capacitors necessary for the next residue generation. Also, C_1 is divided equally into C_{1a},C_{1b}. The first residue evaluation phase is shown in Figure 3.3(a). To evaluate the next residue, C_{2a} is connected to the DAC reference, whereas C_{2b} is kept connected in the feedback. As already mentioned, two capacitors are required for sampling the signal for the next cycle. Therefore, C_{1a} can be used as the required capacitor as shown in Figure 3.3(b). During the remaining evaluation phases, C_{1a} and C_{2a} swap roles, whereas C_{2b} remains connected in the feedback. This process continues until all the bits are generated. Note that after the first evaluation phase, C_{1b} is disconnected from the sum node and is not used in later cycles.

This capacitor-shared scheme reduces the load capacitance considerably: from 2.5C for the flip-around configuration case to 0.75C for the improved 3-cap-shared case. Since scaling increases the input referred thermal noise, the load capacitance must be increased by 1.25 times in order to compensate for the degraded SNR. Consequently, a power savings

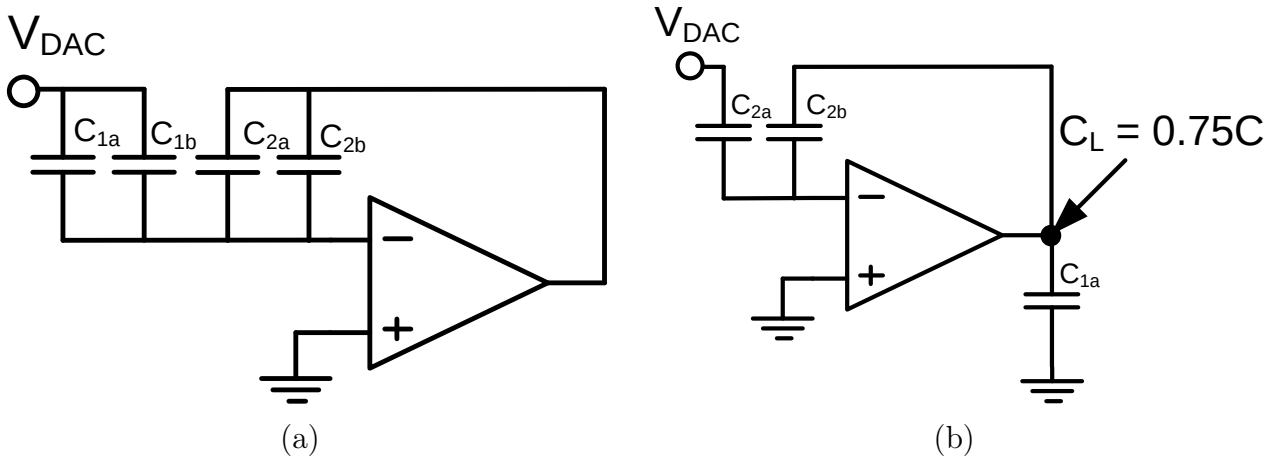


Figure 3.3: Improved 3-cap-shared technique: (a) 1^{st} evaluation phase and (b) 2^{nd} evaluation phase.

of more than 60% can be achieved, compared to that of the flip-around configuration and OTA-shared technique for the same SNR.

3.2.3 Power estimates

To estimate the power savings, it is assumed that OTA's power is proportional to the load capacitance (see (2.18)). Hence, the load capacitance reduction translates directly to the overall power reduction. These capacitor sharing techniques inherently utilize the flip-around configuration and OTA-shared technique. The energy efficiencies of these schemes are listed in Table 3.1 (an extended version of Table 2.3). It is obvious that the improved 3-cap-shared techniques can achieve more than an 85% power reduction compared to that of the conventional scheme.

3.2.4 Summary

A low power technique is proposed that improves the existing low power capacitor-shared technique. The proposed technique utilizes the capacitor-shared technique. In the existing techniques, the capacitor are shared for only the first cycle, whereas in the proposed technique, the capacitor sharing is extended to the next cycle reducing the overall power consumption. The main benefits of this approach are a low power, low area, and ease of design.

Table 3.1: Combining flip-around configuration and OTA-shared technique with capacitor-shared techniques for an N-bit ADC.

Technique	Utilizing flip-around configuration and OTA-shared		
	P_N	T_c	E
Capacitor-shared	0.375	0.5	0.188
2-cap-shared	0.2	1	0.2
3-cap-shared	0.3	0.5	0.15
Improved 3-cap-shared	0.18	0.5	0.135

3.3 Proposed Capacitor-Shared and Capacitor-Scaled Technique

As mentioned earlier in Section 2.3.1, one of the main power saving advantages of pipelined ADCs, over those of algorithmic ADCs, their ability to exploit the interstage capacitor scaling. Such scaling is due to the fact that the noise contributions from the later stages are reduced by the factor of the product of the interstage gains of the preceding stages, as given in (**??**) and is repeated here,

$$\overline{v}_{n,in}^2 \propto kT \left[\frac{1}{C_{s1}} + \frac{1}{2^{2M} C_{s2}} + \frac{1}{2^{4M} C_{s3}} + \cdots \right] \tag{3.1}$$

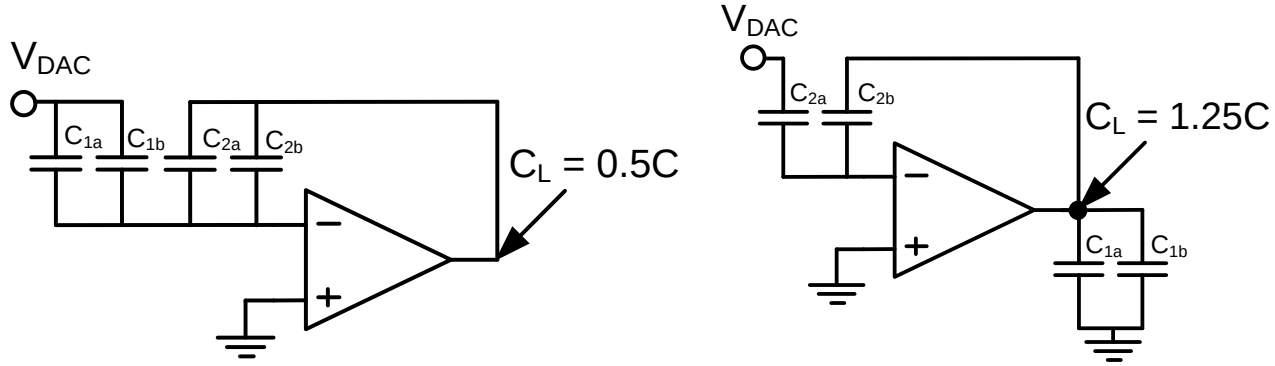
where C_{sI} is the sampling capacitor of the I^{th} stage and 2^M is the interstage gain. Therefore, in an optimal design, the capacitors at each stage is scaled down by the interstage gain [31].

Due to the cyclic nature of algorithmic ADCs, inter-cycle scaling is not possible for typical implementations of algorithmic ADCs. Furthermore, due to their inability to use inter-cycle scaling, algorithmic ADCs are unable to exploit the additional power saving advantages of the capacitor-shared technique, discussed in Section 2.4.3.

In the capacitor-shared technique, the first and second evaluation phases are repeated, as shown in Figure 3.4.It is evident that the OTA's load capacitance during the 1^{st} evaluation phase is 0.5C, whereas during 2^{nd} evaluation phase it is 1.25C. Consequently, the OTA is designed to drive the larger load capacitance of 1.25C, thereby wasting the OTA's power in the first evaluation phase. Therefore, to exploit the maximum advantage of capacitor-shared scheme, a technique utilizing the capacitor-scaled technique is proposed to significantly reduce the power consumption of the algorithmic ADCs.

In the capacitor-shared scheme discussed above, the load capacitance is reduced only for the first evaluation cycle. To extend the capacitor-shared technique to the later cycles, rather than dividing the capacitors into two equal sized capacitors, the sampling capacitors are divided into unit capacitors, C_u, where each $\mathrm{C}_u = \mathrm{C}_s/2^N$, as depicted in Figure 3.5. Here, C_s is the total sampling capacitor size, and N is the ADC resolution.

For example, a 4-bit example in Figure 3.6(a), conveys that the sampling capacitor is divided into eight equal sized unit capacitors. Initially, all the unit capacitors sample V_{in}, and the comparators determine the first bit. To evaluate the first residue, four of the unit capacitors are connected in feedback, and the remaining four capacitors are connected



(a) (b)

Figure 3.4: Capacitor-shared scheme: (a) 1st evaluation phase and (b) 2nd evaluation phase.

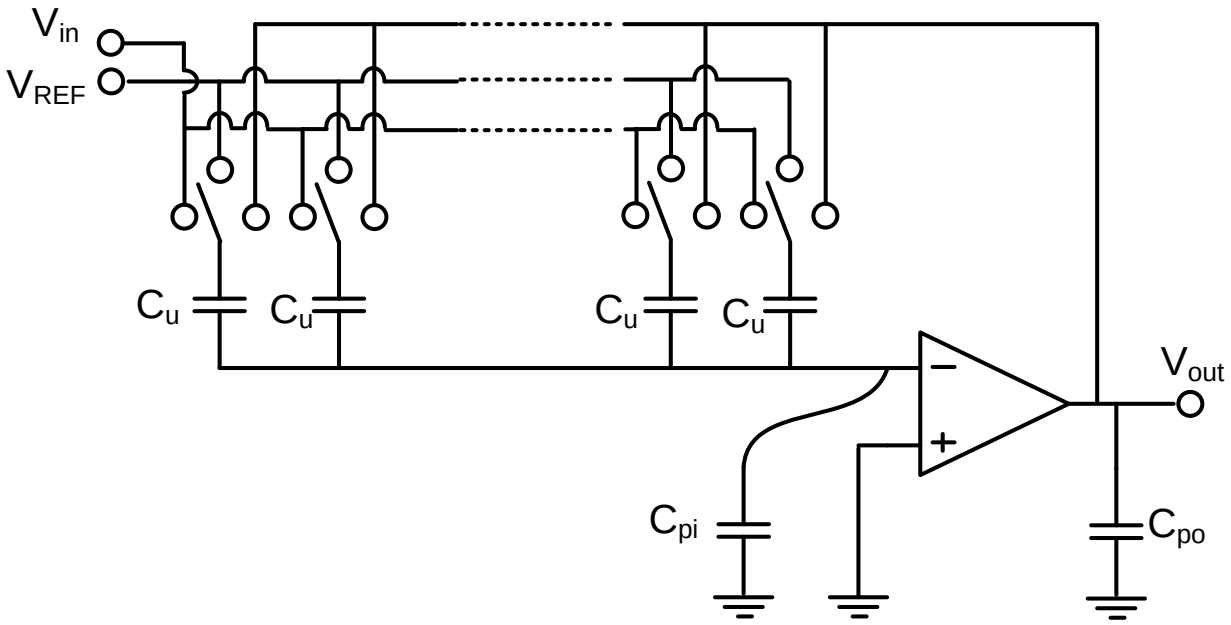


Figure 3.5: Conceptual capacitor-shared and capacitor-scaled algorithmic ADC.

to the appropriate reference voltage, V_{DAC}, as shown in Figure 3.6(b). The feedback capacitors now hold the next cycle's input signal. Since the capacitors, connected to V_{DAC}, are no longer required, they are disconnected from the OTA's sum node (dotted-line). Then, to evaluate the next residue, two of the feedback capacitors are connected to the appropriate DAC levels, and the other capacitors remain connected to the feedback as signified in Figure 3.6(c). The feedback capacitor is further subdivided for each successive bit conversion. Figure 3.6(d) depicts the last evaluation phase.

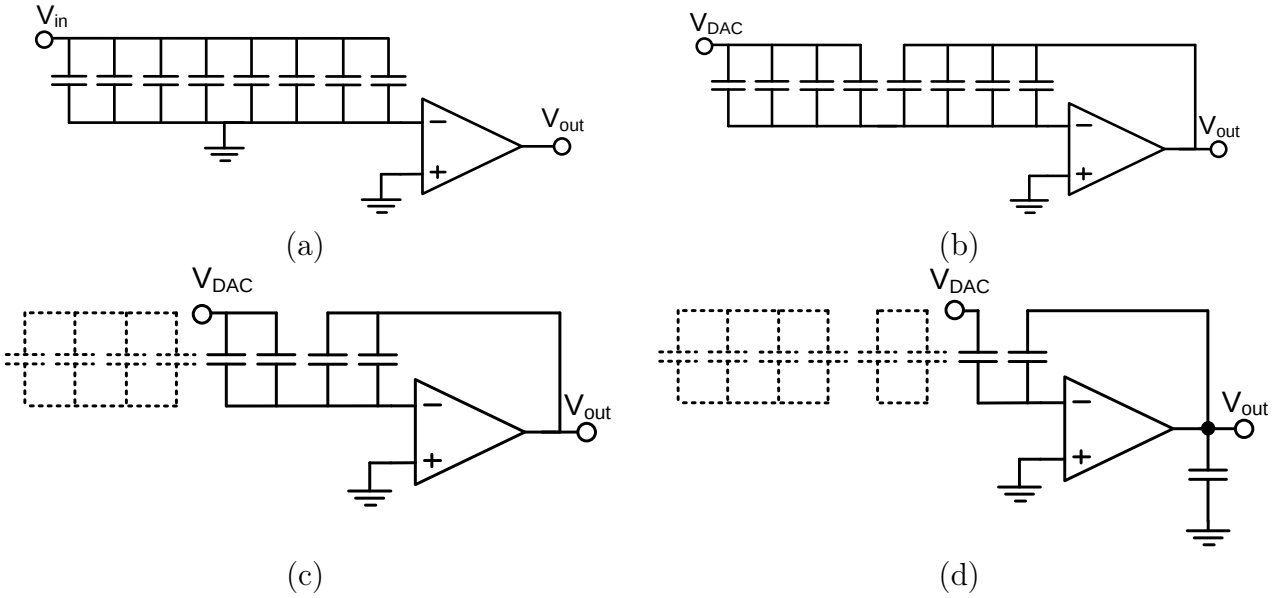


Figure 3.6: Capacitor-scaled scheme. The disconnected capacitors are shown in dotted lines: (a) sampling, (b) 1st evaluation phase, (c) 2nd evaluation phase, and (d) 3rd evaluation phase.

3.3.1 Practical considerations

In the proposed capacitor-shared and capacitor-scaled scheme, the load capacitance is reduced by 50% in each successive cycle. However, the OTA is designed for the larger load capacitance of the first evaluation phase. As shown in (2.29), to meet the settling time requirements, g_m must be scaled such that

$$g_m \propto C_{L,K} \tag{3.2}$$

where $C_{L,K}$ is the load capacitance during the K^{th} evaluation phase. Therefore, g_m is reduced by the same factor as the capacitors, to save power.

3.3.2 Bias current scaling

To reduce the OTA's power as the capacitive load is reduced, one technique might be to scale the OTA's bias current with the capacitive load [69]. Unfortunately, scaling the capacitive load without scaling the OTA's input and output parasitic capacitances,C_{pi} and C_{po}, degrades the feedback factor and reduces the circuit's bandwidth [73]. Referring to

Figure 3.7, the closed-loop bandwidth, which is the product of the feedback factor, β, and the unity-gain-bandwidth, f_T, of the OTA is given by

$$f_{3dB} = \beta \cdot f_T = \frac{1}{2\pi} \cdot \frac{C_u}{2C_u + C_{pi}} \cdot \frac{g_m}{C_L} \tag{3.3}$$

where g_m is the transconductance of the OTA and the load capacitance is expressed as

$$C_L = C_{po} + \frac{C_u (C_u + C_{pi})}{2C_u + C_{pi}} \tag{3.4}$$

Therefore, by rearranging (3.3), the bandwidth becomes

$$f_{3dB} = \frac{1}{2\pi} \cdot \frac{g_m}{2C_{po} + C_{pi} + C_u + \frac{C_{pi}C_{po}}{C_u}} \tag{3.5}$$

In order to maximize the closed-loop bandwidth, (3.5) is differentiated with respect to C_u, and equated to zero to obtain the optimum unit capacitance value,

$$C_u{}^* = \sqrt{C_{pi} \cdot C_{po}} \tag{3.6}$$

Therefore, the maximum bandwidth for the fixed C_{pi} and C_{po} is,

$$f^*_{3dB} = \frac{1}{2\pi} \cdot \frac{g_m}{2C_{po} + C_{pi} + 2\sqrt{C_{pi}C_{po}}} \tag{3.7}$$

This is the maximum bandwidth of a closed loop system for a fixed OTA size.

As portrayed in Figure 3.8, if the OTA is initially designed to operate at point A for the maximum speed, reducing the number of unit capacitors by 50%, reduces the bandwidth, primarily due to the degradation of the feedback factor.

During each cycle of data conversion, the OTA's settling time requirements are relaxed by a factor of $\frac{(N-K+1)}{(N-K)}$ as each bit is resolved (see (2.24)). Figure 3.9 compares the OTA's settling time requirements and the OTA's bandwidth, when the capacitors are scaled by 50% in each cycle. It is evident that while the OTA's settling requirements are reduced by a factor of (N-K+1)/(N-K), due to the reduced resolution requirements of the next cycle, the OTA's bandwidth reduces at a much faster rate after the first few cycles. Therefore, somewhat surprisingly, the OTA's bias must be increased for the later cycles to meet the settling time requirements. Consequently, scaling the OTA's bias current does not yield

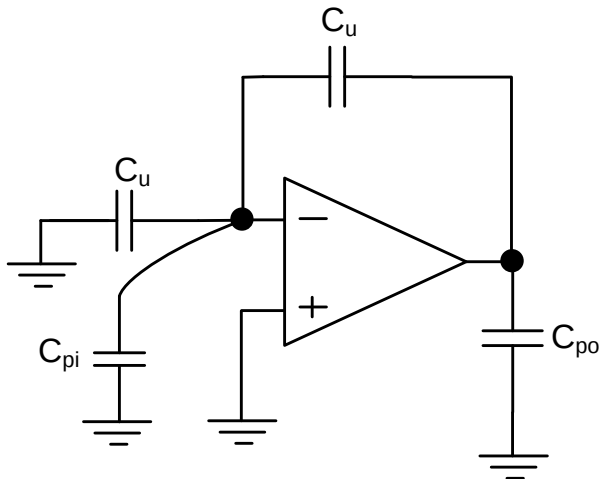


Figure 3.7: Evaluation phase of the U-MDAC stage.

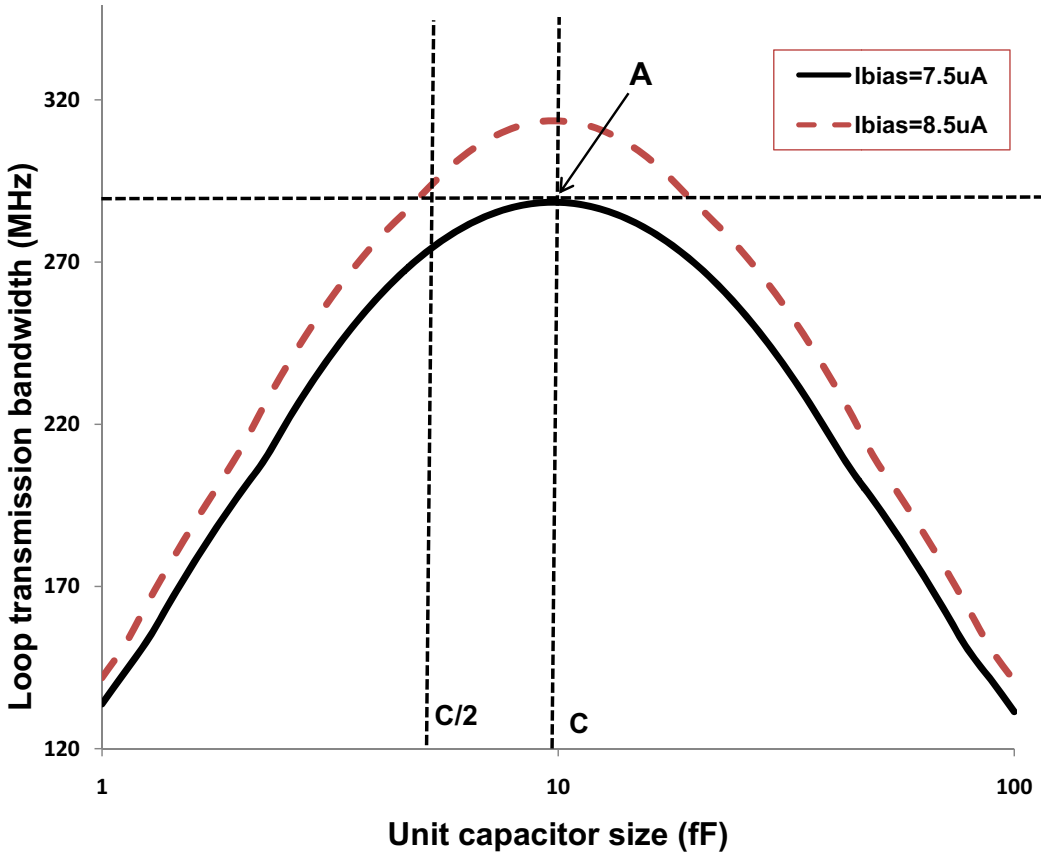


Figure 3.8: Bandwidth versus capacitive load for a cascode OTA in a 130-nm CMOS process with I_{bias}=7.5 μA (solid-line) and I_{bias}=8.5 μA (dashed-line).

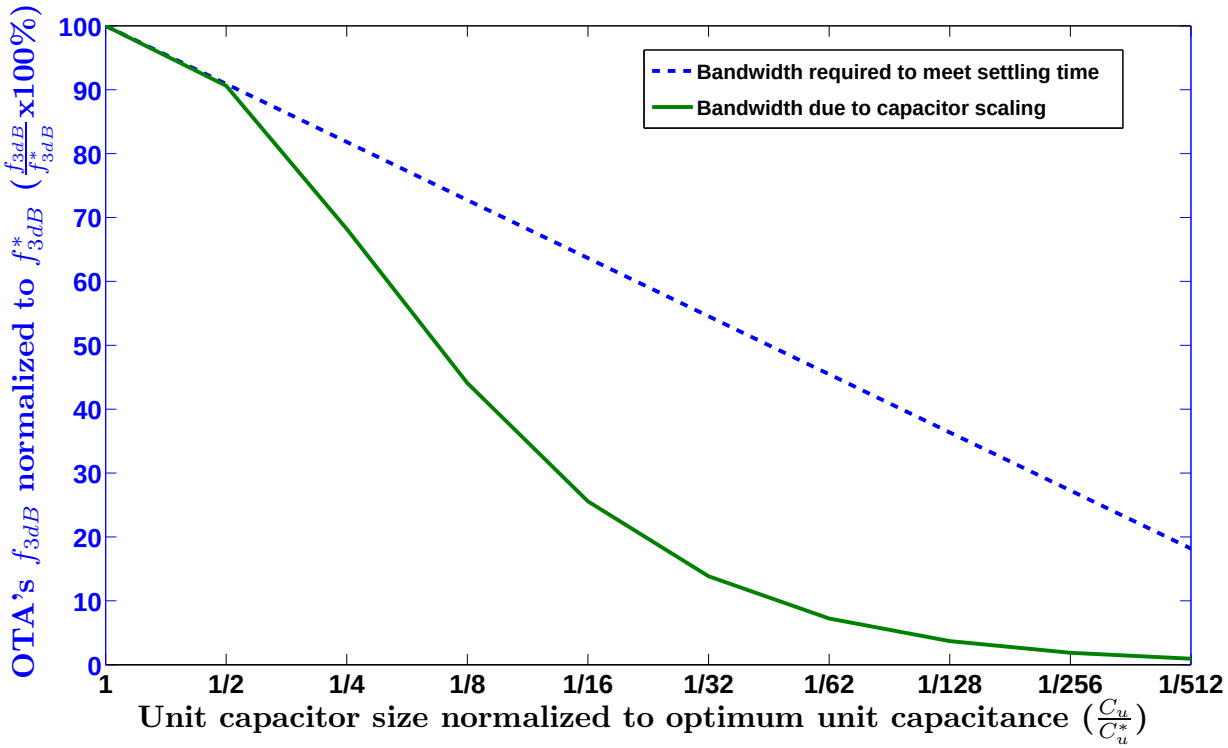


Figure 3.9: OTA's bandwidth normalized to the maximum bandwidth for N=10 versus unit capacitor size normalized to the optimum unit capacitance.

the expected power savings, when the OTA's fixed parasitic capacitors are considered.

3.3.3 Proposed approach: OTA's scaling

A better approach is to design the OTA as a number of unit-OTAs. Since the load capacitors are reduced by half during each cycle, half of the unit-OTAs are powered down and disconnected from the circuit to scale the parasitic capacitances with the load. Also, the unit-OTAs remain optimally biased. To realize the potential power savings, the circuit in Figure 3.6 is redesigned in Figure 3.10, by using a unit-multiplying digital-to-analog converter (U-MDAC) approach. Each U-MDAC consists of a unit-OTA, and its associated pair of unit capacitances.

If the OTA of Figure 3.5 has transistors widths of W, a bias current of I_b and a capacitor area of C, when the OTA is split into M unit-OTAs, each component (including the compensation and common-mode-feedback capacitors) of the OTA is scaled by the 1/M. Hence, each unit-OTA will have transistors width as W/M, a bias current of I_b/M, and capacitor area of C/M. Consequently, each unit-OTA exhibits the same gain and bandwidth as the original OTA, while consuming 1/M of the power and displaying an input referred noise that is $\sqrt{M}$ larger than that of the original OTA. Therefore, for some added wiring and layout complexity, M unit-OTAs in parallel will have the same component area, power dissipation, and input referred noise as the original OTA. Also, multiple unit-OTAs in parallel are commonly used in analog filters and mismatches among the unit-OTAs have not led to a notable degradation in the OTAs' performance [74].

To illustrate the operation, a 4-bit algorithmic ADC based on four U-MDACs and eight unit capacitors is used as an example. To perform a conversion, all eight unit capacitors first sample the input. Then, to evaluate the first residue, half of the unit capacitors are placed in the feedback, and the others are connected to the appropriate V_{REF} as shown in Figure 3.11(a). Once the residue is generated, the capacitors connected to the reference are disconnected from the sum node, in a manner similar to that used in Figure 3.6. To generate the second residue, half of the unit-OTAs are powered down and disconnected from the sum node (OTAs shown in dotted lines), and their associated feedback capacitors are connected to the appropriate V_{REF} as shown in Figure 3.11(b). For the last evaluation phase, the same procedure is repeated as shown in Figure 3.11(c). This capacitor-shared technique and OTA powering down procedure is repeated for each bit of resolution. By using this approach, the OTAs remain optimally biased (point A in Figure 3.8), and the power is reduced by 50% in each cycle.

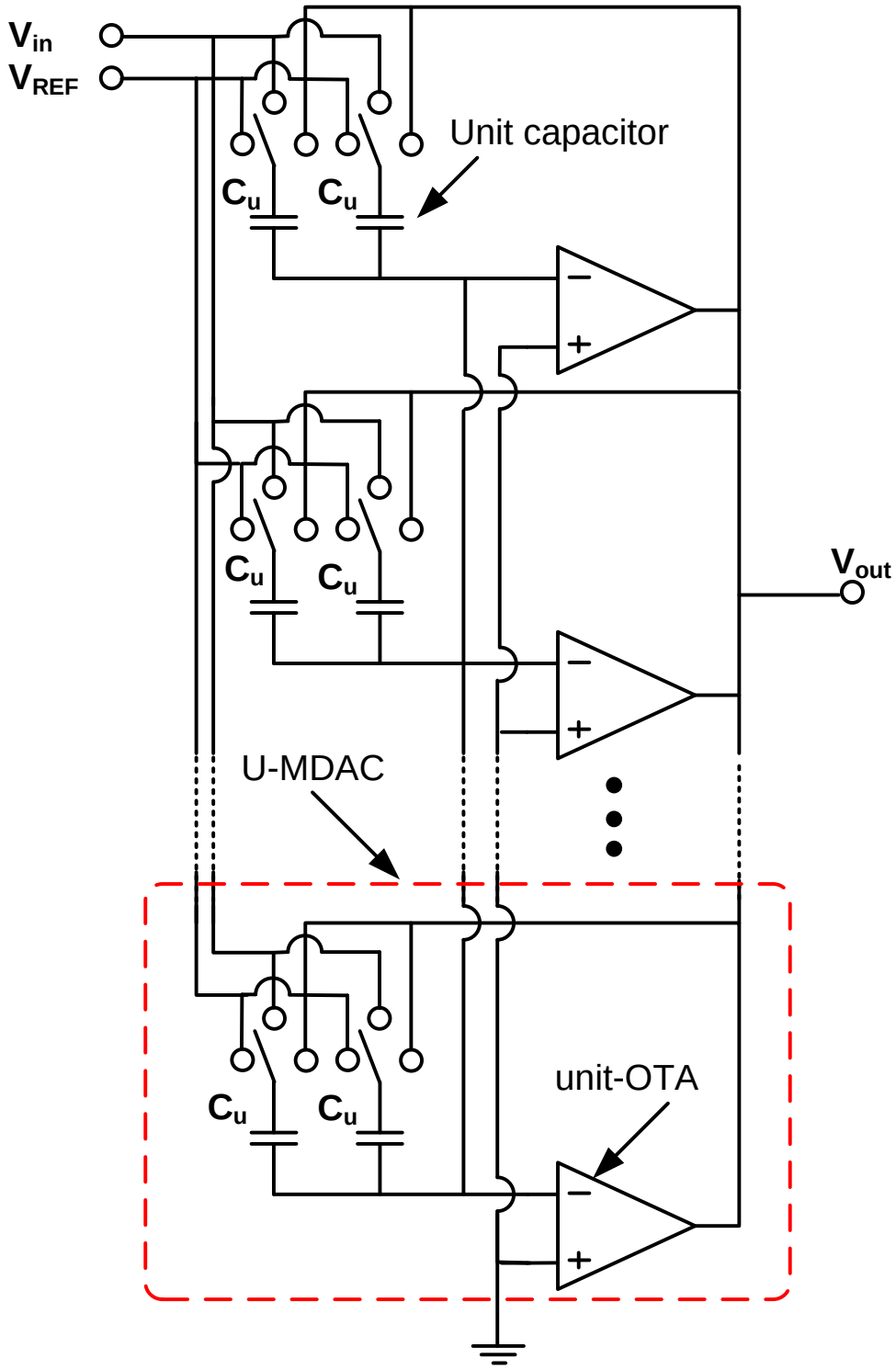


Figure 3.10: U-MDAC approach.

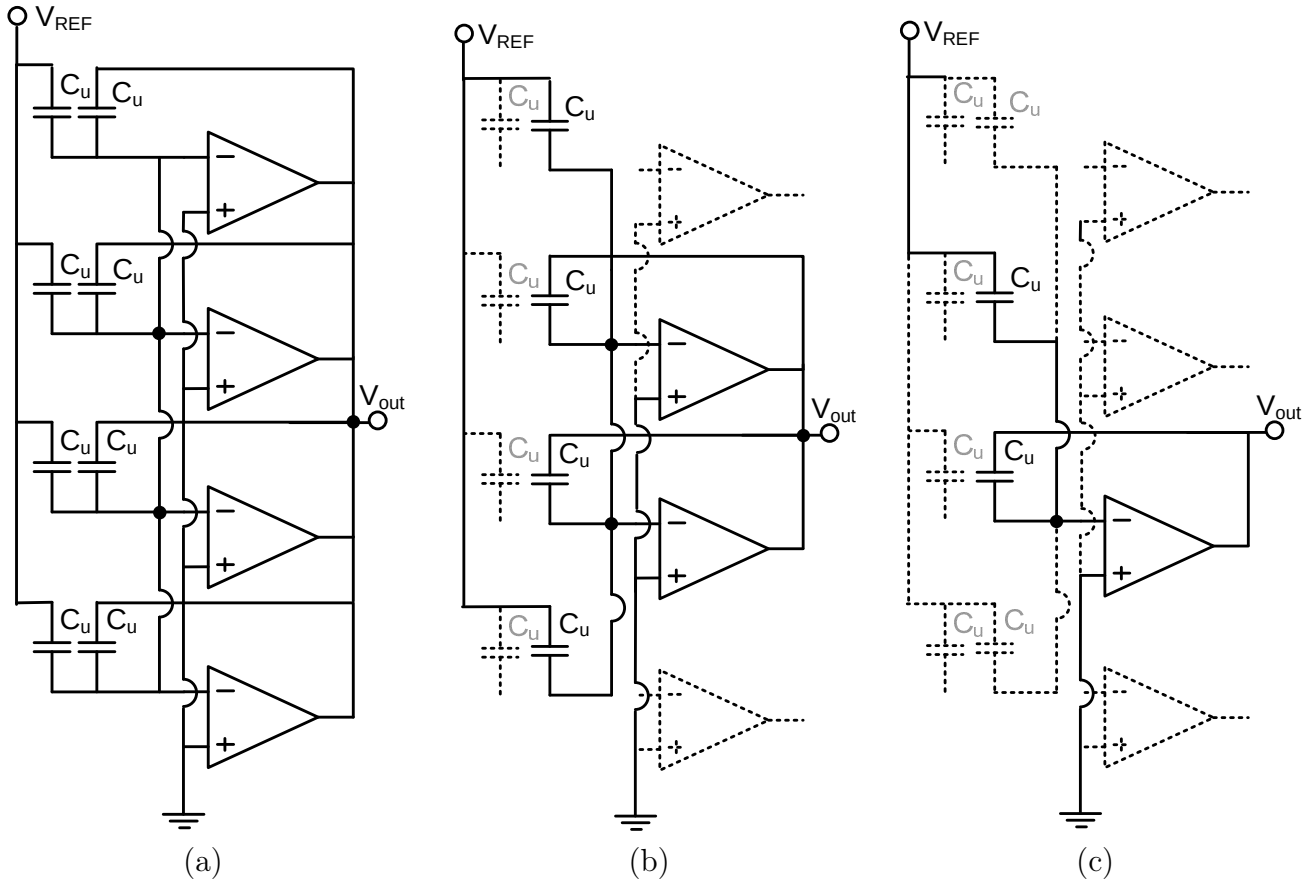


Figure 3.11: U-MDAC phases (the powered down OTA and disconnected wires are represented by the dotted lines): (a) 1st evaluation phase, (b) 2nd evaluation phase, and (c) 3rd evaluation phase.

3.3.3.1 Combined U-MDAC and the 3-caps-shared approach

In a given technology, there is a minimum size for each capacitor, C_{min}. Therefore, a pragmatic approach is to scale the capacitors for the first few cycles. After the cycles, when scaling is incorporated, a single U-MDAC can be used to generate the remaining bits. Because the first few cycles consume the most power, scaling the power, even only in the first few cycles, reduces the power consumption of the ADC substantially. An improvement is possible in the existing energy efficient U-MDAC-based design approach, by splitting the original ADC into two stages: a capacitor-scaled and capacitor-shared stage, and a 3-cap shared stage. Each stage generates N/2 bits in N/2 cycles, resulting in twice the sampling speed and a lower overall power consumption with a minimal increase in the die area.

These capacitor-scaled approaches inherently utilize the flip-around, OTA-shared and capacitor-shared techniques as shown in Table 3.2. It is evident that the combined U-MDAC and 3-cap-shared technique achieves more than a 90% power reduction from that of the conventional scheme.

Table 3.2: Combining the flip-around configuration and OTA-shared technique with the capacitor-scaled techniques for a 10-bit ADC.

Technique	Utilizing flip-around configuration and OTA-shared		
	P_N	T_c	E
U-MDAC	0.15	0.5	0.075
Scaling 4 cycles	0.188	0.5	0.094
U-MDAC + 3-cap-shared	0.175	0.5	0.088

3.3.4 Combining the proposed techniques with phase/bias scaling techniques

Since load reduction techniques are independent of the phase and bias current scaling techniques, phase and bias current scaling can be incorporated into the load reduction techniques to further enhance their energy efficiencies as listed in Table 3.3, for ideal scaling. By incorporating the phase scaling, the conversion time is reduced to 50%, compared to that of the OTA-shared scheme. Bias current scaling reduces the power consumption to 50% ideally. Table 3.3, which summarizes the results from Tables 3.1 and 3.2, illustrates that bias and non-uniform clocking achieve the same energy efficiencies (the last column of Table 3.3). Due to the added complexity of generating non-uniform clocks, the bias scaling appears to be the preferred solution for power savings. While the table illustrates the ideal scaling case, practical circuits, typically scale only for the first few cycles. In the case where scaling is applied for the first four cycles, the power consumption is increased by approximately 50%, compared to that of the ideal case.

From Table 3.3, it is seen that combining the different techniques leads to very energy efficient solutions. The U-MDAC approach, combined with a 3-cap-shared stage and bias/phase scaling, improves the energy efficiency of an algorithmic ADC by more than 90%, compared to the conventional implementation, and more than 70%, when compared to using the flip-around configuration and OTA-shared scheme.

Table 3.3: Comparing energy efficiencies of the different implementation techniques of a 10-bit algorithmic ADC when combined with phase/bias scaling techniques.

Technique	Utilizing flip-around configuration and OTA-shared				
	Phase scaling		Bias scaling		
	P_N	T_c	P_N	T_c	E
Capacitor-shared	0.25	0.25	0.125	0.5	0.094
2-cap-shared	0.2	0.5	0.1	1	0.15
3-cap-shared	0.3	0.25	0.15	0.5	0.075
Improved 3-cap-shared	0.18	0.25	0.09	0.5	0.067
U-MDAC	0.15	0.25	0.075	0.5	0.056
Scaling 4 cycles	0.188	0.25	0.094	0.5	0.07
U-MDAC+3-cap-shared	0.175	0.25	0.088	0.5	0.066

3.3.5 Estimated power savings in the presence of parasitic capacitance

To estimate the power consumption of the different algorithmic ADC configurations, it is assumed that the power dissipation of an ADC is dominated by the power consumption of the OTA. For a single pole OTA, its power consumption is proportional to its load capacitance and bandwidth. Also, by assuming the OTA is working at its optimal point, C_{pi} and C_{po} match the feedback capacitor, C, (see (3.6)). Table 3.4 presents the load capacitance of the flip-around configuration and OTA-shared technique, capacitor-shared technique, 3-cap-shared technique, and the U-MDAC technique in Figure 3.12.

In the U-MDAC approach, both the capacitors and parasitic capacitors are scaled when the unused OTAs are powered down. For a 12-bit ADC utilizing full scaling, the average load capacitance is given as

$$C_{L,avg} = \frac{C_{L1}}{12}\left[1 + \frac{1}{2} + \frac{1}{4} + \cdots \frac{1}{2^{11}}\right] = \frac{1.99}{12} C_{L1} \tag{3.8}$$

when $C_{L1} = 1.67C$ is the OTA's load capacitance during the first evaluation phase as shown in Figure 3.12(d), then

$$C_{L,avg} = 0.28C \tag{3.9}$$

It is well known that scaling the capacitors increases the input referred noise. Therefore,

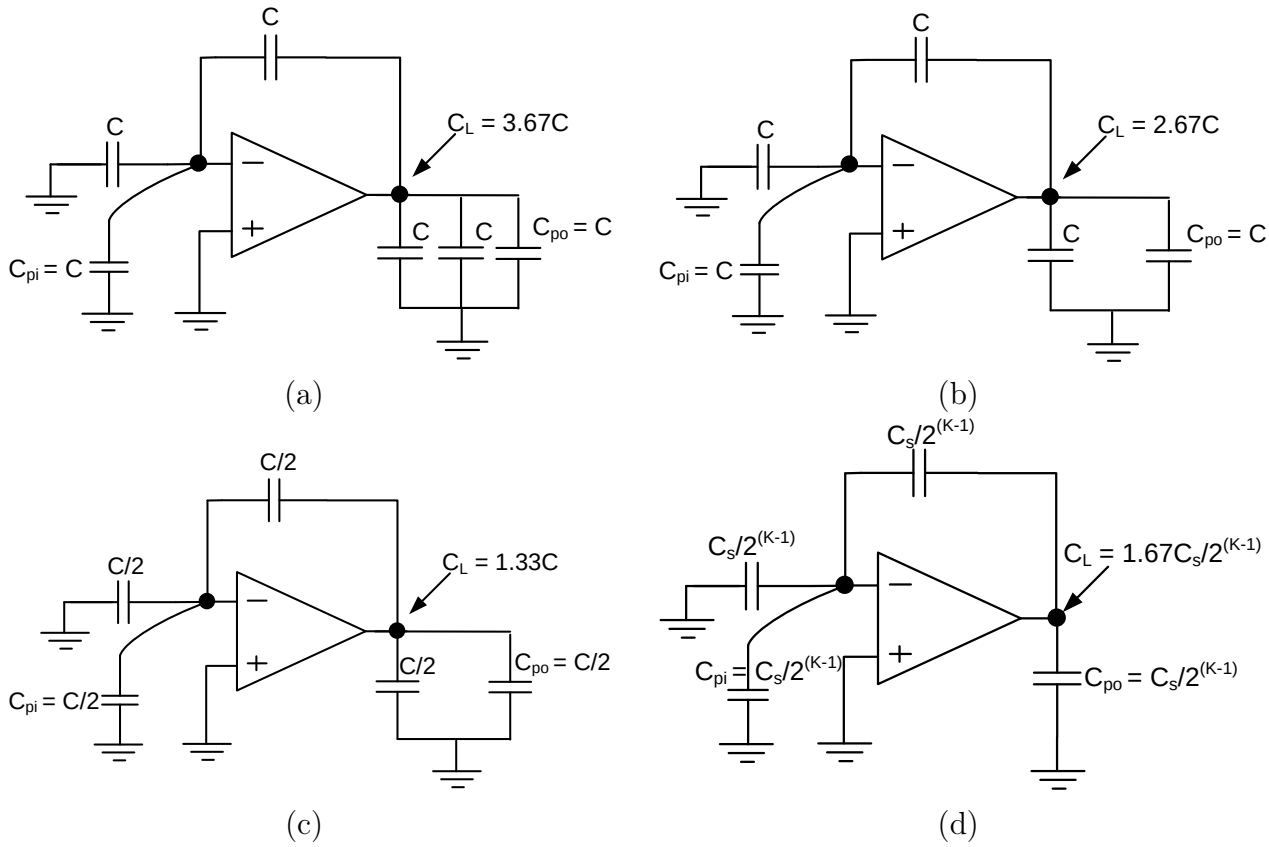


Figure 3.12: Load capacitance of different techniques: (a) flip-around and OTA-shared, (b) 3-cap-shared, (c) Improved 3-cap-shared, and (d) U-MDAC's during the K^{th} evaluation phase.

the sampling capacitor size must be increased by approximately 1.5 times to compensate for the increased noise. This increase in the load capacitance is incorporated into the total load capacitance making it 0.42C (c.f., (3.9)).

The power savings, with respect to the conventional algorithmic implementation and the flip-around configuration and OTA-shared scheme, is also reported in the table. It is evident that the proposed U-MDAC approach is highly power efficient, compared to other capacitor-shared configurations.

3.3.6 Summary

A low power technique utilizing both a capacitor-shared technique and a capacitor-scaled technique is proposed. The proposed technique splits the OTA into multiple unit-OTAs

Table 3.4: Power estimates in the presence of parasitic capacitance.

Circuit Configuration	C_L	% power reduction w.r.t conventional implementation	% power reduction w.r.t the flip-around configuration and OTA-shared
Flip-around & OTA-shared	3.67C	75	-
3-cap-shared	2.67C	82	27
Improved 3-cap-shared	1.66C	89	55
U-MDAC	0.42C	97	89

operating in parallel. This technique reduces the power consumption of a conventional algorithmic ADC implementation by more than 95%.

3.4 Thermal Noise Analysis

In an SC algorithmic ADC, thermal noise is a vital design parameter. It is required that the thermal noise is equal or preferably lower than the quantization noise level. In an algorithmic ADC, noise from the MDAC dominates, and that noise is generated by two sources: switches and an OTA. In this section, a simplified analysis of thermal noise is presented for a capacitor-shared and capacitor-scaled algorithmic ADC.

During the sampling phase, the sampling capacitor, C_s, samples not only the input signal but also the noise. By assuming the two capacitor of the value $C_s/2$, sample the noise, and the mean square noise is represented as as

$$\overline{v}_{n,s}^2 = \frac{kT}{C_s} \tag{3.10}$$

The circuit configuration during the evaluation phase is drawn in Figure 3.13. By assuming that a single stage OTA is used, the settling time of the MDAC is determined by the OTA's bandwidth. It means that the switches on-resistance, R_{on}, is much smaller than $1/g_m$, where g_m is the OTA's transconductance. Therefore, the circuit's noise bandwidth is determined by the OTA's closed loop bandwidth.

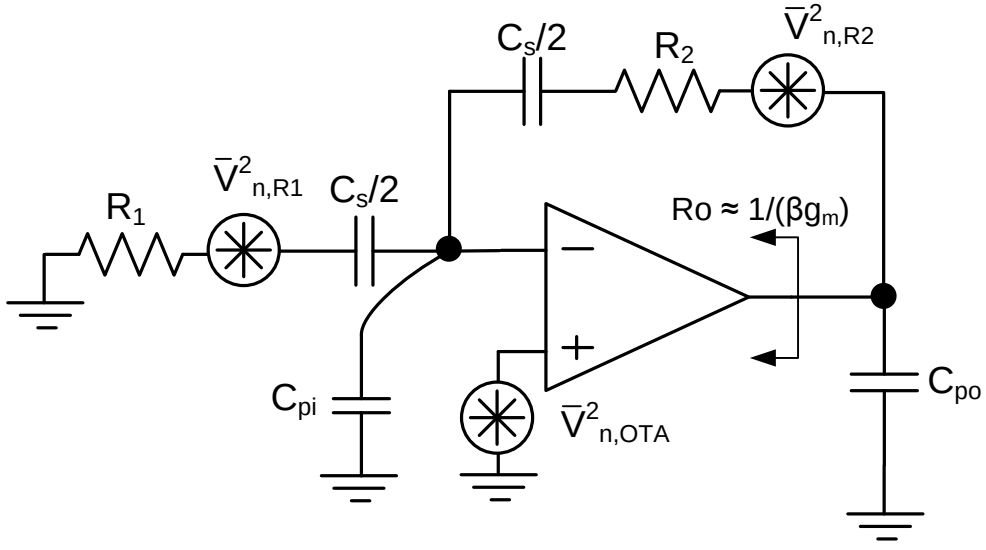


Figure 3.13: Noise analysis of the MDAC during the evaluation phase.

Assume the input and output parasitic capacitance is equal to the feedback capacitor, that is,

$$C_{pi} = C_{po} = \frac{C_s}{2} \tag{3.11}$$

for the first evaluation phase. Therefore, the load capacitance, C_L and feedback factor, β, becomes

$$C_L = \frac{5C_s}{6} \tag{3.12}$$

and

$$\beta = \frac{1}{3} \tag{3.13}$$

Also, the time constant, τ, is given as

$$\tau = \frac{C_L}{\beta \cdot g_m} \tag{3.14}$$

For the above circuit, noise from the switches and the OTA contribute to the overall noise. Since all the noise sources are independent of each other, superposition can be used to calculate their contributions to the output noise. The mean square noise is calculated by [48]

$$\overline{v}_{n,o}^2 = \int_o^\infty S_{n,i}(f) \cdot |H(f)|^2 df \tag{3.15}$$

or is simplified to

$$\overline{v}_{n,o}^2 = S_{n,i}(f) \cdot |H(0)|^2 \cdot BW_{noise} \tag{3.16}$$

where $S_{n,i}(f)$ is the power spectral density (PSD) of the noise source, $|H(0)|$ is the noise gain from the noise source to the output at DC, and BW_{noise} is the equivalent noise bandwidth.

The PSD of switches computed by using

$$S_{n,R1}(f) = S_{n,R1}(f) = 4kTR_{on}[V^2/Hz] \tag{3.17}$$

and the PSD of the OTA is given as [48]

$$S_{n,OTA}(f) = \frac{16kT}{3g_m}[V^2/Hz] \tag{3.18}$$

The noise gain of different noise sources to the output at DC is given as

$$|H_{R1}(0)| = \left|-\frac{C_s}{C_s}\right| = 1 \tag{3.19}$$

$$|H_{R2}(0)| = 1 \tag{3.20}$$

$$|H_{OTA}(0)| = \left|\frac{3C_s}{C_s}\right| = 3 = \frac{1}{\beta} \tag{3.21}$$

As already mentioned, $R_{on} \ll 1/g_m$, hence the equivalent noise bandwidth is given as

$$BW_{noise} = \frac{1}{4\tau} = \frac{\beta \cdot g_m}{4C_L} \tag{3.22}$$

Therefore, the total noise at the output at the end of the first evaluation phase is

$$\overline{v}^2_{no,1} = 2 \cdot \left(4kTR_{on} \cdot \frac{\beta \cdot g_m}{4C_L}\right) + \frac{16kT}{3g_m} \cdot \frac{1}{\beta^2} \cdot \frac{\beta \cdot g_m}{4C_L} \tag{3.23}$$

Since $R_{on} \cdot g_m \ll 1$, the noise due to the switches can be neglected. Therefore, the total output noise becomes

$$\overline{v}^2_{no,1} \approx \frac{24}{5} \cdot \frac{kT}{C_s} \tag{3.24}$$

where $C_L = 5C_s/6$. In the next evaluation phase, all the capacitors are scaled by a factor of two, including the parasitic capacitance. This arrangement will keep β constant. Moreover, the OTA, designed as a number of unit-OTAs, are scaled by half, reducing the overall g_m by a factor of two. Scaling g_m with the scaled capacitors with the same ratio keeps the noise bandwidth constant (see (3.22)). There are two noise contributors to the output, $\overline{v}^2_{no,2}$: noise from the previous cycle, and noise from the OTA.

Since the stage's time constant is much smaller than the settling time of the stage, the charge from the previous cycle disappears at the end of this evaluation phase. Therefore, only the OTA's noise will contribute to the overall noise. The OTA's noise doubles in every cycle, because of the reduction in the g_m without the reduction in the noise bandwidth of the circuit. As a result, noise power at the end of second evaluation phase is

$$\overline{v}^2_{no,2} \approx \frac{48}{5} \cdot \frac{kT}{C_s} \tag{3.25}$$

The noise increases in each cycle during the whole conversion process and can be written

as

$$\overline{v}_{no,K}^2 \approx 2^{(K-1)} \cdot \frac{12}{5} \cdot \frac{kT}{C_s} \tag{3.26}$$

where K is the current evaluation phase.

Therefore, the total noise contribution through the whole conversion is determined by summing the input referred noise of each cycle and is given as

$$\begin{aligned}
\overline{v}_{n,in}^2 &= \frac{kT}{C_s} + \frac{24}{5} \cdot \frac{kT}{C_s} \left[\frac{1}{2^2} + \frac{1}{4^2} \cdot 2 + \frac{1}{8^2} \cdot 4 + \cdots + \frac{1}{(2K)^2} \cdot 2^{(K-1)} \right] \\
&= \frac{17}{5} \cdot \frac{kT}{C_s} \\
&\approx 3.5 \cdot \frac{kT}{C_s} \\
&= n_f \cdot \frac{kT}{C_s}
\end{aligned} \tag{3.27}$$

where n_f is the noise factor. The value of n_f depends on the capacitor scaling ratio, circuit configurations, and the OTA's topology. This is the total integrated noise at the input of capacitor-shared and capacitor-scaled algorithmic ADC.

3.5 Low Power Limit of OTA-Based Capacitor-Shared and Capacitor-Scaled Algorithmic ADC

In this section, a low power limit of OTA-based capacitor shared and capacitor scaled algorithmic ADC is presented. The low power limit is set by the settling time constraints of the OTA. The settling time requirements depend on the load capacitance, and the load capacitance is proportional to the sampling capacitor sizes. The size of the sampling capacitors is dictated by the accuracy requirements of the ADC. The goal of this exercise is to develop a relationship between the power dissipation and the resolution of the proposed capacitor-shared and capacitor-scaled algorithmic ADCs.

For an N-bit algorithmic ADC, the quantization noise is [43]

$$\overline{v_{qn}^2} = \frac{V_{FS}^2}{2^{2N} \cdot 12} \tag{3.28}$$

where V_{FS} is the ADC's signal swing and N is the ADC resolution. For an ADC to take

advantage of the given resolution, the input referred thermal noise must be equal to (or probably greater than) the quantization noise of the ADC[1]. Assuming the input referred thermal noise is

$$\overline{v_{th}^2} = n_f \cdot \frac{kT}{C_s} \tag{3.29}$$

where C_s is the input sampling capacitor and n_f incorporates the noise from the OTA and noise increase due to capacitor scaling. According to (3.27), $n_f = 3.5$. Therefore, by equating (3.28) and (3.29)

$$\begin{aligned} \overline{v}_{th}^2 &= \overline{v}_{quan}^2 \\ \Rightarrow n_f \frac{kT}{C_s} &= \frac{V_{FS}^2}{2^{2N} \cdot 12} \\ \Rightarrow C_s &= \frac{12kT \cdot n_f \cdot 2^{2N}}{V_{FS}^2} \end{aligned} \tag{3.30}$$

This is the minimum capacitor size required for the ADC's SNR to be acceptable at the N-bit level.

To estimate the low power limit of a capacitor-shared and capacitor-scaled algorithmic ADC, it is assumed that the power dissipation of an ADC is dominated by the power consumption of an OTA [75, 76]. Assuming a single pole OTA, from (2.18), OTA's g_m is given as

$$g_{\mathrm{m}} = \frac{(\mathrm{N\text{-}K{+}1}) \cdot \ln 2 \cdot C_{\mathrm{L,K}}}{\beta \cdot T_{\mathrm{set}}} \tag{3.31}$$

By rearranging,

$$(g_m/I_D) \cdot I_D = \frac{(\mathrm{N\text{-}K{+}1}) \cdot \ln 2 \cdot C_{\mathrm{L,K}}}{\beta \cdot T_{\mathrm{set}}} \tag{3.32}$$

This g_{m} yields the minimum supply current I_{D} as,

$$I_{\mathrm{D}} = \frac{(\mathrm{N\text{-}K{+}1}) \cdot \ln 2 \cdot C_{\mathrm{L,K}}}{\beta \cdot T_{\mathrm{set}} \cdot (g_m/I_D)} \tag{3.33}$$

Since an algorithmic ADC takes N clock phases for one data conversion, the settling time is given as

$$T_{\mathrm{set}} = \frac{1}{N \cdot f_s} \tag{3.34}$$

[1] A lower thermal noise compared to the quantization noise is very costly in terms of power consumption, whereas, a higher thermal noise sets the lower limit of the overall signal-to-noise ratio (SNR). In practical ADCs, the difference between the stated bit and effective number of bits (ENOB) is 1.43 [72]

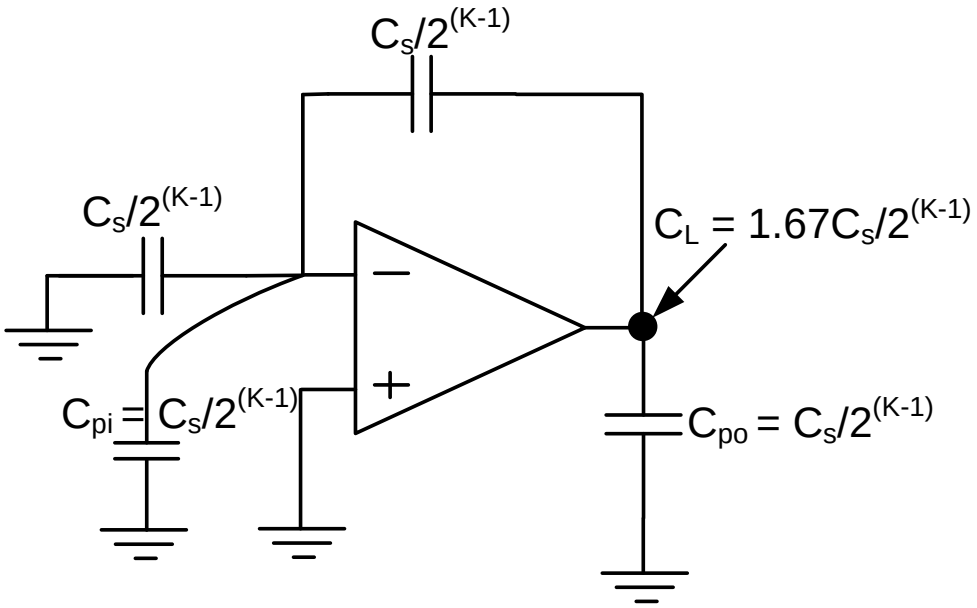


Figure 3.14: K^{th} evaluation phase of the U-MDAC stage.

Consequently, the power consumption of the cycle, while resolving the K^{th} bit is given as

$$P_K = \frac{N \cdot (N\text{-}K\text{+}1) \cdot \ln 2 \cdot C_{L,K} \cdot f_s \cdot V_{DD}}{\beta \cdot (g_m/I_D)} \tag{3.35}$$

Therefore, the OTA's power consumption is proportional to its load capacitance, ADC resolution squared, sampling speed, supply voltage, and biasing conditions.

The K^{th} evaluation phase of the U-MDAC stage is reflected in Figure 3.14. Assuming the input parasitic, C_{pi}, and output parasitic, C_{po} capacitors are equal to C_s. C_s is the sampling capacitor size which is dictated by the kT/C noise. It is a well known that capacitor scaling increases the input referred noise [31]. Therefore, to incorporate the 50% scaling, the sampling capacitor sizes must be increased by $\sqrt{2}$. The sampling capacitor size, given in (3.30), by taking the scaling factor into account, is expressed as

$$C_s = \frac{12\sqrt{2} \cdot n_f \cdot kT \cdot 2^{2N}}{V_{FS}^2} \tag{3.36}$$

Therefore, with

$$C_{L,K} = \frac{5C_s}{3} \cdot \frac{1}{2^{K-1}} \tag{3.37}$$

where the factor, $\frac{1}{2^{K-1}}$, is due to the scaling of capacitors, the load capacitance during the

evaluation of the Kth-bit is

$$C_{\mathrm{L,K}} = \frac{20\sqrt{2} \cdot n_f \cdot \mathrm{kT} \cdot 2^{2\mathrm{N}}}{2^{(\mathrm{K\text{-}1})} \cdot V_{\mathrm{FS}}^2} \tag{3.38}$$

Therefore, if $\beta = 1/3$, (3.35) becomes

$$\mathrm{P_K} = \frac{60\sqrt{2} \cdot n_f \cdot \mathrm{kT} \cdot \ln 2 \cdot \mathrm{N} \cdot (\mathrm{N\text{-}K{+}1}) \cdot 2^{2\mathrm{N\text{-}K{+}1}} \cdot f_s \cdot V_{\mathrm{DD}}}{V_{\mathrm{FS}}^2 \cdot (g_m/I_D)} \tag{3.39}$$

This is the total power of the algorithmic stage during each Kth cycle. As a result, the total power consumption of a capacitor scaled algorithmic ADC is

$$\mathrm{P_{ADC}} = \frac{1}{N} \cdot \sum_{\mathrm{K}=1}^{\mathrm{N}} \mathrm{P_K} \tag{3.40}$$

This is the theoretical limit on the power consumption of an OTA-based capacitor-shared and capacitor-scaled algorithmic ADC. It is noteworthy that this power dissipation bound is valid only for the circuits that require complete settling and are not dependant on static errors, caused by OTA's gain and capacitor matching requirements. Although the OTA's gain and mismatch requirements increases the power dissipation of the OTA, however meeting gain and mismatch requirements are not fundamentally necessary, because the accuracy can be compensated by the digital calibration [52, 53, 66].

3.6 Design Procedure of U-MDAC Algorithmic ADCs

A generic design procedure for U-MDAC-based algorithmic ADCs is introduced here. The goal of this design procedure is to provide a step-by-step procedure to determine the circuit parameters such as transistors widths and lengths and bias currents, for the given ADC's resolution and sampling frequency. The design procedure employs the foundry provided device models, while making use of transconductance-current-ratio (g_m/I_D)-based methodology and optimizes for power consumption.

The design procedure is as follows:

- Determine the number of cycles and unit capacitor (C_u) size from the thermal noise requirements and minimum capacitor size for a given technology.
- Based on the optimal bandwidth condition, input transistor sizes are determined by using the devices' extracted parameters.
- Based on the settling time requirements, the bias current, and hence, power dissipation of a U-MDAC is calculated. This closed form power equation depends on the circuit parameters and biasing conditions.
- Power consumption of the entire ADC is determined.

Step 1: Determining the number of scaling cycles and unit capacitor size

The design of a U-MDAC-based algorithmic ADC requires that the capacitors are scaled in successive cycles. For the ideal case, when the capacitors are scaled down till the last conversion cycle, C_s can be divided into 2^N C_us. Therefore, in case C_s is scaled for N-cycles, C_u is written as

$$\begin{aligned} C_{u,\mathrm{N-cycles}} &= \frac{C_s}{2^N} \\ &= \frac{12kT \cdot n_f \; 2^N}{V_{FS}^2} \end{aligned} \tag{3.41}$$

In practical ADCs, C_s is scaled for the first few cycles. Therefore, in the case where C_s is scaled for four cycles, C_u is given as

$$\begin{aligned} C_{u,4-\text{cycles}} &= \frac{C_s}{2^4} \\ &= \frac{12kT \cdot n_f \ 2^{(2N-4)}}{V_{FS}^2} \end{aligned} \tag{3.42}$$

Table 3.5 presents C_s, $C_{u,\text{N}-\text{cycles}}$ and $C_{u,4-\text{cycles}}$ for the different values of N with $n_f = 6$. It can be seen that for the case when full scaling is employed, C_u has very small values, and hence, impractical to implement. Also, for the case of the fixed number of scaling, the size of C_u can lead to power inefficient solutions.

Table 3.5: Unit capacitor size for full scaling and scaling the first four cycles when $n_f = 6$ and $V_{FS} = 1.5$ V.

N [bits]	$C_s[pF]$	$C_{u,\text{N}-\text{cycles}}$ [fF]	$C_{u,4-\text{cycles}}$ [fF]
8	0.009	0.003	0.54
10	0.139	0.135	8.68
12	2.221	0.542	138.9
14	35.562	2.171	2222.6
16	569	8.682	35562.3

In a given technology, there is a minimum size for each capacitor, C_{min}. Therefore, a pragmatic approach is to divide C_s by $2C_{min}$, and determine the maximum number of cycles, J, as

$$J = \frac{\ln\left(C_s/2C_{min}\right)}{\ln 2} \tag{3.43}$$

and hence C_u, can be estimated by using

$$C_u = \frac{C_s}{2^{J_{\text{int}}+1}} \tag{3.44}$$

where J_{int} is equal to J rounded to the nearest integer such that $J_{\text{int}} \leq J$. J_{int} and C_u for different ADC resolutions, are listed in Table 3.6. For a 12-bit ADC with C_{min} as 60 fF, J_{int} is estimated to be 4 and C_u as 69.5 fF. Therefore, the ADC resolution, N, and the minimum capacitor size for a given technology, C_{min}, set the number of scaled cycles, J_{int}, and unit capacitor size, C_u.

Table 3.6: Unit capacitor size for the optimal number of cycles ($n_f = 6$).

N [bits]	$C_s[pF]$	J_{int}	C_u for scaling M_{int}-cycles[fF]
8	0.009	-	-
10	0.139	-	-
12	2.221	4	69.5
14	35.562	8	69.5
16	569	12	69.5

Step 2: Determining the input transistor sizes

The unit-OTA, along with the associated C_u, during the evaluation phase is shown in Figure 3.15, where C_{pi} and C_{pi} are the input and output parasitics capacitance of the OTA, respectively.

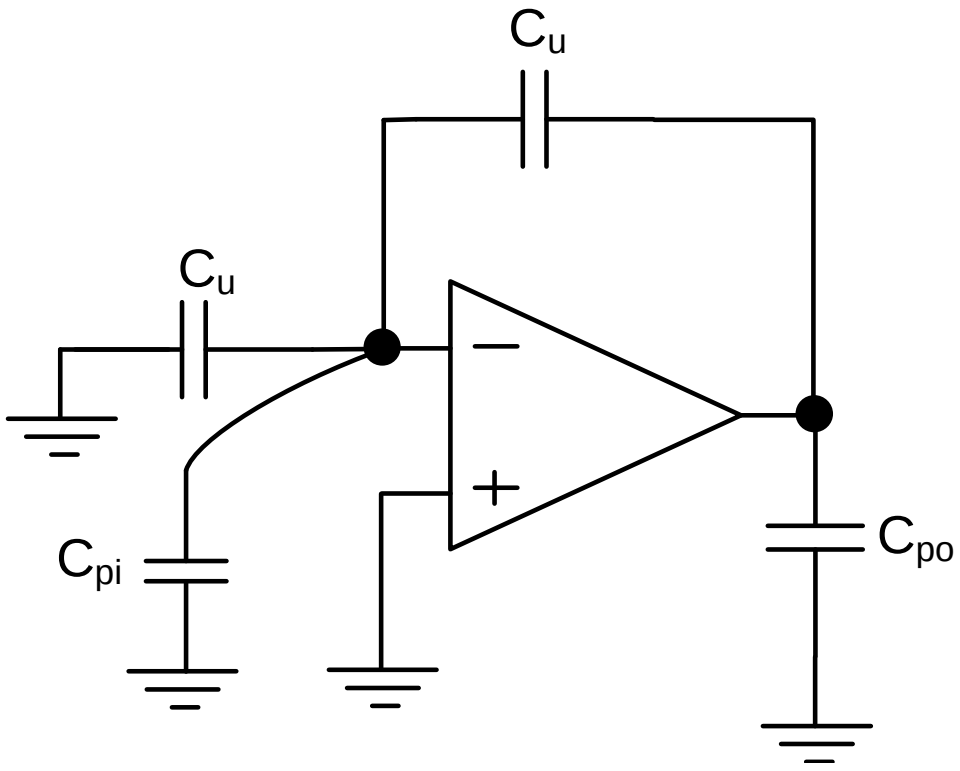


Figure 3.15: MDAC during the evaluation phase.

The output capacitance, C_{po}, is the sum of the drain capacitance of the transistors and

capacitance due to the SC common mode feedback (CMFB) circuit, that is,

$$C_{po} = C_{dd} + C_{CMFB} \tag{3.45}$$

where C_{dd} is the parasitic drain capacitance and C_{CMFB} is the capacitors used in the CMFB circuit. It is assumed that $C_{CMFB} = C_u/\zeta$, where ζ is the ratio of unit capacitor to the CMFB capacitor, and $C_{dd} = C_{pi}/\alpha$, where α can be extracted from the device's characteristics.

It can be seen from (3.7), the maximum bandwidth is the function of input and output parasitic capacitance. And from (3.6), the input and output parasitic capacitance depends on C_u. Hence, (3.6) becomes

$$C_u = \sqrt{C_{pi} \cdot \frac{C_{pi}}{\alpha} + C_{pi} \cdot \frac{C_u}{\zeta}} \tag{3.46}$$

By solving for C_{pi},

$$C_{pi} = -\frac{\alpha}{\zeta} \cdot \frac{C_u}{2} + \sqrt{\frac{\alpha^2 {C_u}^2}{4\zeta^2} + \alpha {C_u}^2} \tag{3.47}$$

The ratio, $\frac{C_{pi}}{C_u}$, is plotted in relation to $\frac{C_{pi}}{C_{dd}}$ for the different values of $\zeta = \frac{C_u}{C_{CMFB}}$ in Figure 3.16 The factor, $\alpha(= \frac{C_{pi}}{C_{dd}})$, is extracted from device's characteristics simulation for the different lengths. For a 130-nm CMOS process, α is plotted for different device's lengths as depicted in Figure 3.17. Since C_{pi} is proportional to the width, W, of the input transistors, W can be determined, providing the desired input and output parasitic capacitances.

Consequently, the input transistors' widths are determined by taking into consideration the size of C_u. Since $g_m \propto C_{pi}$, therefore, the design strategy should minimize the C_{CMFB} and maximize the input parasitic capacitance.

Step 3: Determining the bias current

The required OTA's closed loop bandwidth during the K^{th} evaluation phase, given in (2.18), and is repeated here for convenience such that

$$f_{3dB} = N(N - K + 1) \cdot \ln(2) \cdot f_s \tag{3.48}$$

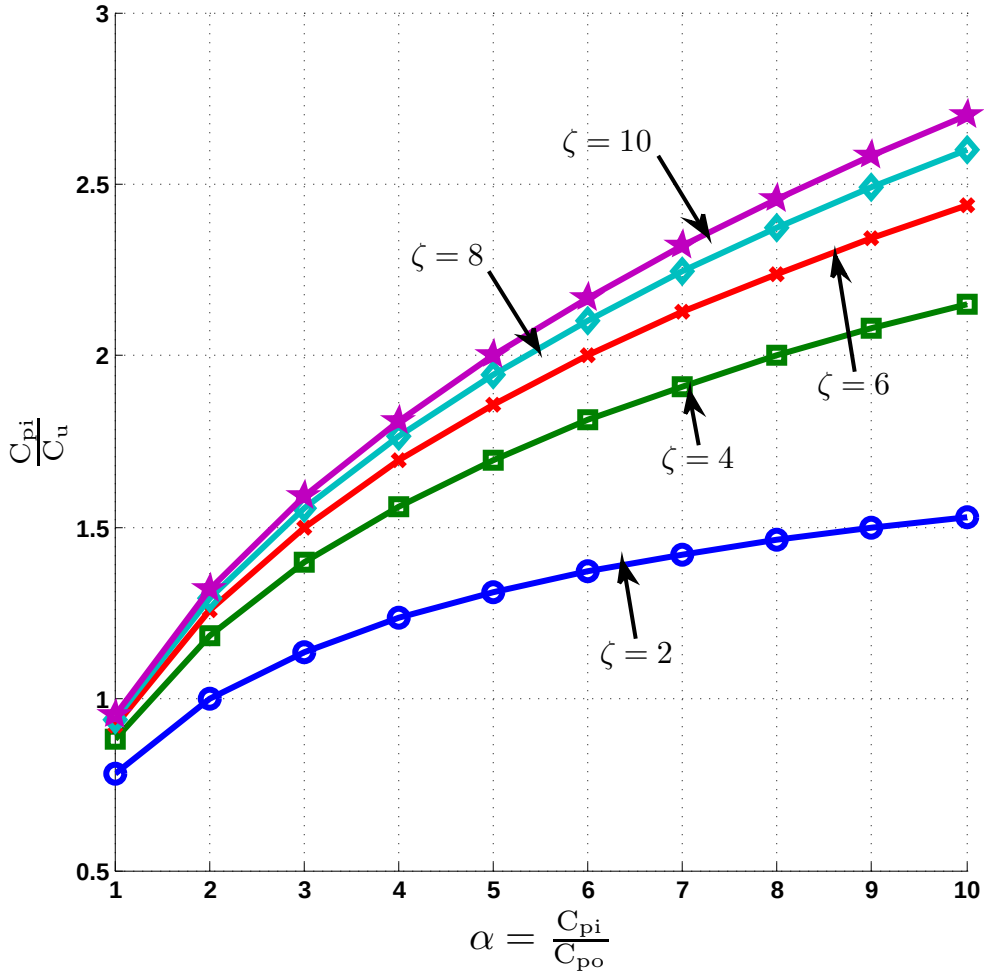


Figure 3.16: $\frac{C_{pi}}{C_u}$ versus $\frac{C_{pi}}{C_{dd}}$ for the different values of $\zeta = \frac{C_u}{C_{CMFB}}$

This required bandwidth must be equal to the maximum bandwidth given in (3.7). Consequently,

$$\begin{aligned}
\frac{g_m}{2C_{po} + C_{pi} + 2\sqrt{C_{pi}C_{po}}} &= N(N-K+1)\cdot \ln 2 \cdot f_s \\
\implies g_m &= N(N-K+1)\cdot \ln 2 \cdot f_s \cdot \left(2C_{po} + C_{pi} + 2\sqrt{C_{pi}C_{po}}\right) \\
&= N(N-K+1)\cdot \ln 2 \cdot f_s \cdot \chi \qquad (3.49)
\end{aligned}$$

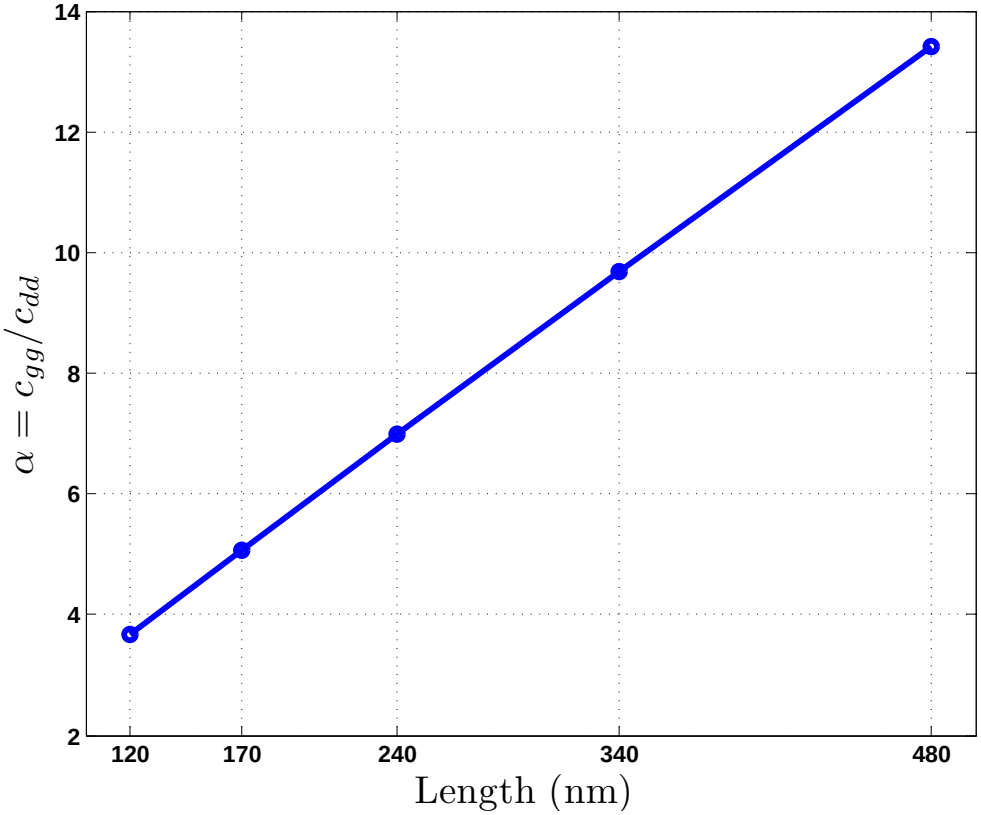


Figure 3.17: α versus different NMOS's lengths for a 130-nm CMOS process.

where $\chi = \left(2\mathrm{C_{po}} + \mathrm{C_{pi}} + 2\sqrt{\mathrm{C_{pi}C_{po}}}\right)$. By rearranging (3.49), the required bias current is dependant on the operating region or transconductance-current-ratio, g_m/I_D, written as

$$\begin{aligned} \left(\frac{\mathrm{g_m}}{I_D}\right) \cdot I_D &= N(N-K+1) \cdot \ln 2 \cdot f_s \cdot \chi \\ \Longrightarrow I_D &= \frac{N(N-K+1) \cdot \ln 2 \cdot f_s \cdot \chi}{(g_m/I_D)} \end{aligned} \tag{3.50}$$

Therefore, the power consumption of each U-MDAC stage is determined by using

$$P_{UMDAC} = I_D V_{DD} = \frac{N(N-K+1) \cdot \ln 2 \cdot f_s \cdot \chi \cdot V_{DD}}{(g_m/I_D)} \tag{3.51}$$

Consequently, the power consumption of the U-MDAC as given in (3.51) depends on the device parasitic capacitance and the bias conditions. The choice of g_m/I_D is based on the operating region and the device's intrinsic unity gain bandwidth. For N=12, f_s=10 MS/s, V_{DD}=1.5 V, χ = 400 fF, and (g_m/I_D) = 20, the power consumption of an U-MDAC is

equal to 20 μW.

In a cascode OTA, the non-dominant pole is usually about $f_{nd} = f_T/5$, where f_T is the intrinsic unity gain frequency of the transistor. Also, for the optimum settling, a phase margin of about 70^0 is required [77]. This sets the f_t of the OTA to approximately $f_{nd}/3$. Thus, an OTA with f_t requirements of 1 GHz, requires that the f_T of the input transistors be more than 15 GHz. Therefore, for a single stage OTA, the largest value of g_m/I_D should be chosen such that f_T is about 15-30 times more that the required f_t of the OTA. For a two-stage OTA, the largest value of g_m/I_D should be chosen such that f_T is about 50-80 times more that the required f_t of the 2-stage OTA [78].

Step 4: Determining the power consumption of the whole ADC

In the proposed design, an algorithmic ADC is split into a number of U-MDACs. These U-MDACs are successively scaled down by half for the number of cycles, J, whose value is given by (3.43). Since the number of scaled cycles is less than or equal to the total number of cycles to perform the complete conversion, the last U-MDAC stage can be used in the rest of the cycles to complete the data conversion. Therefore, the total power of the ADC is given as

$$P_{ADC} = \frac{1}{N} \cdot \left[\sum_{i=1}^{J+1} 2^{(J-i+1)} \cdot P_{UMDAC} + \sum_{l=J+2}^{N-1} P_{UMDAC} \right] \tag{3.52}$$

The first term integrates the power consumed in each scaled cycle, and the second term sums up the power during the cycles when only one U-MDAC is used to generate the remaining bits.

For an ADC resolution of 12-bits and the number of scaled cycles J=4, the power consumption of a capacitor shared and capacitor scaled ADC is about $3 \times P_{UMDAC}$.

This is the total power consumption of an U-MDAC-based algorithmic ADC. It is noteworthy that this power dissipation bound is valid only for the circuits that require complete settling and are not dependant on the static errors caused by OTA's gain and capacitor matching requirements.

3.7 Summary

In this chapter, two low power techniques are proposed. One technique improves the existing capacitor-shared techniques to further reduce the power consumption of algorithmic ADCs. The other new technique utilizes capacitor-shared, capacitor-scaled, and switched-OTA schemes to reduce the power consumption of algorithmic ADCs. These techniques reduce the power consumption of conventional algorithmic ADCs considerably.

An analysis of the thermal noise in the proposed capacitor shared and capacitor scaled scheme is also conducted. The low power limits of the OTA-based capacitor-shared and capacitor-scaled algorithmic ADCs is determined. A detailed design procedure for a U-MDAC-based algorithmic ADC is introduced as well.

Chapter 4

Design Of The Experimental ADCs

Two prototype ICs are designed and fabricated in a 130-nm CMOS process. One prototype, a 10-bit 5 MS/s algorithmic ADC, demonstrates the concept of the 3-cap-shared technique. The other prototype, a 12-bit 10 MS/s algorithmic ADC, proves the feasibility of the capacitor-shared and capacitor-scaled technique and demonstrates its low power advantages. This chapter provides the design details of these prototype chips.

4.1 Design Considerations

The typical ADCs' specifications are the SNR, accuracy, and linearity. These specifications dictate the design requirements of its building blocks. The ADC's SNR, which is dominated by the circuit's thermal noise levels, dictates the size of the sampling capacitors. The accuracy requirements sets the OTA's gain and minimum capacitor size due to the matching constraints. The ADC's linearity is determined by sampling switches' linearity and OTAs' signal swing. Another key ADC requirement is the comparators' offset, which determines the size of input transistors of the comparators' block.

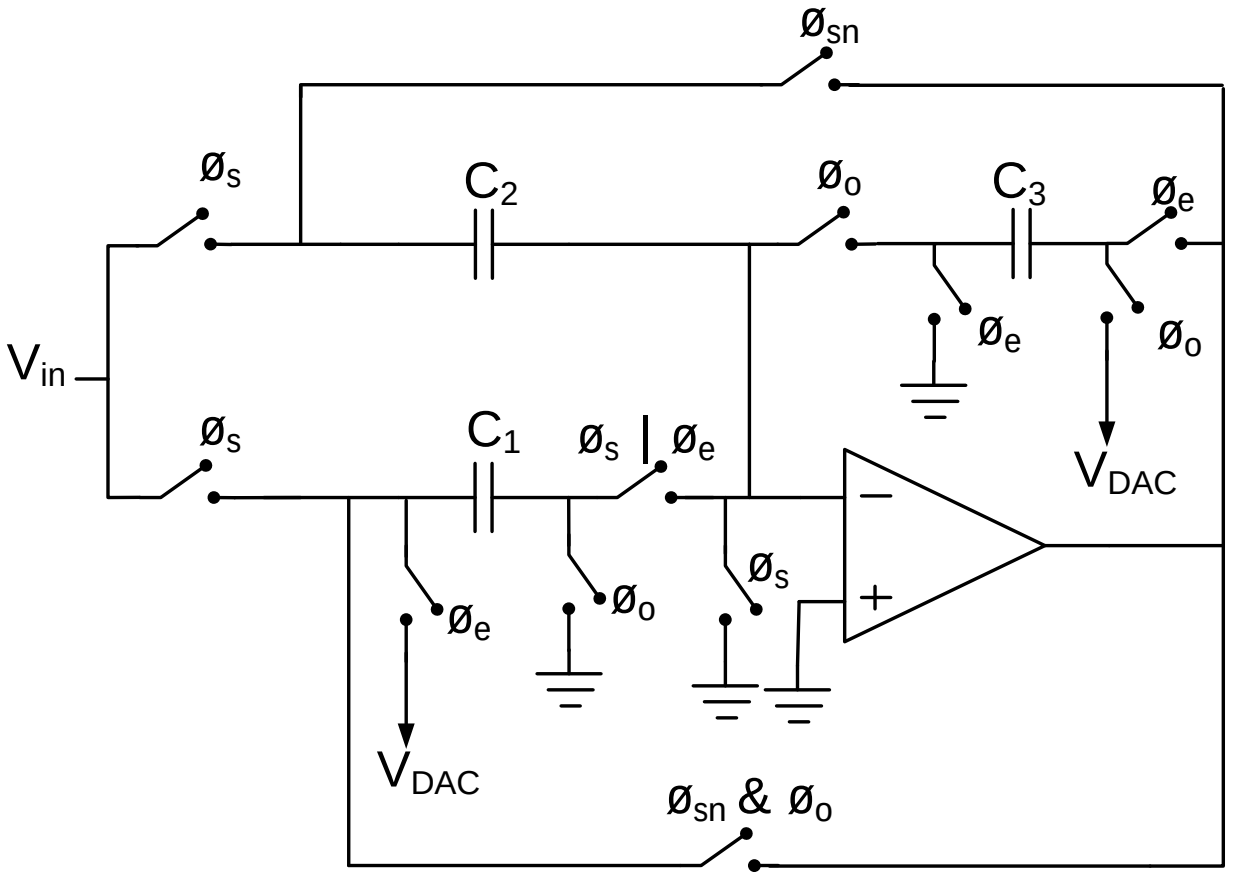
The design considerations of the building blocks of an N-bit SC-based algorithmic ADC are explained in Chapter 2 and 3, and are summarized in Table 4.1.

Table 4.1: ADC's design considerations.

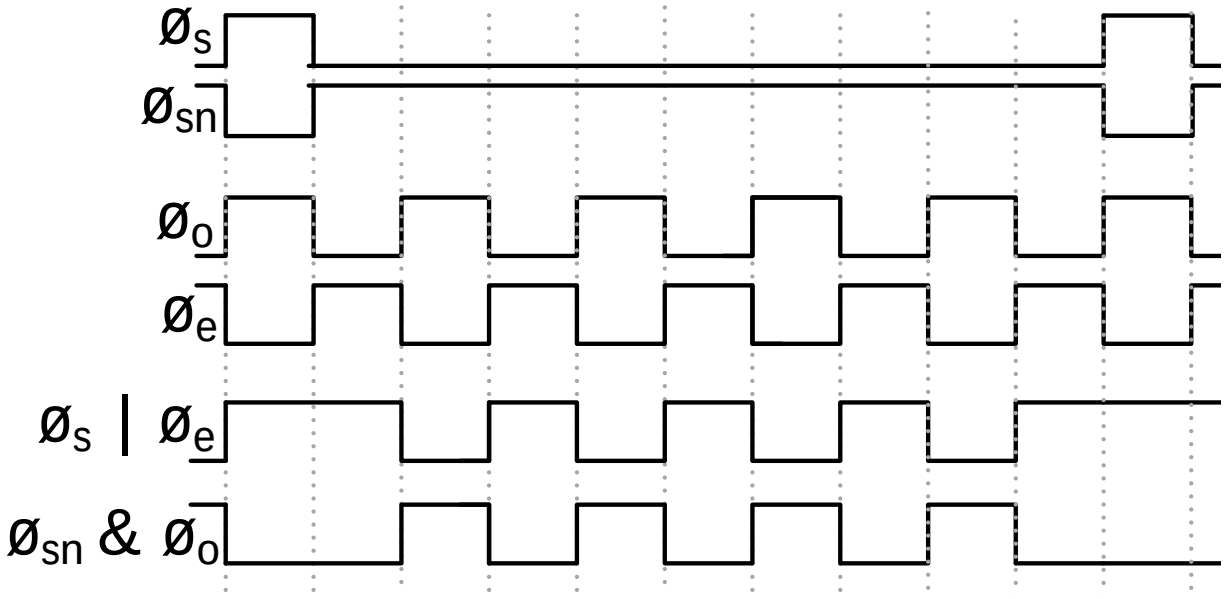
Design Consideration	Eq.#	Ref.	Equation	Example Parameters	Example Value
Sampling capacitor size	(3.30)	[76]	$C_s \geq n_f \cdot \frac{12kT \cdot 2^{2N}}{V_{FS}^2}$ (4.1)	n_f=5, V_{FS} =1.5 V, N = 12	$C_s \geq 1.85$ pF
OTA's DC gain	(2.17)	[79]	$A_v \cdot \beta \geq 2^{(N-K+1)}$ (4.2)	N = 12, K = 1 N = 10, K = 1	$A_v \cdot \beta \geq 72$ dB $A_v \cdot \beta \geq 60$ dB
OTA's bandwidth	(2.20)	[55]	$f_{3dB} = f_T \cdot \beta \geq \left(\frac{(N-K+1)\cdot \ln 2}{2\pi \cdot T_{set}}\right)$ (4.3) $= \left(\frac{N \cdot (N-K+1) \cdot f_s \cdot \ln 2}{2\pi}\right)$ (4.4)	N = 12, K = 1, T_{set} = 16 ns N = 10, K = 1, f_s = 5 MS/s	$f_{3dB} \geq 85$ MHz $f_{3dB} \geq 55$ MHz
Capacitors Mismatch	(2.12)	[80]	$\frac{\Delta C}{C} \leq 2^{-(N-K+1)}$ (4.5)	N = 12, K = 1	$\frac{\Delta C}{C} \leq 0.05\%$
Comparators' Offset		[51]	$\sigma_{\text{static}} = \sqrt{\frac{A_{vt}^2}{W \cdot L} + \frac{1}{(g_m/I_D)^2} \cdot \frac{A_\beta^2}{W \cdot L}}$ (4.6) Also, $3\sigma_{\text{static}} < \pm\frac{V_{ref}}{4}$ (4.7)	A_{vt}=13.5 mV/μm, A_β= 0.5 %μm,(g_m/I_D)= 20, L = 0.48 μm and W = 1 μm	$\sigma_{\text{static}} = 27$ mV

4.2 10-bit 5 MS/s Algorithmic ADC

In this thesis, a 10-bit 5 MS/s algorithmic ADC is designed in a 130-nm CMOS process. The single-ended version of the implemented 3-cap-shared stage and their clocks are illustrated in the Figure 4.1(a) and (b), respectively. During ϕ_s, C_1 and C_2 sample V_{in}. To generate the first residue, C_1 is connected to the DAC reference and C_2 is connected in the feedback. This generated residue is sampled by C_3 and the same residue voltage is also held across the feedback capacitor, C_2. Therefore, the conversion is performed by keeping C_2 connected in the feedback, whereas C_1 and C_3 swap their roles during the ϕ_o and ϕ_e phases. The design criteria for different circuit blocks are as follows.



(a)



(b)

Figure 4.1: Single-ended implementation of a 3-cap-shared stage: (a) SC implementation and (b) clocks.

The switch sizes are dictated by the on-resistance and linearity requirements. Input sampling switches are designed as bootstrapped ones to achieve a high linearity. The switches connected to the OTA's output are gate boosted, and all the switches, connected to the sum node, are simple NMOS switches.

For a 10-bit ADC, the sampling capacitor size is given by (4.1). For n_f=5 and V_{FS} = 1.5 V, C_s must be greater than 115 fF. Therefore, a C_s of 120 fF is chosen in this design.

According to (4.2), the OTA's loop gain, $A_0 \cdot \beta$, $\geq$ 60 dB and from (4.4), the OTA loop bandwidth must be greater than 55 MHz. The OTA, as shown in Figure 4.2, is designed as a gain-boosted cascode OTA [81], with a symmetric loading SC common-mode-feedback (CMFB) [82]. The booster OTAs are implemented as simple folded cascode OTAs.

The chip layout in Figure 4.3 occupies an area of 500 μm x 500 μm.

4.2.1 Simulation results

The ADC is designed by using the IBM 130-nm CMOS process with the MIM capacitor option. The ADC is designed and fully simulated in Spectre, and its post-layout FFT is plotted in Figure 4.4. It is fully functional, verifying the suitability of the proposed technique in algorithmic ADCs. Table 4.2 lists the simulation results.

Table 4.2: Performance summary of the simulated 10-bit 5 MS/s algorithmic ADC.

Technology	130-nm CMOS
Supply	1.5 V
Resolution	10-bit
Sampling frequency (f_s)	5 MHz
Vin_{p-p}	1.5 V
SNDR	50 dB
ENOB	9-bit
Power (P)	150 μW
FOM ($=P/(f_s \cdot 2^{ENOB})$	60 fJ/conversion-step

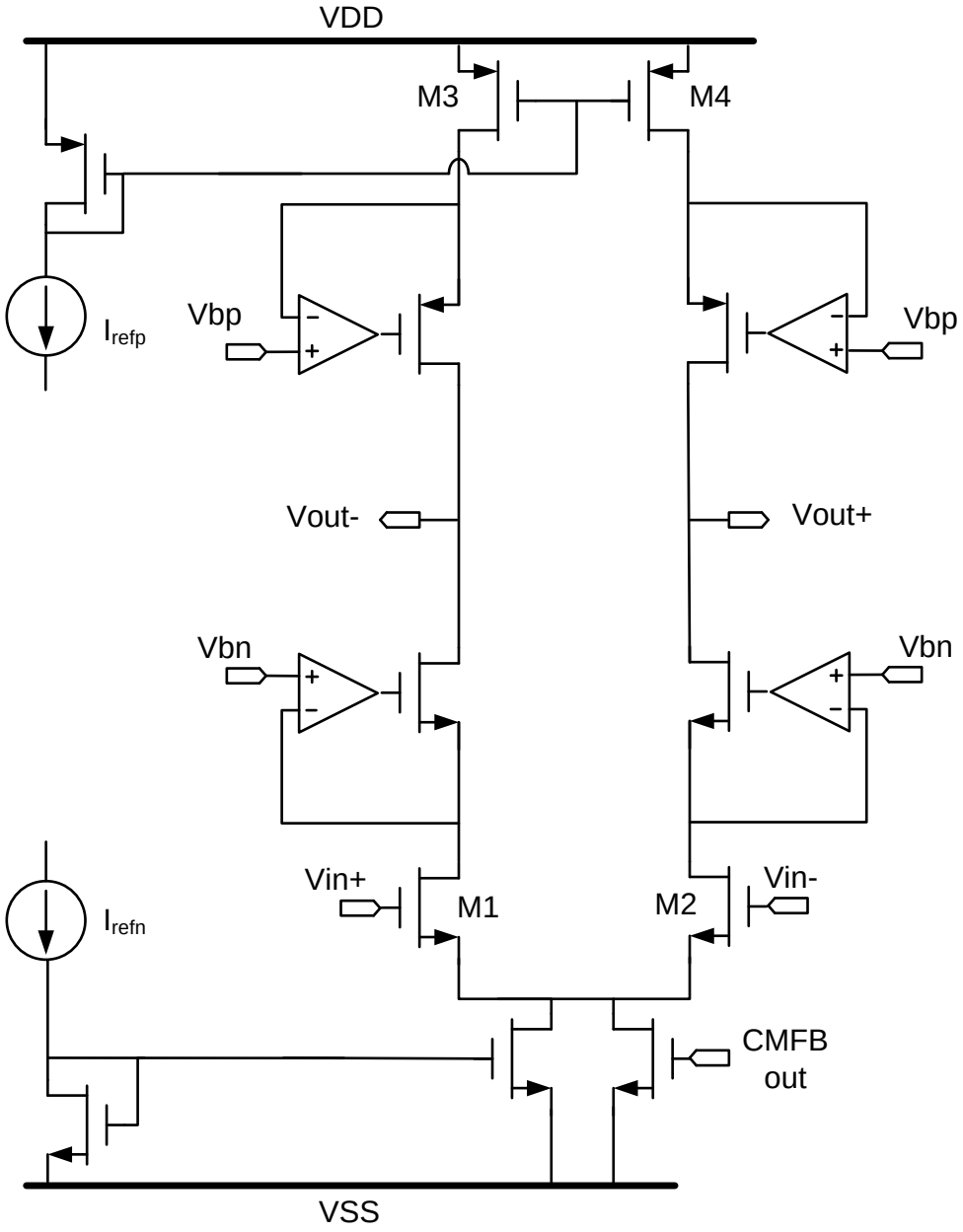


Figure 4.2: Schematic of the OTA.

4.2.2 Testing

A 2-layer FR4 PCB is designed to test the prototype IC in Figure 4.5. Ninety percent of the bottom layer is dedicated to the ground plane. During the chip testing it is found that some vias, connecting one pad (pad -Vref) to the chip core, are missed in the layout.

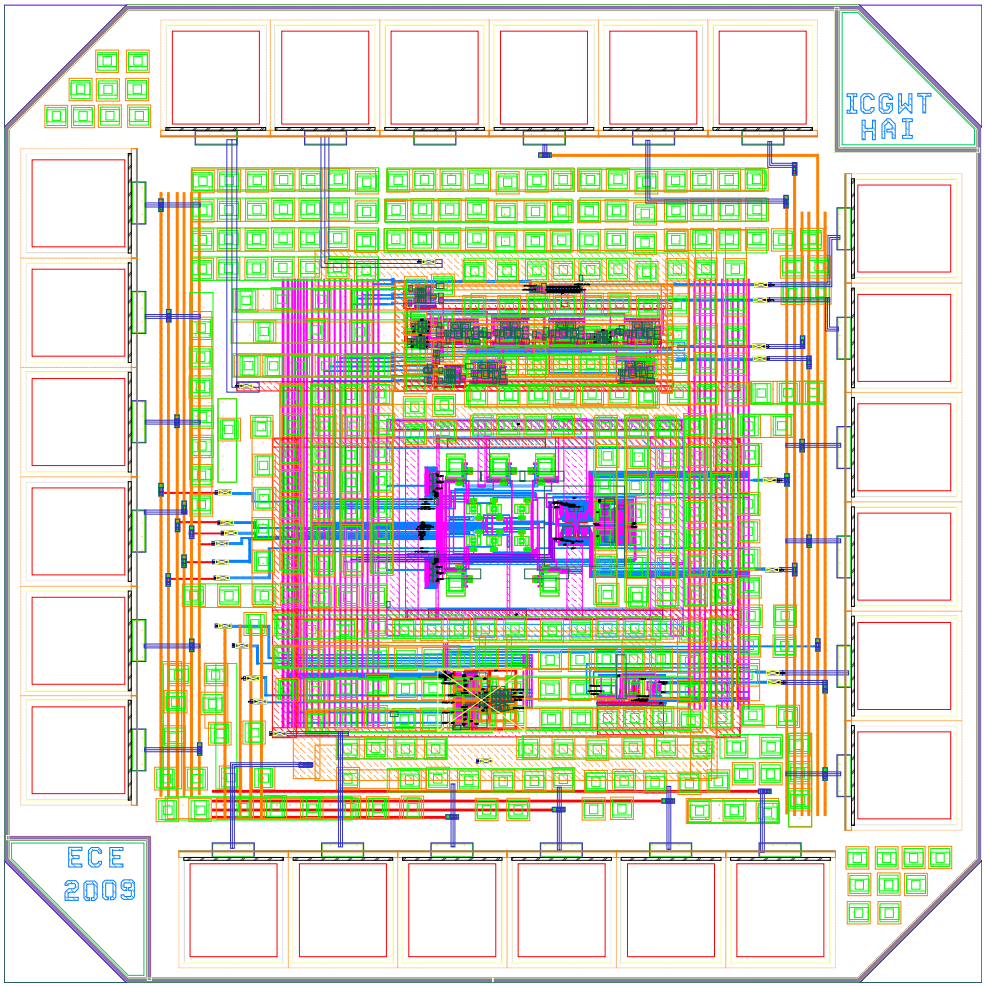


Figure 4.3: Chip layout.

Therefore, measurement cannot be taken.

4.2.3 Summary

A 10-bit 5 MS/s algorithmic ADC is designed in a 130-nm CMOS process to validate the 3-cap-shared low power technique. The simulations results indicate that the implemented ADC has a FOM of 60 fJ/step. In practical case, power supply noise, cross talk from the adjacent signals and other issues that can not be captured in simulations might reduce the FOM a bit.

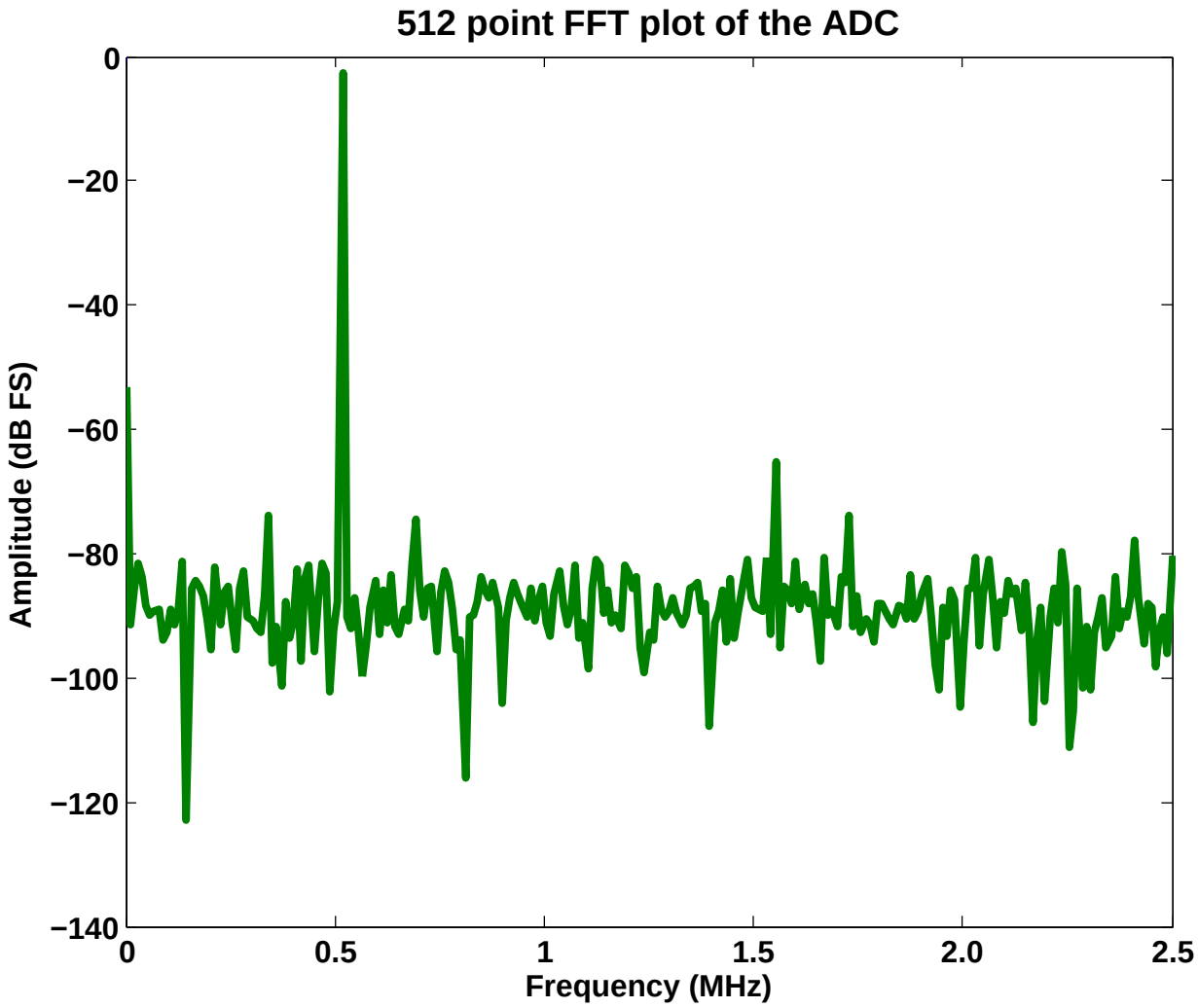


Figure 4.4: 512-point post-layout FFT of the 10-bit 5 MS/s Algorithmic ADC, where f_{in} = 517.57 kHz.

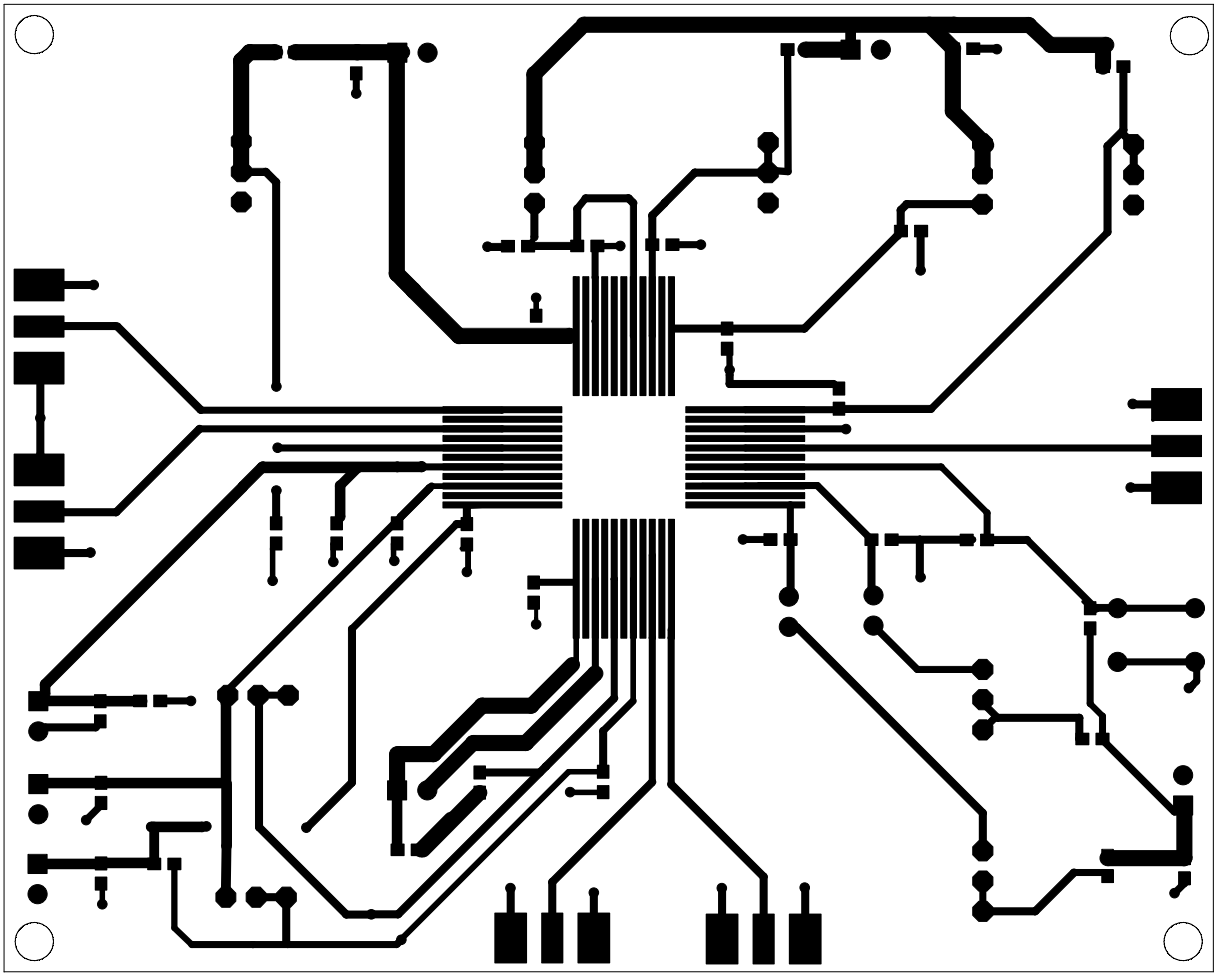


Figure 4.5: PCB layout of the top layer.

4.3 12-bit 10 MS/s Algorithmic ADC

The objective of the prototype ADC is to design a 12-bit ADC sampling at 10 MS/s and consuming low power, while using the proposed U-MDAC approach. In this section, the design of the implemented ADC is explained at system, architectural and circuit levels. Then, the simulation details and results of the measurements are discussed.

4.3.1 System level

At the system level, the sampling capacitor size and number of scaling cycles are determined. The sampling capacitor, as given in (4.1), must be greater than 1.875 pF for n_f=5 and V_{fs}=1.5 V. Therefore, C_s is chosen to be 2 pF.

The 3-sigma percentage mismatch of identical MIM capacitors for the 130-nm CMOS process is given in [83] (pg. 396).

$$3\sigma_{MIM} = \sqrt{\frac{M_A^2}{W \cdot L} + \frac{M_W^2}{W^2}} \tag{4.8}$$

where M_A =4 and M_W=1, and W and L are given in μm. Based on the mismatch data provided by the foundry, matching comparable to 12-bit accuracy is possible [84].

In the chosen 130-nm CMOS process, the minimum MIM capacitor size is 60 fF. Based on (3.43), the number of scaled cycles for C_s=2 pF and C_{min}=60 fF, is expressed as

$$J = \frac{\ln\left(C_s/2C_{min}\right)}{\ln 2} = 4 \tag{4.9}$$

Consequently, 16 U-MDACs are required to be incorporated in four scaling cycles. Since this U-MDAC technique is combined with the 3-cap-shared technique, after six phases (including the sampling phase) the residue is transferred to the next stage, a 3-cap-shared stage, to generate the remaining six bits.

The implementation details are denoted in Figure 4.6. During phase-1, the input is sampled, and the first residue is evaluated during phase-2. At the end of phase-2, eight of the U-MDACs are powered down. During each successive phase, half of the remaining U-MDACs are powered OFF and disconnected from the circuit. During phase-6, a single U-MDAC generates the residue which is sampled by the second stage. The second stage generates the remaining six least significant bits (LSBs). One of the main block of the

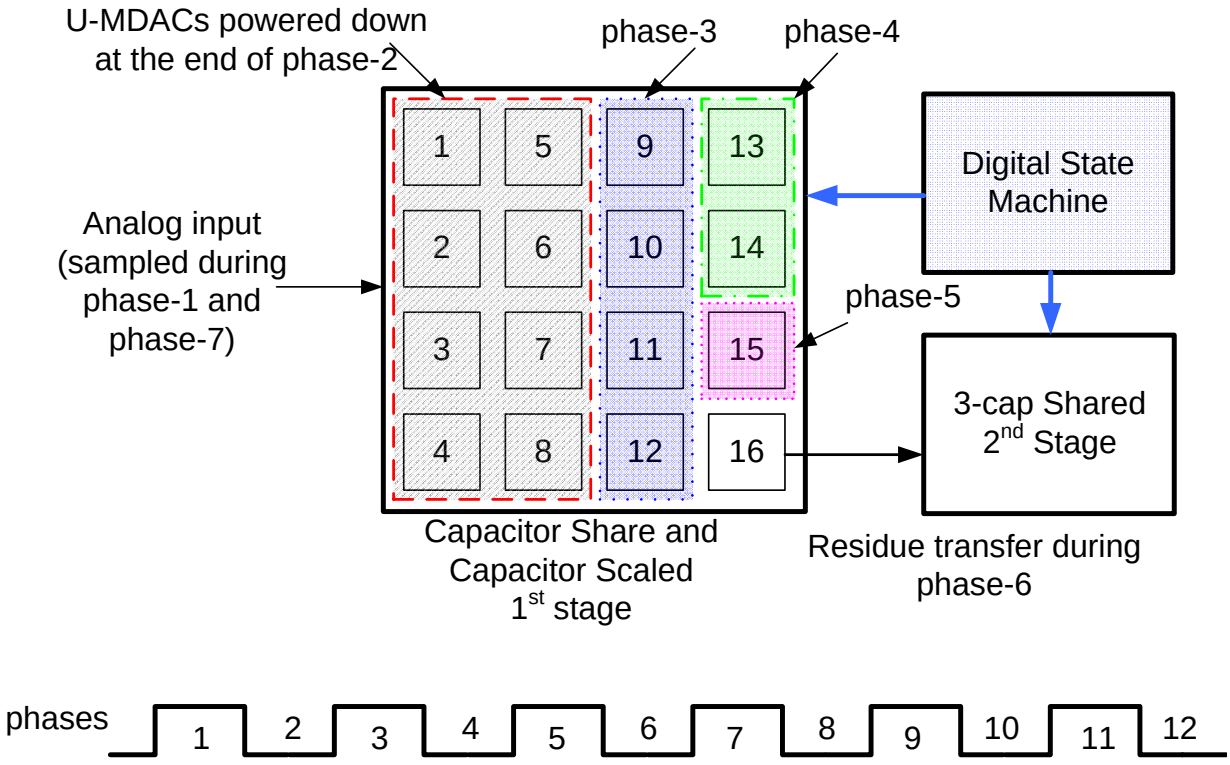


Figure 4.6: Implementation of a 12-bit algorithmic ADC.

implemented ADC is the digital state machine (DSM). The DSM generates the required clock phases to operate the circuit as intended. The complete Spectre schematic of the whole ADC is provided in Appendix Figure A.8.

4.3.2 Architectural level

At the architectural level, the design of an individual U-MDAC is discussed. A single-ended SC implementation of an U-MDAC is shown in Figure 4.7. The stage is similar to that in Figure 2.21 without the explicit load capacitors, C_3 and C_4, and some extra switches. The operation of a generic stage is as follows. During ϕ_1, the input is sampled on both capacitors. During ϕ_2, C_s is connected to the appropriate reference. During $\phi_{f,i}$, C_f is connected to the OTA's feedback to generate the residue, where i is the current evaluation phase. Once the residue is generated, C_f is disconnected from the OTA's output. During ϕ_{i+1}, C_f gets connected to the DAC output, and the DSM generates $\phi_{pd,i}$ to power down the OTA and disconnect its input capacitance from the sum node. At the end of ϕ_{i+2}, the

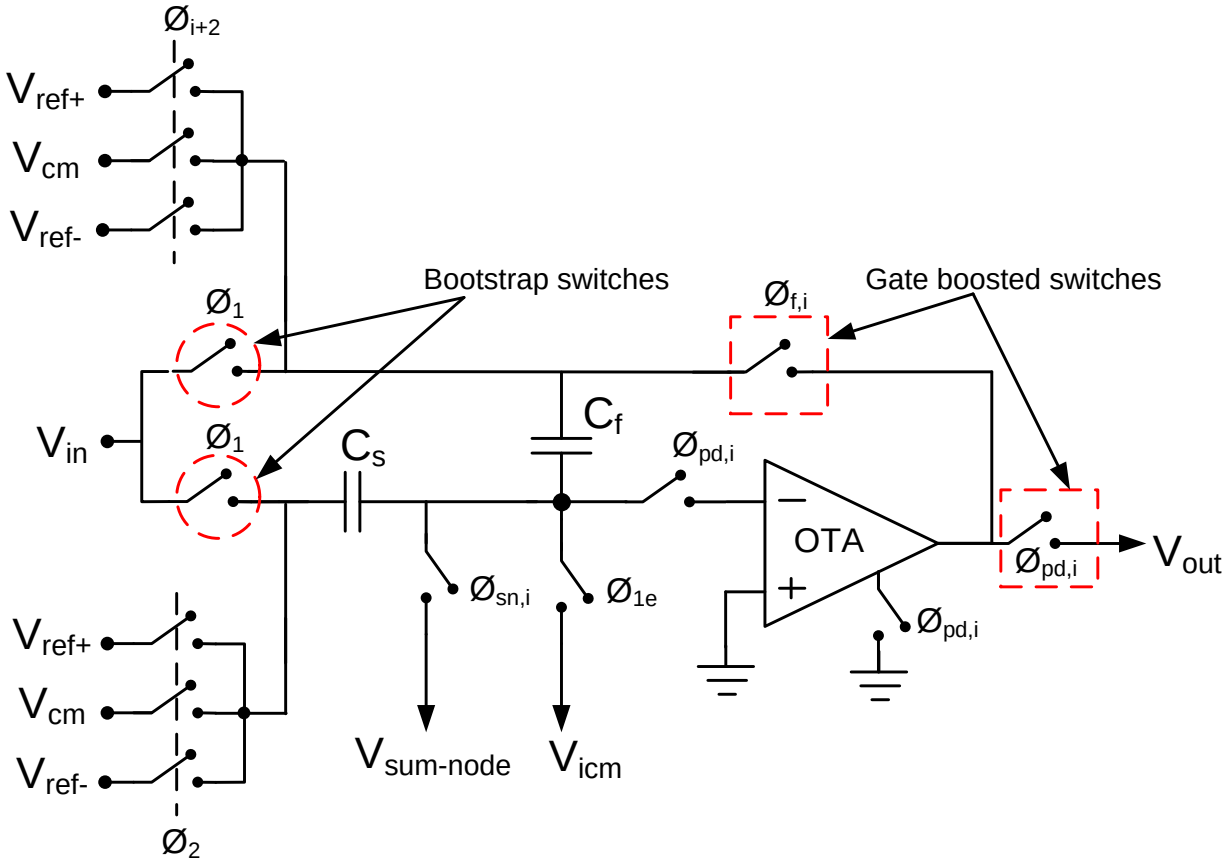


Figure 4.7: Single-ended U-MDAC's implementation.

DSM generates $\phi_{\text{sn,i}}$ to disconnect the sum node of that particular U-MDAC stage from other stages' sum nodes.

A detailed schematic of 16 U-MDACs is signified in Figure 4.8, and the associated clock phases are shown in Figure 4.9. The layout of the U-MDAC is shown in Figure A.9.

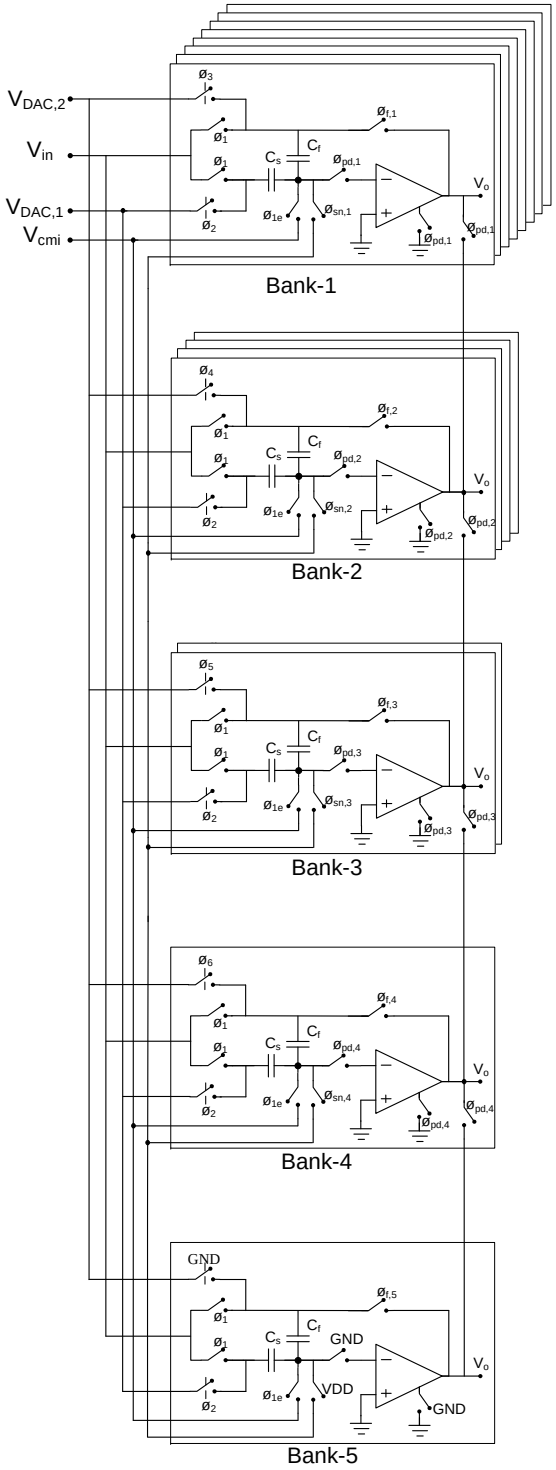


Figure 4.8: Schematic of a 16 U-MDACs' circuit.

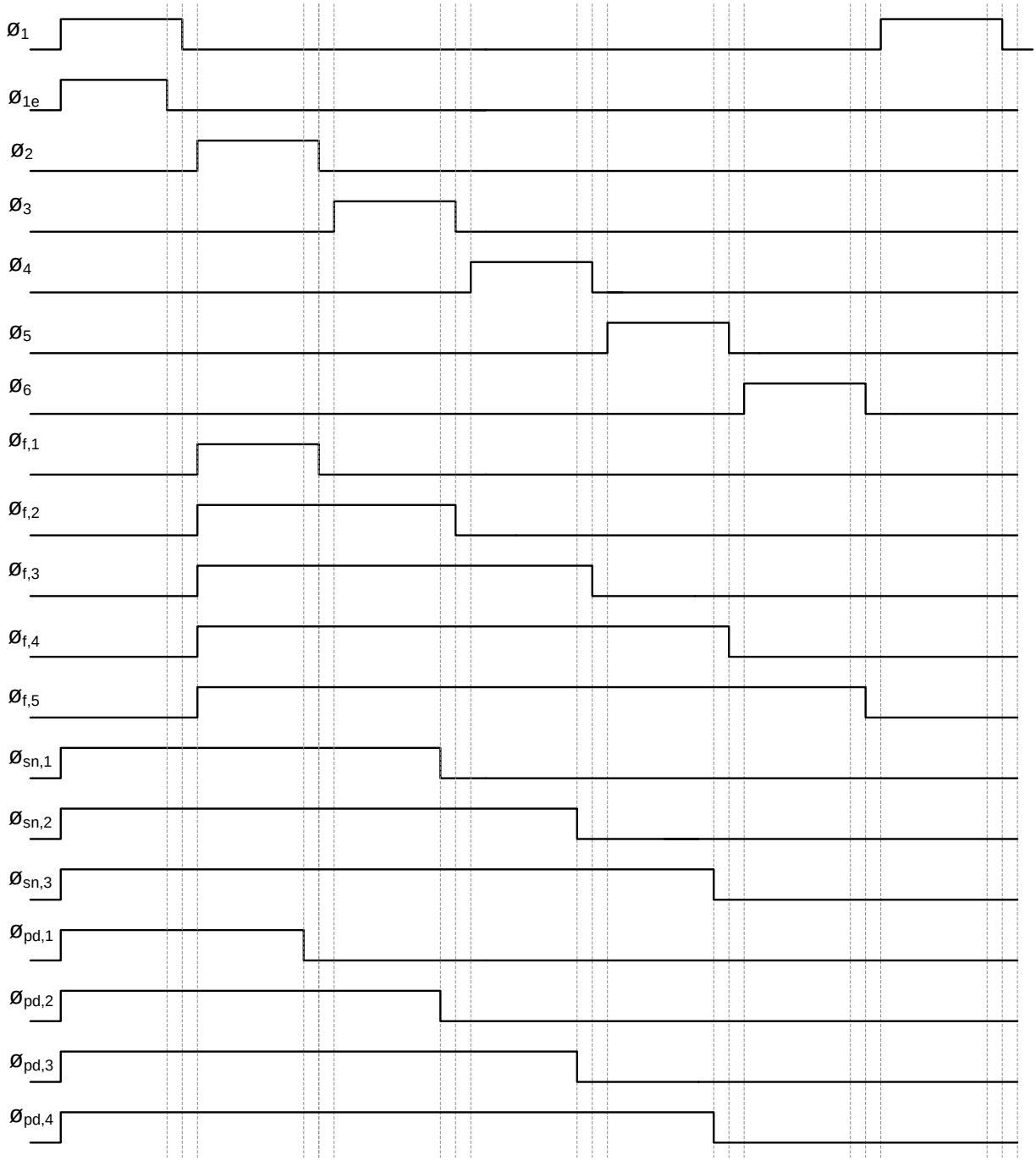


Figure 4.9: Clocks for 16 U-MDACs' circuit.

The 16 U-MDACs are divided into five banks: Bank-1, Bank-2, Bank-3, Bank-4 and Bank-5 with 8, 4, 2, 1, and 1 U-MDACs, respectively. During ϕ_1, all the capacitors sample the input. During ϕ_2, all C_s capacitors are connected to the DAC reference, $V_{DAC,1}$. At the same time, all the C_f capacitors are connected to their respective unit-OTA's output. At the end of $\phi_{f,1}$, all the unit-OTAs of Bank-1 are powered down and disconnected from the sum node. During ϕ_3, all Bank-1 C_f capacitors are connected to the DAC reference, $V_{DAC,2}$, whereas all C_f capacitors of the rest of the banks remain connected to their unit-OTA's output . Once the residue voltage is generated, the sum nodes of Bank-1 U-MDACs are disconnected from the other U-MDACs banks at the end of $\phi_{sn,1}$. The same process is repeated for the rest of the banks.

4.3.3 Circuit level

At the circuit level, the design criteria and transistor level details of each building block of an U-MDAC are presented. These building blocks are switches, OTAs, comparators, DSM, and the 3-cap-shared 2^{nd}-stage. The complete layout of the U-MDAC stage is presented in Appendix Figure A.9.

4.3.3.1 Switches

There is a wide variety of switches available in the 130-nm CMOS process used for fabrication. The test circuit for the switches is displayed in Figure 4.10.

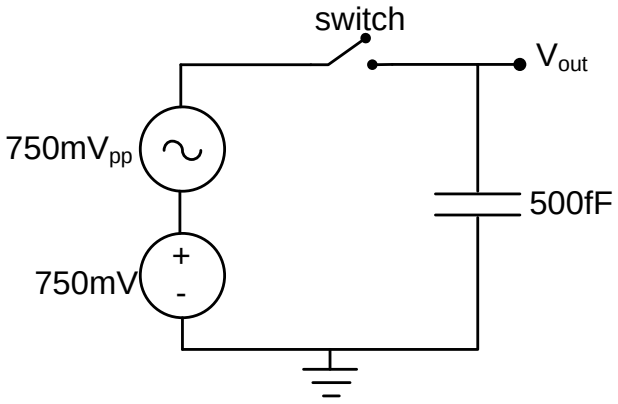


Figure 4.10: Test bench for simulating the THD of switches.

The total harmonic distortion (THD) of different switches for the single-ended and

differential modes are shown in Table 4.3 for W=500 nm and L=120 nm. The input frequency is 1.006 MHz, and a sample rate of 10 MHz is used to generate 1024-points FFT.

Table 4.3: Comparison of THD of various simulated switches at input frequency of 1.006 MHz and a sample rate of 10 MS/s.

Switch	THD (SE) [dB]	THD (Diff) [dB]
NFET	-15.9	-36.66
Thick-oxide NFET	-17.7	-43.54
Transmission gate	-54.04	-74.16
Gate-boosted NFET	-77.88	-81.4
Bootstrap NFET	-81.33	-87.33
Bootstrap Thick-oxide NFET	-100.9	-107.7

To achieve a high linearity, bootstrapped input sampling switches [44, 49] are chosen. The switches connected to the op amp's output are gate boosted switches, and all the switches connected to the sum node, are simple NMOS switches. Bottom plate sampling is selected to eliminate the charge injection errors of the switches.

4.3.3.2 Unit-OTA

The unit-OTA is the most significant active block in the U-MDAC. There are two primary design requirements of an OTA: a high gain to achieve the desired accuracy, and a high speed to settle to the desired accuracy within a given settling time. As given in (4.2), the OTA loop gain, $A_0 \cdot \beta$, must be greater than 72 dB and from (4.4), and for T_{set}=16ns, the OTA loop bandwidth has to be greater than 85 MHz.

The cascode OTA exhibits one dominant pole, and has higher frequency capabilities than those of other topologies. Moreover, it consumes lower power and exhibits less noise. However, cascode OTA are limited by their output swing capabilities. In order to obtain the desired gain from a cascode amplifier, gain boosting is typically employed. Therefore, to meet the high gain requirement, the OTA, shown in Figure 4.11, is designed as a gain-boosted cascode amplifier [81].

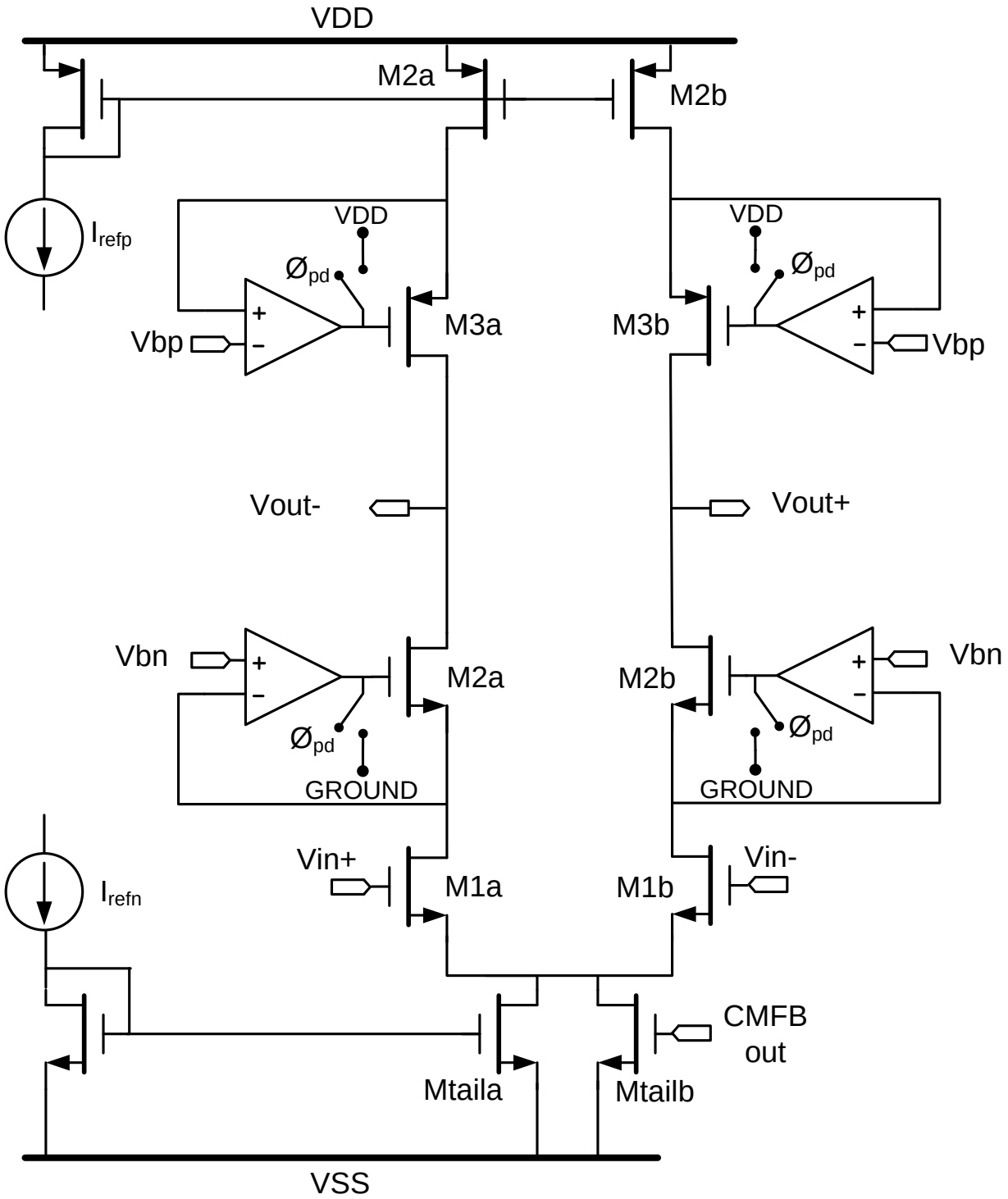


Figure 4.11: Schematic of the OTA with a switched biasing scheme. During ϕ_{pd} the cascode transistors are turned OFF.

Booster amplifiers in a closed-loop can cause stability issues and introduce pole-zero doublets. However, the following conditions ensure that the slow settling, due to pole-zero doublets and stability issues, can be avoided [81] by using

$$\beta \cdot f_T < f_{T,booster} < f_{p2} \tag{4.10}$$

where f_T is the unity gain bandwidth (UGBW) of the gain-boosted OTA, $f_{T,booster}$ is the UGBW of the booster OTA, and f_{p2} is the second pole of the gain-boosted OTA.

To achieve the desired power savings, the OTAs must be turned OFF during their idle period. They are powered down by using the switched-bias technique or the switched-current technique. In the former technique [33], the highly capacitive current source nodes of an OTA are switched between the bias voltage and supply/ground voltage. This technique has the advantages of a very fast turn OFF time and significantly low leakage power wastage, but they are prone to a very high turn ON time. In the switched-current technique, the OTAs are powered down by disconnecting the current path between the power supply and ground. This is achieved by switching the booster OTA's outputs to the appropriate supply such that all the cascode transistors are OFF, as illustrated in Figure 4.11. The disadvantage is that the tail transistors remain connected to the bias voltage, even during the OFF phase. Hence, the bias node suffer little variations compared to the case of the switched-bias technique in Figure 4.12. The switched-current scheme has a faster a turn ON time, compared to that of the switched-bias approach as shown in Figure 4.13.

The booster amplifiers are implemented as simple folded cascode OTAs. The folded cascode topology is selected in order to have a good input common mode range. Single-ended boosters are chosen in order to keep the layout of the OTA symmetric, and also to avoid a CMFB circuit. However, this arrangement increases the area of the overall ADC. These booster amplifiers consume approximately 5 μW of power. The schematic of booster OTAs is drawn in Figure 4.14 The input transistors are laid out in a common-centroid fashion. The device sizes are presented in Appendix Section A.4.

The loop gain and loop phase of the layout parasitic extracted unit-OTA are illustrated in Figure 4.15. The loop gain is around 100 MHz and the phase margin more than 80^0. Each unit-OTA consumes about 37.5 μW of power.

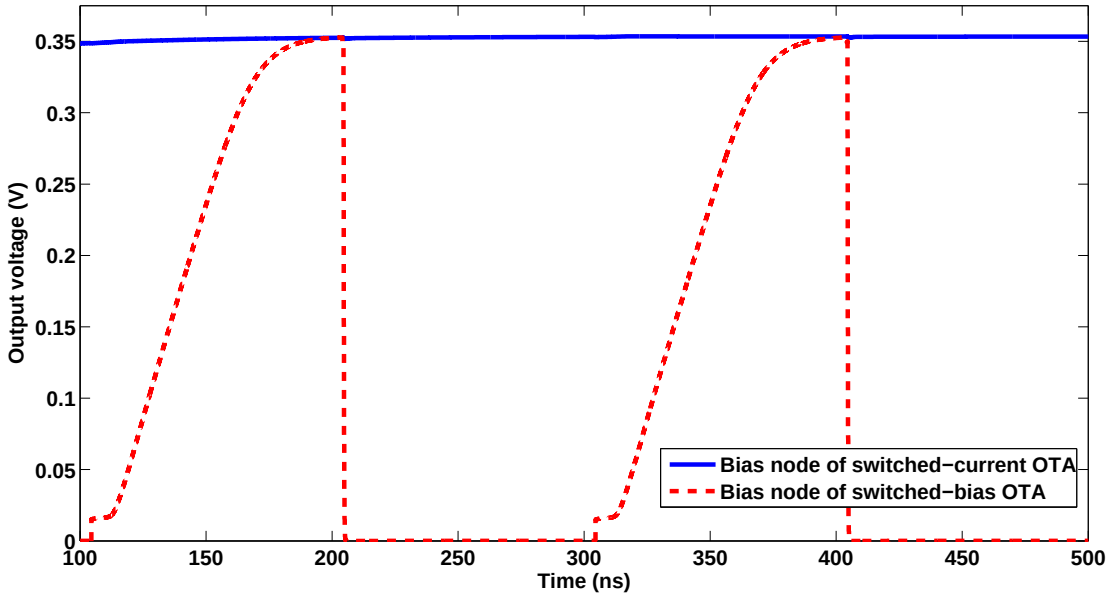


Figure 4.12: Variations of the bias nodes during the OTA's turn ON and turn OFF.

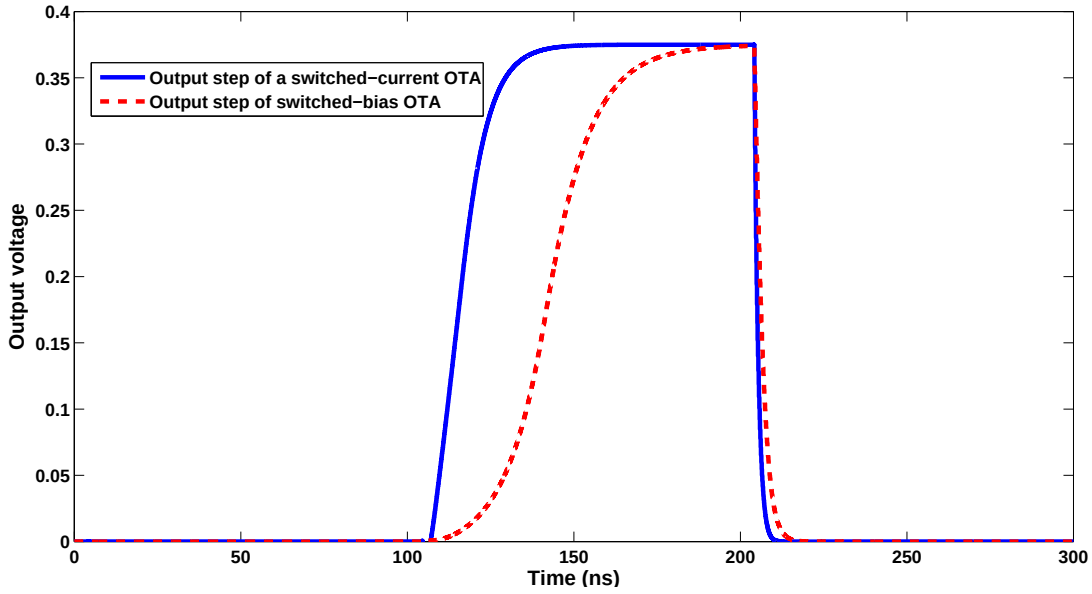


Figure 4.13: OTA's turn ON timings.

4.3.3.3 Comparator

A comparator is one of the principal blocks of an algorithmic ADC, where the operation of a comparator is synchronized with the evaluation phase. At the end of each evaluation phase, the residue is sampled by the comparator. The residue is compared with the reference

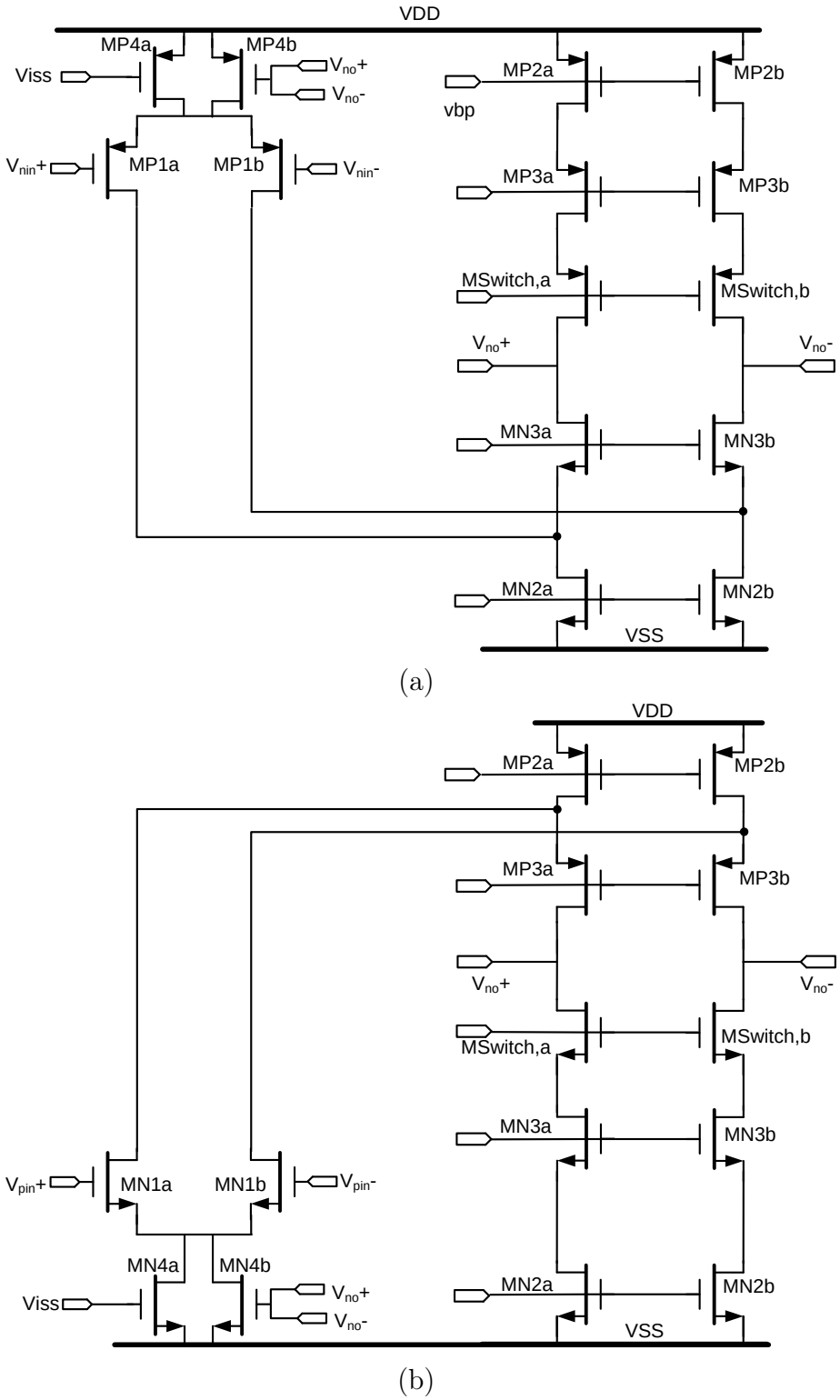


Figure 4.14: Schematic of booster amplifiers: (a) N-booster and (b) P-Booster.

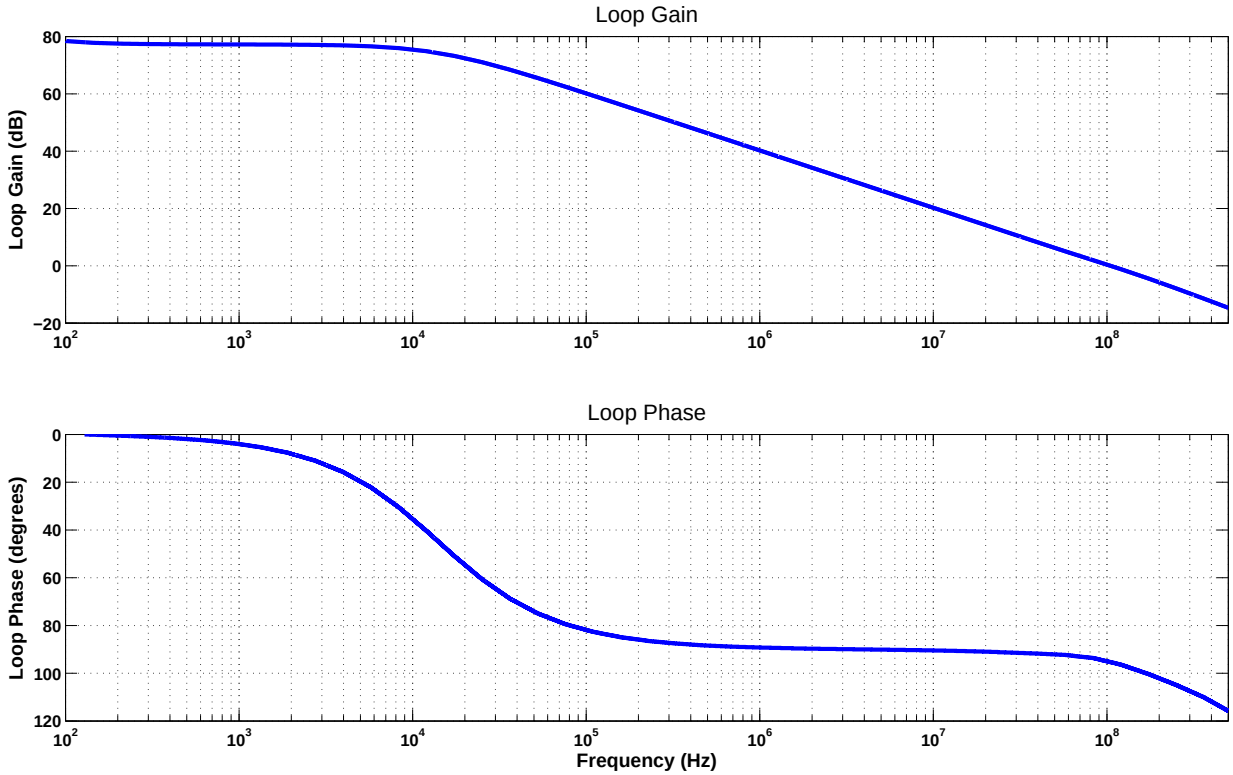


Figure 4.15: Loop gain $|A_0\beta|$ and phase of the OTA.

voltage to make the decision. This comparison is followed by the latching of the comparator for the remainder of the clock phase.

Typically, the requirements of a comparator are speed, low input referred offset, low kickback noise, low input capacitance, and low power consumption. Since the comparison and latching must occur within the evaluation phase, the time taken by the comparator to make a decision directly reduces the time allowed for the OTA to settle.

In an algorithmic ADC employing digital correction, a comparator offset of $\pm V_{REF}/4$ can be tolerated (see (4.7)). The comparators have not only static offsets, but also dynamic offsets. Such offsets are due to the mismatch in the load capacitance at the output nodes. In high speed comparators, the dynamic offsets are much larger than the static offsets. A capacitive imbalance of 1 fF at the output nodes can lead to the input referred offset of several tens of millivolts [85]. One way to reduce the offsets is to use pre-amplifiers. They reduce the input referred offsets by the pre-amplifier gain.

One of the major issues in a latched comparator is its kickback noise. In the latch stage, the positive feedback regenerates the residue into a full-scale digital output. These

large voltage swings can couple into the input nodes through the parasitic capacitances. Since the circuits driving the input nodes of the comparator do not have a zero output impedance, the kickback charge can generate glitches at the input nodes, disturbing the operation of the comparator. The fast and power efficient comparators, especially dynamic comparators [86–88], generate more kickback noise [89]. The easiest and most common solution for the kickback noise reduction is to use a pre-amplifier at the expense of increasing the power consumption.

Because OTAs directly drive the comparators during the evaluation phase, the input capacitance of the comparator directly adds up to the load capacitance of the OTAs. The input capacitance is determined by the area of the sampling transistors. By rearranging (4.7), the area of the input transistors is written as

$$W \cdot L > \left(\frac{12}{V_{ref}}\right)^2 \cdot \left[A_{vt}^2 + \frac{A_\beta^2}{(g_m/I_D)^2}\right] \tag{4.11}$$

For the chosen 130-nm CMOS process, A_{vt} = 13.5 mV/μm and A_β = 0.5%μm. Therefore, for V_{ref}=750 mV and (g_m/I_D) = 20, the transistor area must be greater than $0.4\mu m^2$. Hence, if L = 0.48 μm then W $\geq$ 833 nm. In the design, transistors' width is chosen to be 1 μm. The comparator's device sizes are listed in Appendix Section A.4.

Figure 4.16 is a schematic of the implemented comparator. This comparator, which follows the basic structure presented in [90], has the benefits of being high speed, low offset, low kickback noise, and low input capacitance. The comparator consists of a pre-amplifier, followed by a latch stage, and eventually a set-reset (SR) flip-flop (FF). The SR FF holds the output of the latch when it is in the reset mode.

The pre-amplifier is beneficial in many ways, including amplifying the input signal, reducing the dynamic offset and reducing the kickback noise. The gain of the pre-amplifier is expressed as

$$A_{v1} = \frac{g_{m,1} + g_{m,3}}{g_{m,6}} \tag{4.12}$$

where $g_{m,1}$ and $g_{m,3}$ are the transconductance of the input, and $g_{m,6}$ is the transconductance of the load transistor, respectively. In the implementation, the gain of the pre-amplifier is chosen to be around eight large enough to suppress the dynamic offset in the latch.

The operation of the latch is as follows. During the reset phase, $\phi_{latch} = 1$, the output nodes of the latch are set at V_{GS} of M_{14} and M_{15}. During the regeneration phase, ϕ_{latch} goes low, M_{13} turns OFF pulling the output nodes down because of the charge injection.

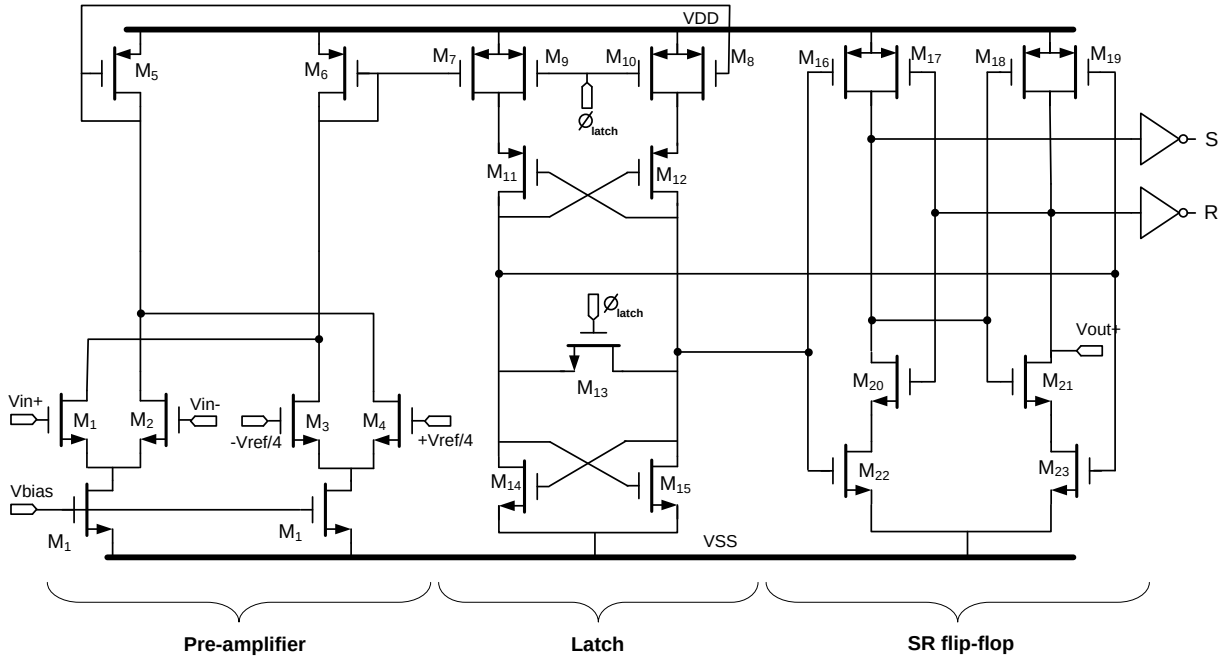


Figure 4.16: Comparator schematic.

Then, depending on the input voltage, one of the output nodes reaches the supply rail, whereas the other goes to the ground. Depending on the latch output, the SR FF modifies its output. After the regeneration phase, the latch resets such that SR FF keeps the output of the latch for the rest of the evaluation phase. The gain of the latch during the reset in Figure 4.17, is written as

$$\begin{aligned} A_{v2} &= g_{m,8} \cdot \left(\frac{R_{13}}{2} \| \frac{-1}{g_{m,15}} \right) \\ &= \frac{g_{m,8}}{\frac{2}{R_{13}} - g_{m,15}} \end{aligned} \tag{4.13}$$

Therefore,

$$\frac{2}{R_{13}} > g_{m,15}$$

for the latch to act as an amplifier during the reset phase.

During the regeneration phase,

$$V_o(t) = V_{in}(t=0) A_{v1} A_{v2} \cdot e^{t/\tau} \tag{4.14}$$

where $\tau = C_L / g_{m,8}$.

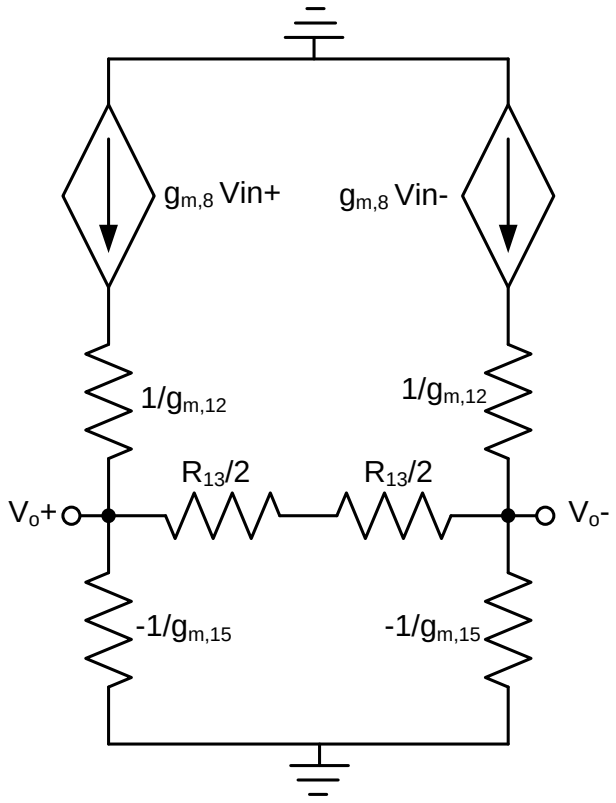


Figure 4.17: Simplified schematic of the latch.

The total input referred offset of the comparator is given by

$$V_{os} = \sqrt{V_{os,1-2}^2 + V_{os,3-4}^2 + \frac{V_{os,5-6}^2 + V_{os,7-8}^2}{A_{v1}^2} + \frac{V_{os,11-12}^2 + V_{os,13-14}^2}{A_{v1}^2 A_{v2}^2} + \frac{V_{os,dynamic}^2}{A_{v1}^2 A_{v2}^2}} \quad (4.15)$$

where the matching of input differential pairs directly affects the input referred offset of the overall comparator. Monte Carlo analysis can be performed to extract the static offsets. However, devices are large and mismatch would be relatively small. The devices' offset information is presented in the design manual of the technology used for implementation [83].

During the layout, care is taken to make the layout as symmetric as possible to avoid any systematic offset. Input differential pairs are laid out in the common-centroid fashion, and dummy transistors are added to maintain the same surroundings around each transistor's finger, as shown in Fig 4.18. The complete layout of the comparator is provided in Appendix Figure A.11.

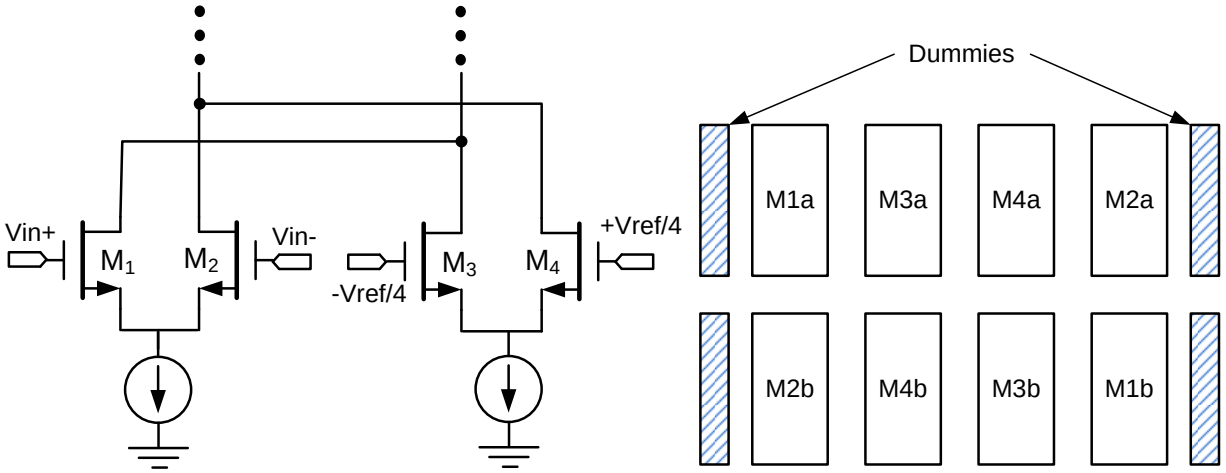


Figure 4.18: Common-centroid layout of the comparator's input differential pair with dummies.

4.3.4 2^{nd} stage design

The requirements for the OTA in the second stage are substantially reduced, compared to those of the first stage. For this stage, an accuracy of only six-bits is required. This relaxes the OTA's loop gain requirements to approximately 30 dB which is met with a simple cascode OTA. The second stage's OTA is similar to the one in Figure 4.11 without the booster amplifiers. As a result, the power dissipation of this OTA is significantly lower than that of the first stage's OTA. For this stage, a unit metal-over-metal capacitor size of 30 fF is adopted to further reduce the power requirements. The vertical natural capacitor (VNC) are used as the 30 fF capacitors. The loop gain and phase of second stage OTA is shown in Figure 4.19. The total power consumed by this stage is 30 μW. The layout of the said stage is depicted in Appendix Figure A.10.

4.3.5 Clock generation

To operate the ADC as intended, different clock phases are generated. The clock generation circuit is designed by using Verilog HDL and simulated in ModelSim. The verilog code is synthesized to generate the schematic in Figure 4.20. The schematic is mapped into cadence schematic by designing the logic cells in a 130-nm CMOS process.

Figure 4.21 portrays the different clock phases generated from the main clock. Non-

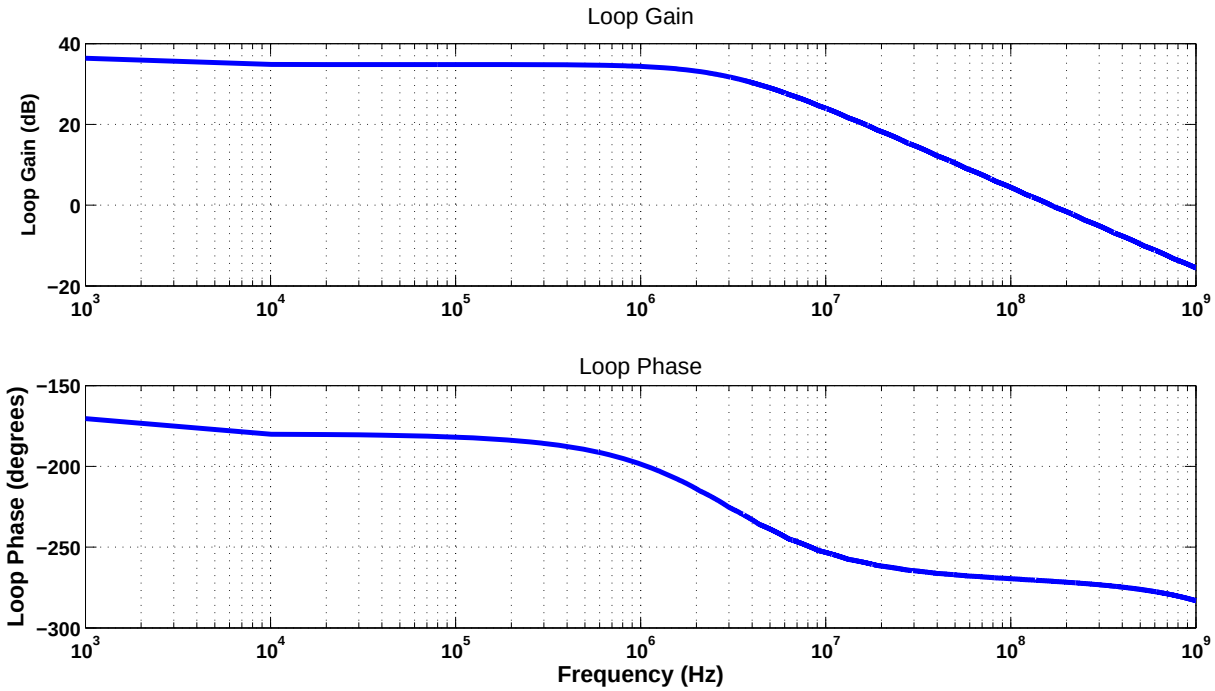


Figure 4.19: Loop gain $|A_0\beta|$ and phase of the second stage OTA.

overlapping phases are generated in order to avoid any charge leakage, as indicated in Figure 4.22. The overlap time is chosen to be around 300ps, as shown in Figure 4.23.

These clock phases turn ON and OFF different U-MDACs at the appropriate times in order to save the power consumption. The clock generation circuit consumes around 180 μW of power.

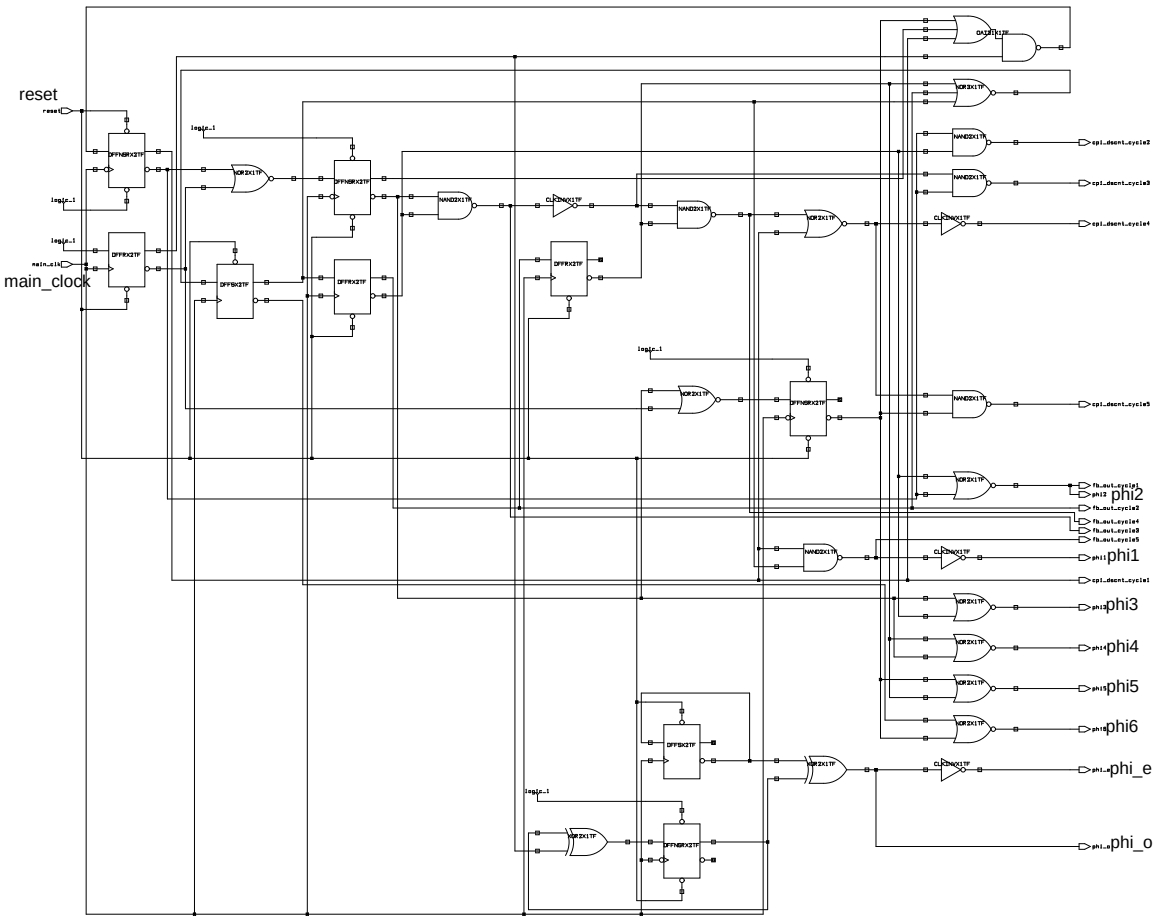


Figure 4.20: Schematic of clock generation circuit.

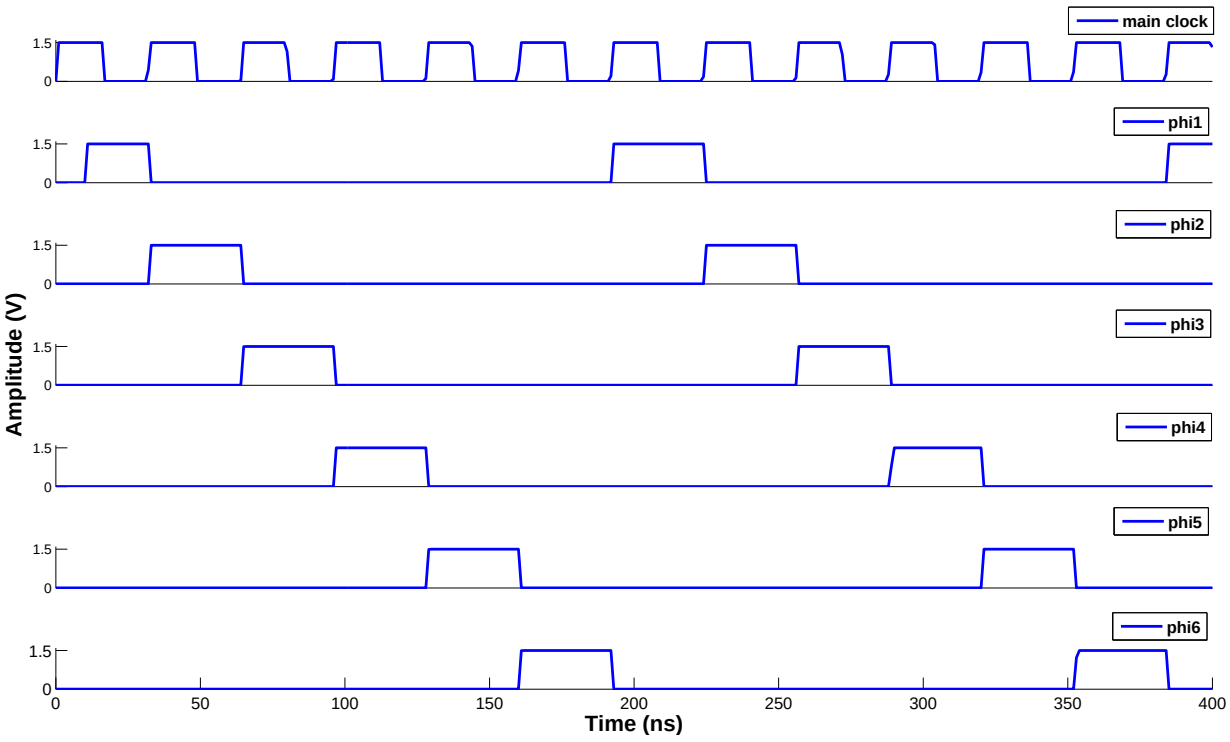


Figure 4.21: Six clock phases.

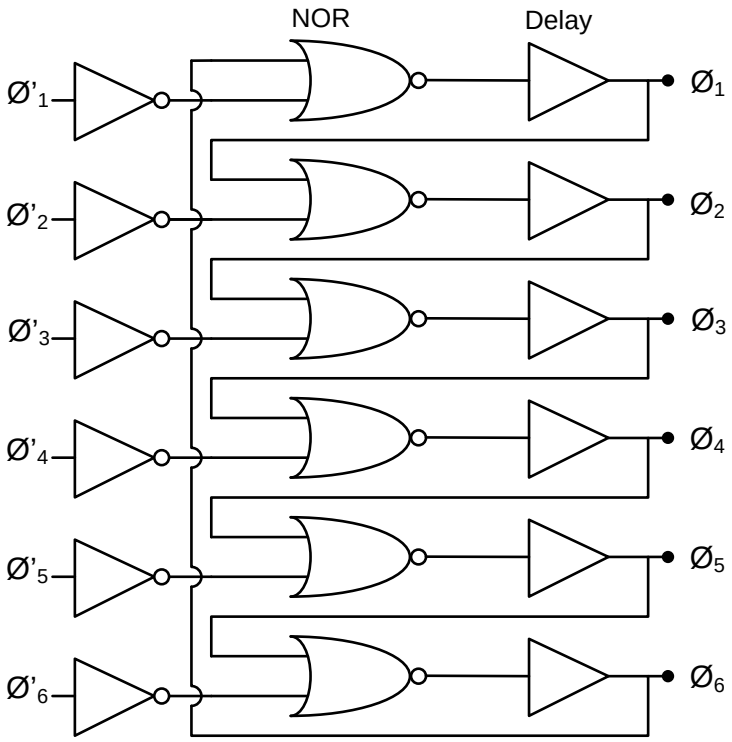


Figure 4.22: Non-overlapping clock generator.

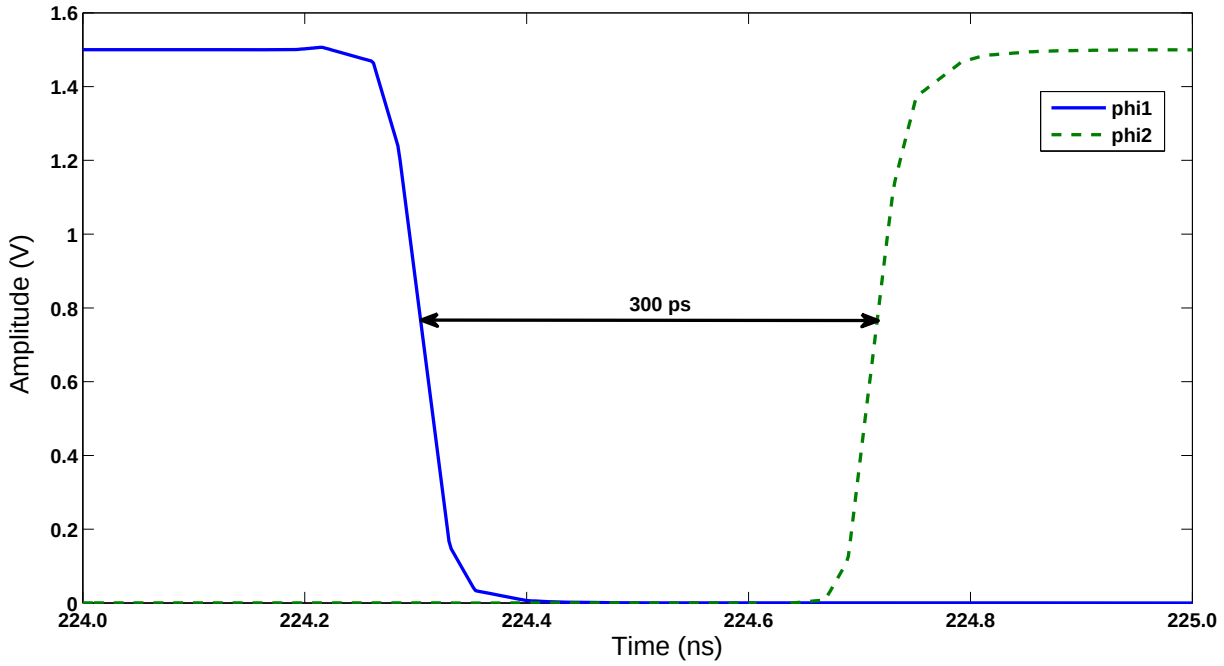


Figure 4.23: Non-overlapping time between ϕ_1 and ϕ_2.

4.3.6 Simulation results

Simulations of the prototype ADC are required to prove the feasibility of the newly developed low power technique by including all the building blocks at the transistor level. The ADC is implemented in a 130-nm CMOS process with a metal-insulator-metal (MIM) capacitor option and occupies a die area of 1.7mm x 0.7mm. The chip layout is displayed in Figure 4.24

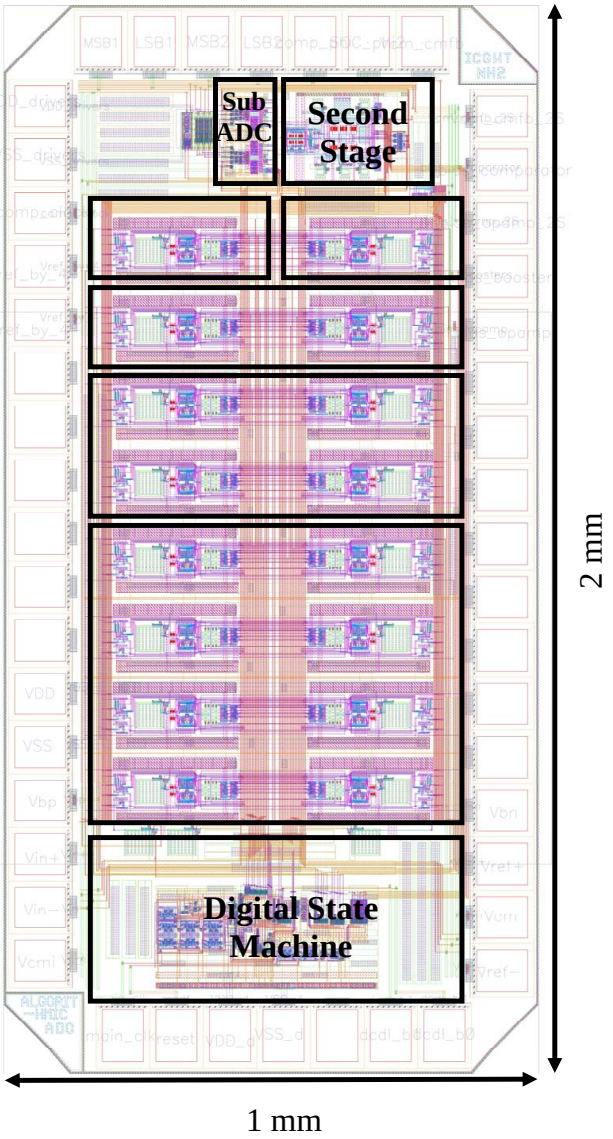


Figure 4.24: Chip layout of the algorithmic ADC.

The simulated power consumption of each block is summarized in Table 4.4.

Table 4.4: Power consumption of different blocks of the simulated ADC.

Design block	Power Consumption (μW)
Core ADC	315
OTA + local biasing	37.5 + 15 = 52.5
2^{nd} stage	30
Global biasing	150
sub-ADCs	2x 60 = 120
DSM	180
Total	1035

It is evident that the chip consumes approximately 1 mW of power, including the digital clock generation circuitry. The core ADC consumes approximately 350 μW, digital clock circuitry consumes 180 μW, 120 μW is consumed by the four comparators, and the local and global biasing consumes approximately 400 μW.

The current profile of the core ADC is depicted in Figure 4.25. It is evident that the current reduces in successive cycles, as the unit-OTAs are powered down. The dashed-line indicates the current consumption in case the OTAs are not switched OFF. The average current consumption of the U-MDAC implementation is represented by the dashed-dot-line in the figure. In this particular current profile, it is shown that the OTAs are active during the sampling phase, however, in the actual implementation the time when the OTAs turn ON during sampling phase is digitally controlled. Therefore, a lower average current is expected, when OTAs remain OFF during most of the sampling phase. The reason of turning ON the OTAs during the sampling phase is to allow sufficient time for CMFB settling, before the evaluation phase.

With the input frequencies of 528.8 kHz and 4.59 MHz input at 10 MS/s, a 256-point FFT is shown in Figure 4.26.

The performance of the ADC is summarized in Table 4.5. Table 4.6 shows the performance comparison of the proposed ADC and recently published algorithmic ADCs. The proposed ADC has the lowest FOM, compared to that of the other published data.

$$\text{FOM} = \frac{\text{Power}}{f_{\text{s}} \cdot 2^{2\text{ENOB}}} \tag{4.16}$$

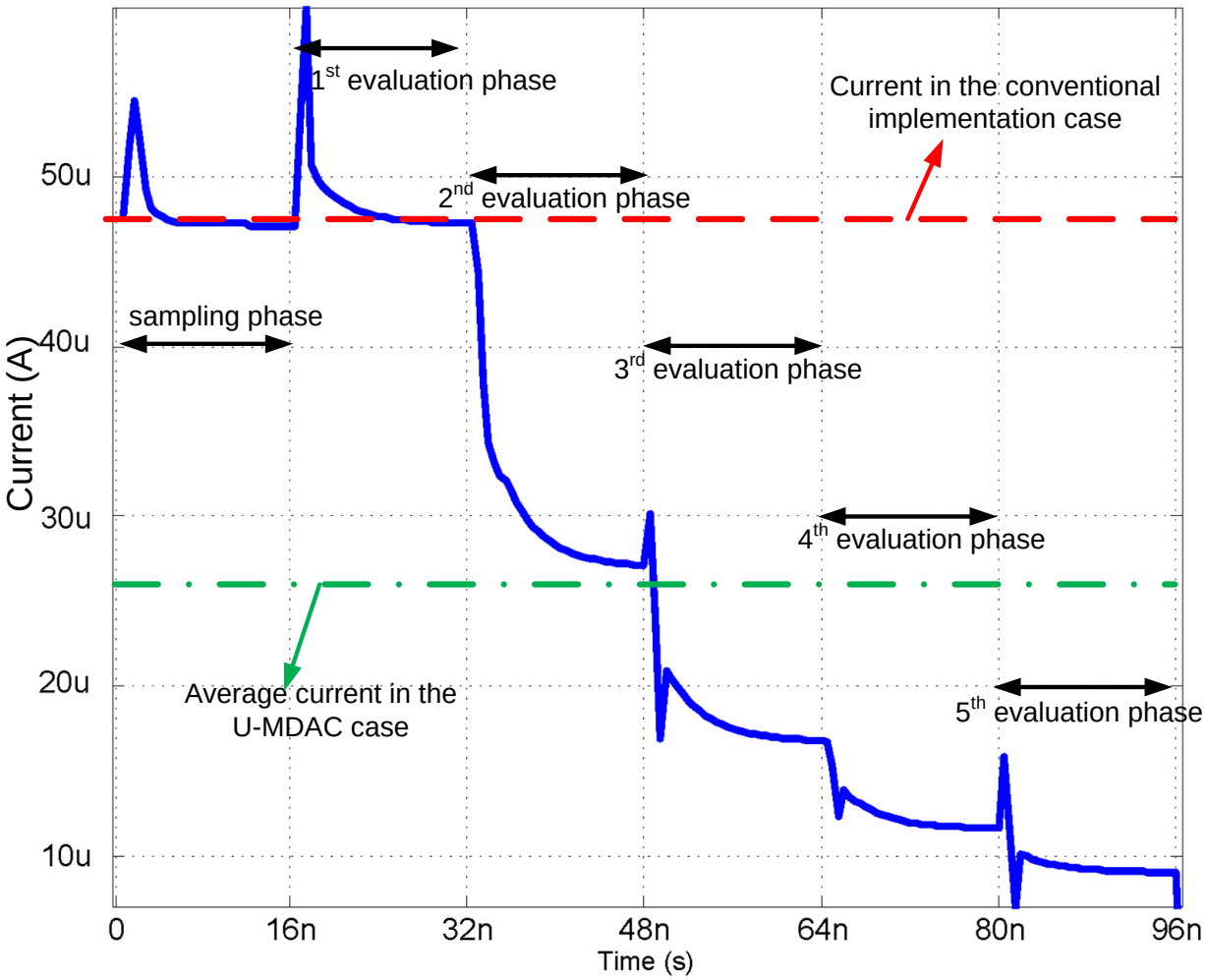


Figure 4.25: Current profile of the core ADC.

where ENOB is the effective number of bits.

The estimated power savings comes from inter-cycle capacitor and OTA scaling, and capacitor sharing. Compared to the conventional techniques, the power consumption in the proposed ADC is reduced by 50% in each subsequent cycle. If noise is neglected and the power of the regular ADC is normalized to unity, the proposed ADC requires a power of

$$P = \frac{1}{N} + \frac{1}{2N} + \frac{1}{3N} + \cdots = \frac{2}{N} \tag{4.17}$$

for an N-bit ADC. Unfortunately, interstage scaling increases the input referred noise by $\sqrt{2}$. Therefore, 70% power savings are expected due to the capacitor scaling. Also, capaci-

Table 4.5: Performance summary of the 12-bit 10 MS/s algorithmic ADC.

Technology	130-nm CMOS
Supply	1.5 V
Resolution	12-bits
Sampling frequency (f_s)	10 MHz
$V_{in,p-p}$	1.5 V
SNDR	66 dB
ENOB	11 bits
Power (P)	1 mW
FOM (=P/($f_s \times 2^{2ENOB}$)	0.02 fJ/conversion-step^2

tor sharing reduces the load capacitance and hence the power consumption further by 50%. Therefore, 85% power reduction is expected with compared to the flip-around configuration and OTA-shared technique, and more than 90% when compared to the conventional technique.

Table 4.6: Comparison the FOM of recently published algorithmic ADCs.

Ref.	P (mW)	f_s (MS/s)	Res.	FOM (fJ/step^2)
[2]	0.09	2	10	0.04
[13]	2.3	1	10	2.19
[26]	15.8	14	10	1.1
[42]	10	1.5	11	1.58
[55]	15	10	9	5.72
[69]	2.85	20	11	0.04
[29]	6.9	50	9	0.55
[91]	0.74	2.5	10	0.3
[92]	0.115	0.02	13	0.1
[30]	11	1.25	9	33.56
[39]	0.069	0.04	11	1.24
[40]	12	5	8	36.62
This work	1	10	12	0.006

4.3.7 Measurement setup and results

A prototype ADC is designed by using a 130-nm CMOS process. The chip occupies an area of 700 μm x 1400 μm, excluding the pads. To facilitate the chip measurements, digital outputs are taken out serially and combined off-chip. In order to test the functionality of the DSM, one clock phase (ϕ_2) is taken off-chip. The purpose of this output is not only to check the DSM functionality but also to align the serial data coming from the comparators.

Separate supply and ground pins are provided for the analog, digital, and output buffer portions of the chip. An analog supply is used for providing power to the core ADC and the pre-amplifiers of comparators. Latches, clock, and digital logic are powered by the digital supply. The output buffers consume very high power so that they are powered with a separate supply to avoid coupling the noise originating from these buffers to analog or digital portions of the chip. The master bias current and reference voltages are provided off-chip for better testability.

A 2-layer FR4 PCB, designed to test the prototype IC, is shown in Figure 4.27. A diagram of the measurement setup is drawn in Figure 4.28. The chip is packaged in a surface-mounted 44-pin CQFP package, and is soldered on the PCB. A 2-layer PCB is designed with about 90% of the bottom layer used as a ground plane to provide a good current return path. All the external capacitors and resistors are surface-mounted ones, whereas through-hole potentiometers are used. All the chip pins are decoupled by a 0.1 μF and 10 μF capacitors. The clock signal is provided by the signal generator. The chip can handle both sine and square wave inputs.

4.3.7.1 Measurement results

In order to take the measurements of the fabricated design, all parts of the ADC must work properly. Unfortunately, in any of the seven chips tested, the DSM and comparators do not work simultaneously. Three chips have DSM working evident in Figure 4.29. Figure 4.30 illustrates that the intended operation of comparators. However, the comparators are working in two other chips, whereas in the remaining chips, neither the clocks nor comparators work.

A properly laid out and simulated circuit is susceptible to failure after manufacturing, if protection circuits are not provided on-chip. Such circuits including clamping diodes and electrostatic discharge (ESD) circuits. Clamping diodes are employed to prevent the circuit

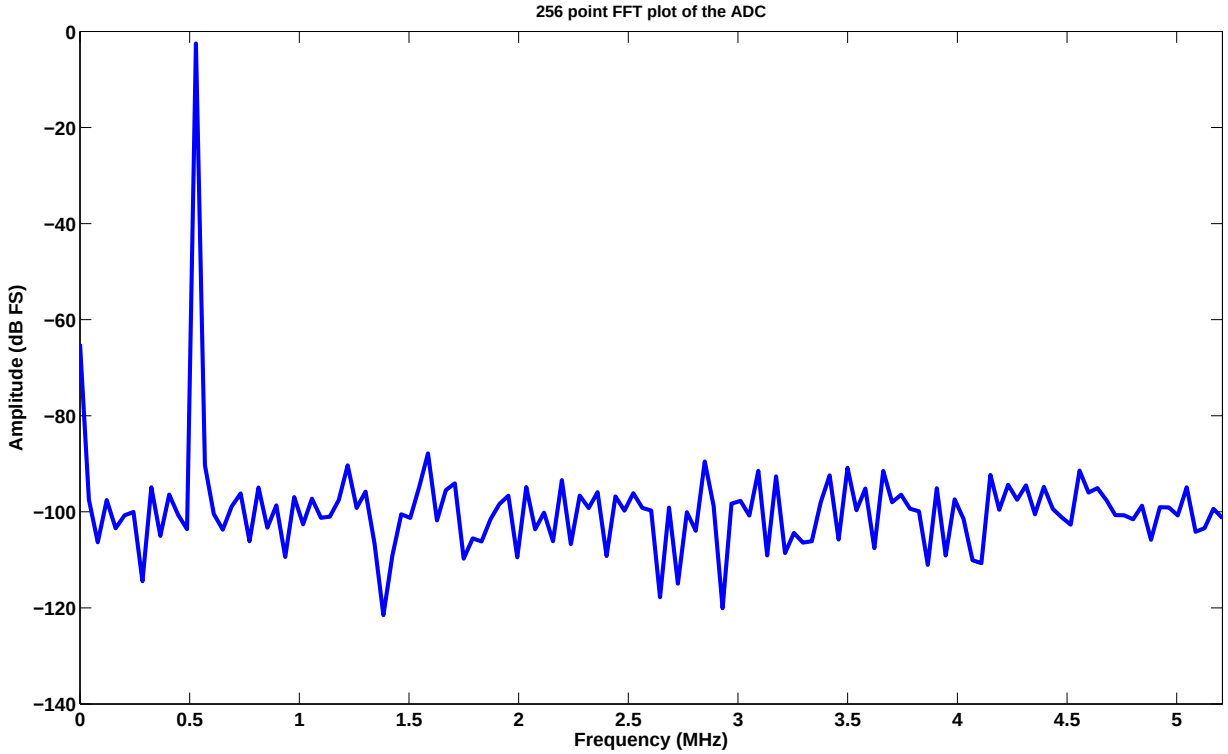
from the overshoot or undershoot of the incoming signal due to the line reflections. ESD protection circuits provide an alternate path for the charge to flow to ground in the case of a highly capacitive object, for example, a human body touches the circuit. Additionally, an IC contains not only the components required to perform the intended operation, but also parasitic components (transistors and diodes). These parasitic elements, under particular operating conditions, can become active and trigger an unintended operation that can result in a fatal fault of the chip. A typical example of an unintended operation is the latchup, which occurs due to the undesirable interaction between the PN junctions of the NMOS and PMOS transistors placed in proximity [48].

Due to the design time and die area limitations, ESD structures are not placed inside the chip. It is noticed that in different chips, different pins are sinking excess current (sometimes more than 20 mA). All of these faulty pins are connected to the gates of the transistors, indicating an oxide breakdown mechanism or internal latchup.

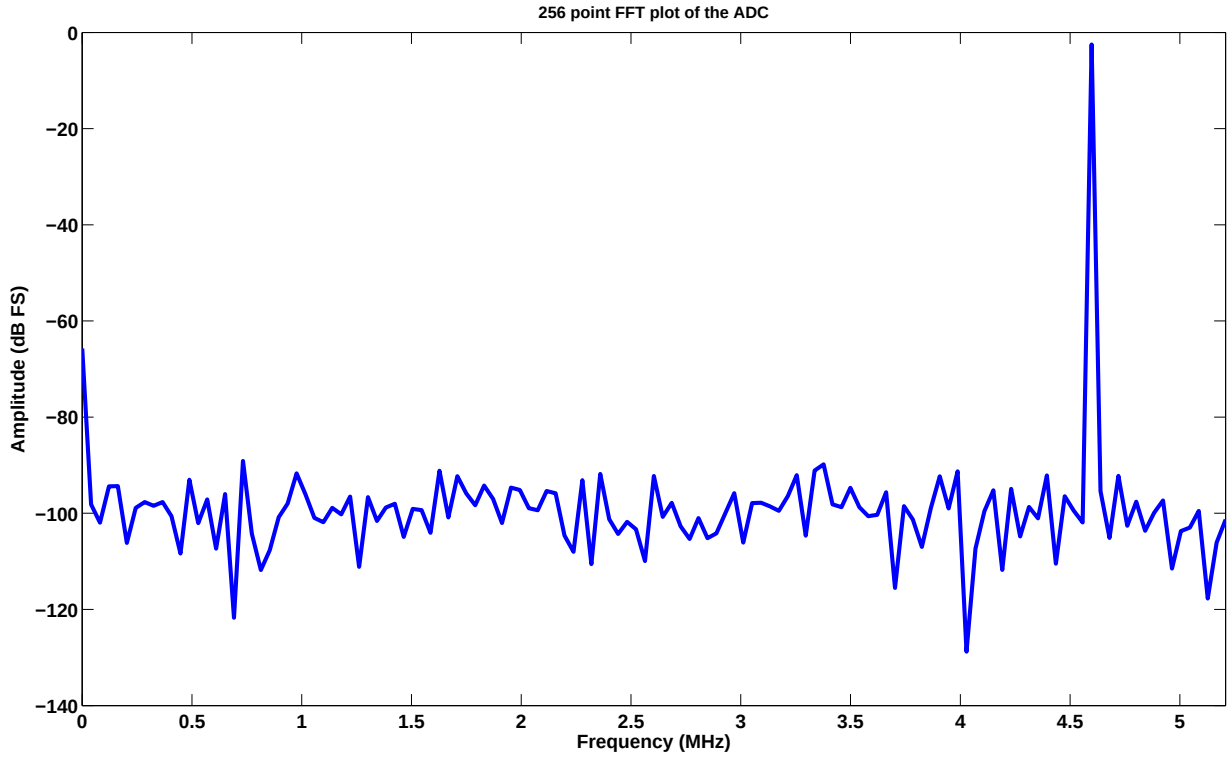
Therefore, the DSM and comparators are operating in different chips. However since they are not working simultaneously on one chip, measurements cannot be taken.

4.3.8 Summary

A 12-bit 10 MS/s algorithmic ADC is designed in a 130-nm CMOS process to validate the capacitor-shared and capacitor-scaled low power technique. The simulations results showed that the implemented ADC has the FOM of 60 fJ/conversion-step. The design parameters, layouts and device sizes are also described.



(a)



(b)

Figure 4.26: Simulated 256-point FFT plot at f_s = 10 MS/s: (a) f_{in} = 528.97 kHz and (b) f_{in} = 4.59 MHz.

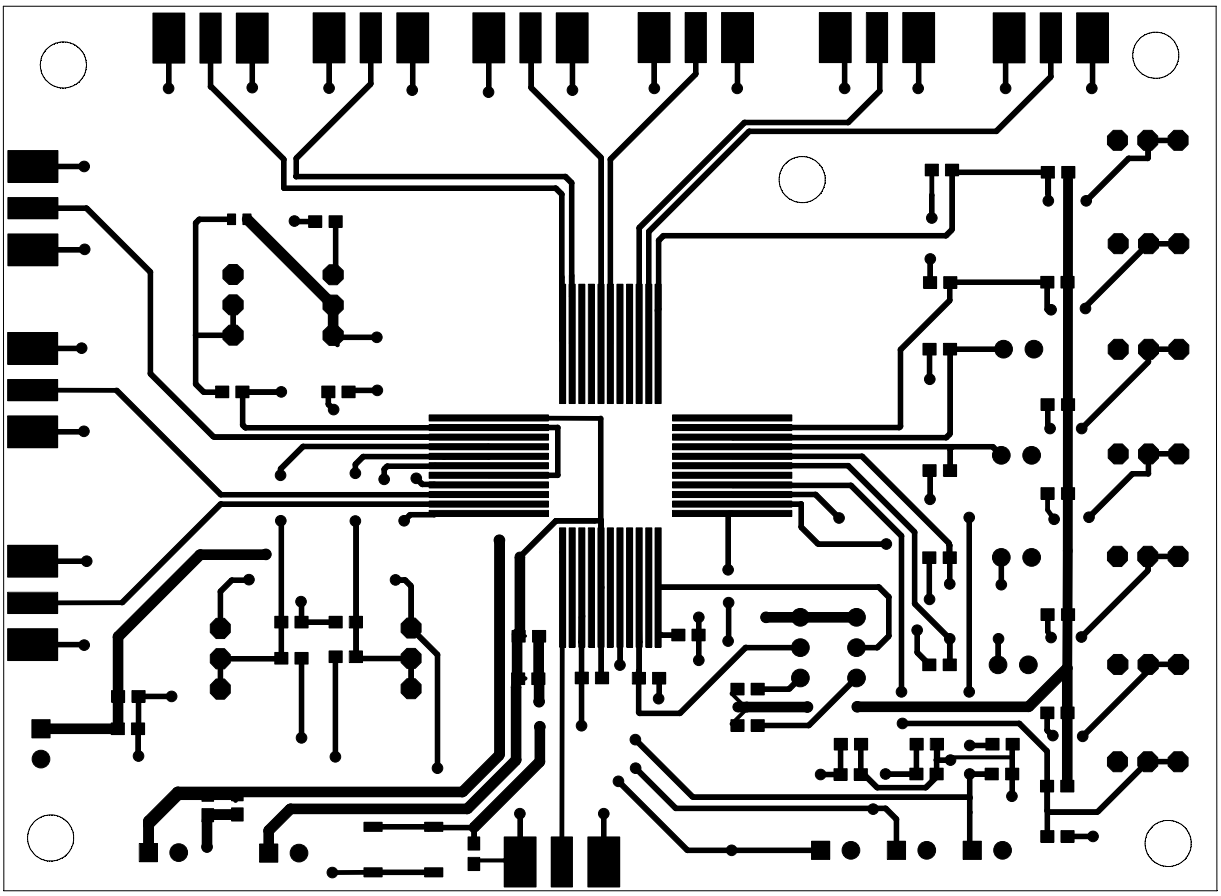


Figure 4.27: PCB layout of the top layer

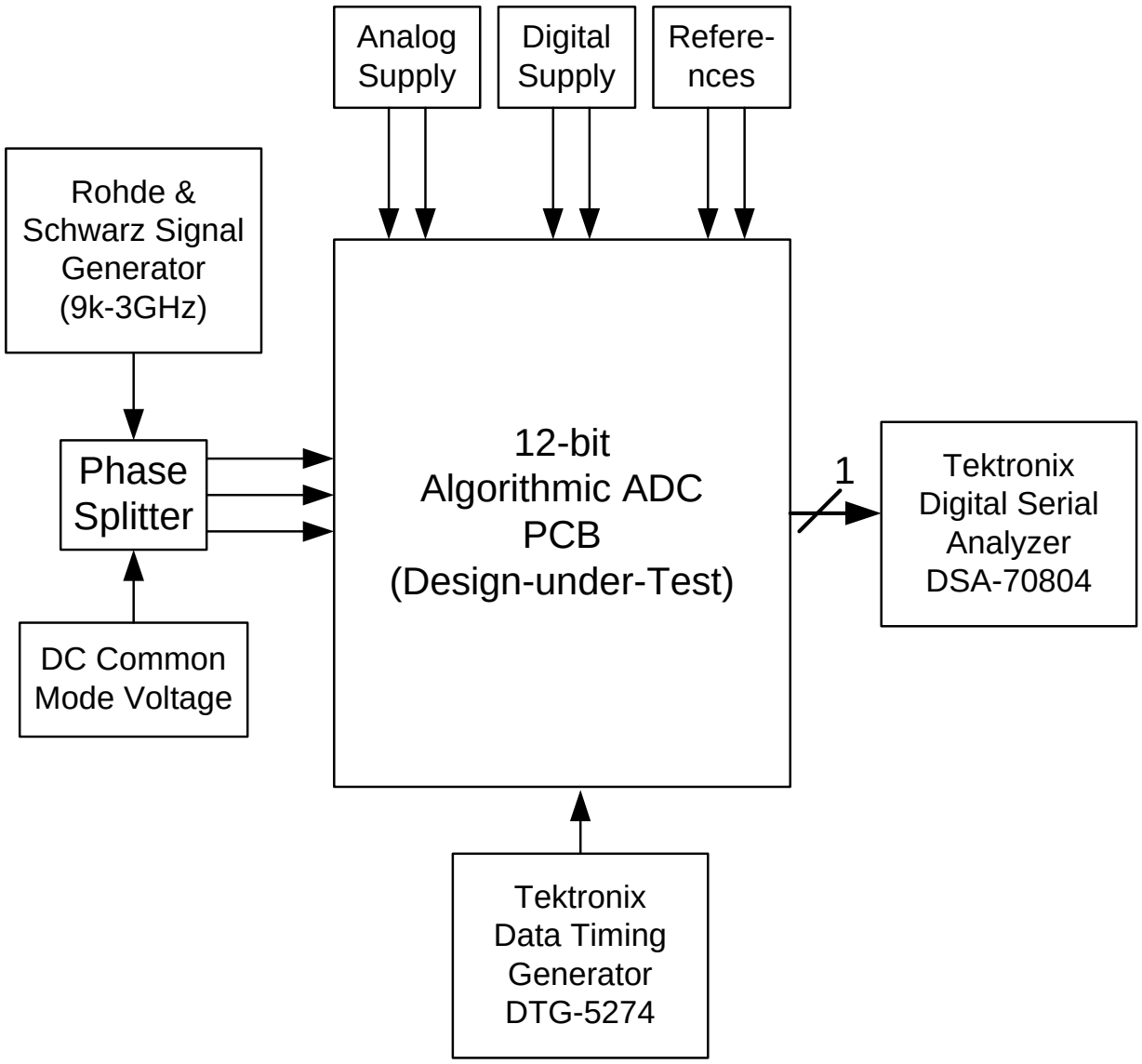


Figure 4.28: Test setup for the 12-bit Algorithmic ADC.

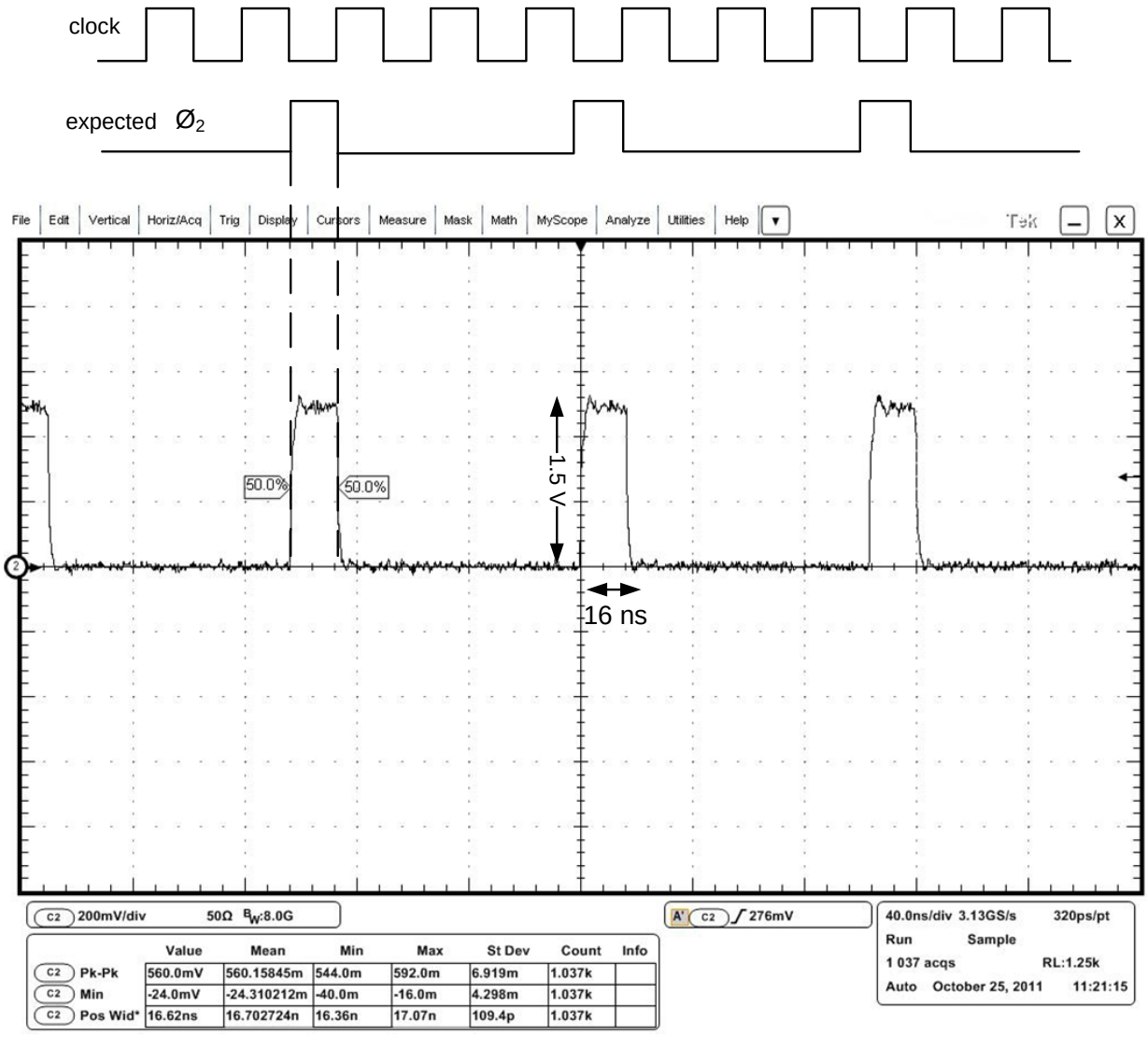


Figure 4.29: Expected and measured ϕ_2 phase indicating the operation of the DSM.

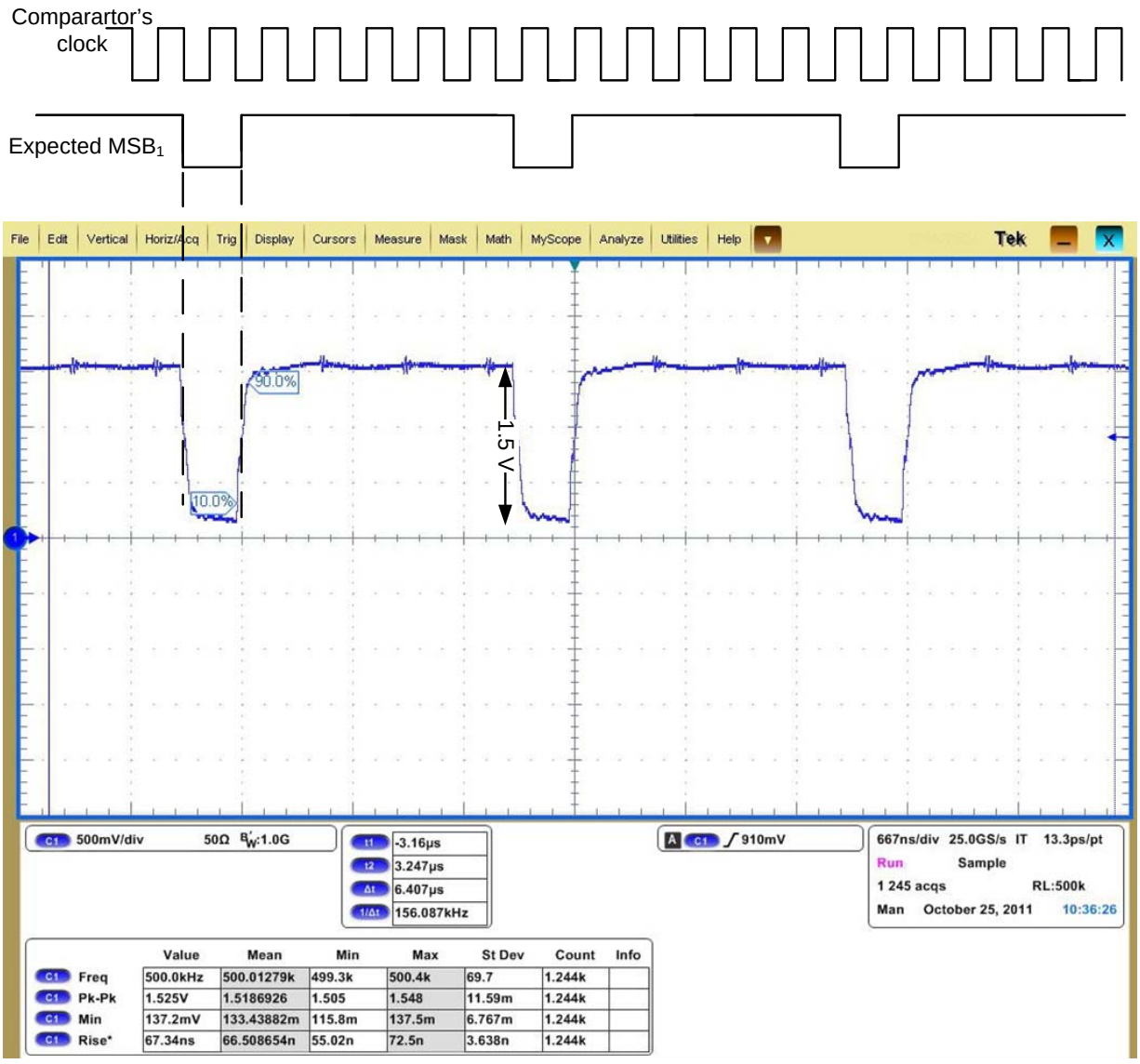


Figure 4.30: Expected and measured MSB when common-mode input is provided. MSB is measured after passing through an inverter buffer.

Chapter 5

Conclusions And Future Work

Algorithmic analog-to-digital converters (ADCs) are commonly used in portable, consumer, sensing, and biomedical applications where medium to high resolutions are required at moderate speeds with a minimum die area and power dissipation. The algorithmic ADC architecture is most closely related to the pipelined ADC architecture. Unlike pipelined ADCs where the residue voltage is propagated through successive stages, an N-bit algorithmic ADC utilizes the same hardware N-times for each bit of resolution. Due to the hardware reuse algorithmic ADCs are very area efficient. However, in terms of power efficiency, compared to that of pipelined ADCs, traditional algorithmic ADCs are inefficient. Pipelined ADCs have greatly benefited from interstage scaling [31], which is not directly applicable to algorithmic ADCs.

In this thesis, two promising low power techniques are presented. These techniques exploit capacitor-shared and capacitor-scaled schemes. In the 3-cap-shared technique, a modification of the capacitor arrangements of the flip-around configuration is proposed. It is demonstrated that the proposed technique can achieve more than an 85% power reduction, compared to the conventional scheme. A prototype chip is designed in a 130-nm CMOS process. The simulation results revealed that a 10-bit 5 MS/s algorithmic ADC, implementing the proposed 3-cap-shared technique, consumes about 150 μW of power.

The other proposed technique utilizes both capacitor-shared and capacitor-scaled schemes for algorithmic ADCs. In the proposed technique, the ADC is designed by using multiple U-MDAC blocks. Each U-MDAC consists of a unit-OTA and its associated pair of unit capacitances. In order to realize the power savings during each successive cycle, half of the unit-OTAs are powered down, along with the disconnection of their associated capac-

itors from the circuit. This technique reduces the power consumption of a conventional algorithmic ADC implementation by more than 90%. Simulation results indicated that a 12-bit 10 MS/s algorithmic ADC, based on the proposed U-MDAC approach, consumes about 1 mW of power.

In this thesis, a comparison of different energy efficient techniques for algorithmic ADCs is conducted. These techniques, when combined with each other, can lead to significant energy efficient solutions. Due to the added complexity of generating non-uniform clocks, the bias scaling appears to be the preferred solution, to combine with the proposed techniques, for power savings. A technique is developed that combines capacitor-shared, capacitor-scaled, OTA-shared, capacitor flip-around, and bias/phase scaling techniques to reduce the power consumption of a conventional algorithmic ADC by more than 93%.

This thesis also presents the detailed analysis of thermal noise in the proposed capacitor-shared and capacitor-scaled scheme. A relationship between the power dissipation and resolution of OTA-based capacitor-shared and capacitor-scaled algorithmic ADCs is presented as well. Furthermore, a detailed design procedure for the U-MDAC based algorithmic ADC is discussed.

5.1 Major Contributions

In this thesis, recent low power techniques are examined. Two different energy efficient techniques for algorithmic ADCs are proposed. In particular, the design technique of splitting an OTA into multiple unit-OTAs is investigated and proved it to be the most promising. The research contributions from this thesis are summed up as follows:

- **U-MDAC-based technique**
  A very low power technique is proposed that utilizes both the capacitor-shared technique and capacitor-scaled technique for algorithmic ADCs. In the proposed technique, the ADC is designed by using the U-MDAC approach, incorporating the OTA scaling and capacitor-scaled technique. Moreover, noise and low power limits are derived [71, 93].

- **3-cap-shared technique**
  A technique is proposed that utilizes a variation of the capacitor-shared technique. The novel technique requires only three capacitors in a single-ended implementation

circuit, compared to the four capacitors in a flip-around configuration and OTA-shared algorithmic ADC stage [93, 94].

- **Comparison of different low power algorithmic ADCs schemes**
  A comparative study of recently published low power techniques for algorithmic ADCs is conducted. These techniques are compared with each other in terms of their energy efficiency. It is shown that when these techniques are combined, energy efficient solutions are accomplished [94, 95].

- **Design procedure for U-MDAC-based algorithmic ADC**
  A step-by-step design methodology is demonstrated for designing unit-OTAs while utilizing current density (g_m/I_D)-based methodology

5.2 Future Work

Although the design is validated at the post-layout level, due to chip failures because of the lack of on-chip ESD circuits, the fabricated chips cannot be measured. In the future, it will be worthwhile to put ESD structures on-chip. At the research level, there are many aspects of this work that can be extended.

1. **Phase and bias scaling**
   The settling time requirements of an OTA relaxes after each successive bit resolution. As a result, bias and phase scaling can be incorporated in the design to further enhance the power efficiency of the proposed techniques.

2. **Calibration**
   There is an on-going trend to use digital calibration to ease analog circuits' design requirements. Since in U-MDAC approach, half of the unit-OTAs are not required, the idle OTAs can be used to generate digital outputs equivalent of the gain errors.

3. **OTA-less scheme**
   Since the OTA is the most power hungry block in a U-MDAC, the OTA-less circuit schemes, as presented in [65, 96], can be utilized to further decrease the power consumption of the ADC.

4. **Time-interleaving of low power low speed ADCs**
   Typically, pushing the design speeds to the technology limits results in a power

inefficient solution. Therefore, a more power efficient way is perform time interleaving of low speed highly energy efficient ADCs, such as the proposed ones, to come up with an energy efficient high speed time-interleaved ADC.

5. **Combining with sensing applications**
   Due to the attractive features of low power, high resolution and moderate speed, the proposed ADC can be readily integrated into a variety of sensor read-out circuits. Another promising area would be design sensors and data converters together to lower the cost of overall sensing system.

These possible avenues of future research can lead to significant power savings or performance enhancements.

Appendices

A.1 ADC Characteristics

Ideal ADCs

Ideal ADCs sample the analog input and quantize it to generate the digital output, as shown in Figure A.1. The analog signal is sampled at uniform time instants[1] and the sampled value is quantized to its corresponding digital code.

Understanding the operations of sampling and quantization is essential to understanding the overall operation of an ADC.

Sampling

The first task of an ADC is to sample the analog input signal. The input signal bandwidth and the sampling rate must meet the Nyquist criterion. The Nyquist criterion states that the input signal bandwidth must be lower than the half the sampling frequency. Assume, f_{in} is the input signal bandwidth and f_s is the sampling frequency, then

$$f_{in} < \frac{f_s}{2} \tag{A-1}$$

However, if the signal bandwidth is greater than $f_s/2$, then the discrete-signals overlap each other. This phenomenon is called aliasing. To avoid this signal overlapping, anti-aliasing filters are used to bandlimit the input signal to be quantized by an ADC.

Quantization

After sampling, the next task of an ADC is to convert the sampled data into its corresponding digital code. As shown in Figure A.2(a) , a range of analog signal values correspond to same digital code. This approximation or rounding effect in ADCs is called quantization.

Due to quantization, the smallest change in the analog input causing a change in the digital output is called the ADC resolution. The resolution is often expressed in LSB or V_{LSB}. V_{LSB} is defined as

$$V_{LSB} = \frac{V_{FS}}{2^N} \tag{A-2}$$

Where N is the number of ADC bits and V_{FS} is the full scale range of the ADC.

[1] Assuming uniform sampling.

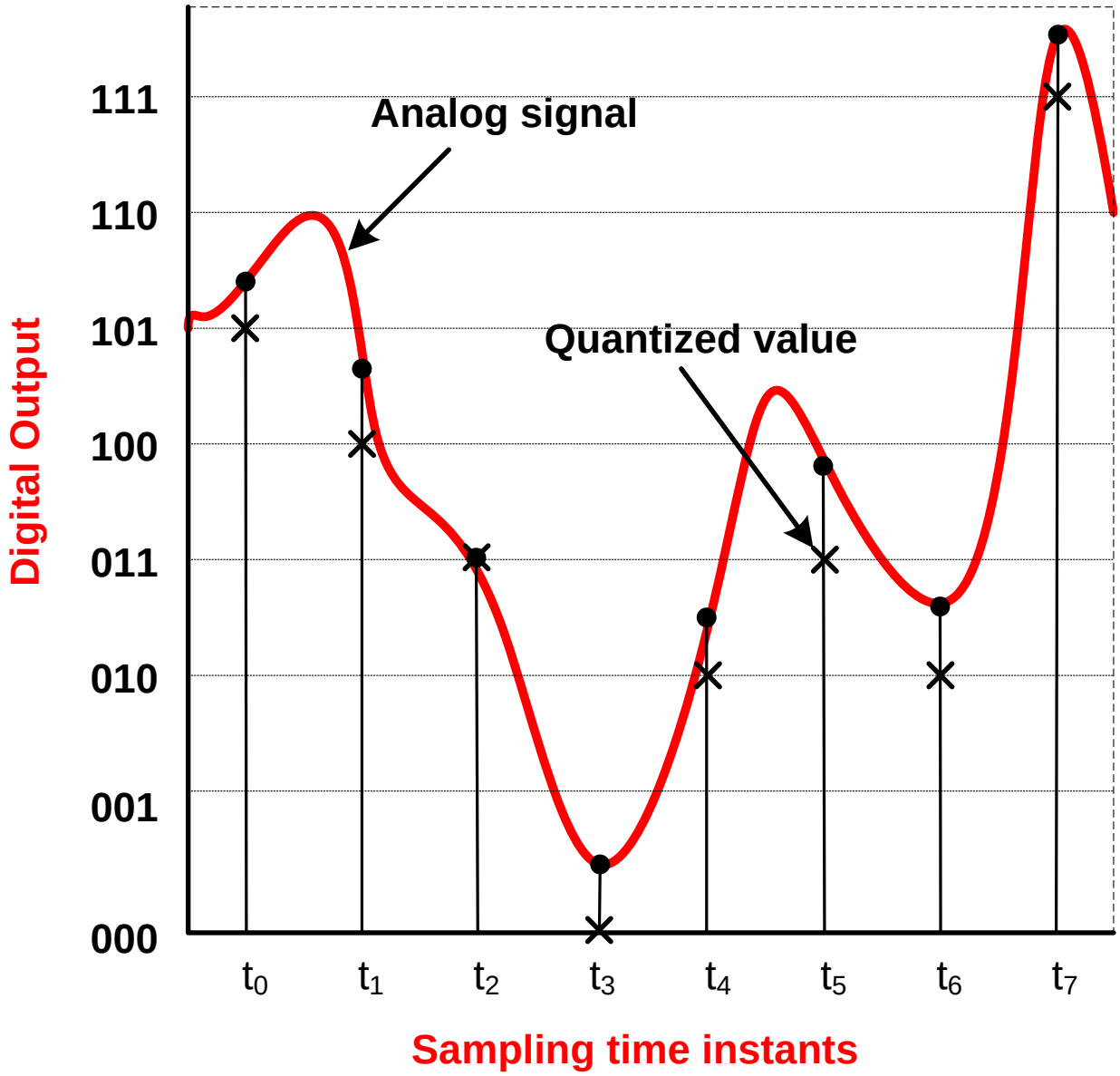
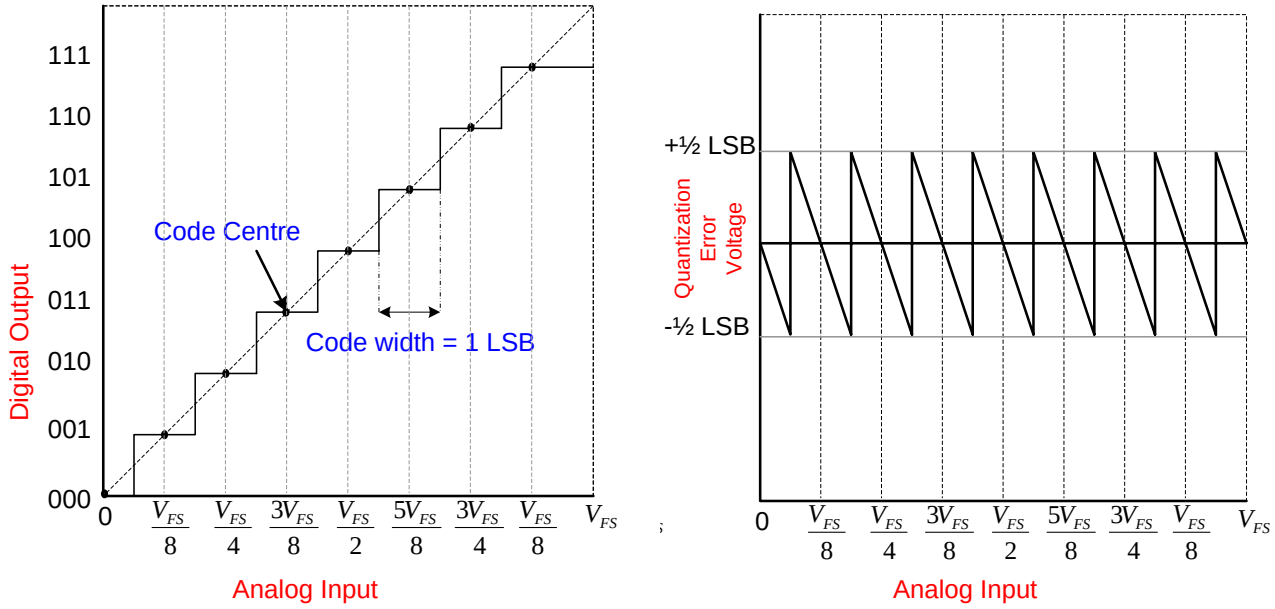


Figure A.1: Basic operation of an ADC; Sampling and Quantization

The quantization process introduces an error into the output of the ADC. This error, denoted as ε, is called quantization noise and it is the difference between the original analog input and the digitized output. Hence, a signal $x = x_j \pm \varepsilon$ will be quantized as x_j if $\varepsilon < V_{LSB}/2$, that is, the error never exceeds $V_{LSB}/2$. The quantization error for an ideal 3-bit ADC is shown in Figure A.2(b).

In an ideal ADC, this quantization noise decreases the signal-to-noise ratio (SNR). SNR



(a) (b)

Figure A.2: (a) 3-bit ADC characteristic and (b) Quantization error for the ideal 3-bit ADC.

is the ratio of the power of a full-scale input signal to the quantization noise power present at the output of a converter. The SNR is given by

$$SNR_{ideal-ADC} = 20\log\left(\frac{\text{RMS Signal Voltage}}{\text{RMS Quantization Noise Voltage}}\right) \text{ (dB)} \qquad \text{(A-3)}$$

An expression for the SNR in such a system can be easily derived if a uniform probability density function (PDF) for ε is assumed over $\pm V_{LSB}/2$. Therefore the quantization noise power is calculated as

$$v_{qns}^2 = \frac{1}{V_{LSB}} \int_{-\frac{V_{LSB}}{2}}^{+\frac{V_{LSB}}{2}} \varepsilon^2 d\varepsilon = \frac{1}{12} V_{LSB}^2 \qquad \text{(A-4)}$$

For a full scale sinusoid signal the SNR is calculated, as shown in Equation A-5 [43].

$$SNR = 20\log_{10}(2^N\sqrt{1.5}) = 6.02N + 1.76 \text{ (dB)} \qquad \text{(A-5)}$$

Equation A-5 shows that each additional ADC bit improves SNR by approximately 6 dB.

In summary, an ideal ADC samples and quantizes the analog input signal. The only noise source in an ideal ADC is the quantization noise. The sample rate determines the

signal bandwidth and the quantization determines the SNR. For ideal ADCs, these are the only specifications.

Real ADCs

The performance of a real ADC is degraded due to the non-idealities of the electronic components from which the ADC is made. The non-idealities include component matching, circuit noise and non-linearities in the circuits. The effect of these non-idealities lead to the need for additional ADC specifications, which is categorized into static and dynamic specifications.

Static specification

The input-output transfer characteristic, as shown in Figure A.2, depicts the static behavior of an ideal 3-bit ADC. However, in real ADCs, circuit imperfections cause errors known as offsets, gain, Differential Nonlinearity (DNL) and Integral Nonlinearity (INL) errors. These errors are discussed below.

Offset errors: The offset error is the deviation of the transfer characteristics of an ideal ADC at zero input. This error affects all codes by the same amount. Offset errors can be easily trimmed by calibration.

Gain errors: The slope of the ADC's transfer characteristic is the line interpolating the transfer characteristic. The deviation of the actual and ideal slopes is called the gain error. Like offset errors, gain errors can be easily calibrated.

Differential non-linearity (DNL): DNL is the deviation of the individual code widths from their ideal value of 1 LSB. DNL is expressed as follows

$$DNL(k) = \frac{[\text{step size of code (k)}] - V_{LSB}}{V_{LSB}} \tag{A-6}$$

Integral non-linearity (INL): INL is the deviation of code centers from their ideal values. INL is also the integral of the DNL from code zero to the code of interest, code i, and is given as

$$INL(k) = \sum_{i=0}^{K} DNL(i) \tag{A-7}$$

In summary, the above four parameters characterize the static specifications of Nyquist ADCs. Static specifications can be tested at very low speeds or even constant voltages. Offset and gain errors are linear errors, whereas, DNL and INL are nonlinear errors.

Dynamic specification

Real ADCs are also limited by the dynamic characteristics of the circuits from which the ADCs are built. An illustration of these errors is shown in Figure A.3. These limitations are due to noise and distortion. There are numerous dynamic performance measures out of which the most common are the signal-to-noise ratio (SNR),the spurious free dynamic range (SFDR), the signal-to-noise and distortion ratio (SNDR or SINAD) and the effective number of bits (ENOB).

Signal-to-noise ratio (SNR): The SNR is the ratio of the power of a full-scale input signal to total noise power present at the output of a converter. The quantization noise and the circuit noise are included in the SNR, but harmonics of the signal are excluded. Hence

$$SNR = 10\log\left(\frac{\text{Signal Power}}{v_{qns}^2 + v_{circuit\_noise}^2}\right) \text{ (dB)} \tag{A-8}$$

Total harmonic distortion (THD): Total harmonic distortion (THD) is defined as the ratio between the RMS sum of the harmonic components and the amplitude of the input signal. THD is given by

$$THD = \frac{\sqrt{\sum_{i=2}^{j} A^2(i.F_{in})}}{A(f_{in})} \tag{A-9}$$

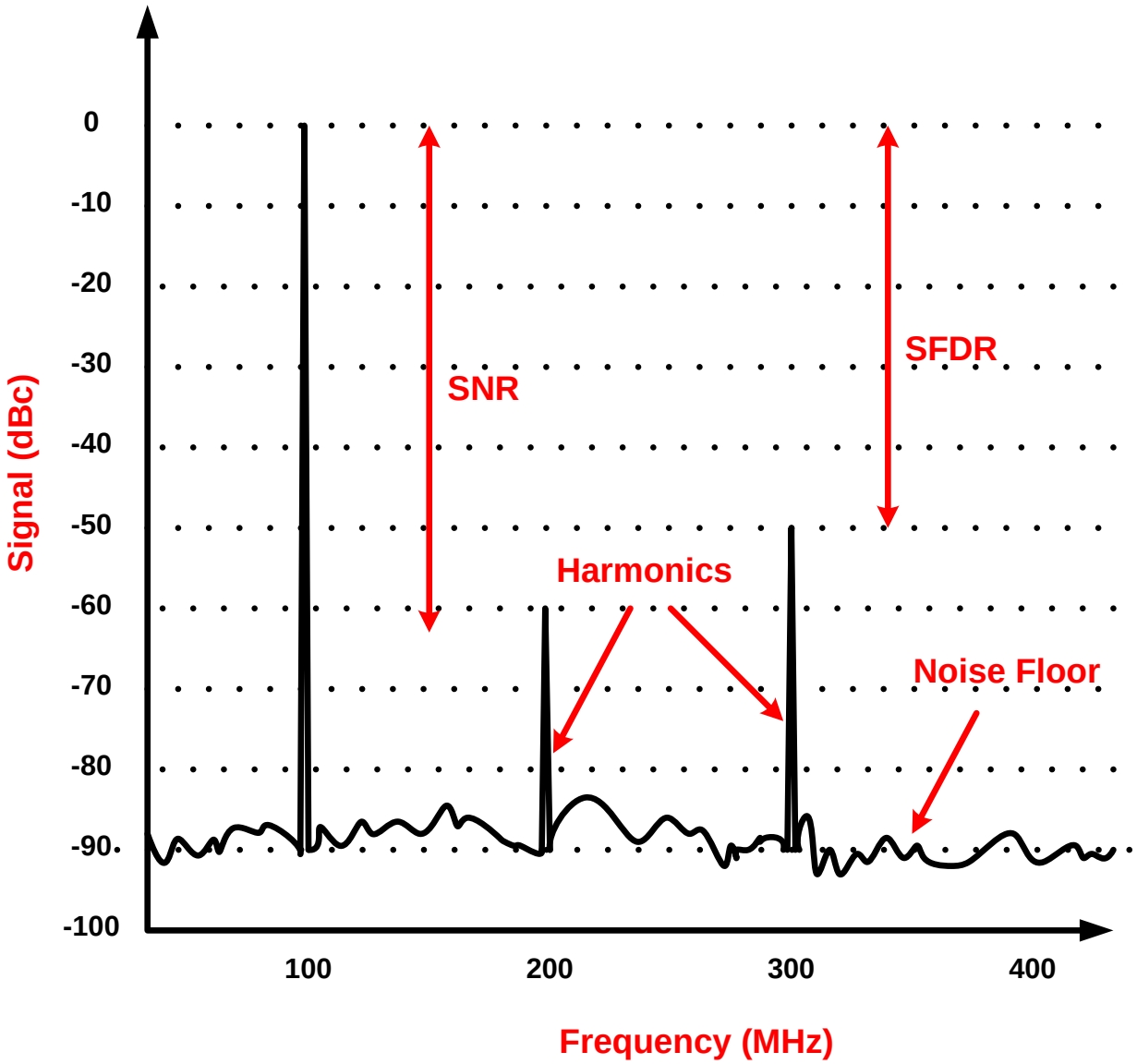


Figure A.3: Frequency domain characterization for 10-bit pipelined ADC (2048 point FFT).

where $A(f_{in})$ is the amplitude of the fundamental input signal and $A(i.F_{in})$ is the amplitude of the i^{th} harmonic and (j) is the number of harmonics considered. Typically first seven harmonics are considered.

Spurious free dynamic range (SFDR): The SFDR is defined as the ratio between the maximum amplitude of the input signal and the amplitude of the next largest spectral

component, as shown in Figure A.3. The SFDR can be less than or greater than the SNR. The SFDR is an important specification in telecommunication applications.

Signal to noise and distortion ratio (SNDR): The SNDR is the ratio between the power of the full scale input signal and the total noise including harmonics and other distortion components and can be written as

$$SNDR = 10 \log \left(\frac{\text{Signal Power}}{\text{Total Noise and Distortion Power}} \right) \text{ (dB)} \qquad \text{(A-10)}$$

SNDR is always less than or equal to SNR. It is also frequently expressed as SINAD.

Effective resolution bandwidth (ERBW): For low input frequencies, the SNDR is more or less constant, but as the input frequency increases, the SNDR decreases. The effective resolution bandwidth (ERBW) is defined as the input frequency at which the system SNR is reduced by 3 dB (or LSB/2) with respect to the SNDR at low frequencies. The ERBW can be less than or greater than Nyquist rate.

Effective number of bits (ENOB): In real ADCs, the SNDR is always less than 6.02N + 1.76 dB. This reduced resolution is captured by expressing the SNDR in terms of effective bits or ENOB. These bits are called Effective Bits. The ENOB is given as

$$ENOB = \frac{SNDR - 1.76}{6.02} \text{ (Bits)} \qquad \text{(A-11)}$$

ENOB is always less than N. For low resolutions, ENOB is approximately equal to N. For low power high resolution ADCs, ENOB is 1 or 2 bits less than N.

In summary, the specifications discussed above are frequently used to characterize real ADCs. The choice of a specification is often application dependant. For example, in voice and speech communication, low resolution low speed ADCs are used and SNDR is the only important specification. Whereas in video and wireless communications, ADCs must deliver high levels of performance in terms of SNR, SNDR and SFDR. In Radar applications, high SFDR and SNDR ADCs are required to prevent weak signals from being masked by harmonics or spurs. Imaging applications need high INL and high DNL ADCs.

A.2 Optimum Scaling Factor Analysis for Pipelined ADCs

In order to quantify both the capacitor scaling and stage resolution, a detailed analysis on choosing the optimum stage resolution and the scaling factor is presented. This analysis is similar to the one presented by Cline-Gray [31]. Initially, the relationship between the power consumption of the whole pipelined ADC and the scaling factor and stage resolution will be derived. Then from that relation, the optimum scaling factor will be found. The optimum stage resolution will be found by utilizing this optimum scaling factor.

In a simplified model, it can be assumed that the dominant noise source in a power optimized pipelined stage is inversely proportional to the sampling capacitor of that stage (kT/C noise). Typically, the capacitors are scaled from one stage to another by a scaling factor n_f, where $\gamma = \frac{C_{I+1}}{C_I}$, as shown in Figure A.4. Here C_u is the unit capacitance and M is the bit resolution of the individual stage and I is the total number of stages in the pipelined ADC. Under these assumptions, the total input referred noise is proportional to

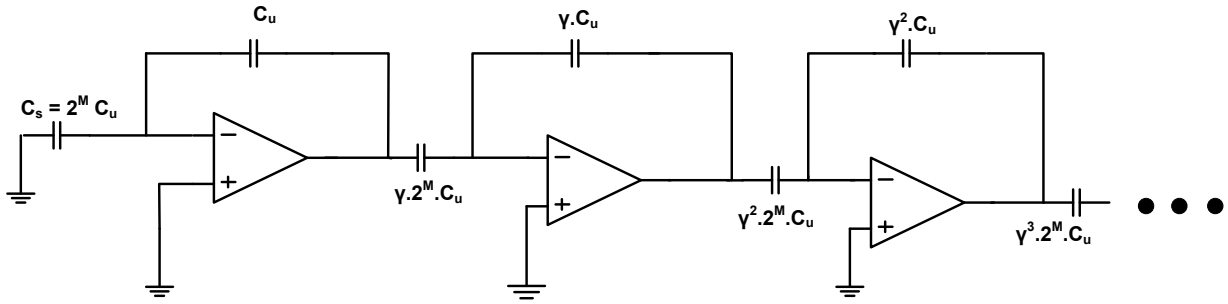


Figure A.4: Capacitor scaled stages. Each stage resolves M bits and the sampling capacitor of each successive pipelined stage is reduced by the scaling factor γ.

the weighted sum of the reciprocals of the sampling capacitors scaled by the factor γ^{I-1} with respect to the sampling capacitor of first stage, where I is the current stage. As a result, input referred noise can be written as

$$\overline{v}_{n,in}^2 \propto kT\left[\frac{1}{2^M C_u} + \frac{1}{\gamma\cdot 2^M C_u\cdot 2^{2M}} + \frac{1}{\gamma^2\cdot 2^M C_u\cdot 2^{4M}} + \cdots\right] \quad \text{(A-12)}$$

$$\propto \frac{kT}{2^M\cdot C_u}\left[1 + \frac{1}{\gamma\cdot 2^{2M}} + \frac{1}{\gamma^2\cdot 2^{4M}} + \cdots + \frac{1}{\gamma^{I-1}\cdot 2^{2(I-1)M}}\right] \quad \text{(A-13)}$$

$$\propto \frac{kT}{2^M\cdot C_u}\left[\frac{1-\left(\frac{1}{\gamma\cdot 2^{2M}}\right)^I}{1-\left(\frac{1}{\gamma\cdot 2^{2M}}\right)}\right] = \frac{kT}{C_s}\left[\frac{1-\left(\frac{1}{\gamma\cdot 2^{2M}}\right)^I}{1-\left(\frac{1}{\gamma\cdot 2^{2M}}\right)}\right] \quad \text{(A-14)}$$

This is the input referred noise of I-stages, where each stage resolves M-bits.

As already assumed, the power consumption of a pipelined ADC is dominated by the OTA power consumption, hence, it is reasonable to say that

$$\text{Power}(P) \propto \frac{\text{Load Capacitance}}{\text{Feedback Factor}(\beta)} \times \text{Number of stages}$$

where, $\beta = \frac{1}{1+2^M}$ for the each stage. Consequently, the power consumption of the whole pipelined ADC can be given as

$$Power \propto \overbrace{\left(1+2^M\right)}^{1/\beta} \overbrace{\left(2^M C_u\right)\left(\gamma + \frac{1}{1+2^M}\right)}^{\text{Load Capacitance } C_L} \overbrace{\left(1+\gamma+\gamma^2+\gamma^3\cdots+\gamma^{I-1}\right)}^{\text{Capacitor scaling}} \quad \text{(A-15)}$$

$$\propto \left(1+2^M\right)\left(2^M C_u\right)\left(\gamma + \frac{1}{1+2^M}\right)\left(\frac{1-\gamma^I}{1-\gamma}\right) \quad \text{(A-16)}$$

Since stage scaling increases the noise contribution from the later stages, the power consumption must be increased to keep the same SNR. Therefore, combining Equation A-14 and A-16.

$$Power \propto 2^M(1+2^M)\left(\gamma + \frac{1}{1+2^M}\right)\left(\frac{1-\gamma^I}{1-\gamma}\right)\left(\frac{1-\left(\frac{1}{\gamma\cdot 2^{2M}}\right)^I}{1-\left(\frac{1}{\gamma\cdot 2^{2M}}\right)}\right)\cdot C_u \quad \text{(A-17)}$$

Also, the size of the unit sampling capacitor, C_u, of an M-bit stage can be 2^{1-M} times the unit sampling capacitor of a 1-bit stage while meeting the thermal noise requirements. This unit-capacitor-factor, ξ, is defined as $\xi = \frac{2}{2^M} = 2^{1-M}$. So, the above equation becomes

$$Power \propto 2^M(1+2^M)\left(\gamma + \frac{1}{1+2^M}\right)\left(\frac{1-\gamma^I}{1-\gamma}\right)\left(\frac{1-\left(\frac{1}{\gamma\cdot 2^{2M}}\right)^I}{1-\left(\frac{1}{\gamma\cdot 2^{2M}}\right)}\right)\left(2^{1-M}\right)\cdot C_u \quad \text{(A-18)}$$

Equation A-18 shows the relationship between the ADC's power consumption and the scaling factor and the stage resolution.

As defined in the Cline-Gray model [31], a term taper-factor (x) is introduced here, which relates to the scaling factor by the equation $\gamma = \frac{1}{2^{Mx}}$. Hence Equation A-18 can be

written as

$$Power \propto 2^M(1+2^M)\left(2^{-Mx}+\frac{1}{1+2^M}\right)\left(\frac{1-2^{-IMx}}{1-2^{-Mx}}\right)\left(\frac{1-2^{IM(x-2)}}{1-2^{M(x-2)}}\right)\left(2^{1-M}\right) \quad \text{(A-19)}$$

Equation A-19 shows the relationship among the ADC's power consumption, the taper factor and the stage resolution. This equation is similar to the one derived in [31], but they have not included the effect of the feedback factor, and they assumed that I is infinite. Also this analysis is done considering regular pipelined stages, whereas [31] analyzed the flip-around scheme.

The power dissipation of an infinite pipelined ADC is plotted in Figure A.5. For the

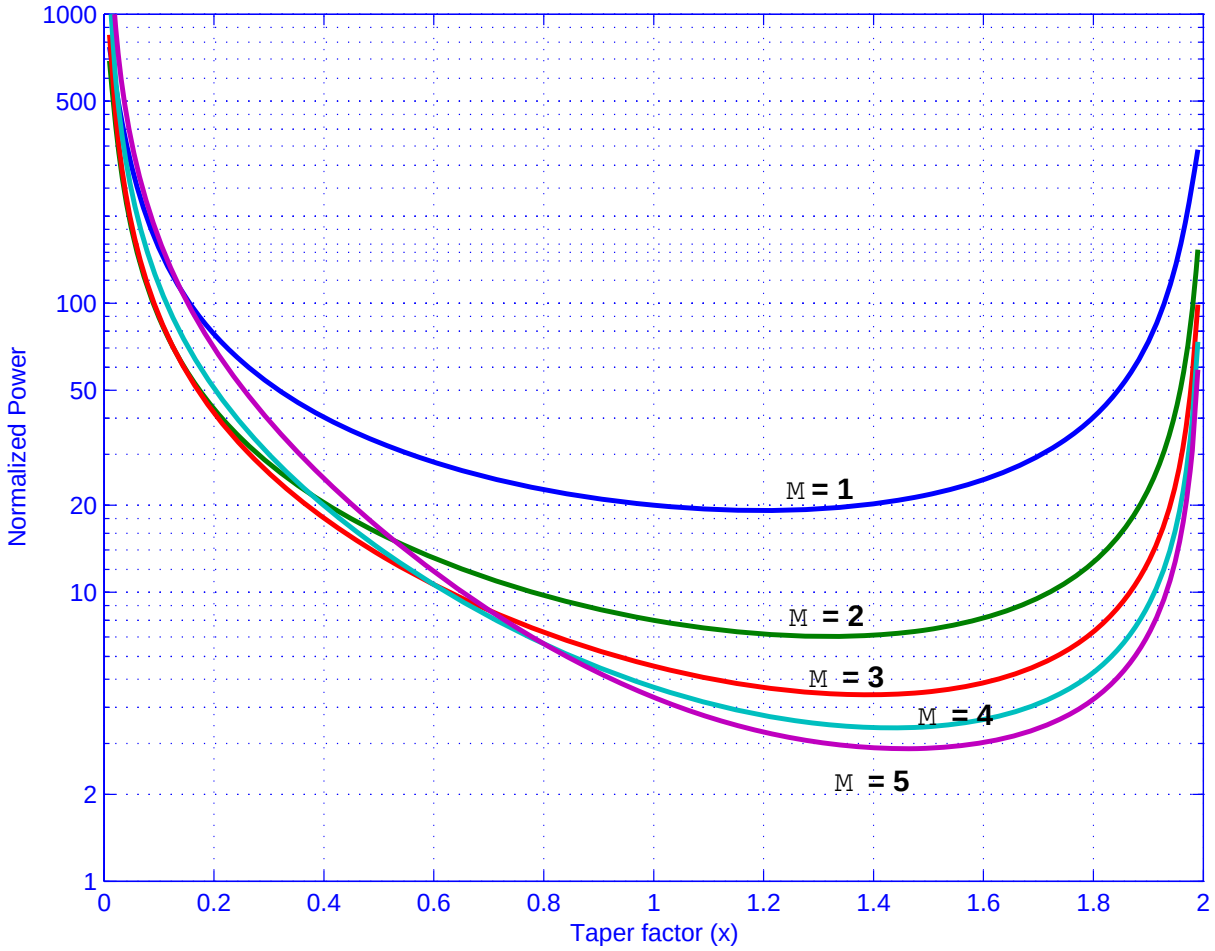
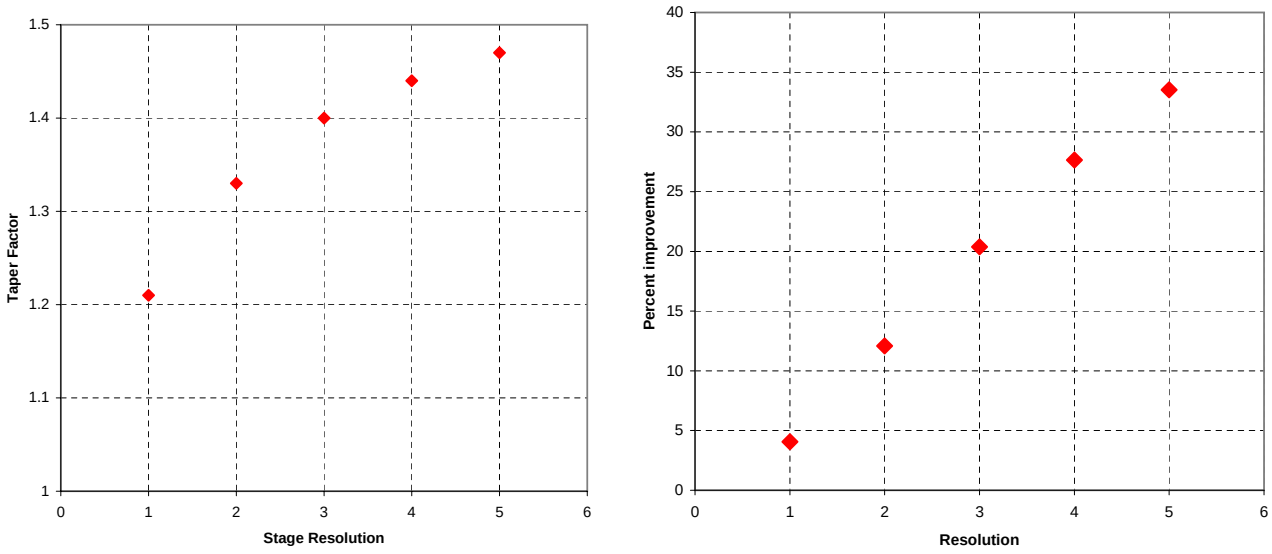


Figure A.5: Normalized power versus the taper factor

M=1 case, significant power savings are possible due to capacitor scaling. The optimum

scaling factor γ_{opt} is approximately equal to the reciprocal of the interstage gain of the pipelined stage, that is, the optimal taper factor x_{opt} is equal to one. In a typical pipelined ADC, when no capacitor scaling is utilized, then power dissipation of the whole pipeline ADC is proportional to the N times the power consumption of the first stage. In contrast, when the optimal scaling factor is used then the power of the whole ADC is proportional to two times the power consumption of the first stage. However, due to scaling, the power consumption of the first stage must be increased, therefore, the total power saving is around 70%, and not 80% as might be expected.

The optimum scaling factor is plotted against the per stage bit resolution in Figure A.6(a). It can be seen that x_{opt} is between 1 and 1.5, and the scaling factor increases with the increase in stage resolution. The relative power consumption between using the optimal taper factor and the taper factor of reciprocal of the stage gain is plotted in the Figure A.6(b). The power improvement is not significant in lower resolution stages, however, this power improvement increases for higher stage resolutions.



(a) (b)

Figure A.6: (a) Optimum scaling factor versus stage resolution (M) (b) Relative power improvement when optimum taper factor is used against when the taper factor as the reciprocal of the stage gain is used.

Once the optimal taper factor is found, it is possible to find the optimal stage resolution assuming the optimal taper factor is used. Figure A.7 shows the total pipeline power consumption versus the bits resolution per stage (assuming the same number of bits in all

stages). From the figure, it can be seen that large power savings are possible when going from one bit per stage to two bits per stage.

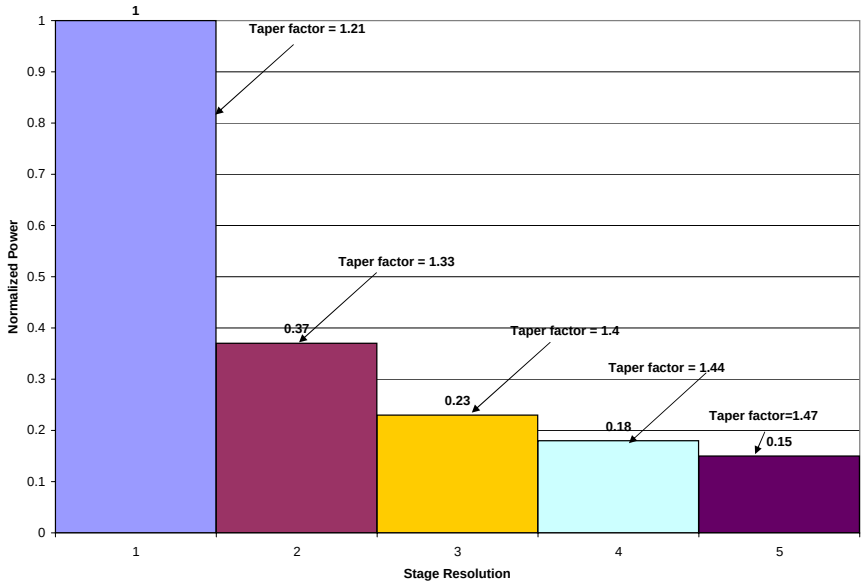


Figure A.7: Normalized power versus the stage resolution. Here optimum taper factor of each stage resolution is used

In summary, a relationship between power dissipation of a pipelined ADC and optimum capacitor scaling factor is derived. It is shown that the optimal scaling factor is slightly different from the reciprocal of the interstage gain. Although power improvements are not very high in lower per stage resolution, the power improvements is significant when more than 3-bit/stage resolutions are used. Furthermore, it is shown that large power savings are possible when going from one bit per stage to two bits per stage.

A.3 Derivation of Minimum Sampling Power

Fundamentally, all ADCs must sample the analog signal, and the accuracy of the sampled signal must be enough to meet the SNR requirement. In practical circuits, the analog signal is sampled on the capacitor along with the thermal noise. By increasing the capacitor size, the relative SNR is improved. Therefore, one should size the sampling capacitor for the desired SNR, then the power required to charge the sampling capacitor at the required

rate will limit the minimum power dissipation. The sampling noise is given as

$$\overline{v}_{ns}^2 = \frac{kT}{C_s} \tag{A-20}$$

where C_s is the sampling capacitor. For a supply voltage of V_{FS}, the maximum sinusoidal power is

$$v_s^2 = \frac{V_{FS}^2}{8} \tag{A-21}$$

which gives a SNR of

$$SNR^2 = \frac{v_s^2}{\overline{v}_{ns}^2} = \frac{V_{FS}^2 \cdot C_s}{8kT} \tag{A-22}$$

Hence, one can determine the required C_s for any desired SNR and V_{FS} as:

$$C_s = \frac{8kT \cdot SNR^2}{V_{FS}^2} \tag{A-23}$$

Therefore, in order to double the SNR (6 dB), four times the C_s is required. Also, when the supply voltage is reduced to half, then four times the sampling capacitor is required again.

To charge a capacitor to full scale voltage V_{FS} requires a charge of

$$Q = C_s \cdot V_{FS} \tag{A-24}$$

If this is done at a sample rate of f_s, the average current will be given by

$$I = f_s \cdot C_s \cdot V_{FS} \tag{A-25}$$

which yields a minimum power of

$$P_s = I \cdot V_{FS} = f_s \cdot C_s \cdot V_{FS}^2 \tag{A-26}$$

to sample a signal. By substituting (A-23) for C_s, the fundamental power required to sample a signal for any desired SNR is found to be[1]

$$P_s = 8kT \cdot f_s \cdot SNR^2 \tag{A-27}$$

[1]In practice the signal is not always at V_{FS}, so the power consumption is reduced some what. The amount of the reduction depends on the characteristics of the signal. For a pure sine wave, (A-26) should be scaled by $1/\sqrt{2}$.

However,

$$SNR^2 = 1.5 \cdot 2^{2N} \tag{A-28}$$

Therefore, (A-27) becomes

$$P_s = 12kT \cdot f_s \cdot 2^{2N} \tag{A-29}$$

The above equation states that the power consumption in an ADC is proportional to 2^{2N}, and the sampling frequency. Note that, (A-29) is technology independent and sets the lower bound for any sampling based ADC.

A.4 Layouts and Device Sizes

In this section, designed layouts and devices's sizes are provided. The complete Spectre schematic of the 12-bit 10 MS/s ADC is presented in Figure A.8

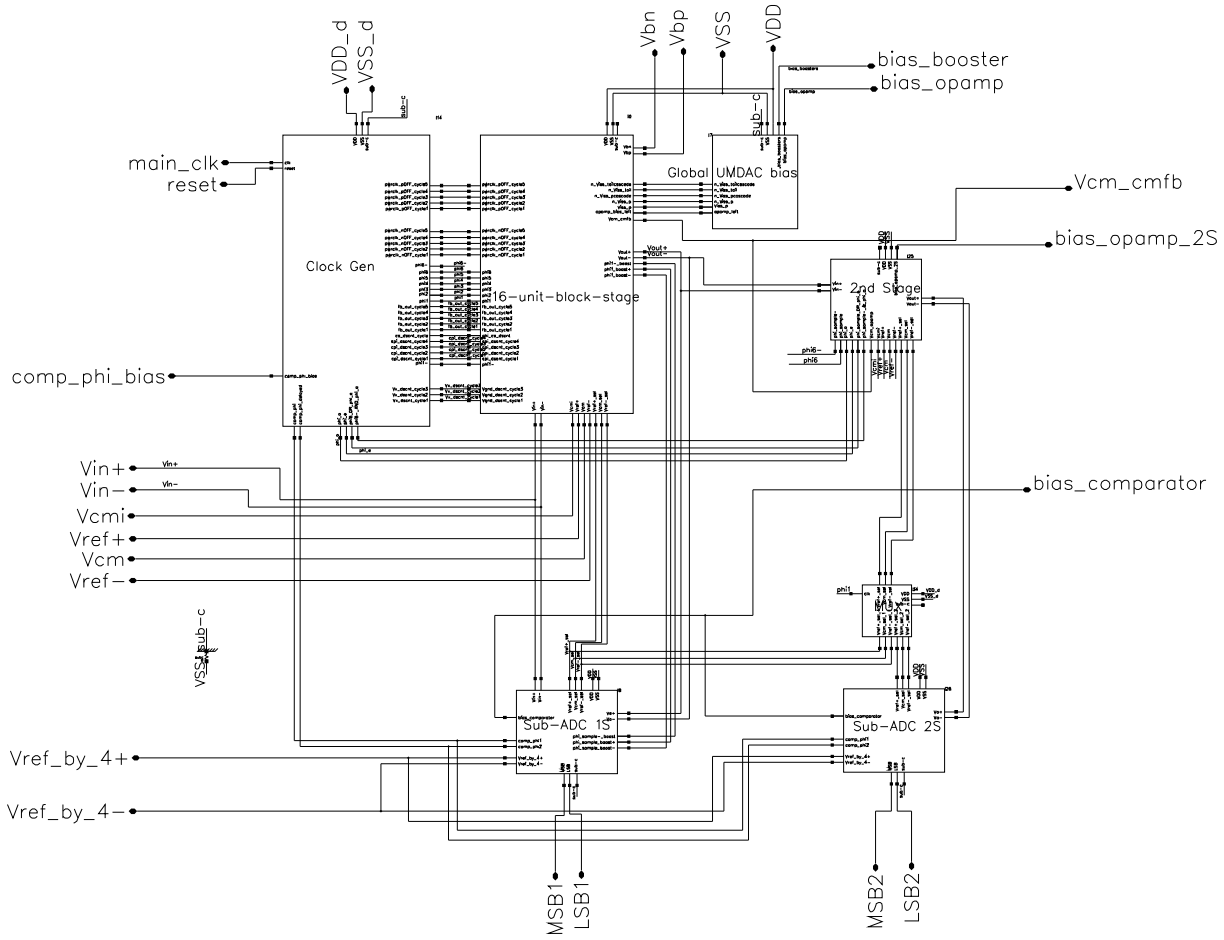


Figure A.8: Complete Spectre schematic of the 12-bit 10 MS/s ADC.

U-MDAC layout

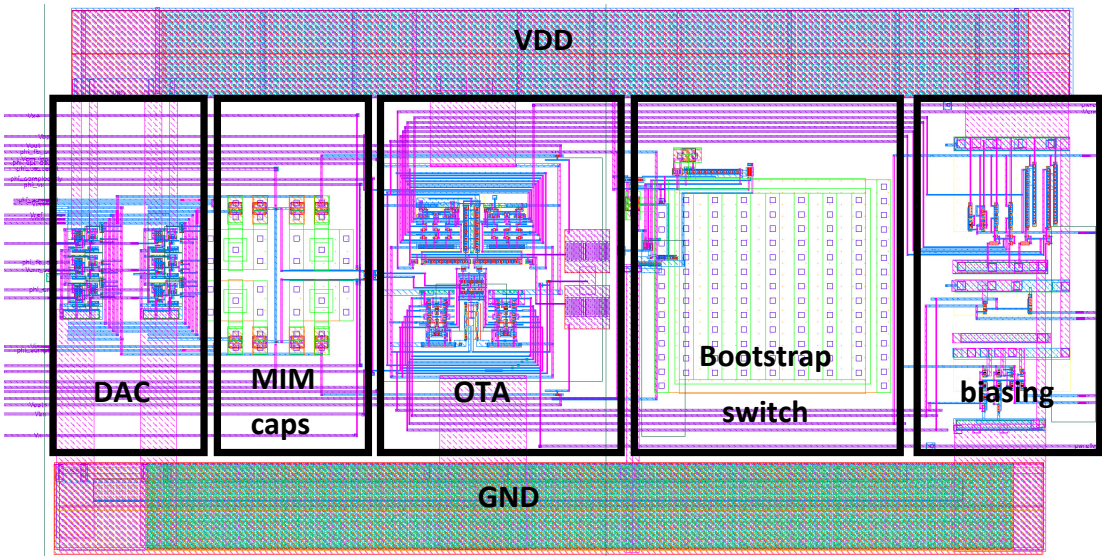


Figure A.9: Layout of the U-MDAC's stage.

2^{nd} stage layout

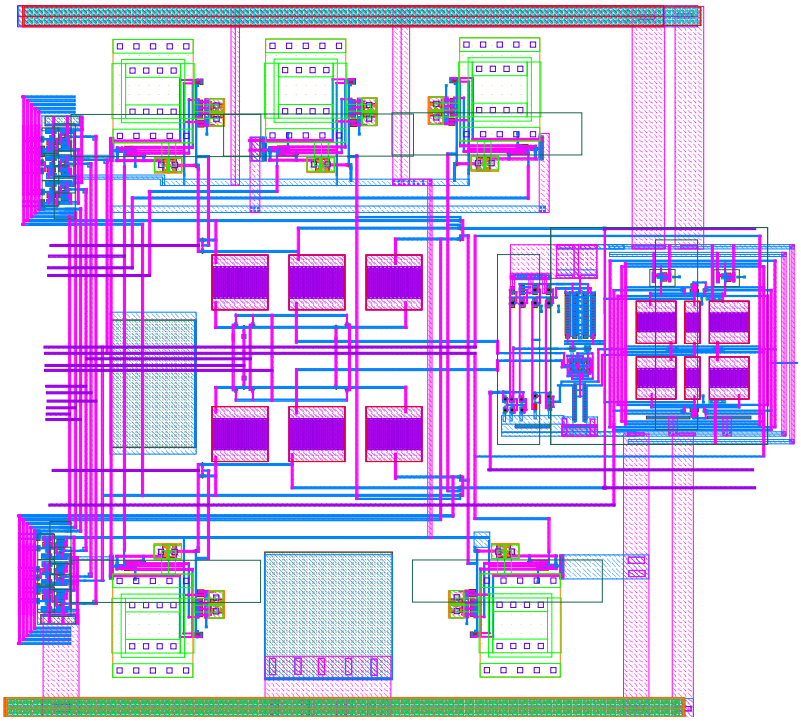


Figure A.10: Layout of the second stage.

Comparator layout

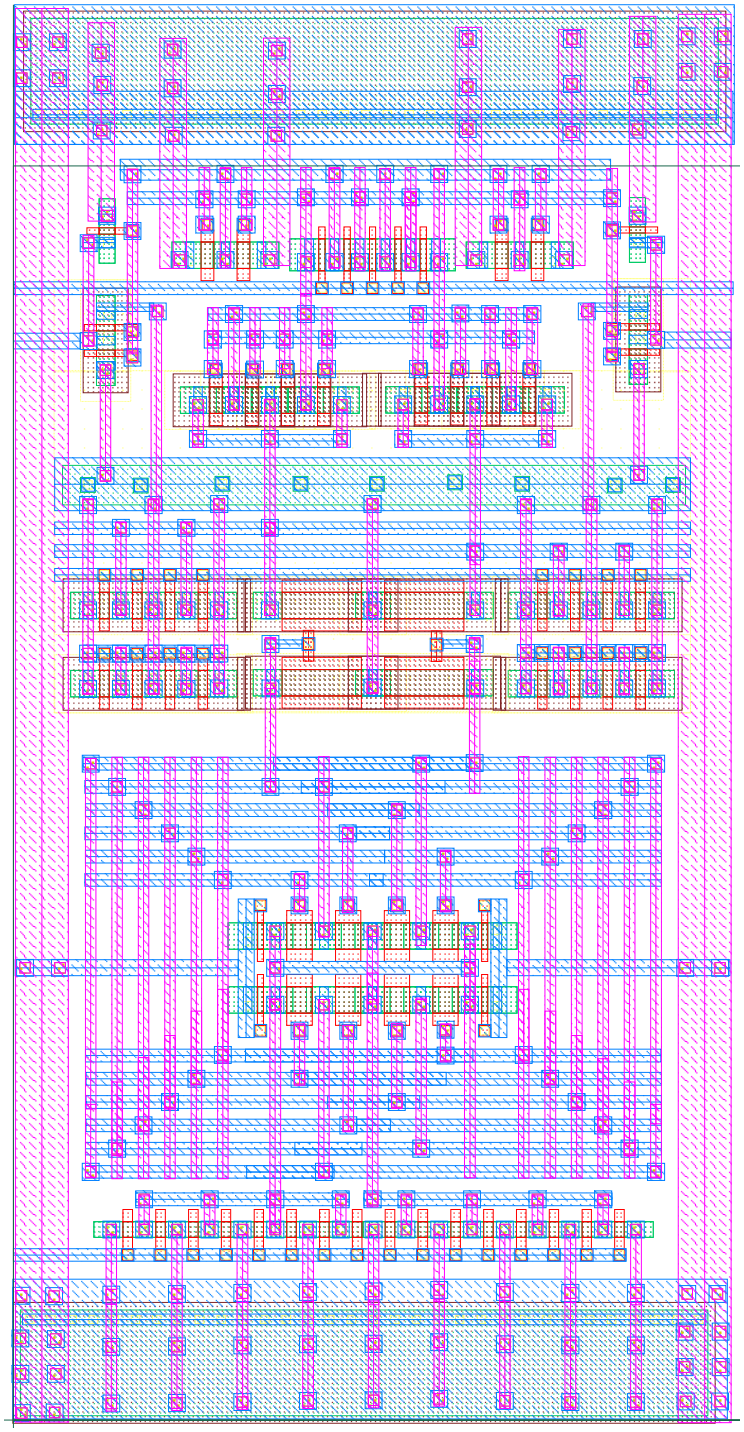


Figure A.11: Layout of the comparator.

Device Sizes

unit-OTA and booster amplifiers

Device	Width (μm)				Length (μm)
	Finger width (μm)	Fingers	Multiplicity	Total	
Main OTA					
$M1_{a,b}$	0.6	2	4	4.8	0.18
$M2_{a,b}$	1.2	1	1	1.2	0.18
$M3_{a,b}$	0.5	16	1	8	0.18
$M4_{a,b}$	0.5	16	1	8	0.18
$Mtail_{a,b}$	0.3	14	1	4.2	0.18
N-Booster					
$MP1_{a,b}$	0.3	1	1	0.3	0.3
$MP2_{a,b}$	0.6	2	1	1.2	0.48
$MP3_{a,b}$	0.6	2	1	1.2	0.48
$MN2_{a,b}$	0.3	1	1	0.3	0.18
$MN3_{a,b}$	0.3	1	1	0.3	0.16
$Mswitch_{a,b}$	0.3	1	1	0.3	0.18
P-Boosters					
$MN1_{a,b}$	0.36	1	1	0.36	0.3
$MN2_{a,b}$	0.3	1	1	0.3	0.48
$MN3_{a,b}$	0.3	1	1	0.3	0.48
$MP2_{a,b}$	0.3	1	1	0.3	0.18
$MP3_{a,b}$	0.3	2	1	0.6	0.48
$Mswitch_{a,b}$	0.3	1	1	0.3	0.18

Comparator

Device	Width (μm)				Length (μm)
	Finger width (μm)	Fingers	Multiplicity	Total	
M_{1-4}	0.5	1	1	0.5	0.48
M_{5-8}	0.5	1	1	0.5	1.5
$M_{9,10}$	0.5	4	1	2	0.18
$M_{11,12}$	0.5	1	1	0.5	0.24
$Mtail_{14,15}$	0.5	1	1	0.5	0.24
M_{13}	0.6	5	1	3	0.12
$M_{16,19}$	0.5	1	1	0.5	0.12

10-bit 5 MS/s Algorithmic ADC chip micrograph

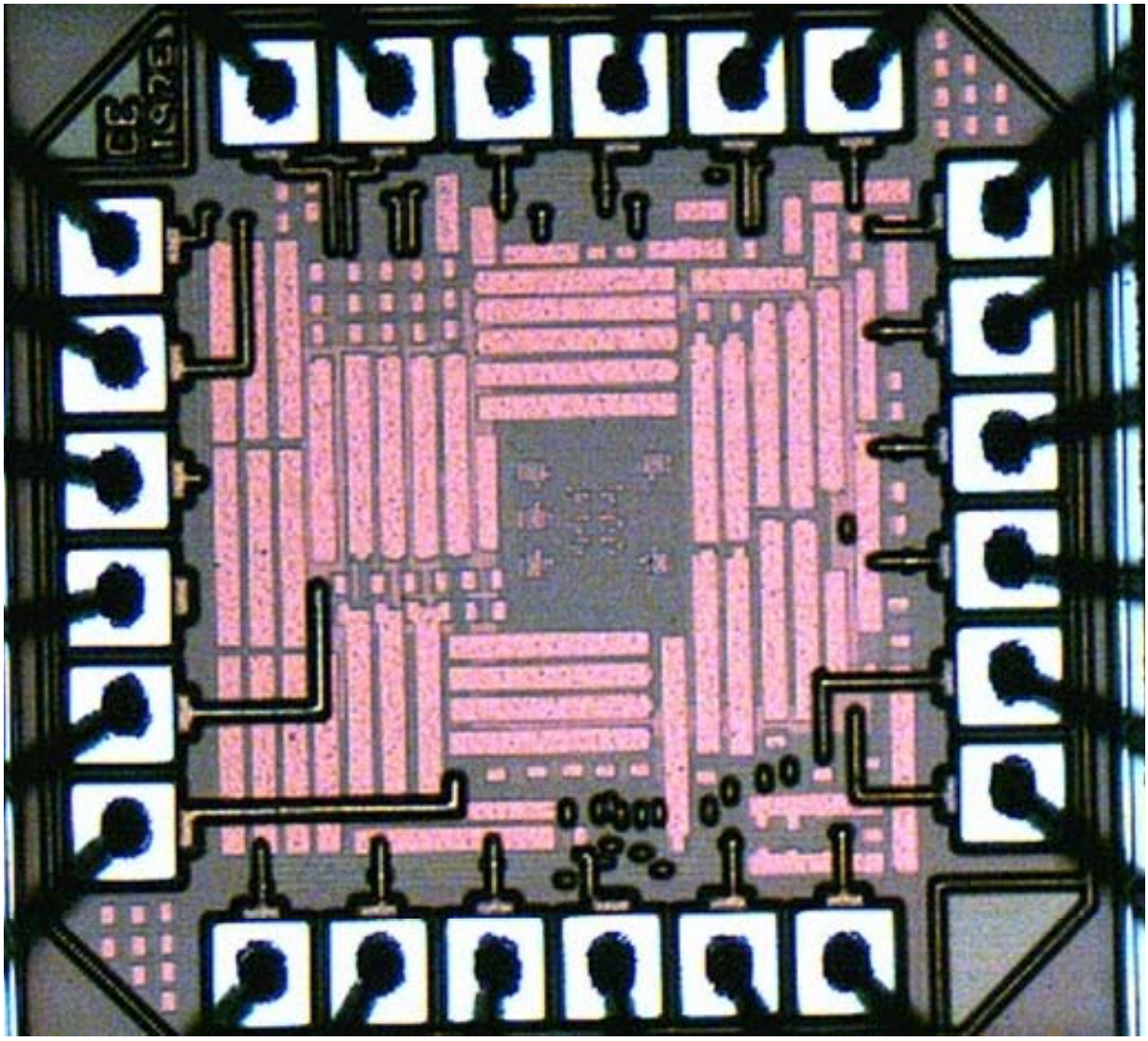


Figure A.12: Chip micrograph of the 10-bit 5 MS/s algorithmic ADC.

12-bit 10 MS/s Algorithmic ADC chip micrograph

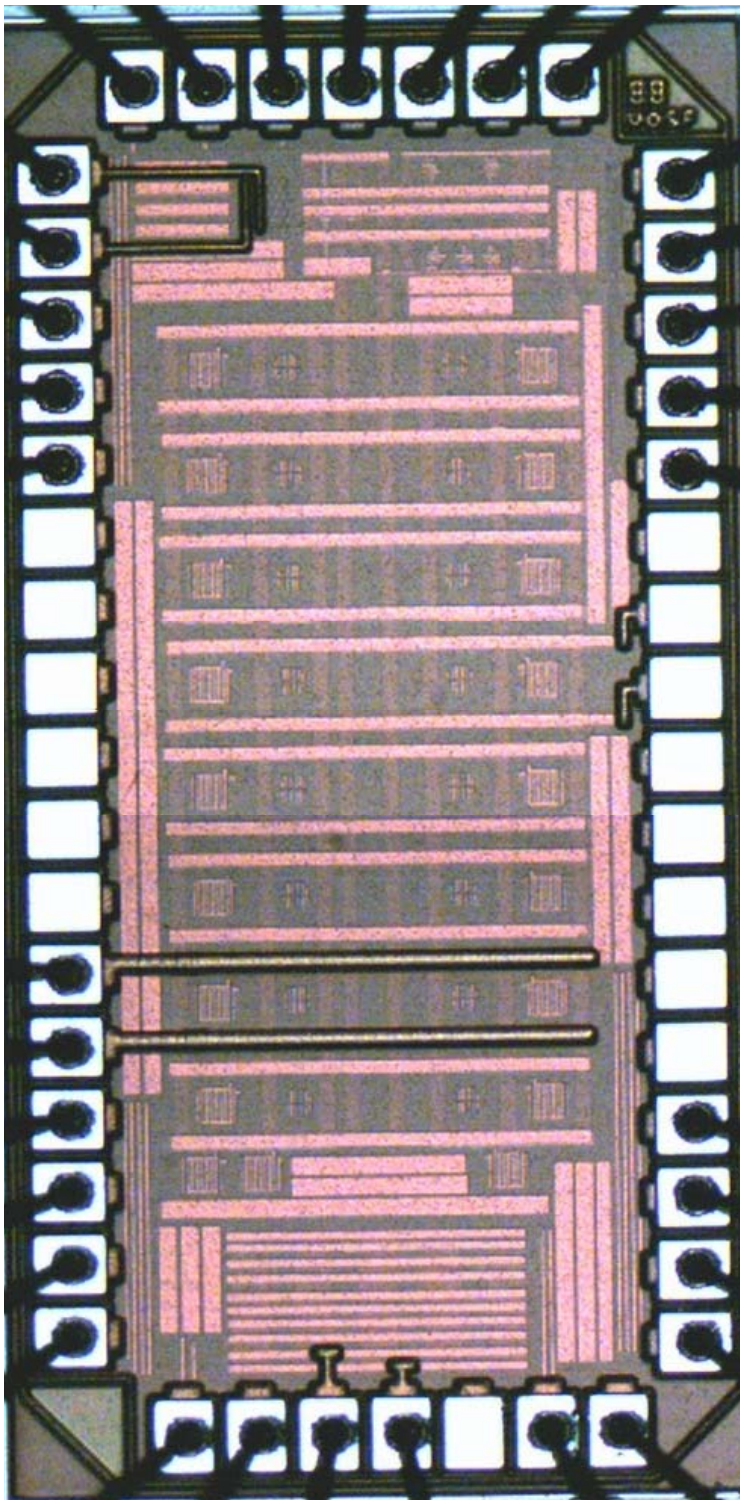


Figure A.13: Chip micrograph of the 12-bit 10 MS/s algorithmic ADC.

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