Integrated Antennas and Active Beamformers Technology for mm-Wave Phased-Array Systems

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

In this thesis, based on the indoor channel measurements and ray-tracing modeling for the indoor mm-wave wireless communications, the challenges of the design of the radio in this band is studied. Considering the recently developed standards such as IEEE 802.15.3c, ECMA and WiGig at 60 GHz, the link budget of the system design for different classes of operation is done and the requirement for the antenna and other RF sections are extracted. Based on radiation characteristics of mm-wave and the fundamental limits of low-cost Silicon technology, it is shown that *phased-array is the ultimate solution for the radio and physical layer of the mobile millimeter wave multi-Gb/s wireless networks.* Different phased-array configurations are studied and a low-cost single-receiver array architecture with RF phase-shifting is proposed. A systematic approach to the analysis of the overall noise-figure of the proposed architecture is presented and the component technical requirements are derived for the system level specifications. The proposed on-chip antennas and antenna-in-packages for various applications are designed and verified by the measurement results. The design of patch antennas on the low-cost RT/Duroid substrate and the slot antennas on the IPD technologies as well as the compact on-chip slot DRA antenna are explained in the antenna design section. The design of reflective-type phase shifters in CMOS and MEMS technologies is explained. Finally, the design details of two developed 60 GHz integrated phased-arrays in CMOS technology are discussed. Front-end circuit blocks such as LNA, continuous passive reflective-type phase shifters, power combiner and variable gain amplifiers are investigated, designed and developed for a 60 GHz phased-array radio in CMOS technology. In the first design, the two-element CMOS phased-array front-ends based on passive phase shifting architecture is proposed and developed. In the second phased-array, the recently developed on-chip dielectric resonator antenna in our group in lower frequency is scaled and integrated with the front-end.

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Dedication

To my beautiful wife, *Zahra*
To my parents

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List of Abbreviations

CMOS: Complementary Metal Oxide Semiconductors

DRA: Dielectric Resonator Antenna

EIRP: Equivalent Isotropically Radiated Power

GaAs: Gallium Arsenide

InP: Indium Phosphide

IPD: Integrated Passive Device

LOS: Line-of-Sight

LTCC: Low Temperature Co-fired Ceramic

mm-wave: Millimeter-Wave

NLOS: Non-Line-of-Sight

RFIC: Radio Frequency Integrated Circuit

RFID: Radio Frequency Identification

SiGe: Silicon-Germanium

SNR: Signal-to-Noise-Ratio

Chapter 1

Introduction

1.1 Advantages of mm-wave frequency range

In the endless pursuit for higher data-rates for wireless communications, researchers and industries are becoming increasingly interested in the millimeter wave (mm-wave) spectrum [1]– [7]. The benefits of using millimeter-waves for communication and radar systems have been known for many years. The term *mm-wave* is generally used for a wide range of frequencies between 30 GHz and 300 GHz where the range of the wavelength is in the order of millimeters. The mm-wave frequency range is desirable for several applications for a few reasons.

- The available bandwidth at mm-wave is much larger than the lower frequencies. For instance, the 5-percent bandwidth around 60 GHz is 3 GHz which is a suitable bandwidth for the broadband wireless data communications. This small fractional bandwidth relaxes the bandwidth design considerations for the circuits in this frequency range. This leads to the superiority of mm-wave ultra-broadband systems which are challenging to achieve if not impossible.
- At the mm-wave regime the size of the antenna shrinks with the wavelength. Hence, the total RF system including the antennas and the front ends can be integrated in a very small package.
- The radiowave propagation characteristics for the mm-wave offer advantages for particular communication systems. For example, the intrinsic atmospheric attenuation near 60 GHz due to oxygen absorption provides an appropriate channel for secure short-range wireless communications.

The new license-free bands, such as the 24 GHz, 60 GHz, 77 GHz, and 92 GHz, could be exploited by applications such as Wireless Local Area Networks (WLAN) devices [8, 9], Wireless Personal Area Networks (WPAN) [10, 11], car anti-collision radars [12] and phased-array radars [13]. New opportunities for a number of general

applications will become available if compact and low-cost transceivers with an acceptable performance could be implemented in mm-wave.

The major obstacle for the wide deployment of the commercial wireless systems in this band is the high cost and poor performance of the state-of-art devices. In recent years, thanks to the extensive developments in the silicon integrated circuit technology, the cost of mm-wave circuits has eventually become as low as the commercially available wireless devices like those used in the cell phones and WLAN cards.

1.2 Millimeter-Waves: Enabling technologies for a future generation of ultra-broadband radio networks

Due to the saturation of the microwave frequency bands, and the growing demands for novel high data-rate systems, there is a necessity to use new frequency bands that have not yet been utilized for commercial applications. State-of-art radio technology must be able to exploit the available bandwidth of the mm-wave to implement these high data-rate systems. In the emerging ultra-broadband mobile communication networks, there are some applications which need high data rate wireless communications such as:

- Wireless equivalent of Gigabit Ethernet (GigE)
- Wireless connection between video sources and projectors
- Wireless delivery of high-definition uncompressed baseband audio and video (A/V) without wires

It can be shown that the mm-wave band is the only feasible spectrum that all these wireless applications could be implemented with an acceptable performance.

1.2.1 The application of mm-wave for Gb/s wireless communications

The mm-wave frequencies, particularly the 7 GHz unlicensed band around the 60-GHz spectrum, provide unique opportunity to enable multi-gigabit wireless links. In particular, the 60 GHz unlicensed band provides the following advantages:

- A wide bandwidth allocation (Typically 7 GHz in North America and Japan).

- Allows for higher level transmitted power. Unlike the strict transmit power restrictions on the ultrawide band unlicensed operation, the millimeter-wave band allows for larger Effective Isotropic Radiated Power (EIRP) [14, 15].
- Spectrum with lower interference. There are not any widely deployed 60 GHz radio systems in the home or office, so there is less chance for interference.
- The smaller antenna size at 60 GHz makes the overall system packaging more compact and convenient. The small apertures in 60 GHz can generate high radiation gains.

The high-volume markets for 60 GHz systems are promising if compact low-cost transceivers with high performance exist. There are several challenges to implement low-cost high performance wireless systems at 60 GHz. These challenges include the need for higher precision in the fabrication of the antennas and in other blocks of the circuits as well as more difficult intra- and inter-board interconnections, which make chip-level integration highly desirable. Particularly, improper packaging can ruin the overall performance of the system. In recent years, a few standards and specifications have been developed for the emerging wireless devices in 60 GHz band such as WiGig, WirelessHD, IEEE 802.15.3c and ECMA-387.

1.3 Motivations for investigating on mm-wave phased-arrays

As mentioned earlier, the mm-wave band provides a unique opportunity for short range ultra-broadband mobile data communication due to the broader available bandwidth. The channel capacity is therefore much higher compared to lower frequency. In addition, the fast development of silicon technology in mm-wave circuits and systems facilitates the design and development of low-cost integrated mm-wave systems. These all have led to a fast growing market for low-cost ultra-broadband mm-wave technologies which is another motivation for research in this area.

1.3.1 Channel capacity for high frequency wireless communications

Wireless communications in the mm-wave is attractive because of its much broader available bandwidth. However, the benefit of a large bandwidth will be lessened by the limited available power of active devices. Intrinsic losses of materials including the loss of the dielectrics and metals can also deteriorate the overall Signal-to-Noise Ratio (SNR) at the receiver. The trade-off between moving to higher frequencies and a higher bandwidth with the aforementioned losses can be determined by the

well-known Shannon's theorem [16]. If the channel bandwidth of the system is B and C is the capacity of the channel then:

$$C = B \log_2(1 + SNR) \tag{1.1}$$

It can be shown that in a point-to-point wireless link, the peak in the channel capacity appears to move to higher frequencies for shorter distances and larger fractional bandwidths. The peak moves to higher frequencies with higher transmit EIRP or lower noise figure, both of which can be improved by implementing phased-arrays [17]. Therefore, the mm-wave band shows a great potential for the short range high capacity wireless systems.

1.3.2 The feasibility of integration on silicon

The high market demand and the rapid advancement of silicon-based technologies such as Complementary Metal Oxide Semiconductor (CMOS), Silicon-Germanium (SiGe) and Bipolar CMOS (BiCMOS) technology are the main reason for the growth of wireless applications utilizing the spectrum under 10 GHz over the past 10 years. The main barriers to implementing mass market consumer applications in the higher frequency bands in the past were the poor performance of existing Si-based devices and the higher cost of the existing compound semiconductor technologies such as Gallium Arsenide (GaAs) and Indium Phosphide (InP). In comparison to the compound semiconductor technology, the silicon-based technologies are promising for the large scale integration of the digital blocks and the baseband section with the RF section of the system on a single chip. Nowadays, the state-of-art CMOS and SiGe transistors, have cut off and maximum oscillation frequencies comparable with compound semiconductor devices, providing the opportunity to implement the mm-wave systems in the silicon-based technology. The implementation of the high frequency systems in CMOS technology will enable unique levels of integration, making it possible to realize new architectures that combine microwave, analog, and digital circuitry on the same substrate and at a low cost.

1.3.3 The market

The demands of the fast growing market for wireless sensor and communication applications using the millimeter wave can only be satisfied by low-cost, low-profile, and low-power RF transceivers. The potential high-volume millimeter-wave bands are:

(a) 60 GHz

The 60-GHz band offers ample, license-free bandwidth. In the US, the range is from 57 to 64 GHz while in Japan, 59 to 66 GHz is available. With

seven gigahertz of bandwidth, in addition to more conventional systems, there are numerous emerging high data rate applications such as combination communication along with sensing and imaging that were unimaginable in the past. The 60 GHz band is ideally suited for Personal Area Network (PAN) applications. While other standards are evolving to address this market (802.11n and UWB), the 60-GHz is considered to be viable candidate for short distance links. In following, we will have a quick review on these standards and their specifications.

- The need for wireless connection for the outgrowing digital multimedia cannot be supported by current wireless standards. As a result, there has been a drive to develop new standards that can support these applications. The applications of Wigig are instant wireless sync and IP-based P2P applications such as Kiosk Sync and data exchange for example, or HD streams over HDMI, such as wireless display; or cordless computing and internet access using native Wi-Fi and 802.11ad support. The Wireless Gigabit Alliance (WiGig), that was announced in 2009, is one of the organizations that has developed a standard for employing 60 GHz band for multi-gigabit wireless communications in short range. In WiGig standard the wireless devices are allowed to communicate for applications such as high-performance wireless data and wireless display. This standard is basically a compliment for the today's wireless LAN devices. The specifications of WiGig include supports for data transmission up to 7 Gbps, low-power handheld devices with advanced power management, Wi-Fi natively, beamforming for robust communications at ranges beyond 10 m, and the high-performance wireless implementation of HDMI, display port, USB and PCI. In addition, WiGig enables the device to switch between 820.11 networks in 2, 4, 5 and 60 GHz bands [18].
- WirelessHD is a wireless technology interface for high definition digital contents which operates in the unlicensed 60 GHz frequency band [19]. The specifications of wireless HD was finalized in 2008. The wireless HD specification allows the compressed or uncompressed transmission of high-definition video and audio and data signals on the 7 GHz of unlicensed band at 60 GHz. The 1.1 version of the specification increases the maximum data rate to 28 Gbit/sec to support 3D formating, 4K resolution, WPAN data and so on. The range of operation of the products for indoor point-to-point non line of sight applications is within 10 m. Sibeam was the first company who developed a full transceiver at 60 GHz for this standard.
- IEEE 802.15.3c [20] is basically the first IEEE wireless standard for data rates over 1 Gb/s [21]. This standard was approved by IEEE Standards Board in 2009. This standard introduces three PHY modes with data rates exceeding 1 Gb/s at 60 GHz. The usage models presented by IEEE

802.15.3c are: uncompressed video streaming and multivideo streaming, office desktop, conference ad hoc and Kiosk file downloading.

- ECMA-387 is the European version of the 60 GHz standard for the 60 GHz wireless communication. ECMA 387 defines three types of devices (Type A, B and C) for 60 GHz spectrum [22] based on the operational requirements such as maximum range, bit rate and system complexity. Similar to IEEE 802.15.ec, several operational modes have been proposed for each type.
- The IEEE 802.11ad had confirmed that an amendment was made for enabling multi-gigabit wireless communications to the 802.11 standard at 60 GHz in May 2011. The developed WiGig specification was mainly contributed to the IEEE 802.11ad standardization process [23]. In table 1.1 the summary of the status of each standard is listed [24].

Table 1.1: Summary of 60 GHz Standards [24]

Name	Forum type	Status	Maximum data rate (Gbps)		Applications
			OFDM	SC	
Wireless HD	Industry consortium	Spec 1.1, April 2010	7.138	–	Uncompressed HD video
ECMA-387	International standard	Draft 1.0, Dec 2010	4.03	6.35	Bulk data transfer and HD streaming
IEEE 802.15.3c (TG3c)	International standard	Spec 1.0, Nov 2009	5.67	4.54	Portable point-to-point file transfer and streaming
IEEE 802.11ad (TGad)	International standard	Target completion date Dec 2012	> 1.00		Rapid upload/download, wireless display distribution of HDTV
WiGig	Industry consortium	Spec 1.0, May 2010	6.75	4.62	File transfers, wireless display, docking streaming high definition

(b) Licensed E-band

This band is for point-to-point communications, useful for telecommunication backhauls or point-to-point local-area networks. In the US, bands have been set aside at 71-76, 81-86 GHz, and 92-95 GHz. As compared to 60 GHz, the benefits of licensed E-band are two-fold, firstly, the license itself which protects a registered link from interference, and secondly, operation in a band free from oxygen absorption.

(c) Vehicular Radar

The 76-77 GHz band is allocated to the forward-looking vehicular radar. Such radars are also called "adaptive cruise control" or "collision avoidance" radars, and provide drivers with useful warnings about obstacles in their path. These radars will be an evolutionary step towards intelligent traffic systems.

(d) 94-GHz Band

The 94-GHz band can be used for imaging or wireless communications. This band is included in the licensed E-band allocation. Regarding imagers, the wavelength at 94 GHz provides excellent resolution. Since many materials, including clothes, are transparent at 94 GHz, the 94 GHz band provides an opportunity for various security applications, such as airport screening, while insuring privacy rights are maintained. At mm-wave frequencies black body radiates at an almost constant power density (for example white noise) [25] which is proportional to the temperature of the radiating object. The low attenuation signal transmission at different mm-wave bands such as 35, 94, 140 and 220 GHz, enables transmission through the objects such as cloth, smoke and dust. The phased-array architecture shows significant advantages over focal plane arrays for millimeter-wave imaging applications. For example, NASA's one-dimensional L-band pushbroom scanning array ESTAR [26], which was flown on a P-3 aircraft about 20 years ago was a successful example of microwave imaging with phased-arrays. Using lens-based beamforming generating the mm-wave image data in real time is feasible [27]. mm-Wave radiometers have been used since the 1960s [28]. Due to rapid progress in monolithic integrated circuits technology, the real-time mm-wave imaging techniques have become attractive. mm-Wave imaging can be used for remote sensing, security surveillance, and nondestructive inspection for medical and environment field [28]. Employing the benefits of silicon technology scaling, the integration of high-performance mm-wave systems in a single-die is possible. Moreover, high packing density technology for CMOS realizes the possibility of building a low-cost multi-pixel focal plane array for mm-wave imaging.

The introduced applications are all below 100 GHz which standard integrated silicon technologies such as CMOS and SiGe operate. Recently, due to development of technology, implementing integrated devices above 100 GHz is feasible [29, 30]. The possible applications for above 100 GHz can include industrial sensors, active imagers for biomedical applications, passive imagers for remote sensing, night vision, security, and 10-40 Gb/s wireless I/Os for chip-to-chip communication within 3-D electronic systems [29].

1.4 Why phased-arrays for mm-wave?

Power generation in the higher frequencies is more challenging. The losses in the dielectric substrates of the transmission lines as well as the conductors and metals, reduce the efficiency of the power generated by the RF sources. A conventional approach for power generation is to combine the power generated by a number of sources. Power combining in the planar circuit suffers from the intrinsic losses of dielectrics and metals. Therefore, a low loss method should be chosen to combine the powers with minimum loss. Spatial power combining is one of the best candidates for signal power combining with maximum efficiency. Using a *phased-array* architecture, the radiated signals can be combined in-phase in a certain direction. By changing the phase of the signals the radiation beam can be steered.

A phased-array system consists of multiple antenna elements, which are fed coherently. The feed circuit uses variable phase, time-delay or variable amplitude control devices for each element or a group of elements to shape and/or scan a beam in space. Variable amplitude control is commonly provided for pattern shaping. Electronically scanning the beam direction of an array was a natural evolution of the fixed beam array that was initially developed in the late 1920's [31]. Early scanning arrays were employing mechanical devices to provide the time-delay or phase shift but after 1950s due to progress in phase shifter technology, the forefather of the present day phased-arrays emerged. Due to the multiplicity of the antenna elements, arrays provide a more precise control on the radiation pattern and sidelobes. However, the primary reason for using the phased-array is to provide a directive beam that can be scanned electronically. Phased arrays have a wide range of applications in satellite communications [32], radar [33], radio astronomy [34], optics [35] and RFID [36].

The phased-arrays' advantages for mm-wave applications is its ability to provide both power combining and electronic beam steering simultaneously. In the mm-wave, the free-space loss can be so high that the signal level can easily drop below noise. The SNR improvement in the receiver system is a very effective approach to recover the signal.

1.5 Objective of the research

Different aspects of the developing wireless systems for the emerging applications in mm-wave are shown in Fig. 1.1. In order to develop a high performance phased-array with an efficient front-end and low power in mm-wave band, a comprehensive system design should be accomplished. In the system level design, by modeling the channel and choosing the radio structures and needs for system design the proper technology for designing the system blocks should be chosen. After doing the system design and finding the specifications of each block, the

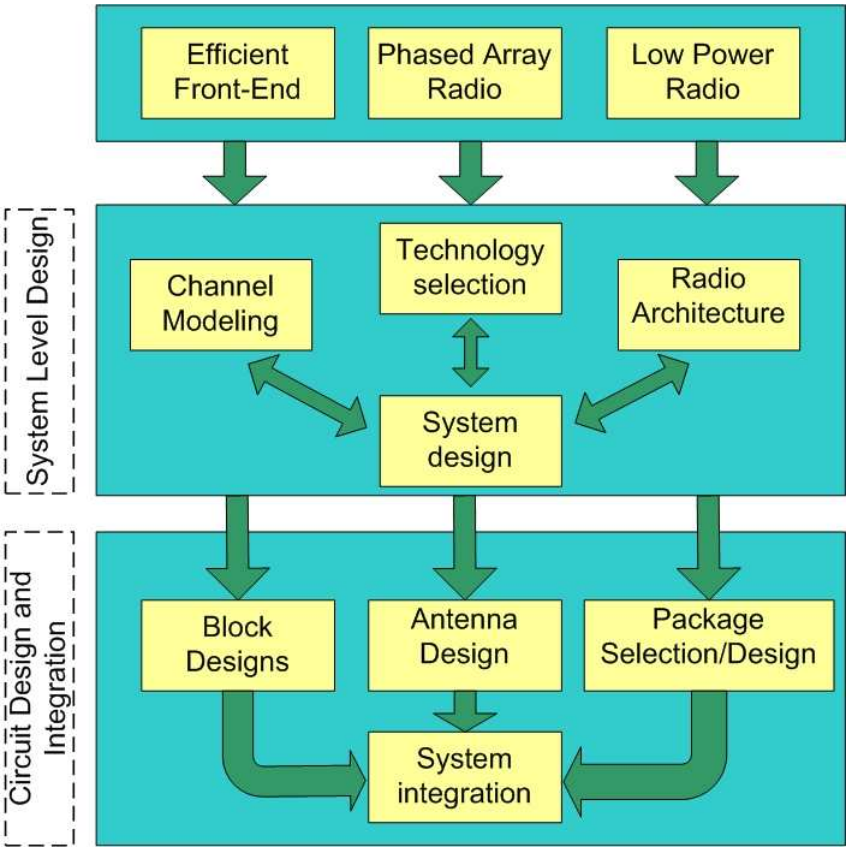

Figure 1.1: Integrated millimeter-wave radio and objectives of this research

design of each system element such as circuit elements, antenna and package should be done. After verification of the system performance, the last step would be the system integration. The main objective of this research is to investigate low-cost architecture and technology for the mm-wave integrated wireless systems. The phased-array architecture is uniquely positioned to address several shortcoming of low-cost technology such as those based on silicon. Phased array systems using an intelligent algorithm can maximize the performance of the radio links by concentrating transmitted energy and received signal in directions of interest as the physical environment is continuously varying with time in an unpredictable manner. Although the ideas, methods and other research results developed during the course of this investigation are general in nature, we have chosen the 60 GHz band, due to its importance as our main application focus. As mentioned before, the 7 GHz license-free band around 60 GHz can provide high data-rate wireless communications at the rate of gigabits per second. Due to the prospective wide-spread deployment of the wireless systems for the point-to-point short range applications, the low-cost and high performance system in 60 GHz is in high demand. The goal of this research is development of a reliable solution for the front-end and the antenna.

For this purpose, to determine the system level requirements, the mm-wave channel for indoor, point-to-point short range applications must be modeled and characterized first. The channel model is experimentally verified for the Line-Of-Sight (LOS) and Non-Line-Of-Sight (NLOS) scenarios. Afterwards, based on the channel characteristics, the fundamental mm-wave blocks are designed and verified. Although the developed concepts can be implemented in any integrated circuit technology, considering possible and available options for university level research, the 0.13 μm and 90 nm CMOS technologies have been chosen as good candidates for fundamental blocks such as low-noise amplifier and phase shifters. For the antennas, based on the system analysis for the available standards in mm-wave band, different antenna solutions have been proposed. These solutions are off-chip, in-package and on-chip solutions. Finally, the phased-array system has been designed for different wireless applications. The previously developed on-chip in-package antenna in our group [37, 38] has been scaled and integrated with the phased-array system.

In Summary the major contributions of the author can be listed as follow:

- The design of passive reflective-type phase shifters in CMOS technology.
- The channel study and systematic analysis of the wave propagation in the mm-wave band.
- The implementation of efficient high gain antennas in a new passive silicon technology at 60 GHz.
- The design of efficient on-chip antennas.
- The extensive measurement and characterization of on-chip antennas and millimeter-wave circuit blocks.
- The implementation of a high gain CMOS amplifier at 60 GHz.
- The implementation and demonstration of a two element 60 GHz phased-array front-end in low-cost CMOS technology.
- The implementation and demonstration of a two element 60 GHz phased-array front-end integrated with on-chip antenna in CMOS technology.

1.6 Outline of this Research

Chapter 2 of this dissertation presents the system analysis of the wave propagation for an indoor environment for a fixed-antenna single-channel and phased-array radio at 60 GHz. The effect of the human body in the 60 GHz channel has been investigated. Chapter 3 starts with the review of phased-arrays in silicon technology. Furthermore, it has been shown how a phased-array receiver can

improve the SNR in a NLOS condition for a typical application of 60 GHz wireless system. Chapter 4 focuses on the design of three types of antennas based on the system analysis done in chapter 3.

In Chapter 5, the design of two kinds of phase shifters are explained. The first phase type is the reflective-type phase shifter using CMOS technology and the second type is the reflective-type phase shifter using MEMS technology.

Chapter 6 presents the design of a millimeter-wave phased-array front-end. This chapter describes the proposed receiver architecture and presents two approaches for RF phase shifting based on passive phase shifting as well as power combining. Furthermore, a phased-array system integrated with the on-chip in-package antennas is designed and tested.

Finally, Chapter 7 concludes this research and proposes directions for future research.

Chapter 2

Channel Measurement and System Analysis of the mm-Wave Wireless System

2.1 Introduction

GaAs has been the dominating material in commercial Micro/Millimeter wave Monolithic Integrated Circuits (MMIC) for decades [5]. Nonetheless, with the aggressive scaling of gate lengths, CMOS is pushing further into the mm-wave region and becoming a low-cost technology option for mm-wave systems on chip. Today CMOS is the dominating technology for most wireless products below 10GHz such as WLAN, Bluetooth, Global Positioning System (GPS) and wireless sensors, and will most probably remain so in the foreseeable future. This dominance has been achieved by the reliability, low-cost, and high device count advantages of CMOS compared to other semiconductor technologies such as SiGe and GaAs. Moreover, CMOS is the most promising technology for system-on-chip design, because it enables the integration of the required analog RF circuits, as well as the digital signal processing and baseband circuits in the lowest possible chip area, which leads to a lower cost and more compact solution. The nano-scale CMOS technology, such as 90 nm, 65 nm and 45 nm, offers commercial mm-wave solutions for short range and higher frequency/data-rate applications. However, several system and circuit level challenges must be met, such as the efficient and low-cost antenna and packaging solutions, dealing with the low output power, the nonlinearity of the power amplifiers, severe path loss, shadowing loss, limited gain of the LNA and its high noise figure.

In this chapter, in order to calculate the system requirements for an indoor short range wireless link, a mm-wave propagation channel for an office is studied. The study involves both line-of-sight and non-line-of-sight scenarios where a human

body is main source for the shadowing loss. These measurements are used for the link budget calculations of the system.

In the next sections, in order to calculate the system requirements for an indoor mm-wave wireless communication, the LOS and NLOS scenarios have been studied. In the LOS scenario, a room with a maximum length of 10 m is assumed and the transmitter was located at the ceiling of the room. Then the level of the signal is calculated for the LOS scenario and the antenna specifications were derived from these calculations. In the second scenario, an indoor short range high data-rate wireless communication inside a regular office space was considered. The CAD Laboratory located on the third floor of the EIT building at the University of Waterloo was used as a typical indoor wireless environment. In this example the transmitter was located at the ceiling and the receiver can be anywhere in the room. The main source of blockage of the signal and shadowing is the human body moving in the office. In the first step, the indoor channel propagation was analyzed and the effect of shadowing by humans was simulated.

2.2 Line-of-sight indoor mm-wave oropagation channel

2.2.1 Required antenna characteristics for IEEE and ECMA standards

Communication link parameters such as antenna gain, transmitter power, receiver noise figure, and so forth, can be derived from standard specifications. The technology limitations as well as the domestic regulations should also be considered in the determination of the aforementioned parameters. For 60 GHz short-range wireless communications the standard drafts such as IEEE 802.15.3c, ECMA 387, Wireless HD and WiGig have been released so far. IEEE 802.15.3c defines three classes for different wireless (single carrier) applications [20]:

- Class 1 addresses the low-power low-cost mobile market with a relatively high data rate of up to 1.5 Gb/s.
- Class 2 supports for data rates up to 3 Gb/s.
- Class 3 supports high performance applications with data rates in excess of 5 Gb/s.

Similar to IEEE 802.15.3c, ECMA 387 defines three types of devices (Type A, B and C) for the 60 GHz spectrum [22] based on the operational requirements such as maximum range, bit rate and system complexity. Several operational modes have been proposed for each type. Table 2.1 shows the requirements of the basic and

Table 2.1: Mode dependent parameters of Type A, B and C devices in ECMA standard

Mode	Max. Range	RX Sensitivity	Data-Rate	Constellation
A0	10 m	-60 dBm	0.397 Gb/s	BPSK
A9	< 10 m	-40.7 dBm	6.35 Gb/s	16-QAM
B0	3 m	-60.7 dBm	0.794 Gb/s	DBPSK
B2	< 3 m	-54.6 dBm	3.175 Gb/s	DQPSK
C0	1 m	-62.2 dBm	0.8 Gb/s	OOK
C2	< 1 m	-53.5 dBm	3.2 Gb/s	4ASK

Table 2.2: mm-Wave Physical Channelization

Channel	1	2	3	4
Frequency	57.24-59.4	59.4-61.56	61.56-63.72	63.72-65.88

highest-rate modes of each device type. The basic mode has the lowest bit-rate amongst all the modes and operates at the maximum range. Other modes can operate at a lower range. In the following, the main parameters of the physical layer of these two standards, which must be considered in the antenna design, are discussed.

Antenna bandwidth

In both standards, the 60 GHz spectrum has been divided into four channels, as shown in Table 2.2. Each channel has a bandwidth of 2.16 GHz. Any device must support at least one channel. In North America, the first three channels have been released. Channel four has been released in Japan and Europe.

Antenna gain

In a communication link, if the same antennas are used for both the transmitter and the receiver ($G_R = G_T = G_a$), then the transmitter power (P_T) is related to the antenna gain, receiver sensitivity (S_{min}) and path loss (PL) by

$$P_T + 2G_a \geq S_{min} - PL \tag{2.1}$$

where P_T and S_{min} are in dBm and G_a and PL are in dB. The right-side of (2.1) is determined by the standard. But the left-side gives a freedom to the designer to choose the suitable power amplifier and antenna.
Fig. 2.2 demonstrates the transmitter power versus the antenna gain at 60 GHz

for the basic modes as described in Table 2.1, for LOS links. This figure also shows the FCC limit on the indoor EIRP (document 47 CFR 15.255).

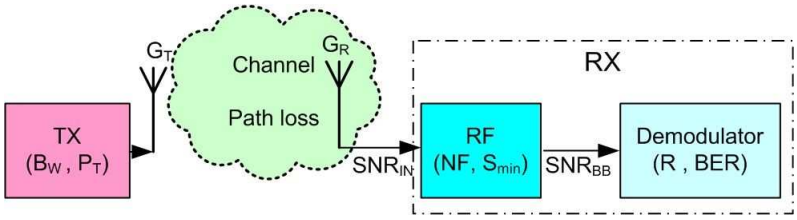

Figure 2.1: The transmitter-receiver link and the related parameters used in this work.

FCC limit for indoor propagation

The transmitted power must be kept as low as possible to increase the battery life of the portable device and reduce the interference to other users. FCC regulation (47 CFR 15.255) limits the maximum indoor EIRP to 27 dBm. As shown in Fig. 2.2 the use of a very low gain antenna for type A devices, for example, $G_a \leq 0.6$ dBi violates the FCC limit. For a radio frequency integrated-circuit (RFIC), the transmitted power is limited by the semiconductor processing technology. For example at, 60 GHz the 1 dB gain compression power of a 90 nm-CMOS (P_{1dB}) is limited to 10 dBm [39, 40], whereas for GaAs, P_{1dB} can be as high as 1 W (for example, 2.8 W at Q-band [41]). The horizontal lines in Fig. 2.2 show the typical technology limits for CMOS technology (0-10 dBm). Fig. 2.2 shows that for CMOS-compatible Type C devices a low gain antenna ($G_a \leq 2.7$ dBi) is sufficient. For Type B devices in CMOS the antenna gain can vary from 3.3 to 8.3 dBi. However for Type A, which is considered as the *high end-high performance* device [22], a high-gain antenna is necessary. An antenna with an affective gain of 13.7 dBi at 57 GHz for $P_T = 0$ dBm is ideal for mode A0 operating at the maximum range of 10 m. For transmitting higher bit-rates at the maximum range either an array of such antenna can be used or the transmitter power can be increased. Therefore, one of the objectives of the gain antenna is to design a compact antenna with a maximum gain above 13 dBi. The RX-TX antenna polarization mismatch or misalignment can be compensated by a small increase (1-3 dB) in the transmitter power.

Antenna beamwidth

For 60 GHz applications antennas with higher gains (such as 13.7 dBi for Type A) are required, which have directional patterns. For certain receivers connecting to an Access Point (AP) in a room, such as cell phone or laptop, an omni pattern is not required.

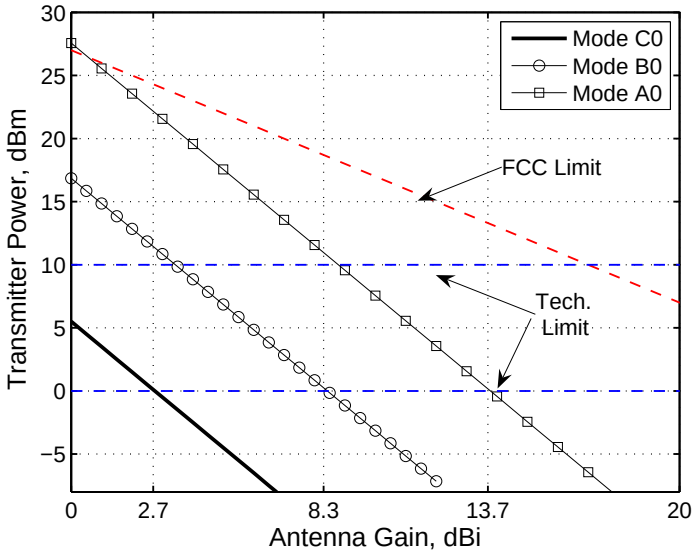

Figure 2.2: Transmitter power versus antenna gain for different operational modes at 57 GHz.

In the following, a methodology to find the maximum beamwidth for a receiver antenna inside a room (piconet) is proposed.
Assume a square room with a size of $l \times l$ and the height of 3.5 m. An AP has been installed at the center of ceiling with a hemispherical pattern. It is also assumed that the user distribution along the z-coordinate is uniform ranging within 1.5 m to 2.5 m from the ceiling (AP). To find the required coverage angle, 20000 random user locations were generated. The angle between the line connecting the user to the AP and the z axis was calculated for each user, and the histogram of all calculated angles was plotted. Fig. 2.3 shows the required values for the beamwidth to cover 90% and 100% of the indoor users versus room size ($2 \leq l \leq 10$) for uniform user distribution. For the maximum room size (10 m), the RX antenna coverage must be respectively 72° and 77.5° to include the 90% and 100% of users.

2.3 Non-line-of-sight indoor mm-wave propagation channel

Indoor propagation at mm-wave frequencies can be modeled using a Geometrical Optics (GO) ray-tracing method enhanced by uniform asymptotic diffraction theories and experimental models. The reliability of the channel characterization results obtained by the ray-tracing method at microwave frequencies has been confirmed by different measurements [42] – [44]. For indoor applications at 60 GHz, the high penetration loss of the material isolates adjacent rooms and significantly

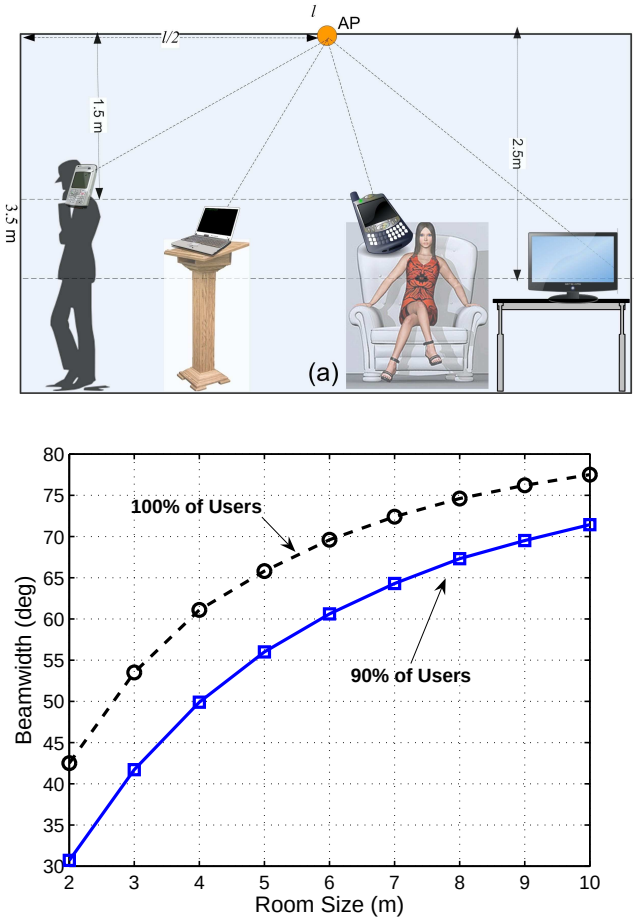

Figure 2.3: Finding the beamwidth of the antenna. (a) Simulated scenario. (b) Antenna angular coverage versus room size for uniform user distribution.

limits the received interference, so only those objects inside the room need to be included in the ray-tracing simulation. In this in-room propagation channel, both Line of Sight (LOS) and Non Line of Sight (NLOS) rays must be considered. The NLOS rays are caused by reflections from the objects inside the room as well as some significant first order diffracted rays. Furthermore, the propagation loss in the ray-tracing modeling consists of free-space loss according to the Friis formula, gaseous loss, and the reflection, transmission and diffraction losses.

In this work, a 3D ray-tracing model (GO plus diffraction) is employed to assess the signal coverage at 60 GHz for a regular office area. The CAD Laboratory, located in the EIT building at the University of Waterloo, ,was used as a typical indoor wireless environment (see Fig. 2.4(a)). The lab is furnished with tables, chairs and shelves mostly constructed of wooden and plastic material. The walls consist of layers of different material such as plasterboard, concrete, and wood. Moreover, various electronic equipments such as computers, printers and test

devices were placed in this lab. The empirical data reported in [45] and [46] was used to calculate the reflection coefficients of the material. Moreover, to evaluate the human body shadowing effect the measured permittivity data for biological tissues in [47] was used. Table 2.3 summarizes the measured permittivity data at 60 GHz used in this work.

Table 2.3: Measured Permittivity of Indoor Materials at 60 GHz

Type	**Complex** ϵ_r
Acrylic Glass	$2.5298 - j2.5298$
Chipboard	$2.8556 - j0.1586$
Concrete	$6.1326 - j0.3014$
Glass	$5.2839 - j0.2538$
Plasterboard	$2.8096 - j0.0461$
Wood	$1.5671 - j0.0962$
Human Body	$13.2 - j10.4$

The transmitter antenna in Fig. 2.4 is located 10 cm below the center of the ceiling (facing down) which is 3.45 m above the floor. The receiver is located on a wooden table 75 cm above the floor. To simulate the shadowing effect, a human-body blocks the LOS path between the transmitter and the receiver as shown in Fig. 2.4(b). To model a mobile user (portable end-device), the receiver antenna moves within a 2 m$\times$1.75 m grid located 1 m above the floor (25 cm above the table). The resolution of the grid-cells varies from $\lambda/5$ to $\lambda/2$.
Fig. 2.5 demonstrates the ray-tracing results at 60 GHz for the rectangular grid in front of the human body in Fig. 2.4. The human body model is 1.8 m tall centered at (-0.5 m, 1.4 m, 2.54 m) relative to the transmitter antenna. The white area in Fig. 2.5(a) illustrates the relative opaqueness of the human body at 60 GHz. The transmitter antenna was a 2×2 microstrip patch array with a maximum gain of 10 dBi (see Section 4.2 for the radiation pattern of the antenna) and the input power to the antenna was 2 dBm. An isotropic antenna was used as the receiver. Fig. 2.5(b) shows the received power on two horizontal lines, named *Path A* and *Path B*, in the region shown in Fig. 2.5(a). Path A and Path B are respectively 20 cm and 80 cm in front of the human body and 1.7 m and 2.3 m away from the projected transmitter position in Fig. 2.4(b). The human body shadowing attenuates the received power level by 10 to 40 dB for Path A and by 15 to 30 dB for Path B. The other objects in the room cause up to $\pm$5 dB in fluctuations in the received signal level. In calculating the received power the time-delay and phase of all rays, which their magnitudes are above -120 dBm, have been considered. This threshold is almost 40 dB below the thermal noise power with 2.16 GHz equivalent bandwidth.

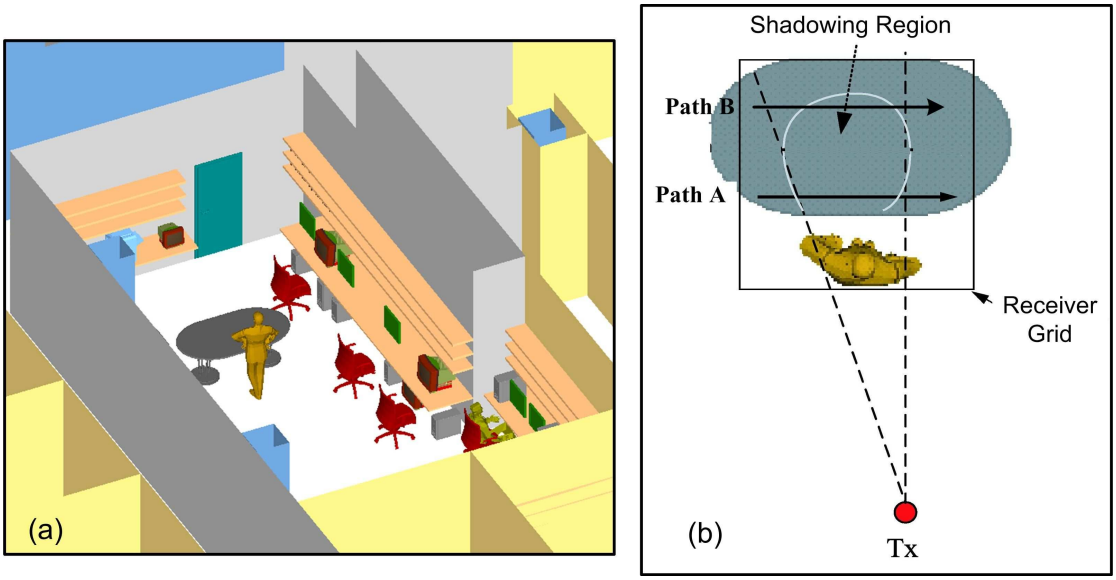

Figure 2.4: (a) Simulated 3D view, and (b) top view of the propagation environment (CAD Lab at the University of Waterloo).

2.3.1 Measurements

Fig. 2.6(a) demonstrates the developed test set-up to measure the shadowing loss of the human body over the frequency range of 50-75 GHz. Two rectangular horn antennas with a 24 dBi gain at 60 GHz and a 10° beamwidth were used as the transmitter (Tx) and receiver (Rx). The Agilent $E8267D$ programmable signal generator connected to the $E8257DS15$ mm-wave source module was used to generate the source signal. On the receiver side, the Agilent $E4448A$ spectrum analyzer connected to the $11974V$ preselected mixer was used to measure the spectrum of the received signal. The transmitted power was around 12 dBm. Wave absorbers with 40 dB of attenuation were used to weaken the reflections from the source module and mixer. The Tx and Rx antennas were installed at the height of 135 cm and 130 cm, respectively. The horizontal distance between the Tx and Rx antennas in Fig. 2.6(b) was 3 m. The Tx antenna was fixed, but the Rx antenna was moved along a horizontal line in steps of 5 cm (the orientation of the Rx antenna was kept unchanged). At each point the received power spectrum was measured (after calibration) at three frequencies, for example 57, 60 and 64 GHz. For each spectral measurement, the average of 100 successive frames was taken to smooth the instantaneous fluctuations. Fig. 2.6(c) shows the LOS (no shadowing) measured spectrum at one of these Rx locations. It is seen that the measured power level reduces as the frequency increases, due to the larger path loss at the higher frequencies.

Fig. 2.6(d) compares the measured shadowing loss with the ray-racing results for the same room. There is a good agreement between the simulation and

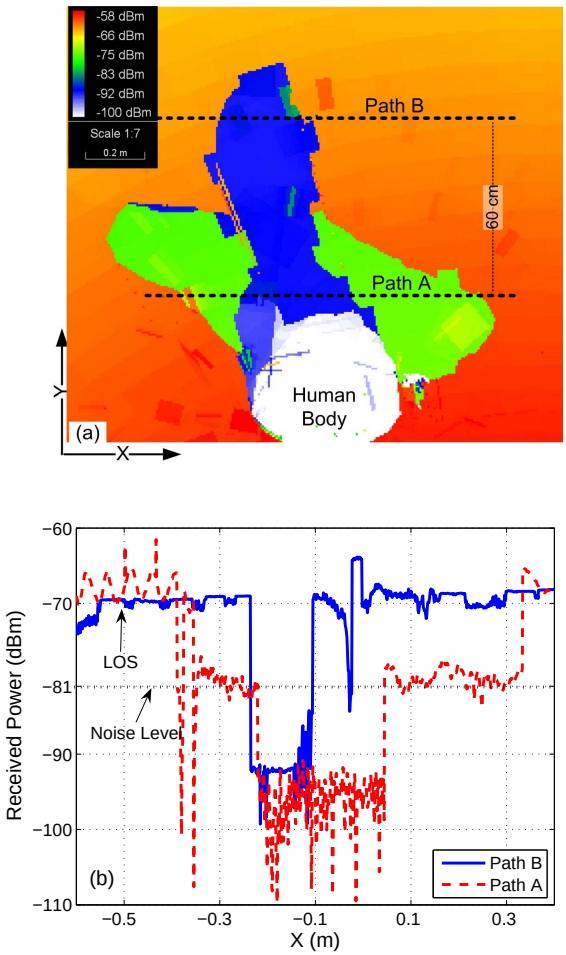

Figure 2.5: (a) Received power over the rectangular grid in Fig. 2.4(b) around the human body. (b) Received power on Path A and Path B shown in Fig. 2.4(b).

measurement from x=-20 to x=60 cm. The maximum shadowing loss is around 40 dB which occurs when the human body blocks the LOS path completely. Ray-tracing results show that at the deep shadowing region all LOS rays are absorbed by the human body, so the measured received power is the combination of NLOS rays. This result has been verified by the measurements in Fig. 2.6(d). A phased-array receiver has the potential of steering the array beam to the direction of the strongest NLOS ray when the receiver is inside the deep shadowing region.

2.3.2 Link budget design for wireless mm-wave network

The severe free-space and shadowing losses at mm-wave necessiate of an accurate link budget design before planning a wireless system. For short-range wireless mm-wave networks such as WPAN the maximum coverage range is $R_{max} = 10m$, so the maximum LOS path loss at 60 GHz based on the Friis relation is 88 dB.

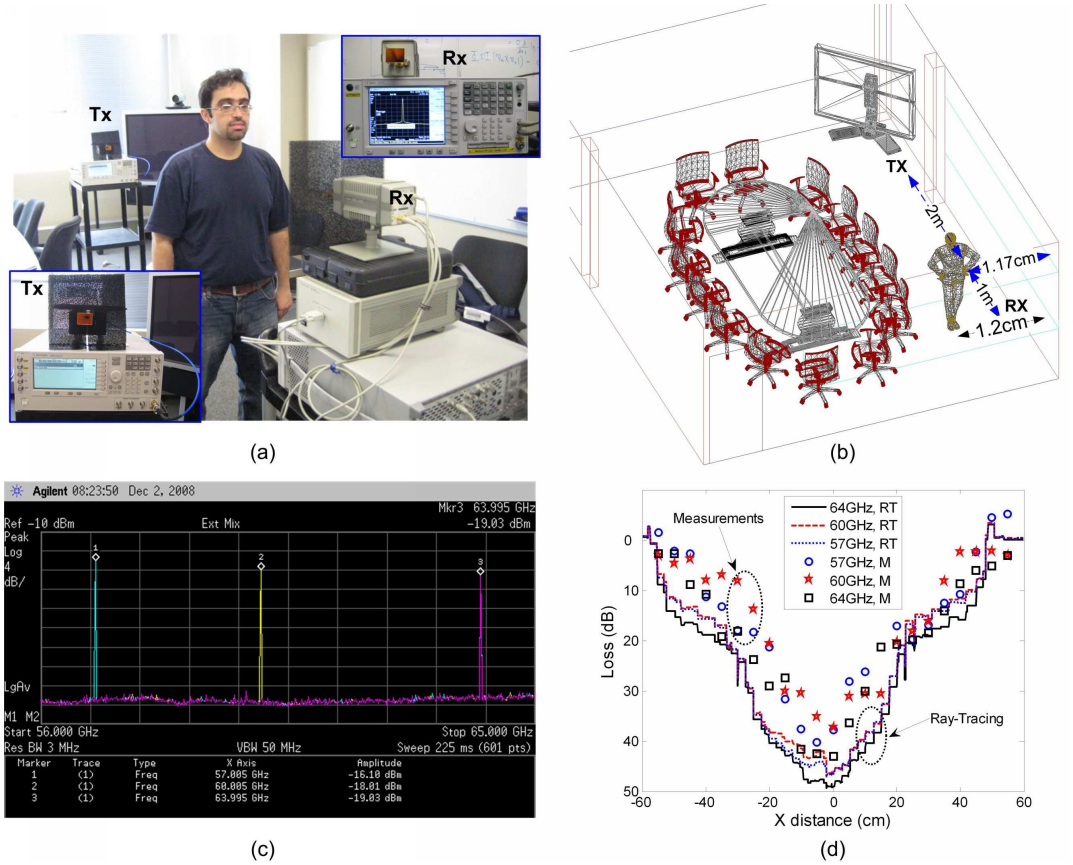

Figure 2.6: Measurement environment and results. (a) Test set-up with transmitter and receiver. (b) Tx and Rx antenna locations in the room. (c) One sample of the measured spectrum at 57, 60 and 64 GHz. (d) Comparison of the measured and simulation results.

Moreover the shadowing effect can attenuate the received power between 20-40 dB as shown in Fig. 2.5(b). In this section the link budget for a noise-limited system, where the thermal receiver noise dominates, and an Additive White Gaussian Noise (AWGN) model can be used.

The required sensitivity of a receiver is determined by the desired Bit Error Rate (BER) and modulation scheme. For a non-fading AWGN channel, analytic expressions for the BER of different modulation schemes versus the SNR are given in [48]. Fig. 2.7 shows the BER versus SNR for the AWGN channel. It is seen that an SNR of at least 10 dB must be delivered to the receiver base-band by the RF front-end to keep the BER below 10^{-6} for most of the modulation schemes. For a fading channel various diversity techniques (time, frequency or space) can be applied to improve the performance.

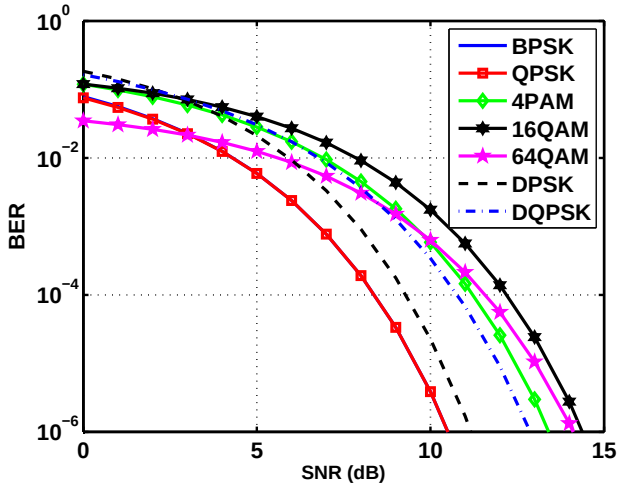

Figure 2.7: Bit Error Rate versus SNR for different modulations.

Fig. 2.8 shows the received SNR for LOS propagation at different points of the empty office of Fig. 2.4, when one single wide-beam antenna with 10 dB of gain, $\pm 30^\circ$ of coverage and 2 dBm of input power has been used as the transmitter. CMOS technology's intrinsic limits do not allow the increase of input power. It is evident that the required SNR for a low BER signal reception, such as 10 dB can not be achieved with such a transmitter and therefore an array of antennas and power amplifiers must be used at the transmitting node. Furthermore, to cover the maximum distance (the dashed circle in Fig. 2.8) multiple transmission nodes should be considered [7]. The effectiveness of using array architecture depends on the noise-loss trade-offs of the hardware and using an efficient beamforming algorithm. Therefore, using an adaptive array at the transmitting/receiving node is mandatory.

On the receiver side, it is possible to use high-gain antennas to increase the received SNR, however for a mobile portable receiver such as laptop or cell phone, the direction of the antenna main-beam must change adaptively as the user moves. Moreover if the LOS path is blocked, even a high gain antenna cannot compensate for the huge shadowing losses which could be as large as 50 dB. In summary the only solution to provide wireless mm-wave service to a mobile receiver is to use a low-noise adaptive array with an efficient beamforming algorithm at the receiving node. In the following sections an architecture for a phased-array considering all fundamental limits of CMOS technology is proposed. Furthermore the novel and fast beamforming algorithm to steer the antenna beam and compensate for the hardware inaccuracies developed in our group [49] is applied on the system. Table 2.4 shows the range of the parameters used in the link budget design of a mm-wave wireless network with CMOS phased-arrays.

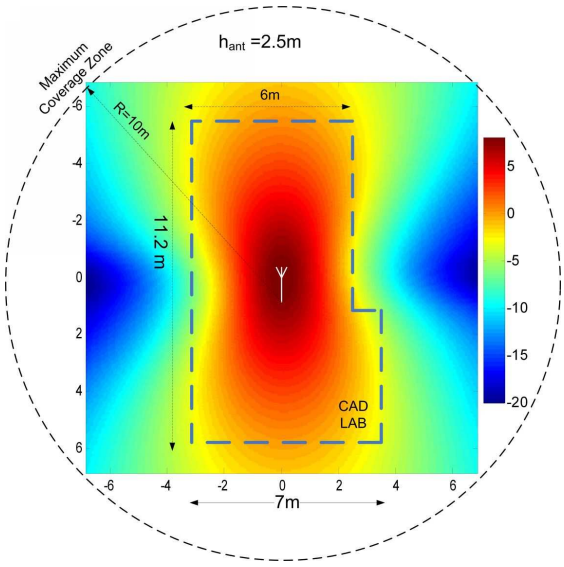

Figure 2.8: Received SNR for LOS propagation at different points of the coverage zone (CAD LAB) when a 2 patch array antenna has been used at the transmitter node.

Table 2.4: Parameters used for link budget design of 60 GHz system in CMOS technology

Application Specifications	Coverage Range	$\leq 10m$
	Center Frequency	60 GHz
	Bandwidth	$\geq$ 2 GHz
	Thermal Noise (B=2GHz,$T_0 = 290^{\circ K}$)	-81 dBm
	Bit rate	$2-4$ Gbps
Channel Specifications	Maximum LOS loss	88 dB
	Oxygen Attenuation	0.16 dB
	Shadowing (Multipath) Loss	20-40 dB
Intrinsic CMOS Limits	P_T Power Amplifier	$\leq$ 2 dBm
	LNA Gain	$\leq$ 25 dB
	Receiver Noise Figure	6-10 dB

2.4 Chapter summary and conclusions

In this chapter, a system analysis for the LOS and NLOS propagation channel of an indoor wireless system was done. Based on IEEE 802.15.3c and ECMA 387 standards, the radiation characteristics of the antenna such as gain, bandwidth and beamwidth have been derived. The developed antennas fully meet the requirements

for the point-to-point line-of-sight applications and maximum signal coverage. For the NLOS scenario, it is shown that the human body has a shadowing effect on the received signal at 60 GHz. The human body can attenuate the received signal by 40 dB. The phased-array can compensate the shadowing effect by steering the beam toward a non-line-of-sight ray.

Chapter 3

A mm-Wave Phased-Array Architecture for Wireless Applications

3.1 Introduction

The current tendency of the integration of phased-arrays on silicon for non-military applications is characterized by a set of different challenges when compared to a prototype phased-array for military applications. Military phased-arrays are traditionally used in high-performance radar systems and hence employ thousands of elements to achieve a fine spatial resolution [50]. Beam-scanning is used to locate and track multiple targets simultaneously. The novel commercial applications, such as high data rate wireless communications at 60 GHz and vehicular radars at 22-29 GHz and 77 GHz, are relatively low-performance systems when compared with military systems. The link distances involved are of the order of a few meters and a fine spatial resolution is not required. As a result, these commercial phased-arrays will likely employ tens of radiating elements, rather than thousands. The unit cost is a critical issue for market success, and hence, the integration with silicon-based technology is essential. This is rendered feasible by the lower required performance, in terms of EIRP and array sensitivity for example, and the ability of the latest generation of silicon-based technology to handle millimeter-wave frequencies. Table 3.1 outlines a qualitative comparison of the early millitary phased-arrays versus emerging commercial phased-arrays [50].

The packaging of the single-chip antenna arrays at millimeter-wave frequencies constitutes another challenge. Specifically, the interface between the single-chip and the off-chip antennas introduces channel mismatches that can deteriorate the array performance significantly. Calibration circuitry allows for the correction of packaging mismatches, and hence can greatly reduce packaging effort and cost. As silicon-based technology has only recently attained mm-wave capability, the

phased-arrays have traditionally been built using discrete compound semiconductor components based on compound semiconductors.

Table 3.1: Comparison of conventional antenna arrays suitable for military applications versus those suitable for the emerging commercial applications [50].

	Conventional (> 50 years)	**Emerging (≈5 years)**
Applications	Military Radar	Wireless Communications Automotive Radar
Typical Range	Long Range (> 1km)	Short Range (< 100m)
Array Size	Large (100-10000)	Small (4-64)
Why an Array?	Focussed, High-Power Beam Multiple, Simultaneous Beams Spatial Interference Cancellation SNR Improvement in RX	SNR Improvement in RX Relaxed PA Requirement Link Reliability (Comm.) Spatial Selectivity (Radar)
Driver (in order)	Performance Size Cost	Cost Size Power Consumption
Realization	Module-based	Single Chip
Technology	III-V	Silicon

In this chapter, after a short review of the phased-array systems from the system analysis in chapter 2, the feasibility, the system architecture and the key components of a low-cost and low-noise mm-wave integrated transceiver for a mm-wave broadband wireless network was analyzed. It is shown that a phased-array with a small number of elements can tolerate the limited performance of the power amplifiers and low noise amplifiers in millimeter wave and, at the same time achieve the required signal to noise ratio for multi-Gb/s wireless communication in a picocell (such as a regular office). Nevertheless, a robust beamforming algorithm is essential to realize the phased-array's potential. For the studied system in chapter 2, it is shown that a 9 or 16 elements of the CMOS phased-array can offer the required performance. The following will present, the low-cost architecture for a phased-array transceiver, and the design and analysis of its key components for a 60 GHz system. Finally, novel beamforming algorithms developed in the group for the phased-array receiver is applied to the proposed system.

3.1.1 Phased-arrays and timed-arrays

The beam steering arrays usually inject variable delay elements in the path of various antennas to/from the receiver/transmitter. These variable time delays once adjusted properly can change the direction of the radiation pattern of the

radiation system without the mechanical movement of the antenna. The time delay elements compensate the delay difference due to the different wave front paths to various antenna elements. Utilizing an ideal time delay element in an antenna array, theoretically offers an infinite bandwidth for the system , as they compensate exactly the same delay in the received signals regardless of signal bandwidth and the carrier frequency. To analyze the behavior of the system, let us consider the time-delay system shown in Fig. 3.1 where the received signal at any antenna is $x_i(t)$ and the signal at the first antenna is $x_1(t) = A(t)\cos(\omega_0 t - \phi(t))$

Therefore for the rest of the signals that we have:

$$x_i(t) = A(t-(i-1)\tau)\cos\big(\omega_0(t-(i-1)\tau) - \phi(t-(i-1)\tau)\big) \tag{3.1}$$

If any of the time delay elements introduces a time delay $\tau_i' = (N-i)\tau$, then the overall signal would be:

$$x_{total}(t) = \sum_{i=1}^{N} A(t-(i-1)\tau-\tau_i')\cos\big[\omega_0(t-(i-1)\tau-\tau_i') - \phi(t-(i-1)\tau-\tau_i')\big] \tag{3.2}$$

After simplification we have:

$$x_{total}(t) = N.A(t-(N-1)\tau)\cos\big[\omega_0(t-(N-1)\tau) - \phi(t-(N-1)\tau)\big] \tag{3.3}$$

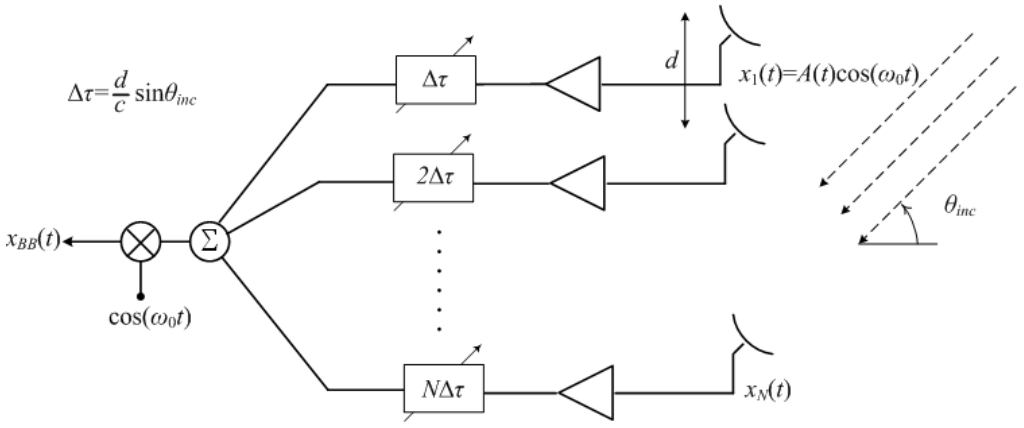

Figure 3.1: Time arrays architecture

Which means the power gain of the coherent signal is N^2 where the power gain of the non-coherent noise is N and therefore, at least theoretically, the SNR is improved by N, theoretically .

In practice, the majority of the systems have a narrow operational bandwidth. In narrowband systems the required time delay can be approximated with the related phase shift over the entire narrow bandwidth. Therefore, the time-delay element can be replaced by a phase shifter and the system essentially becomes a phased-array. Fig 3.2 shows the general block diagram of a phased-array. The

validity of the narrowband approximation of the delay by phase shift is highly dependent on the actual bandwidth of the system. This approximation may fail if the overall bandwidth is moderately high. The phase-shift, apparently aligns the carrier phase of different paths but the modulating signal is not delayed appropriately, which leads to some dispersion in the demodulated signal. A higher modulation-bandwidth-to-carrier-frequency ratio results in larger signal dispersion and hence results in an increased Bit Error Rate (BER) in the wireless communication systems using phase-array radios [17].

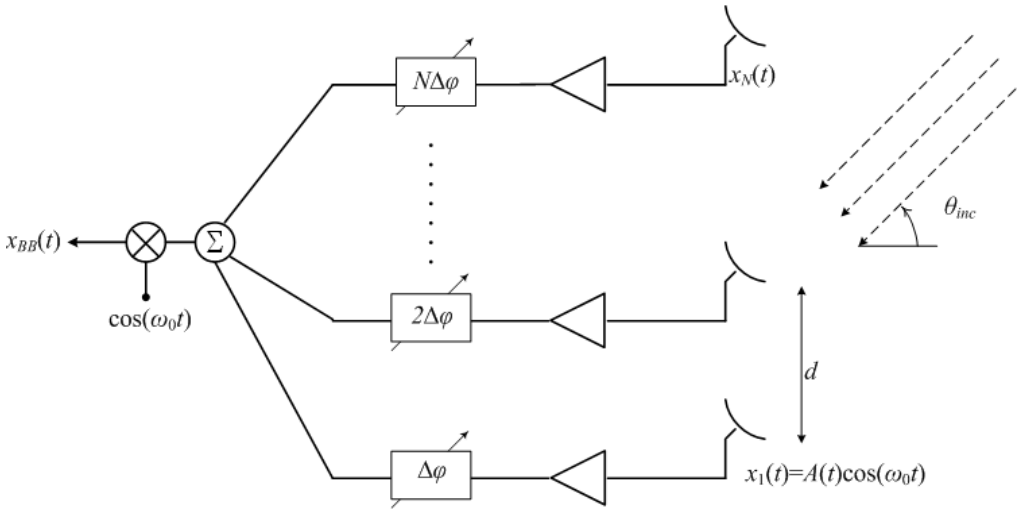

Figure 3.2: Phased arrays architecture

3.1.2 Phased-array architectures

To steer the main beam of the phased-array antenna, phase shifters are incorporated in different stages of a receiver or transmitter and hence, different phased-array configurations can be obtained. These configurations, which are shown in Fig. 3.3, are known as RF Phase-Shifting [51], LO Phase-Shifting [52], IF phase shifting [53] and Digital Beamforming Phased-Arrays [54].

In the RF phase shifting architecture, depicted in Fig. 3.3(a), different RF paths are phase shifted and then combined at RF frequency. The combined signal is then down-converted to the IF or baseband. In this architecture the spatial filtering of the strong undesired signals are performed at the combination point prior to the mixer. Hence, the upper dynamic range requirement of the mixer is relaxed and the level of unwanted in-band inter-modulations after mixer decreases. The design of the phase shifter, however, remains a challenge in this architecture. In addition, the insertion loss variation with the phase change should be small; otherwise, the beamforming gain will deteriorate [55].

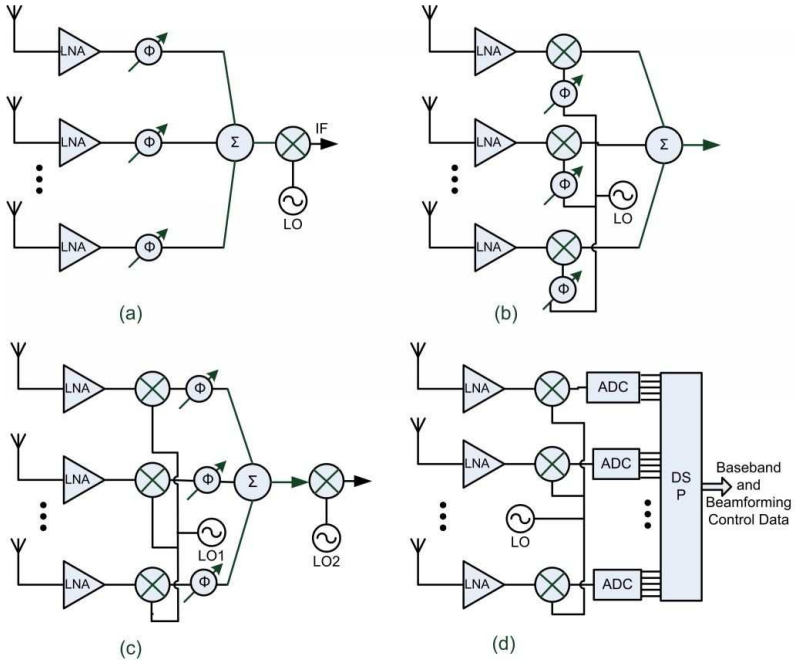

Figure 3.3: Different phased-array configurations (a) RF phase shifting, (b) LO phase shifting (c) IF phase shifting, and (d) digital beamforming array.

The LO phase shifting architecture is displayed in Fig. 3.3(b). The main advantage of this architecture over the RF phase shifting architecture of Fig. 3.3(a), is that since the phase shifter is not in the RF path its loss, non-linearity, and noise performance do not directly affect the receiver performance. However, as compared with the RF phase-shifting architecture, the number of components has increased. This leads to a higher cost of the overall system. Since the combining of signals and beamforming are performed after the mixers, in-band intermodulations are stronger. Also the upper dynamic range of the mixer must be high enough to stand strong interference signals.

Fig. 3.3(c) shows the IF phase shifting architecture. The phase shifters are placed at the first IF stage and the phase shifted IF signals are combined before the down conversion to baseband. As compared to RF phase shifting, some of the challenges in the phase shifter design is relaxed. However, since it needs multiple mixers, this architecture is still not a proper option for a low-cost and low power phased-array transceiver. Fig. 3.3(d) illustrates the digital array architecture. Down-converted to a suitable IF frequency, each RF path is digitized by an Analog-to-Digital Converter (ADC) and all outputs are passed to a Digital Signal Processing (DSP) unit, which executes all tasks of beamforming and recovering of the desired signal from the undesired interferences and noise. The dynamic range of mixers and ADCs must be high enough to withstand the probable strong

Table 3.2: Overall comparison of different phased-array architectures

Architecture	Power Consumption	Cost	Design Challenge
RF Phase-shifting	Low	Low	Efficient front-end Phase Shifter Beamforming Algorithm
LO-Phase Shifting	High	High	Linearity LO distribution Coupling
IF-Phase Shifting	High	High	Linearity LO distribution
Digital Array	High	High	Linearity High dynamic range A/D

interferences. For the emerging systems in the mm-wave band with high symbol rate where the data rate may exceed 2Gbps, very high-speed ADC's are required and to accommodate the required dynamic range each ADC must have a large number of bits which increases the ADC cost and power consumption extensively.

Table 3.2 summarizes the comparison of different phased-array architectures in terms of power consumption, chip area and design challenges. In order to overcome a high path loss and shadowing loss at 60 GHz in addition to a reasonable level of CMOS output power and low noise figure, multiple array elements and thus phase shifters are also required. So from a practical point of view and considering Table 3.2, the most appropriate configuration to lower the cost and power consumption and to achieve an integrated phased-array transceiver is the RF phase shifting architecture if the design challenges can be met properly. For this purpose, designing an efficient front-end as well as developing efficient and novel beamforming algorithms become very important and are the keys to overcome the phase shifter non-idealities and challenges in the RF path.

3.1.3 Integrated phased-arrays on silicon

The success of silicon integration over the last three decades, has burgeoned the vast investments in research and also has led to rapid improvement of device's speed and reliability. Scaling of the transistors, following Moore's law [56], has resulted in faster and smaller devices with better performances and hence lowered the cost for the mass production of the high performance systems.

Originally CMOS was a silicon process optimized for the design of digital circuits using both NMOS and PMOS devices on a common substrate. Multiple layers of metal either copper or aluminum are considered for interconnects. More recent technologies such as CMOS 90 nm, 65 nm and 45 nm offer copper rather than aluminum interconnects for reduced resistivity, and additional extra thick metal

layers for low resistivity connections. Generally, a P-type substrate is used, so PMOS devices are formed inside n-wells. The parasitic effects between adjoining P and N regions produce two cross-coupled common emitter amplifiers in a positive feedback loop. Under certain conditions, these common emitter amplifiers may begin conducting destructively large currents from the supply to the ground. This situation in CMOS process is called latch up [57]. The latch up problem can be solved partly by using a low-resistivity bulk silicon wafer with the resistivity of 0.01-20 Ω -cm, which reduces the equivalent substrate resistance, R_{sub} ,to prevent the transistor from being turned on. This relatively low resistivity is the main source of loss for passive integrated elements and leakage through the substrate, which in turn are particularly problematic for RF applications. For example, in the case of inductors, the eddy currents generated in the substrate contribute significantly to loss leading to a typical on-chip inductor Q of 15-35. While the inductor can be shielded from the substrate by patterned ground shields [58], the shielding increases the parasitic capacitance of the inductors leading to lower self-resonance frequency.

From the perspective of RF systems, the silicon process technology has advanced exponentially over the years, with the state-of-the-art f_t in excess of 200GHz for CMOS and SiGe transistors. Unfortunately, the same scaling that improves transistor speed also leads to lower breakdown voltages.

In spite of these shortcomings, the silicon integration is a very promising solution for millimeter-wave systems because of the great advantages it can offer. The simultaneous integration of the digital baseband circuitry and the analog RF circuits enables mm-wave system-on-a-chip solutions that would improve the performance while lowering the cost. In recent years, there has been several efforts to implement phased-arrays with silicon technologiy in microwave and mm-waves [12, 52, 59–69].

A fully integrated phased-array receiver in 24 GHz on SiGe technology was implemented in [52]. This integrated system uses the LO phase shifting method. Sixteen generated phases from a local oscillator core are distributed to each receiving path to feed the mixer as the LO signal. The appropriate phase for each path is selected using analog multiplexers. The overall gain of this array is 61 dB and it improves the SNR by 9 dB. In [59] a phased-array analog front-end chip and the antennas are realized. A 4-element antenna array is designed and implemented in 0.13 μm CMOS. There, by focusing on the phase shifters which are vector summing type phase shifters, an array of 4 antennas with the beampointing error less than 2 degrees was assembled. The integrated CMOS flip chip containing phase shifters was packaged with antennas in the LTCC substrate. The authors in [12] the first fully integrated 77-GHz phased-array transceiver was presented. The LO Phase shifting phased-array was implemented in SiGe. The effective isotropic radiated power (EIRP) of the 4-element phased-array was 24.5 dBm. In [63] a four element phased-array front-end receiver was reported. This phased-array was implemented on 0.18 μm SiGe technology in the Q-band. The phase shifting method was RF phase shifting and a 4-bit vector sum phase shifter was used to operate at range 30-50 GHz. The authors in [65] introduced a six-element 60-GHz

band phased-array transmitter in CMOS 90 nm technology, with baseband phase shifting method. The step of phase shifting of each phase shifter is 90°. The authors in [64] showed a fully integrated dual-antenna phased-array RF front-end receiver architecture in 60 GHz. The transceiver used RF phase shifting architecture and was implemented in CMOS 0.13 μm technology. The measured phased-array in the receiver achieved a total gain of 34.5 dB which in their design improved the SNR by 4.5 dB. In [68] the researchers at Intel came up with a 60 GHz 32 element bidirectional phased-array TX/RX chip. The design employs RF phase shifting method and the gain of array was 12.4 dB with a 11 dB noise figure. This integrated phased-array which is connected to the package through the flip-chip connection was implemented in CMOS 90 nm technology. In [66] the researchers at IBM introduced a fully integrated 16-element 60-GHz phased-array receiver in BiCMOS technology. The receiver used RF-path phase-shifting architecture and was designed for multi-Gb/s non-line of sight links in the 60-GHz band. In [69] a 4-element phased-array transceiver implemented in 65 nm CMOS was introduced. This array utilizes baseband phase shifting architecture. Each receiver element shows 24 dB gain where the output power of transmitter was 4.5 dBm.

3.2 Phased array system design for mm-wave applications

The proposed mm-wave phased-array system concept, comprising front end and antennas of the mm-wave phased-array is shown in Fig. 3.4. The system is composed of an integrated front-end chip in a flip-chip package attached to the antenna. The connection is through the small balls between the chip and the substrate (Fig. 3.4). This conceptual diagram shows the overall structure

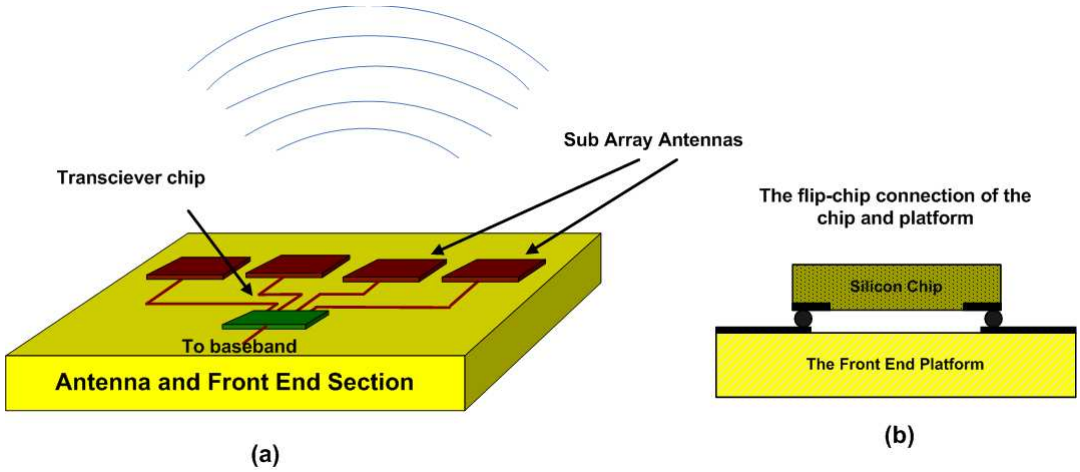

Figure 3.4: Conceptual proposed front end and antennas.

of the system, where the antennas can be designed to be either off-chip or integrated on-chip structures. The block diagram of the phase shifting 60 GHz phased-array transceiver chip is demonstrated in Fig. 3.5. In the receive section, the received signals from different antennas are phase-shifted after amplification by low noise amplifier stages and then combined by a power combiner before the first downconversion. The receiver architecture is a dual conversion architecture. The first mixer downconverts the combined RF signal to the first IF and the second I and Q down-conversion translates the IF signal directly to the baseband. The downconverted baseband signal is amplified and after filtering is converted to a digital signal through two high speed A/D converters in the I and Q channels. A fraction of the IF signal goes to a power detector and provides an estimate of the power level for the beamforming algorithm. The algorithm adjusts the phase shifters (and gain of each LNA if required).

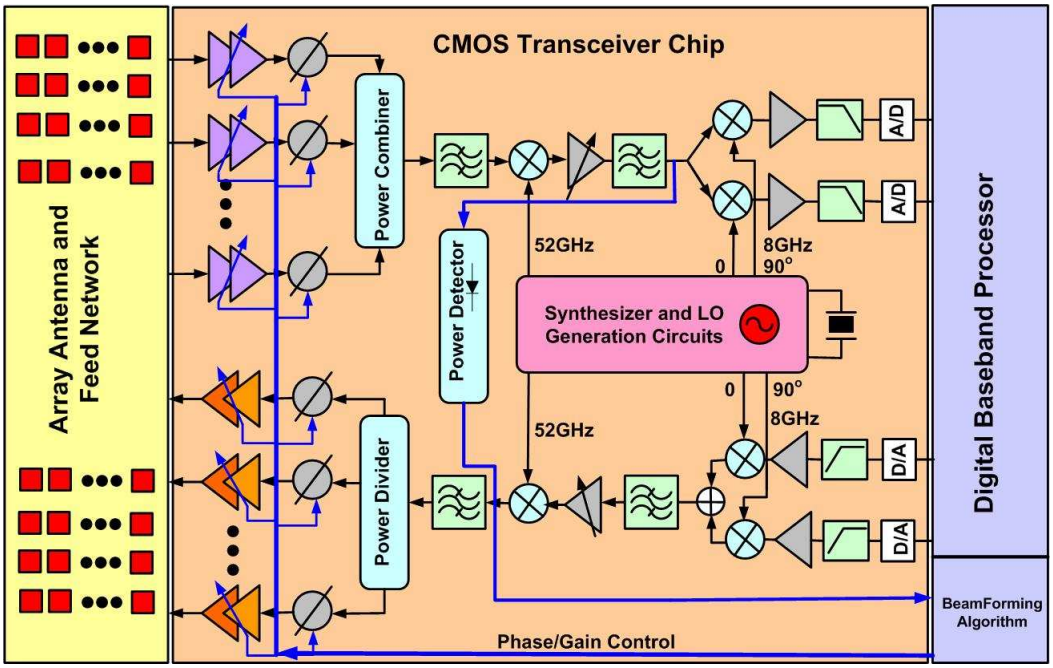

Figure 3.5: Block Diagram of the proposed RF phase shifting 60 GHz phased-array transceiver.

In the transmit section, both the I and Q digital signals are converted to the analog domain through two high speed D/A converters. The harmonics of the converted signals and spurious signals are rejected by two low pass filters. The filtered signal is then up-converted to the IF frequency through the first I and Q up-conversion stage. After another stage of filtering and amplification the signal is up-converted to 60 GHz at the second stage of up-conversion. The LO feed-through and generated spurious at the output of the second mixer are filtered out by the band pass filter centered at 60 GHz. The 60 GHz signal is then divided and applied

to a number of paths. The signal in each path passes through a phase shifter block and experiences a phase shift. The phase shifted signals are then amplified by the power amplifier stages and applied to the sub-array sections of the transmit antenna array. The saturated output power of a 90 nm-CMOS PA is around 10 dBm but to accommodate sufficient linearity for the complex amplitude sensitive modulations such as QPSK or QAM, the output power of power amplifier is set to 2 dBm to keep the PA in its linear operation region.

3.3 Design and analysis of 60 GHz phased-array receiver front-end components

In this section, the criteria for designing a low noise phased-arrays system were presented. To minimize the total noise figure of the system and accommodate the demands for performance, cost-effectiveness and compactness, various design approaches, such as using on-chip versus off-chip antennas, are studied and compared. Finally the overall noise figure of the receiver was calculated.

3.3.1 Overall noise figure of the phased-array receiver

A comprehensive analysis on the received noise at the output of phased-array can be found in Appendix A. The direction of the received signal may affect the level of received noise at the output of the phased-array. For the sake of simplicity, by disregarding the variation of the background noise temperature over the space, a general noise analysis of the system based on the method introduced in [70] was performed. Fig. 3.6(a) illustrates the equivalent noise model of the phased-array receiver. The total received noise, n_0 at the combining point [70] is

$$n_0 = \sum_{k=1}^{M} n_k \ , \tag{3.4}$$

where M is the number of branches, and n_k, the total noise of each branch, is given by

$$n_k = \frac{kT_eB\ g}{L_fL_dL_k} + \frac{kT_0B(L_f-1)g}{L_fL_dL_k} + \frac{kT_0B(NF-1)g}{L_dL_k} + \frac{kT_0B(L_d-1)}{L_dL_k} + \frac{kT_0B(L_k-1)}{L_k} \tag{3.5}$$

where B is the noise bandwidth, T_e is the antenna equivalent noise temperature, T_0 is the room temperature, $k = 1.38 \times 10^{-23} J/K$ is the Boltzmann constant, and g and NF denote the gain and noise figure of the LNA. Also L_f, L_d, and L_k denote the front-end loss from the antenna to the LNA, the downstream loss from the LNA to the phase shifter and the variable attenuation of each channel,

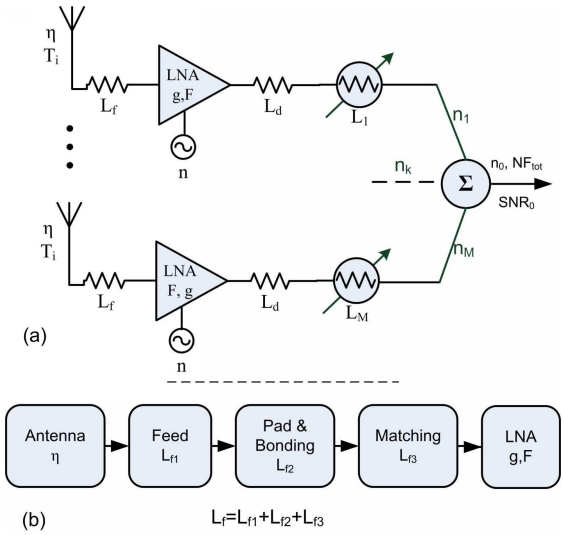

Figure 3.6: (a) The equivalent noise model of a single receiver phased-array antenna. (b)The dominant contributing factors to the total NF of the system.

respectively. Parameter L_k is directly related to the phase shifter characteristic at the operational frequency, and the beamforming algorithm. The antenna equivalent noise temperature is related to the brightness noise temperature (T_b) [71]:

$$T_e \;=\; \eta T_b \;+\; (1-\eta)T_0 \;. \tag{3.6}$$

Assuming all antennas and LNAs are identical, the overall noise temperature of the system is given by [70]:

$$T = T_e + T_0 \left(L_f NF - 1 - \frac{L_f}{g} + \frac{N}{\sum_{k=1}^{N} 1/L_k} \frac{L_f}{g} L_d \right) \;. \tag{3.7}$$

Hence, the total noise figure, is given by

$$NF_{Tot}|_{dB} \;=\; 10 \log_{10} T/T_0 \;. \tag{3.8}$$

If the LNA gain is sufficiently high ($g \gg 1$), the system noise temperature simplifies to

$$T \;\simeq\; \eta T_b + T_0 \left(L_f NF - \eta \right) \tag{3.9}$$

Equation (3.7) reveals that antenna efficiency, front-end loss (L_f), LNA noise figure (NF) and LNA gain (g) have the most significant contributions to the total noise figure of the system. Hence the key issues in designing a low noise receiver are to design an efficient antenna, reduce the front-end loss from the antenna to the LNA, reduce the NF of the LNA and increase its gain. Fig. 3.6(b) illustrates the contributing factors to the total NF of the system. The front-end loss consists

of three components: antenna feed loss L_{f1}, pad/bonding parasitics and loss L_{f2}, mismatch loss L_{f3}.

As an example, table 3.3 shows the results of noise figure calculation for a 16 element phased-array assuming that $T_0 = 290°K$ and $T_b = 400°K$ [17]. The patch array which is explained in next chapter is used as antenna.

Table 3.3: Summary of the parameters used in Noise Figure calculations

Antenna	η	LNA Gain	LNA noise figure	L_f	NF_{Tot}
Patch array	$\geq 90\%$	18.5–25.5 dB	6.1–7 dB	1–3 dB	6.8–9.8 dB

3.4 Beamforming

In this section using a developed method in the group [49], the optimum beamforming for the LOS and NLOS scenarios was studied. More details of the beamforming algorithm is in Appendix B.

3.4.1 SNR calculation at the array output

The received SNR at the array output (combination point), SNR_0 is

$$SNR_0 = SNR_I \frac{G_e(\overrightarrow{\mathbf{r}}) \times G_B(\overrightarrow{\mathbf{r}})}{NF} \tag{3.10}$$

where $\overrightarrow{\mathbf{r}}$ denotes the received signal direction, $G_e(\overrightarrow{\mathbf{r}})$ is the gain of the antenna element and $G_B(\overrightarrow{\mathbf{r}})$ is the beamforming gain (array factor). NF is calculated from (3.8). Finally SNR_I is the SNR received by an isotropic antenna, which is related to the transmitter's $EIRP$ in the direction of receiver antenna, the total path loss from the transmitter antenna to the receiver $L_P(\overrightarrow{\mathbf{r}})$, and the background noise (kT_0B):

$$SNR_I = \frac{EIRP_T(\overrightarrow{\mathbf{r}})L_P(\overrightarrow{\mathbf{r}})}{kT_0B} \tag{3.11}$$

The goal of the beamforming algorithm is to increase G_B to provide the required SNR_0 determined by the BER constraints. The ideal limit of G_B is equal to the number of array elements, however as we will show, the variable insertion loss of the phase shifter reduces the beamforming gain.

3.4.2 Aided beamforming results for LOS propagation

Fig. 3.7 demonstrates the results of the aided beamforming algorithm for a typical case where it is assumed that the equivalent noise bandwidth is 2GHz, the receiver

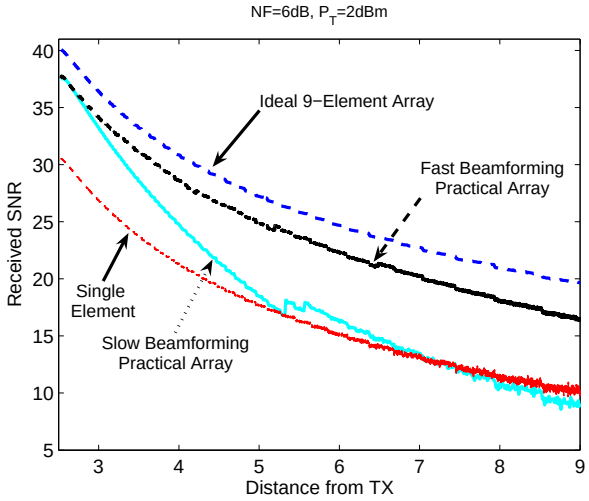

Figure 3.7: SNR for a 9-element Array.

NF is 6 dB, the output power of the power amplifiers is 2 dBm, and the antenna element is the 2×2 patch array shown in Fig. 4.4. In Fig. 3.7 it is assumed that the user is moving away from the transmitter while both receiver and transmitter antenna axes are parallel (to the vertical axis). Fig. 3.7 compares the results of the ideal, fast and slow beamforming for a 9-element array. Slow beamforming is the case where during one iteration of the algorithm user moves more than 1 cm, while in fast beamforming the user's displacement is less than $1mm$. The difference between ideal and fast beamforming when the user is close to the transmitting node ($r \leq 3m$) is 2 dB, however as the distance increases to $r \geq 9m$ this difference raises to more than 3.5 dB.
Another important result of Fig. 3.7 is that the beamforming gain depends on the SNR_I. So as the distance between the portable receiver and the transmitting node increases, the performance of the beamforming degrades. Moreover, the beamforming speed affects the beamforming gain.

3.4.3 Aided beamforming results for NLOS propagation

In this case, location information is not available and the receiver seeks for the strongest signal by running a beam-search mode (acquisition phase). The details of the beamforming algorithm are given in [49]. Fig. 3.8 shows the results of the beamforming when the receiver moves along Path A and B as shown in Fig. 2.5. When the receiver is close to the human body (Path A) the width of the fading region is larger ($x = -0.4m$ to $x = 0.35m$) and the shadowing loss varies from 10 dB to 40 dB. Fig. 3.8(a) shows the array output SNR which is always above 12 dB. Fig. 3.8(b) shows the improvement in the SNR after applying the proposed beamforming algorithm to a 16-element phased-array. This improvement is due

to three factors, using a 16-element array at the access point to increase $EIRP_T$, using a 2×2 patch antenna element at the receiver instead of an isotropic antenna, and the beamforming gain. While the improvement for the LOS section is 28 dB, it increases up to 42 dB in the shadowing region, implying that the proposed beamforming algorithm has an *excess gain* (up to 14 dB) when shadowing occurs.

3.5 Summary and conclusions

In this chapter, we first had a brief review of the phased-arrays and their architectures. Among the four introduced phased-array architectures, RF phase shifting has the minimum die size, consumed power and complexity. However, the challenges such as phase shifter design, efficient front-end and also effective beamforming algorithm need to be resolved in this architecture. After a quick review of the developed phased-array developed using silicon technology in recent years, an RF phase shifting phased-array block diagram was introduced. Based on the channel modeling done in Chapter 2, the beamforming algorithm is applied on the system for both LOS and LOS scenarios and it is seen that with 9 and 16 array elements, one can overcome the free space and shadowing loss at 60 GHz.

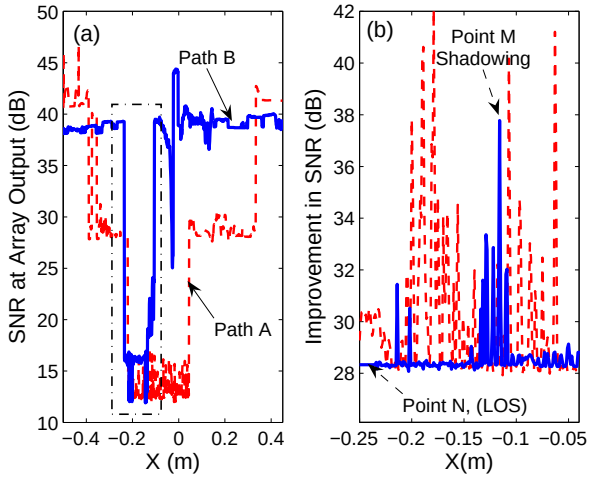

Figure 3.8: Beamforming results for a 16-element array. The dashed and solid curves correspond to the receiver location on Path A and Path B in Fig. 2.5. (a) SNR at the array output after beamforming. (b) The improvement in SNR due to using phased-array for the region shown by a rectangle in Fig. 3.8(a).

Chapter 4

Integrated Antenna Technologies for mm-Wave Systems

4.1 Introduction

Recently, antenna design for 60 GHz short-range wireless communication has become a subject of great interest [72]- [82]. Many of these antennas do not satisfy some of the requirements enforced by the recent 60 GHz standards such as IEEE 802.15.3c [20] released in Dec. 2009, and ECMA 387 [22]. Therefore, antenna design for 60 GHz applications has been a hot research topic in recent years and most probably will continue to be for the next few years.
For emerging mass market millimeter-wave radio networks, the system-on-chip radio modules integrated with compact planar antenna seem to be an attractive solution. A number of on-chip or in-package 60 GHz antennas have been reported so far [73, 74]. They are generally low-gain/low-radiation efficiency structures. Given the very low transmitted power and poor receiver sensitivity of low-cost millimeter-wave technology, such antennas cannot mitigate the severe path loss, which is close to 88 dB for 10 m range at 60 GHz. Some of the designed antennas have a narrow beam [75] (30°), which makes them suitable only for point-to-point applications.

In order to design the antenna for the mm-wave applications, the radiation parameters for the system design, the high volume fabrication and assembly costs should be considered. These days, due to the progress of PCB fabrication and assembly technology, solutions with high performance and decent cost are available. In order to design the antenna for the mm-wave applications, the radiation parameters for the system design, the high volume fabrication and assembly costs should be considered. These days, due to the progress of PCB fabrication and assembly technology, solutions with high performance and decent cost are available. Basically, for the mm-wave systems four types of antennas can be considered, off-chip antennas with connection to the front-end through the wirebond or flip-chip

bonding, off-chip in-package antennas, on-chip antennas, and on-chip in package antennas. The on-chip antennas suffer from a lack of radiation gain and efficiency. Therefore by adding auxiliary elements such as dielectric resonators, the gain and efficiency of the antennas can be increased significantly [82]. The off-chip antenna can be fabricated on a low loss PCB with PCB thick film technology. The cost of this solution is low but the main issue is the insertion loss due to the interconnection as well as the matching elements between the antenna and RF die. In this type of antenna, the insertion loss due to the connection from the antenna to the RF die can decrease the efficiency of the antenna and mitigate the performance of the system. For the off-chip in-package antenna, the antenna can be implemented on the package's PCB or on a high performance passive IC platform such as an IPD (Integrated Passive Device). Using high-performance interconnections such as a flip-chip as an efficient transition from the RF package to the antenna is feasible. However, a portion of power (more than 1 dB) will be dissipated through the flip-chip bonding [66]. The other solution is the on-chip antennas for mm-wave applications. The benefits of using an on-chip antenna is that the matching elements between the antenna and front-end can be removed and the antenna is connected to the RF front-end directly. This facilitates the packaging of the die in the system. The gain and efficiency of the on-chip antenna is very low due to the loss low-resistivity silicon substrate. The efficiency of the antenna can be increased by partially integrating antenna on the die and using on-chip in-package solutions such as dielectric resonator antenna configuration shown in [38,83], antenna performance will be improved.

According to the developed standards introduced in section in section 1.2.1, there are different modes of operations for each device class. For the applications with maximum range (10 m) and Non-Line-Of-Sight (NLOS) signal, the off-chip or off-chip in-package antennas are the better solution, because they show higher gains and have a smaller chip area. For the medium range (3m) applications with Line-Of-Sight (LOS) and NLOS signals, the off-chip or on-chip in-paqckage antennas in the phased-array or single antenna form can be used. For the short range applications (1m) with LOS signal, a single antenna in the form of on-chip antenna or antenna-in-package (AiP) can be utilized. A summary of the antenna options are shown in table 4.1.

In this chapter, based on what was introduced, three antennas were designed and verified. The first antenna is a patch array antenna on a low-loss substrate for the short range applications. The second class is the antenna implemented with IPD technology for the medium or short range applications and the third antenna which is an on-chip DRA with slot antenna for the short range applications.

Table 4.1: Summary of the antenna classes for mm-wave applications

Type	Gain (dBi)	Efficiency (%)	Application	Challenge
Off-chip	5-10	> 80	HD streaming and point-point data transfer	Interconnection to the die, Yield (in mass production), fabrication tolerance
Off-chip (AiP)	4-7	> 60	Docking,Short range HD stremaing, point-to-point data transfer	Fabrication errors, Yield in mass production
On-chip in-package (e.g. with DRA)	0-4	> 50	file transfer, short range data transfer, imaging	Cost, Chip area
On-chip	< -10	< 10	very short range file transfer, imaging	Die area, Low efficiency

4.2 Off-chip wide-beam antenna design

Compatibility with the emerging standards for the 60 GHz spectrum is the starting point for the antenna design. Narrow-band or low-gain antennas do not comply with the aforementioned standard requirements. For example, the bandwidth of an active antenna for WPAN applications in [72] is about 0.8 GHz which is below the bandwidth requirement for 60 GHz devices (around 2 GHz). Finally, the fabrication cost and complexity of the antenna is another major issue which affects its usability. In [79] a high gain with an acceptable bandwidth have been achieved by a CPW-fed integrated horn antenna with a simulated gain of 14.6 dBi. However the size of this end-fire antenna is 32 mm $\times$ 20 mm and requires a complex fabrication process.
Based on the analysis of the two proposed standards for 60 GHz wireless systems, IEEE 802.15.3c and ECMA 387, this work attempts to develop low-cost optimal antenna structures, which can deliver the required antenna gain, bandwidth and beamwidth. Thus, two optimized, 2$\times$2 compact microstrip array antennas are presented. The first antenna is optimized for point-to-point applications which require a high gain antenna. A maximum gain of 13.2 dBi has been measured for an area of 0.25 cm^2. The second antenna is optimized for point-to-multipoint applications requiring a wide beam. The measured beamwidth of this antenna exceeds 76° for an area of only 0.16 cm^2. Both antennas cover at least two channels of the 60 GHz spectrum. The developed antennas can be considered as a low-cost and low-profile (planar) solution for various classes of services described in IEEE 802.15.3c and ECMA 387 standards.

4.2.1 Antenna design and optimization

Three main parameters that must be taken into account to design the antenna element for the mm-wave networking are the maximum radiation gain, the HPBW and the antenna efficiency. The radiation gain and efficiency of the antenna directly affect the link budget design, and the HPBW is a fundamental parameter to determine the antenna coverage. Although employing a high-gain antenna relaxes the signal to noise requirement of the front-end RF system, its narrow beam cannot cover the entire zone for point-to- multipoint wireless connections. In this section, two antennas for different 60 GHz applications are proposed based on the IEEE 802.15.3c and ECMA 387 standards. The first antenna is designed for the maximum gain for point-to-point applications over the maximum distance of 10 m. The second antenna is optimized to give the maximum beamwidth for point-to-multipoint applications such as WPAN. Each antenna is an array of four patch elements. The distances between patch elements are optimized to obtain the maximum gain or beamwidth.
The patch antenna is a planar, high-gain and efficient radiator that can be integrated easily with the rest of the system. A single rectangular patch antenna typically provides 7 dB gain and more than 100° beamwidth when its fundamental mode (TM10) is excited [84].
In this work a very low loss substrate (RT/duroid-5880) with 10 mil height , $\tan\delta = 1 \times 10^{-3}$ and dielectric constant of $\epsilon_r = 2.2$ is used as the substrate for microstrip antennas and the feeding lines. The patch and the ground plane are printed on the top and bottom of the dielectric substrate, respectively. The dimensions of the single patch antenna on such substrate are optimized to achieve the maximum gain at 60 GHz. The size of the patch element is 1.85×1.45 mm^2. The simulations in Ansoft HFSS show that this single patch has 7.7 dBi gain at 60 GHz. The simulated HPBW in E-plane exceeds 96°, but the HPBW in H-plane is limited to 68°.

High-gain antenna design

In this section, an array of four patch antennas is formed, and the x and y spacings between antennas are optimized to achieve the highest gain. Fig. 4.1(a) shows the 2×2 patch array gain versus the patch spacing at 60 GHz obtained by HFSS simulation. It is seen that the maximum gain of 13.5 dBi is achieved for $x = 3.5$ mm and $y = 3.2$ mm. The effect of the feed network on the array gain was also studied. After optimization, it is seen that the maximum gain is obtained for $a_1 = 0.2$ mm and $b_1 = 0.45$ mm. Parameters a_1 and b_1 are shown in Fig. 4.2(a). As shown in Fig. 4.2(a) the size of the patch array for the optimized spacing is 5.35 mm×4.65 mm. Fig. 4.2(b) shows the reflection coefficient of this array. It is seen that this antenna covers two channels of the 60 GHz spectrum from 57.24 GHz to 61.46 GHz. The return loss is always more than 7.5 dB. The resonance frequency is at 59.4 GHz,

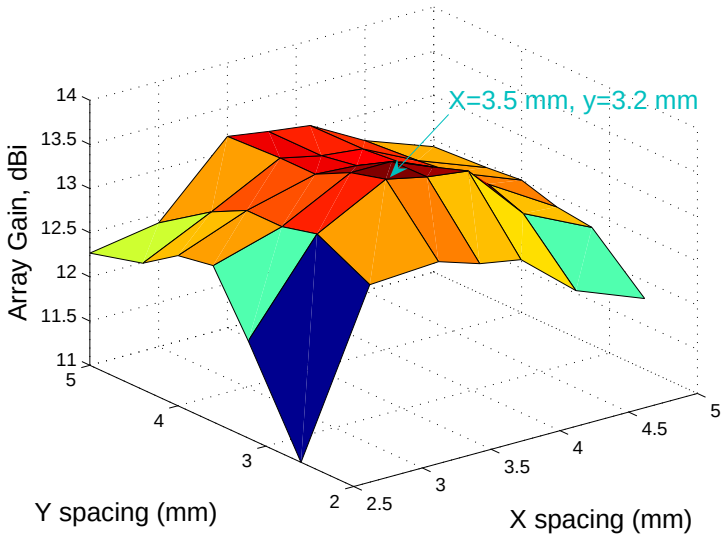

Figure 4.1: Antenna array gain versus patch spacing.

the common edge of the two adjacent channels, therefore the most efficient use of the antenna bandwidth has been achieved. Fig. 4.3 shows the radiation patterns

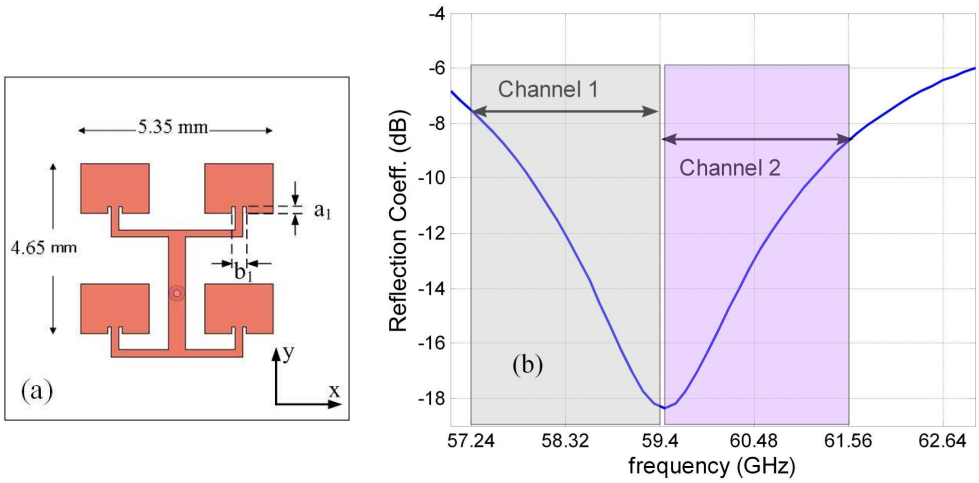

Figure 4.2: (a) Top view of the high-gain 2×2 patch array. (b) Reflection coefficient of this antenna.

of the high-gain 2×2 patch array at E and H-planes. The 3 dB beamwidth of the array in $\phi = 0°$ plane ($x - z$ plane) and $\phi = 90°$ ($y - z$ plane) are $41°$ and $36°$, respectively. The first pair of nulls happen approximately at $\pm 50°$. Fig. 4.3(b) shows that the radiation pattern is symmetric around the normal axis.

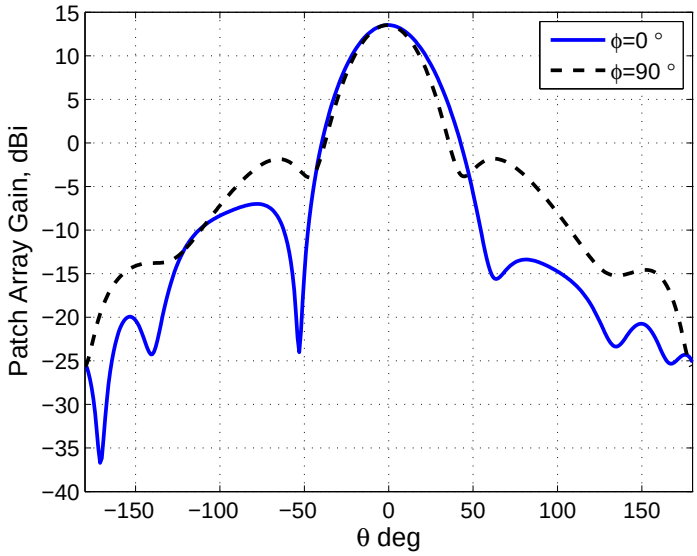

Figure 4.3: 2D radiation pattern of the high-gain 2×2 patch array.

4.2.2 Fan-beam antenna design

To achieve the required beamwidth of 77.5° as discussed in Section 2.2.1, another patch array was designed and the element spacing was optimized to obtain the maximum beamwidth.
Table 4.2 shows the maximum gain of 2×2 array at 57 GHz for different element spacings. It is seen that the gain increases with the element spacing since the effective aperture size increases. For $y \geq 2.6$ mm the maximum gain is always above 10 dBi. We choose $G_a \geq 10$ dBi as a criterion to find the optimum patch spacing. If a higher gain was required two of these fan-beam antennas can be arrayed in the y-direction to give around 13 dBi gain while the maximum beamwidth at $\phi = 0°$ surface is unaffected. Table 4.2 indicates that the element spacing along x-axis must be equal or larger than 2.6 mm to obtain 10 dBi gain. Table 4.3 and Table 4.4 present the patch array beamwidth in the E-plane and the H-plane versus the element spacing. The beamwidth in the E-plane reduces as the element spacing

Table 4.2: Maximum Gain of Fan-Beam Patch Array versus Element-Spacing.

X (mm)	2	2.2	2.4	2.6	2.8	3
Y=2.2 mm	9.35	9.57	9.81	10.05	10.3	10.53
Y=2.3 mm	9.5	9.65	9.9	**10.17**	10.43	10.55
Y=2.4 mm	9.52	9.67	9.91	10.28	10.44	10.62
Y=2.5 mm	9.63	9.7	9.94	10.18	10.25	10.55

increases; however, the beamwidth in the H-plane is almost insensitive to x-spacing for the values shown in Table 4.4. We choose the spacings which lead to the largest E-plane beamwidth while the gain is above 10 dBi. Table 4.3 shows that for $x = 2.6$ mm and $y = 2.3$ mm a beamwidth of 78° is achieved. The size of the patch array

Table 4.3: Beamwidth of Fan-Beam Patch Array in E-plane.

X (mm)	2	2.2	2.4	2.6	2.8	3
Y=2.2 mm	83°	81°	80°	80°	79°	79°
Y=2.3 mm	80°	79°	78°	**78°**	76°	75°
Y=2.4 mm	77°	78°	76°	75°	75°	73°
Y=2.5 mm	75°	75°	75°	74°	74°	74°

Table 4.4: Beamwidth of Fan-Beam Patch Array in H-plane.

X (mm)	2	2.2	2.4	2.6	2.8	3
Y=2.2 mm	55°	50°	49°	46°	44°	40°
Y=2.3 mm	53°	50°	49°	**46°**	43°	41°
Y=2.4 mm	54°	51°	49°	46°	43°	40°
Y=2.5 mm	55°	51°	49°	46°	43°	41°

shown in Fig. 4.4(a), for the optimized spacings is 4.45 mm ×3.7 mm. Fig. 4.4(b) shows the reflection coefficient of the fan-beam 2×2 patch array. The resonant frequency of the antenna is at 59.5 GHz, and the 10 dB bandwidth covers channel 1 and 2 of the 60 GHz spectrum. Fig. 4.5 shows the 2D radiation patterns of the fan-beam 2×2 patch array. The 3 dB beamwidths of the array in the E-plane and the H-plane are 78° and 46°, respectively. The first pair of nulls is far away from the maximum gain direction at ±90°. Hence, any possible rotation or misalignment of the antenna cannot nullify the received signal. Fig. 4.5(b) shows that the radiation pattern in $y - z$ plane is symmetric, while the pattern in $x - z$ plane is asymmetric due to the feed line effect.

4.2.3 Fabrication and measurements

This section describes the test set-up and presents the measured results of both patch antenna arrays.

High-frequency waveguide to microstrip Transition

An accurate measurement requires the minimal interconnect loss between various parts of the test setup. Most of the measuring systems at mm-wave frequency

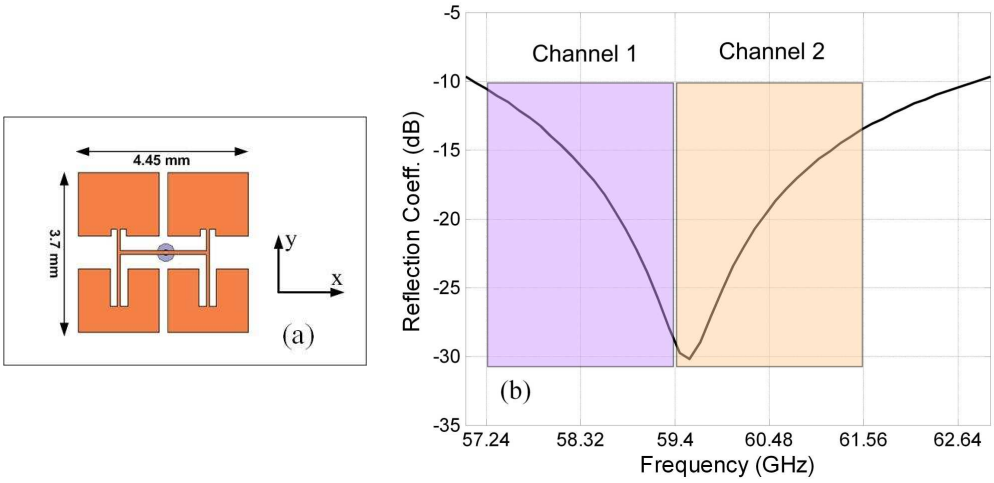

Figure 4.4: (a) Top view of the fan-beam 2×2 patch array. (b) Reflection coefficient of this antenna.

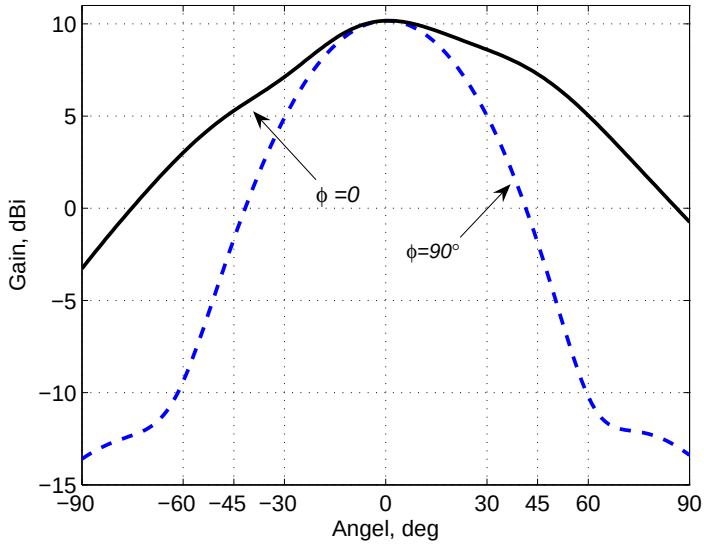

Figure 4.5: 2D radiation pattern of the fan-beam 2 × 2 patch array.

have WR-15 waveguide ports, therefore in this work a low insertion/reflection loss waveguide to microstrip transition (WMT) at 60 GHz band was developed for the characterization of the patch antenna arrays.
To lower the fabrication cost, a two-part machined metallic structure made out of aluminum was designed and fabricated for the transition. For the microstrip antenna connection, a perpendicular coaxial transition was developed. This configuration was preferred to an end-launch type due to the easier implementation

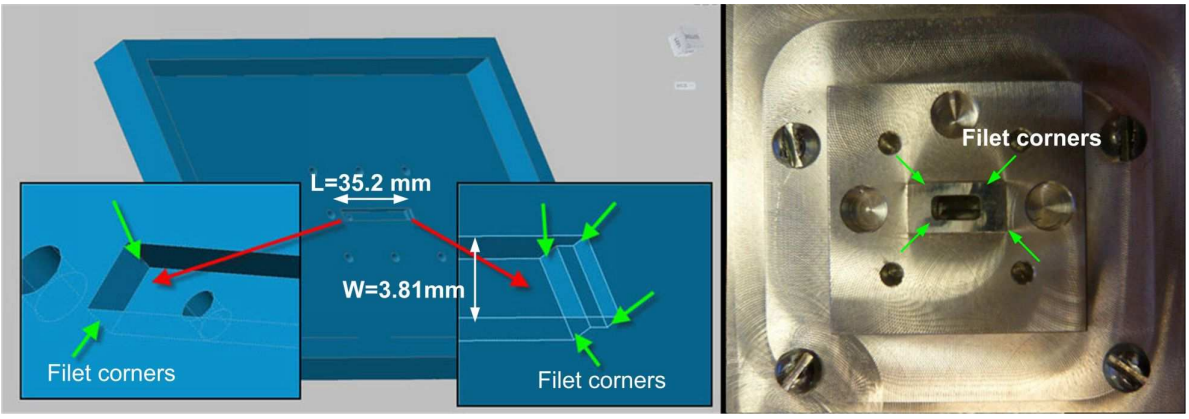

Figure 4.6: Transition design features and manufacturing implementation.

and better narrow-band matching. The cost is also reduced by using simple Corning glass-based 50-ohm coax probes that connect the waveguide section to the microstrip antenna. The narrow air-gap between the two parts of the waveguide assembly creates a discontinuity in the surface current of dominant TE10 mode. This could potentially increase the loss. As a remedy a larger number of sealing screws and a raised ridge was used. The drawing and the picture of the developed WMT are illustrated in Fig. 4.6. The WR-15 waveguide section has a width of the channel is 0.15 (3.81 mm), and the channel length of WR-15 waveguide section was chosen for mechanical convenience. Note that the channel length (L) must include a $0.25\lambda_g$ (the quarter guided wavelength in the waveguide) section between the probe location and the shorted section of the waveguide optimized for matching. In our case, the total waveguide length is close to 7λ (or 35.2 mm). To determine the performance of this WMT, two identical structures were connected in a back-to-back configuration and tested. The measurement setup involves two WR-15 type waveguides, which are calibrated in a 2-port setup, and a coaxial two-sided probe to mate these two identical structures. Fig. 4.7(a) and (b) compare the simulated and measured S_{11} and S_{21} of the back-to-back configuration. The measured transmission S_{21} illustrates that at 60 GHz the insertion loss of this configuration is close to 2.0 dB, which indicates that a single WMT has around 1.0 dB loss. The information provided by Fig. 4.7(b) is used to de-embed the insertion loss of WMT from the measured antenna gain in next section.

Measurement results

Fig. 4.8 shows the fabricated 2×2 patch antenna arrays. The antennas were mounted and attached to the transitions described earlier. The antennas combined with WMT were simulated in HFSS to see the effects of the transition on the reflection coefficient of the antennas. Fig. 4.9(a) and 4.9(b) show the measured and simulated S_{11} of the high-gain and fan-beam 2×2 patch antenna arrays, respectively. The bandwidth of the high-gain and fan-beam antennas is 3.5 GHz and 3.6 GHz

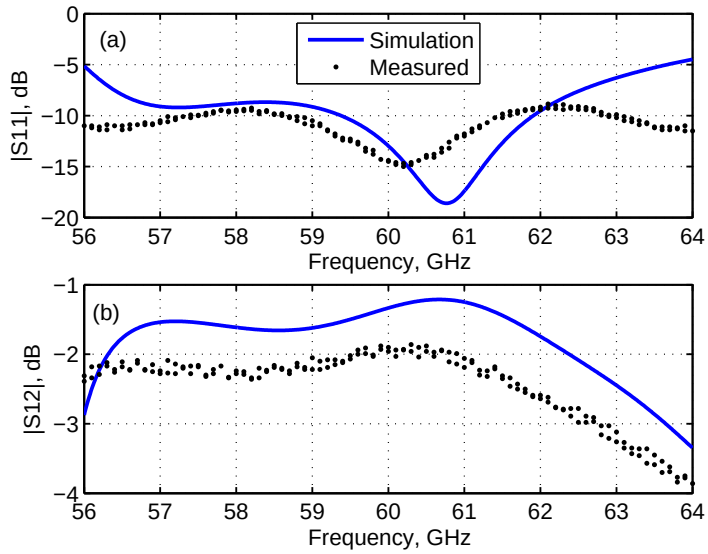

Figure 4.7: Performance of the back-to-back configuration of two microstrip to waveguide transitions. (a) S_{11}. (b) Insertion loss S_{21}.

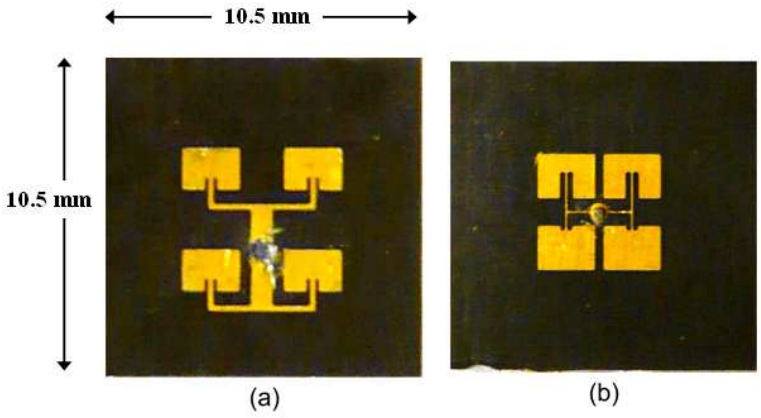

Figure 4.8: Fabricated high-gain and fan-beam 2×2 patch array antennas.

around 60 GHz and 61.70 GHz, respectively. As it is shown in both figures, there is more than one resonance over the frequency range 50-75 GHz. These resonances show the non-radiating cavity modes of the waveguide section of WMT. This was experimentally verified by using absorbers to suppress the radiating fields into free space. While the resonances of the radiating modes were affected significantly, the non-radiating cavity modes did not change, enormously. Comparing these figures to Fig. 4.2(b) and Fig. 4.4(b) and considering the good agreement of HFSS simulations and the measurement results, we can conclude that the array antennas without WMT met the required bandwidth specifications for the aforementioned wireless standards.

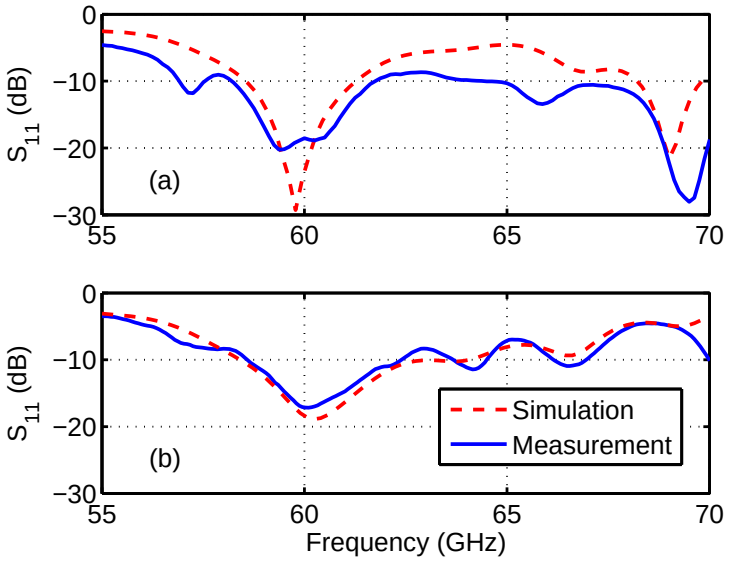

Figure 4.9: S_{11} Simulation and Measurement results of the 2×2 patch array antennas connected to the waveguide transitions. (a) High-gain antenna. (b) Fan-beam antenna.

Fig. 4.10 shows the measured co-polarization and cross-polarization radiation pattern of the high-gain 2×2 patch antenna array at 60 GHz frequency. The maximum measured gain at this frequency is 13 dBi after de-embedding the insertion loss of the WMT (see Fig. 4.7) and considering the 0.3 dB loss for the coaxial probe which feeds the antenna. The measured beamwidth is 42°. Comparing this figure to Fig. 4.3 which shows the simulated gain and radiation pattern, it is found that the maximum gain at 60 GHz has dropped by only 0.5 dB. The measured beamwidth and overall pattern shape are in very good agreement with the simulated values. The maximum cross-polarization gain of the high-gain array with respect to its co-polarization gain is at least -10 dB which is at $\theta = 40°$. Fig. 4.11 depicts the measured co-polarization and cross-polarization radiation pattern of the fan-beam antenna at 60 GHz. The HPBW of the fan-beam antenna

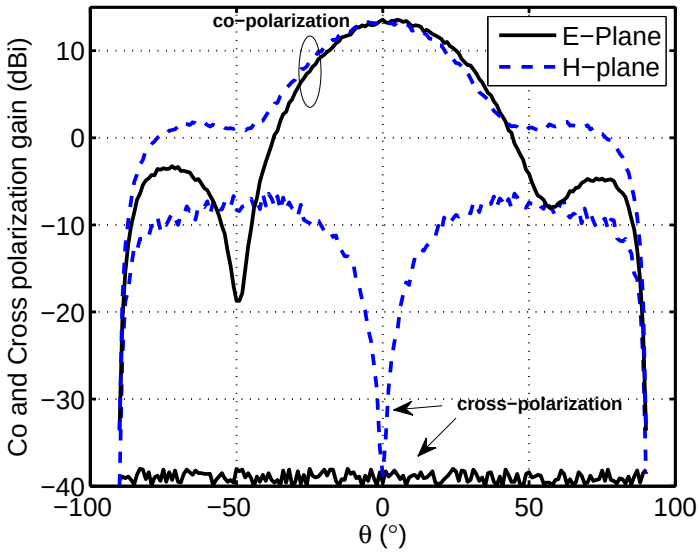

Figure 4.10: Measured co-polarization and cross-polarization radiation patterns of the high-gain 2×2 patch antenna arrays at 60 GHz frequency.

is 76° and its maximum gain is 10.3 dBi. Comparing this figure to Fig. 4.5 shows that the agreement between simulated and measured patterns is very good. The beamwidth has slightly decreased (by about 2 degrees) which is within the fabrication tolerances. The cross polarization gain of the fan-beam array antenna is at least 25 dB less than the co-polarization term at any direction. Fig. 4.12 depicts the measured maximum gain of patch antenna arrays over the frequency range of 55-65 GHz after de-embedding the insertion loss of WMT. The maximum gain of the high-gain array varies from 12.25 dBi at 57 GHz to 13.25 dBi at 65 GHz. For the fan-beam array, the maximum gain varies from 9.5 dBi at 57 GHz to to 10.5 dBi at 61 GHz. So, the variation of the radiation gain of both antennas over 7 GHz bandwidth (57-64 GHz) is less than 1 dB.

4.3 A 60 GHz on-chip slot array antenna in silicon integrated passive device technology

One important application of the 60 GHz spectrum is transferring data in a Line-of-Sight (LOS) path over a distance less than 3 m [20]. Fast downloading and live video streaming with very low power and compact implementation with data rates up to 3.4 Gbps are two widely advertised examples [85]. A key problem that needs to be investigated in such applications is the integration of the antenna with the rest of the radio circuit in a miniaturized package. Several off-chip antennas and Antennas-in-Package (AiP) have been proposed for the millimeter-wave wireless

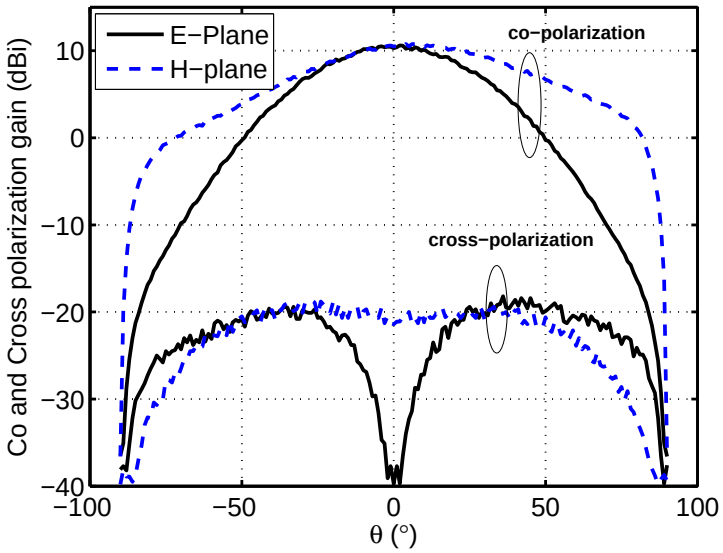

Figure 4.11: Measured co-polarization and cross-polarization radiation patterns of the fan-beam 2×2 patch array at 60 GHz frequency.

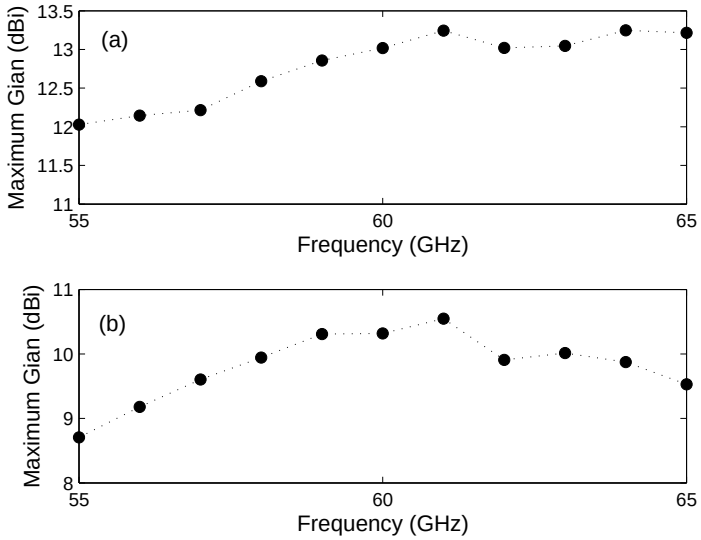

Figure 4.12: Measured maximum gain of patch antenna arrays over the frequency range of 55-65 GHz. (a) High-gain array. (b) Fan-beam array

applications in literature [72, 73, 75, 78, 79, 86] Partly or fully on-chip antennas are essential for implementing fully integrated radio systems in ultra-compact modules. Using an on-chip antenna significantly simplifies the matching network and improves the system performance through reducing the front end loss and

noise figure. However, the required antenna gain cannot be achieved by an on-chip antenna on standard silicon substrate such as CMOS and SiGe due to the low resistivity requirement of such substrate for active devices. Techniques such as micro machining to remove the low resistivity substrate under the antenna [87] or on-chip dielectric resonator antenna [88] have been proposed to increase the efficiency of the on-chip antenna. Fabrication complexity, cost and packaging are the issues for high volume production using such techniques. Reduction in the area and the fabrication cost of antenna, and increase in the radiation efficiency and gain improvement are necessary to realize low-cost millimeter wave devices suitable for high-volume market.

This section presents a microstrip-fed slot antenna implemented using a low-cost Integrated Passive Device (IPD) technology. IPD technology provides a unique opportunity to implement low-cost and efficient millimeter-wave integrated antennas in silicon with a low cost. The antenna has been designed and optimized to operate in at least two channels of the 60 GHz band with more than a 5 dBi radiation gain. The entire size of the die is $2mm \times 4.5mm$. The proposed miniaturized antenna in a flip-chip die can be integrated with other active elements of the mm-wave systems in the same to obtain a fully integrated 60 GHz radio.

4.3.1 IPD technology

IPD technology provides a unique integrated technology platform for the implementation of low loss, high-Q (Quality factor) and low profile passive elements for RF components such as filters, baluns, couplers and duplexers on using silicon technology for a wide range of RF/microwave and millimeter-wave integrated system applications. This technology employs high resistivity silicon as the substrate versus the low resistivity silicon substrates in CMOS and SiGe technologies. Fig. 4.13 shows the cross section of the metal layers and the silicon of this technology provided by ON Semiconductor Company [89]. The technology is a three metal layer process with two 5 μm copper layers and one 2 μm aluminum layer. There are two options of wirebonding and flip-chip for the pad. The feasibility of the mm-wave antenna on IPD technology was first introduced by authors in [90]. Recently a few papers were published on the design of on-chip antennas in this technology [90–93]. This section demonstrates the high gain millimeter wave on-chip antennas in this technology as well as their measurement results.

4.3.2 Antenna-in-package design

Flip chip assembly is known as one of the best solutions for the interconnection from the RF chip to the antenna at millimeter-wave band for AiP systems [75, 94].

In this section, using the benefits of IPD technology for implementing miniaturized and integrated on-chip antennas, a slot radiator is designed. This antenna

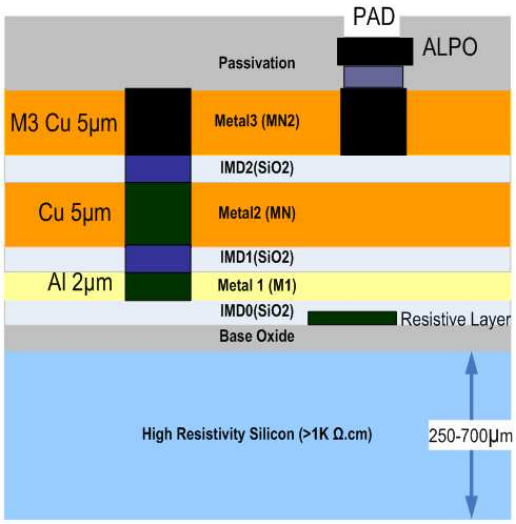

Figure 4.13: A cross section of ON semiconductor IPD technology

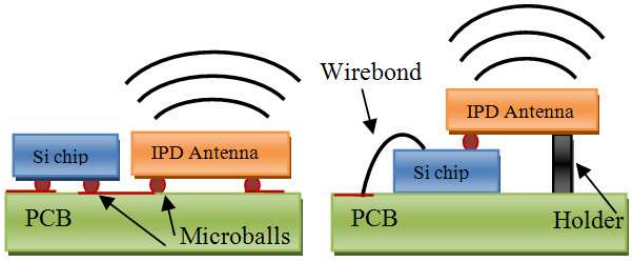

Figure 4.14: The conceptual block diagram of the IPD antenna and their integration with the entire system

which radiates through the back of the silicon substrate can be integrated with the RF front-end in a same package using the flip chip interconnections. Fig 4.14 shows the conceptual block diagram of the possible options for integrating this antenna in a package. The antenna can be assembled over a PCB as shown in Fig 4.14a. The IPD antenna is linked to the RF chips through the transmission lines over the PCB. The alternative option is to assemble the IPD antenna directly over the RF chip which is shown in Fig 4.14b. The DC and baseband connection to the PCB from the silicon chip can be made with the wirebond interconnections. The link budget design for applications under 3m range shows that high efficiency antennas with a minimum gain of 5 dBi can satisfy the radiation gain requirement [95]. There are several options to implement the miniaturized and integrated antennas at mm-wave frequency ranges. The slot antenna is one of the best options to implement antennas at 60 GHz. One of the main issues in designing the antennas with silicon technology is the effect of the dummy filling metals close to the main radiator. This issue becomes more critical when the antennas are excited by electric

currents realized by antennas such as metallic dipole [74] and Yagi [96]. Conversely, slot antennas are principally implemented over the ground plane. Therefore, the dummy filling metals have negligible parasitic effects on the radiation characteristics of the antenna. Slot antennas can be fed either by a CPW line or microstrip couple line. With this technology, since we can use the low loss high resistive silicon as a superstrip, the slot should be implemented over the bottom metal line. Therefore microstrip line coupling is the most efficient way of excitation. In this design, the signal trace and the ground of the microstrip line has been implemented over the M1 and M3 metal layers, respectively. The thickness of the dielectric between M1 and M3 (SiO2) is $14\mu m$. Therefore, the width of a 50Ω microstrip line becomes $8\mu m$. A rectangular slot is inserted in the ground of the microstrip line. The power transferred through the microstrip line would couple into the slot line which is located under the microstrip line. The slot as a magnetic current source will deliver most the coupled power into the high resistive silicon substrate. The thickness of the silicon substrate is $280\mu m$ with the relative permittivity and conductivity are $\epsilon_r = 11.9$ and $\sigma = 0.1S/m$, respectively. The analysis of the microstrip-fed slot radiating in the air is reported in [97] and [97]. Their results for designing the initial dimensions of the slot can be used with some considerations. The length of the slot is half wavelength; where $\lambda_g = c/\epsilon_{eff}$. The slot is between the silicon substrate and thin silicon dioxide layer, therefore $\epsilon_{eff} \approx \epsilon_{r,silicon}$ and $\lambda_g \approx 1.45mm$.

The slot has been optimized in Ansoft HFSS to have a good matching at the microstrip line input port, as well as maximizing the efficiency of the antenna at 60 GHz. The optimized dimension of the slot is $700\mu m \times 150\mu m$. The HFSS simulations show that the gain of a single element is about 3 dBi. Theoretically, the radiation gain of a slot which is radiating in free space is 1.5 dBi. In this structure, the high resistivity silicon layer guides the radiation in the direction of dielectric substrate and increases the gain by 1.5 dB. The next step to design a higher gain antenna is using an array of the aforementioned slot. A 2-by-1 array of the slot has been designed and optimized. Fig. 4.15a shows the structure of the antenna used in the HFSS simulator. The spacing of the elements is 0.4λ which is 2 mm. λ here is the free space wavelength at 60 GHz. The microstrip feed network has been designed to feed both antenna elements and match the input impedance of the antenna array to 50Ω. The entire chip area is $2mm \times 4.5mm$. The die micrograph of the slot array antenna is shown in Fig. 4.15b.

The simulation results of the antenna shows that maximum radiation gain is along the $\theta = 180^\circ$ direction. As expected, since the silicon substrate is at the bottom of the antenna, most of the power would be radiated through the high resistivity silicon. The simulated and measured radiation gain and pattern of the antenna are explained more in the next section.

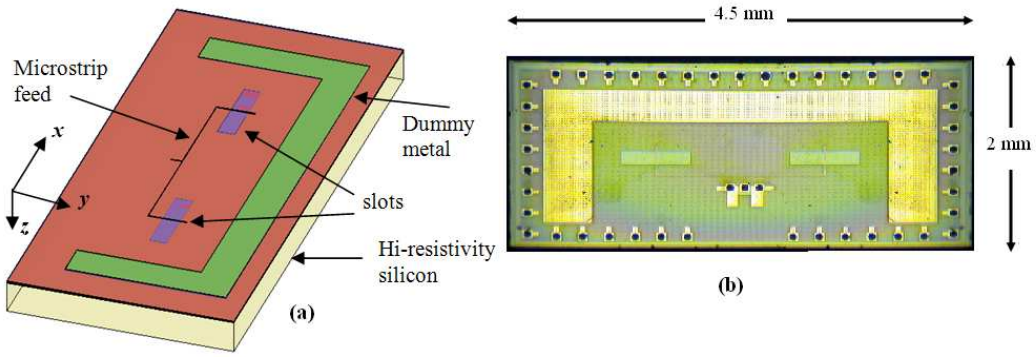

Figure 4.15: (a)3D schematic of the slot array antenna in IPD technology. Microstrip feed and slots are over M3 and M1 layers, respectively. (b)Die micrograph of top view of the antenna.

4.3.3 Measurement setup and measurement results

In order to measure the radiation pattern of the antenna array structure, a recently developed in-house on-wafer pattern measurement system, shown in Fig. 4.16, was used [98]. As shown, the system is composed of a metallic table with a hole in the middle for holding the antenna-under-test (AUT).

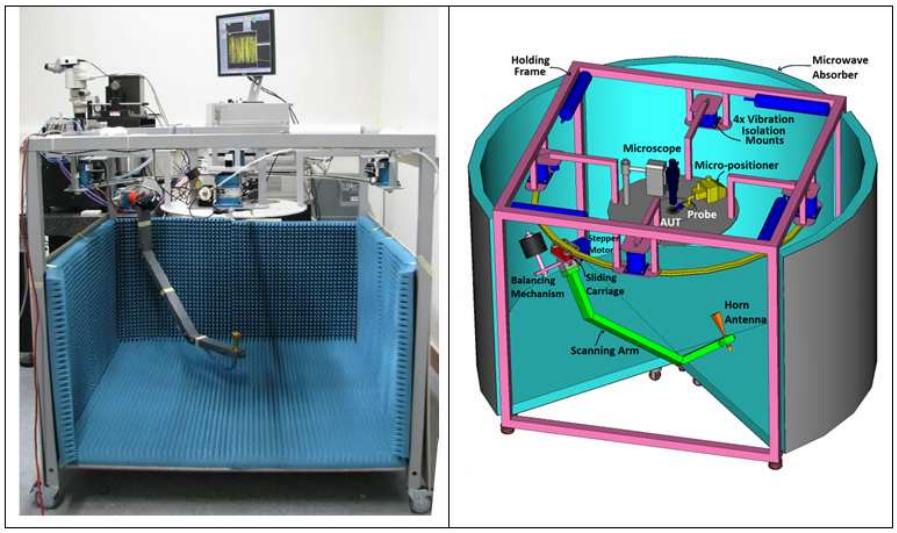

Figure 4.16: On-wafer measurement system used to measure the manufactured antenna array.

In the measurements introduced in [92] and [93], the probe is contributing to the radiated field and therefore the radiation of the antenna cannot be separated from that of the probe accurately. The present measurement system is designed specifically for the antennas which are fed from one side and radiate to the other

side. In these cases, the metallic table would increase the accuracy of the pattern measurements by reducing the effect of GSG probes on the radiated power form the antenna. For the antenna array investigated here, the AUT is probed by a 150-μm-pitch-GSG probe from the top side and it radiates to the bottom. The radiated power is then captured by a standard horn antenna mounted on a rotating arm. The arm can be controlled in the azimuth plane manually while it is controlled electronically in the elevation plane. Note that, the inaccuracy in the measurement results is estimated as $\pm 0.5dB$ for the broad-side direction and $\pm 0.9dB$ for the end-fire direction, respectively. The simulation and measurement results of the normalized radiation pattern and the gain of the antenna are shown in Fig. 4.17 and Fig. 4.18, respectively. The simulations show that the maximum gain of the antenna is 5.3 dBi and the beamwidth of the antenna is 100° and 65° at $\phi = 0°$ and $\phi = 90°$ planes, respectively. The measurement results are in a good agreement with the simulated results for both radiation pattern and gain. The measured gain of the antenna is more than 5 dBi at 60 GHz which shows that by using an array of two slot antenna, we can increase the gain of the single element by more than 2 dBi.

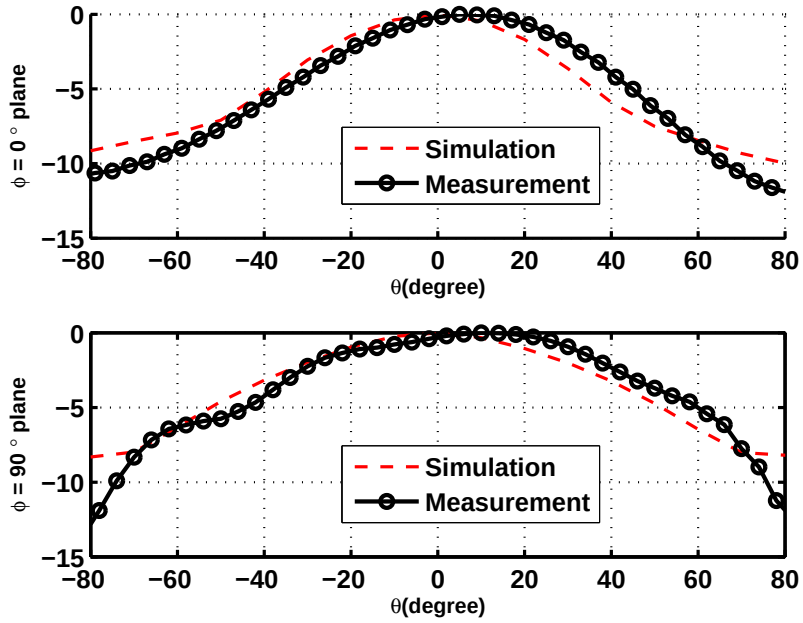

Figure 4.17: The normalized radiation pattern of the antenna at $\phi = 0°$ and $\phi = 90°$ planes versus θ

The measured radiation pattern has a wider beamwidth which could be due to the fabrication errors and measurement inaccuracies. The measured 3 dB beamwidth of the antenna at $\phi = 0°$ and $\phi = 90°$ planes are $\phi = 105°$ and $\phi = 76°$, respectively. The simulated efficiency of the antenna is 80% at 60 GHz.

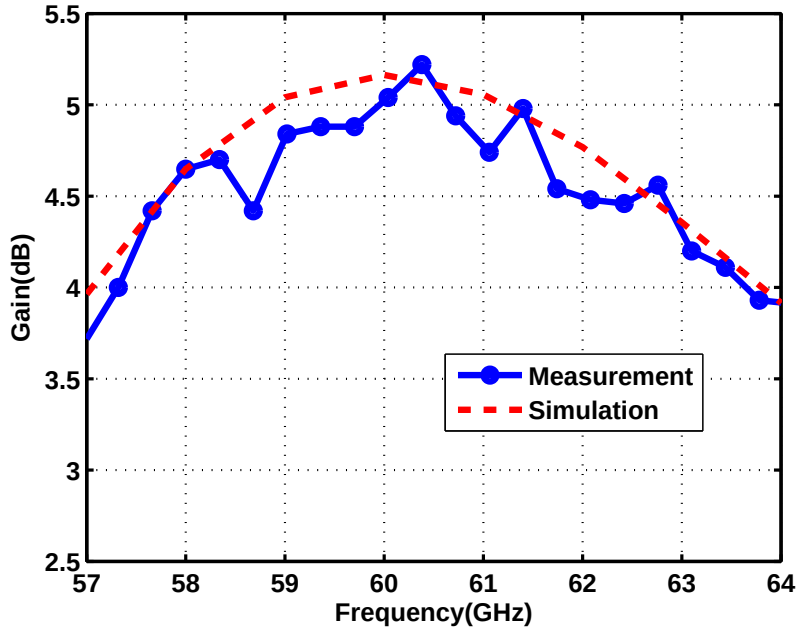

Figure 4.18: The simulated versus measured gain of the IPD antenna at the range 57-64 GHz.

The measured and simulated S_{11} of the antenna are shown in Fig. 4.19. The antenna shows a return loss better than 10 dB over the frequency band 57-64 GHz. The presence of the high-resistivity silicon increases the operational bandwidth of the antenna. The impedance bandwidth of the antenna is more than 7 GHz. The comparison of performance of this antenna with other state-of-art on-chip antennas at 60 GHz is show in table 4.5.

Table 4.5: The comparison of state-of-art on-chip antennas performance.

Ref.	Process	Architecture	Freq(GHz)	BW(GHz)	Gain(dBi)	Area(mm^2)
[74]	CMOS	Dipole	65	10	-12.9	1.04
[96]	CMOS	Yagi	60	10	-10.6	10.45
[92]	IPD	Slot	60	10	3.5	1.7
[93]	IPD	Yagi	60	11	6	17.4
This antenna	IPD	Slot	60	7	5	9

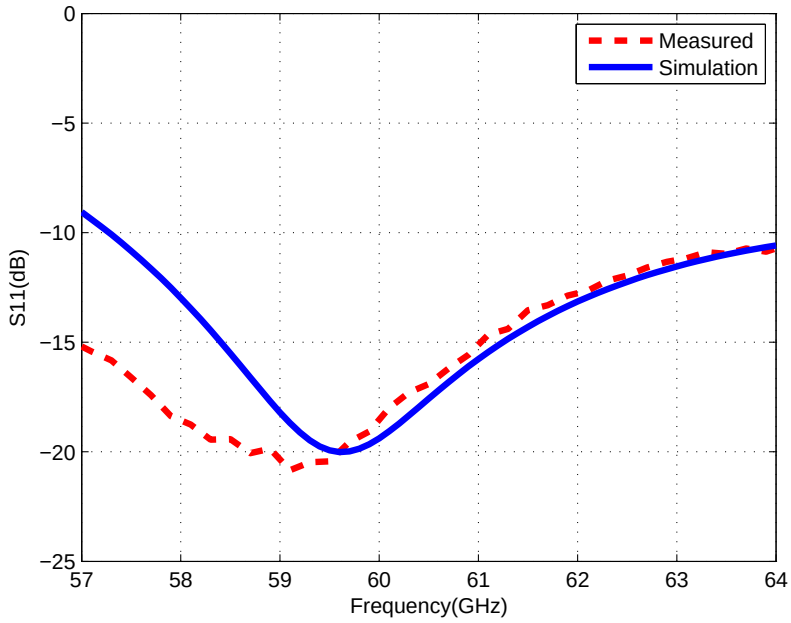

Figure 4.19: The measure and simulated S_{11} of the antenna.

4.4 CPW-fed chip-scale dielectric resonator antenna for mm-wave applications

In CMOS technology, the effective use of chip area has major importance and the corners of chip are the places which are wasted in some of designs. In this section, the effective employment of the chip area is accomplished by placing the antennas at the corners. Moreover, the CPW structure is employed because of low dispersion and compatibility to the other active RF components such as the Low Noise Amplifier (LNA) and the Power Amplifier (PA) [99]. In addition, the CPW line is desirable due to its straightforward excitation for on-wafer measurements using Ground-Source-Ground (GSG) probes. In this section two resonance structures including the CPW-fed slot antenna and the Dielectric Resonator Antenna (DRA) are combined together to yield an efficient antenna with a fairly wide bandwidth at 60 GHz [100]. The slot type I and slot type II designs proposed for CPW-Fed slot are shown in Fig. 4.20(a) and (b), respectively. The slot can be implemented on the top thick metal of any IC technology.

Both of the CPW-Fed slots and DRs should resonate at the same frequency to provide the optimization goals such as higher gain and wider bandwidth. To this end, the dimensions of the DR should be adjusted in a way to have the appropriate resonance mode at 60 GHz. The available materials from the commercial supplier (TCI Ceramics) for the design are the ceramics with ϵ_r=12 and ϵ_r=36. The quality factor of the rectangular DRs is inversely proportional to the relative permittivity of

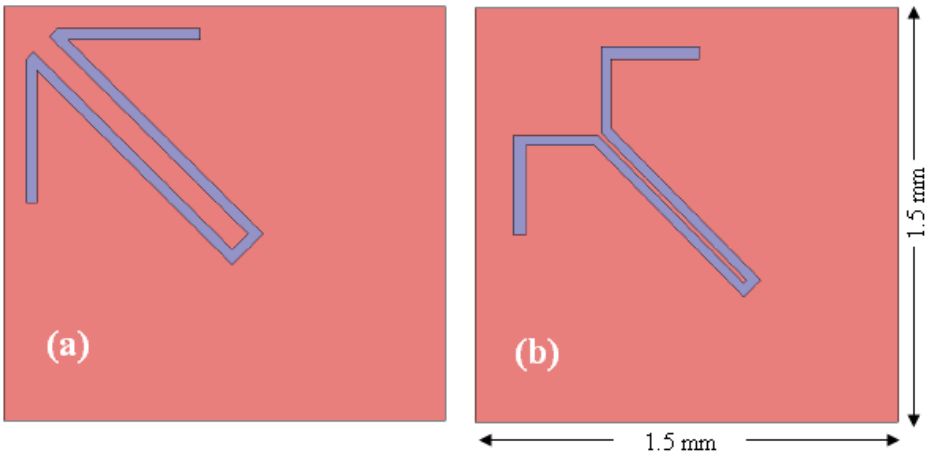

Figure 4.20: (a) CPW-Fed slot of type I; (b) CPW-Fed slot of type II

the dielectric [101]. This effect results in a wider bandwidth for ϵ_r=12 and a higher efficiency for ϵ_r=36. Furthermore, the materials with higher relative permittivity leads to smaller DR dimensions for the specific resonating mode at the design frequency.

By investigating the resonant modes of the rectangular dielectric, it is apparent that two modes of operations offer better radiation behavior due to the stronger tangential components of the electric field on the surface of DR. One of these two modes stated above is the low order mode of this structure shown in Fig. 4.21(a), and the other is higher order mode shown in Fig. 4.21(b). The former can be achieved by having a smaller size, however the latter provides better radiation results in term of gain of the antenna.

The dimension of the CPW-fed slot should be designed and optimized to merge the resonant frequency of the CPW-fed slot and the DRA in order to maximize the power coupled into the DRA. Furthermore, the dimensions can be designed such that the input impedance of the antenna can be matched to 50Ω. The design and optimization of these structures are accomplished by Ansoft HFSS.

By sweeping the position and direction of the dielectric on the slot, different results for the bandwidth and maximum gain were observed. To determine the best design, a figure of merit is defined as the product of the bandwidth and maximum gain of the antenna. Based on this figure of merit, antenna type I and antenna type II were the best ones which are shown with same scale in Fig. 4.22(a) and (b), respectively.

In antenna type I, the DR with ϵ_r=12 is fed by CPW-Fed slots of type I while in antenna type II, the DR with ϵ_r=36 is excited by CPW-Fed slots of type II. It is worth mentioning that in these cases the field distribution of slot coincide with field distribution of resonance mode of dielectric. As expected, due to using the DRA with ϵ_r=36 and the exciting dominant mode, the DRA height of antenna type II

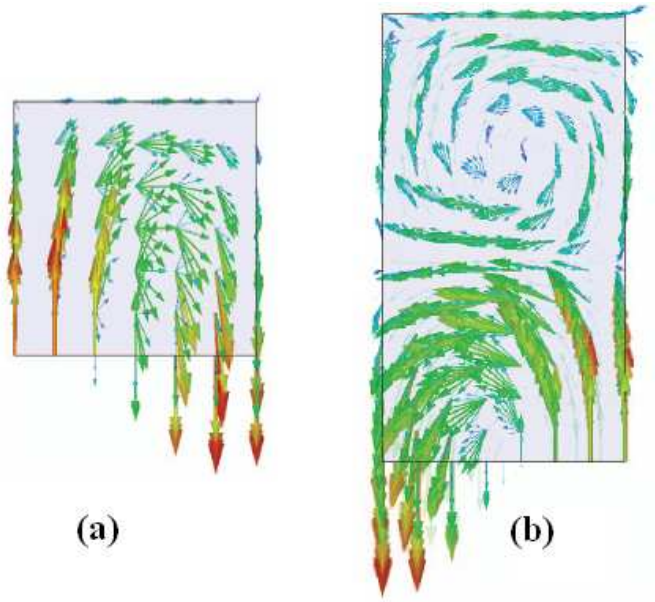

Figure 4.21: (a) Low order resonant mode of the rectangular dielectric; (b) Higher order resonant mode of the rectangular dielectric

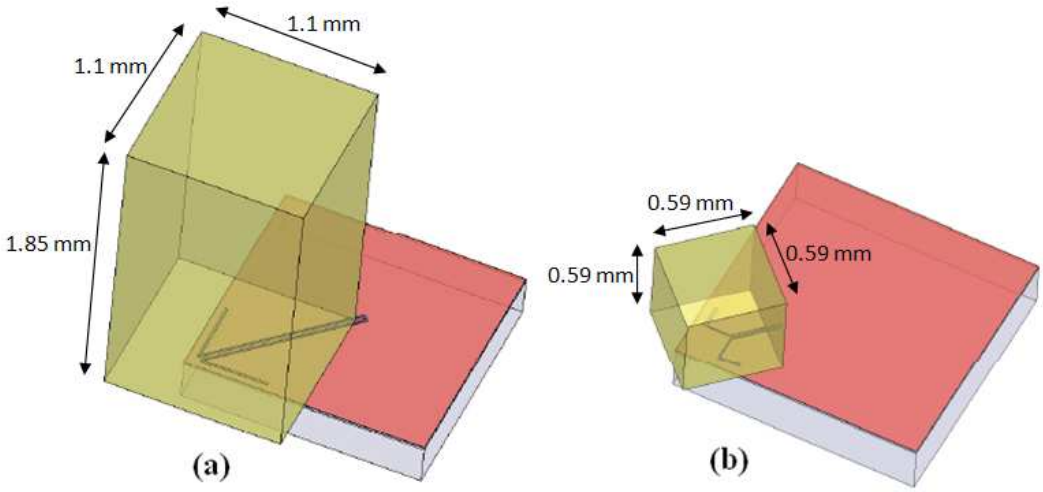

Figure 4.22: The optimized structure in HFSS (a) Antenna type I excited with slot type I and DR with ϵ_r=12 (b) Antenna type II excited with slot type II and DR with ϵ_r=36.

is much smaller providing a low profile structure. The chip area in both designs is $1.5mm \times 1.5mm$. The dimensions of the DRs are $1.85mm \times 1.1mm \times 1.1mm$ in antenna type I and $0.59mm \times 0.59mm \times 0.59mm$ for antenna type II.

4.4.1 Simulation results

The various radiation results of these two designs are obtained by HFSS. The radiation pattern of the antenna type I and antenna type II is shown in Fig. 4.23(a) and Fig. 4.23(b), respectively. The maximum gain of antenna type I is 2.52 dBi and the antenna type II featuring maximum gain of 3.6 dBi at 60 GHz.

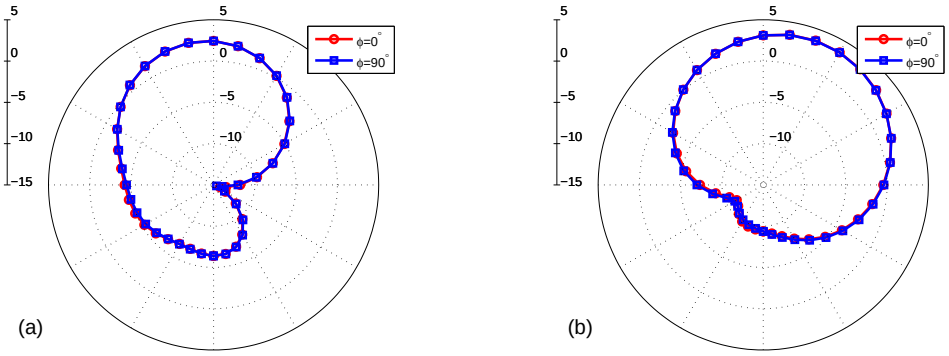

Figure 4.23: Simulated gain of antenna type I at $\phi = 0°$ and $\phi = 90°$ (a)Type I (b)Type II

Additionally, the simulated S_{11} of the designs is represented in Fig. 4.24(a) and (b), respectively. The 10% bandwidth for antenna type I is wider in comparison to antenna type II having 6.7% bandwidth. The bandwidth of the antenna is defined as a part of frequency range in which S_{11} is less than 10 dB. Ultimately, the radiation efficiency of these designs is calculated by HFSS which is 40% for antenna type I and 72% for antenna type II at 60 GHz.

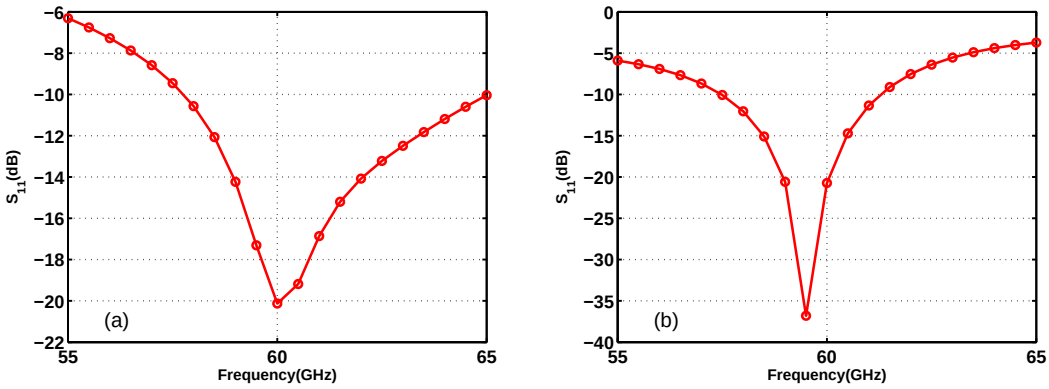

Figure 4.24: (a) Simulated S_{11} of antenna type I. (b) Simulated S_{11} of antenna type II.

This design is under fabrication and measurement and the measured results along with the comprehensive study of the radiation characteristic will be published in future academic publications.

4.5 Chapter summary and conclusions

In this chapter, first the two optimized 2×2 patch array antennas for emerging millimeter-wave radio networks were presented. The gain, bandwidth and beamwidth have been derived in chapter 2. The developed antennas fully meet the requirements for the point-to-point line-of-sight applications and maximum signal coverage. These two antennas can be easily integrated with phase shifters to form high-gain array antennas with beam-scanning capabilities. To our best knowledge, this was the first academic work for the antenna design based on the system design of the emerging wireless applications in 60 GHz.

Then, a new 2-by-1 array of microstrip -coupled slot antenna in IPD technology has been designed, fabricated and characterized. The measurement results show that the antenna which operates in the frequency range of 57-64 GHz, has a maximum gain of about 5 dBi and the simulated radiation efficiency at 60 GHz is more than 80%. The proposed antenna can be integrated with other elements of the system in a flip-chip configuration in a same package. Our group was one of the first groups in the world who used this technology for the antenna design.

Finally, two different designs were proposed for on-chip in-package dielectric resonator antenna with CPW-Fed slot. Significantly miniaturized with high efficiency antenna was presented using DRA with high relative permittivity. However, to achieve wider bandwidth, another design employing DRA with low relative permittivity was considered. The major contribution of this part was the compact on-chip antenna design which saves a lot of chip area. The measurements are under development and more results will be published upon finalizing the test and verifications.

Chapter 5

mm-Wave Integrated Phase Shifters

5.1 Phase shifters for wireless applications

Phase shifters are used to change the transmission phase angle of a 2-port network. Ideal phase shifters provide low and equal insertion loss in all phase states and over the entire bandwidth. Most phase shifters are reciprocal networks, meaning that they work effectively on signals passing in either direction. Phase shifters in general, can be controlled electrically, magnetically, optically or mechanically. The applications of phase shifters include are but not limited to [102]:

- **Beamforming**: Phase shifters are used in phased-array antenna systems to steer the beam direction to the point of interest. The phase shifter is the key element of the phased-array system for beam steering.
- **Power amplifier linearization:** In the feed forward linearization method for the power amplifiers, the phase shifter is used to cancel the inter-modulation signal [103].
- **Measurement systems and equipments:** Phase shifters are used in the residual phase noise measurement setup. The received signal from DUT and the phase shifted reference signal will be mixed and the residual IF signal will be sent to the FFT analyzer for the phase noise measurements [104].
- **Phase and Delay Locked Loops:** They are used to align the phase of the oscillator signal with that of a reference Delay-Locked Loop (DLL) [105].
- **Butler matrix** Butler matrices are beam forming networks for linear arrays. They are formed by a combination of hybrids and fixed phased shifters.

5.1.1 Phase shifter characterization

In order to design and characterize a phase shifter, following parameters should be studied [102]:

- Phase shifting range: Depending on the required phase shift the range needed might be up to 360°.
- Phase resolution: For the analog tuning phase shifters the phase resolution is infinity. For the digital tuning phase shifters, the phase resolution produces some error on the system performance
- Group delay: For broadband signals a group delay might be important to consider.
- Insertion loss/gain: Depending on the type of phase shifter, there might be insertion loss or gain.
- Variation of insertion loss versus the phase: This is essential for the beamforming applications which might affect the phased-array's performance [55].
- Bandwidth: : For the broadband systems, the group delay might have significant effect on the system performance.
- RF large signal capabilities: The saturation of the phase shifter, specifically when they are used in the RF path will affect the nonlinear performance of the system.
- Power consumption: This is zero for the passive phase shifters.
- Device size: For the integration application the size is essential for the final cost of the product.
- Noise figure: For the applications where the phase shifter is connected directly to the antenna, it is important for the noise figure to be as low as possible.

5.1.2 The effect of limited phase shifting range on the performance of the phased-array system

In order to have perfect beam steering at any direction the maximum phase shifting up to 360° is required. The question is what if the phase shifting range is limited to a number less than 360°. In this part we want to investigate how reducing the maximum phase shift from 360° affects the array factor of a phased-array antenna. Let's assume a N element linear array with spacing d along the x-axis as shown in Fig. 5.1. Each antenna is followed by a phase shifter with a maximum phase shift

of Φ degrees and the output power of the antenna is combined after phase shifting. A radiating point source at far-field region rotates from $\theta = -90^\circ$ to $\theta = +90^\circ$ in the $x - z$ plane. For each source location, the array weights (phase shifts) should be adjusted to maximize the received power. The voltage at each antenna port is:

$$v_1 = v_0, v_2 = v_0 e^{j\beta d sin\theta}, v_3 = v_0 e^{j2\beta d sin\theta}, ... \tag{5.1}$$

Therefore the total voltage after power combining becomes:

$$\begin{aligned} v_{total} &= v_0 e^{-j\phi_1} + v_0 e^{-j\phi_2} e^{j\beta d sin\theta} + v_0 e^{-j\phi_3} e^{j2\beta d sin\theta} + ... && (5.2) \\ &= v_0 \sum_{n=1}^{N} e^{-j\phi_n} e^{j(n-1)\beta d sin\theta} && (5.3) \end{aligned}$$

In order to set the amount of phase shift for each RF chain, depending on the maximum phase shift of each branch (ϕ_{max}) and $\theta_0(\theta_0 = \beta d \sin\theta)$ we can choose the phase shift at each branch from the table 5.1.2.

Table 5.1: The look up table for chosing the proper phase shift for the maximum signal level at the output of power combiner when the maximum phase shift is less than 2π.

if $0 < (n-1)\theta_0 < \frac{\pi}{2}$	if $2\pi - (n-1)\theta_0 < (n-1)\theta_0 + \phi_{max} < 2\pi$	$\phi_n = \phi_{max}$
	if $2\pi \leq (n-1)\theta_0 + \phi_{max}$	$\phi_n = 2\pi - (n-1)\theta_0$
	else	$\phi_n = 0$
if $\frac{\pi}{2} < (n-1)\theta_0 < \pi$	if $2\pi - (n-1)\theta_0 < (n-1)\theta_0 + \phi_{max} < 2\pi$	$\phi_n = \phi_{max}$
	if $2\pi \leq (n-1)\theta_0 + \phi_{max}$	$\phi_n = 2\pi - (n-1)\theta_0$
	else	$\phi_n = 0$
if $\pi < (n-1)\theta_0 < \frac{3\pi}{2}$	if $(n-1)\theta_0 + \phi_{max} < 2\pi$	$\phi_n = \phi_{max}$
	if $2\pi \leq (n-1)\theta_0 + \phi_{max}$	$\phi_n = 2\pi - (n-1)\theta_0$
if $\frac{3\pi}{2} < (n-1)\theta_0 < 2\pi$	if $(n-1)\theta_0 + \phi_{max} < 2\pi$	$\phi_n = \phi_{max}$
	else	$\phi_n = 2\pi - (n-1)\theta_0$

For $d = 0.5\lambda$, Fig. 5.2 and Fig. 5.3 show the array factor versus source angle (θ for a 4-element array ($N = 4$) and 8-element array $N = 8$, respectively. It is seen that for $N = 4$ and $\Phi \geq 180^\circ$ the mean array factor is more than 5.6 dB, resulting in a mean error of 0.4 dB compared to the ideal phased-array. This value for $N = 8$ is 8.51 dB is 0.49 dB less than ideal phased-array. This means that if the phase shifting range is less than 360° but is still greater than 180° the average of array factor is only 0.5 dB less than the ideal phased-array.

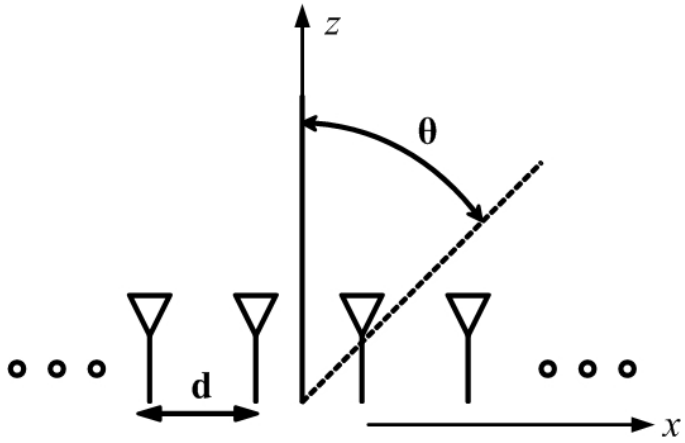

Figure 5.1: The N element phased-array system with spacing d between elements.

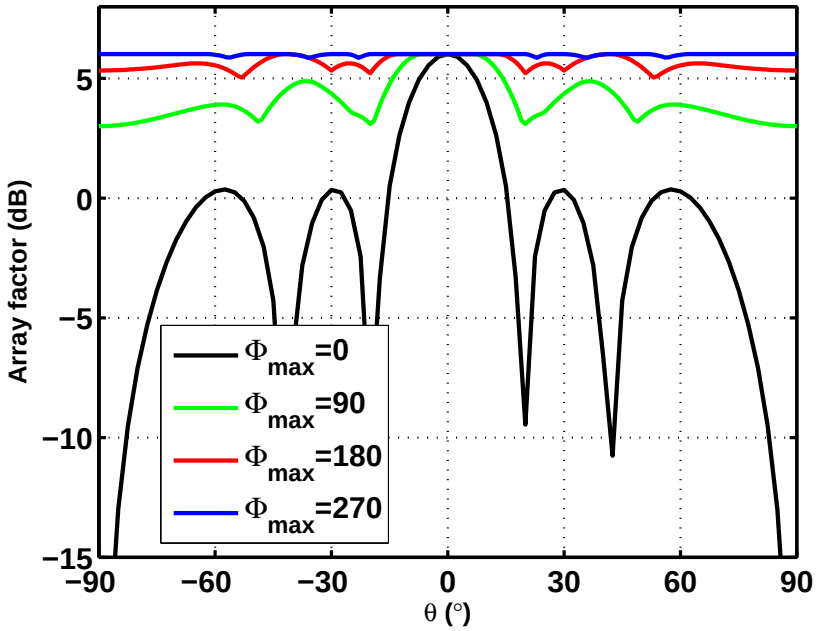

Figure 5.2: The array factor as a function of θ for $N = 4$ and $d = 0.5\lambda$

The results shown above have been calculated assuming that all four channels of the phased-array are ideal and identical. However, fabrication errors as well as environmental effects, such as temperature, affect the phase response of the RF chains. A great advantage of the analog phase shifters to digital phase shifters is that they can compensate such errors. Hence, it is necessary to consider an extra phase-shift of around 30 degree for calibration [106].

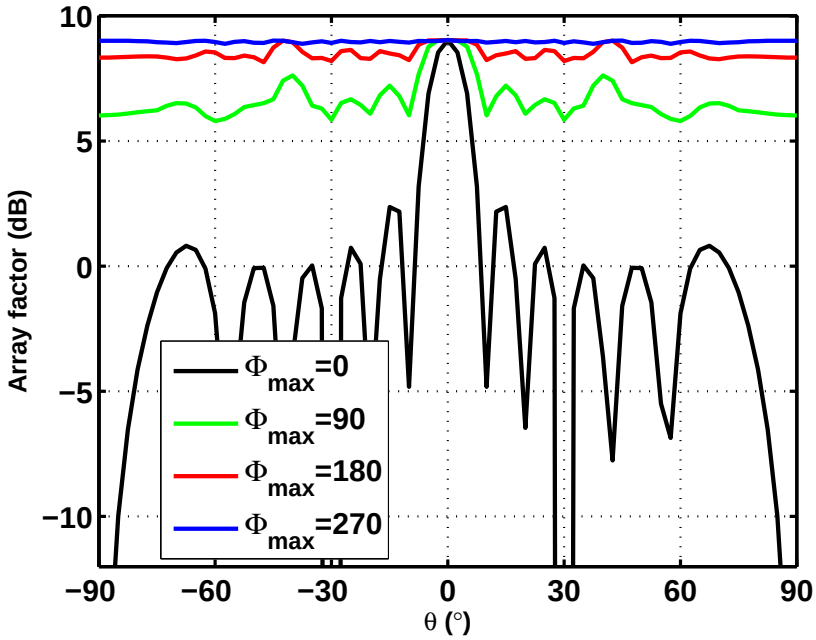

Figure 5.3: The array factor as a function of θ for $N = 8$ and $d = 0.5\lambda$

5.2 Integrated microwave and mm-wave phase shifters

There are several types of phase shifters proposed and implemented in microwave and mm-wave monolithic integrated circuits. The main challenge in designing these phase shifters is to implement a linear voltage controlled phase shift with minimum insertion loss. Generally, the overall insertion loss of the phase shifter can be compensated by an amplifier before or after it. The amplification after phase shifter is easier but this will increase the overall noise figure of the phase shifter. The insertion loss is an important issue in designing the phase shifter; however, the more important problem is the variation of the overall loss of the phase shifter as a function of the phase shift. The imbalance phase shifter insertion loss can deteriorate the phased-array gain enormously. Using non-coherent beamforming is an appropriate way to compensate the loss variation. It has been shown in [55] that in a practical array the overall gain of the array can be recuperated up to 1.6 dB.

Generally, phase shifters can be classified into digital and analog types. In digital phase shifters, multi stages phase shifter bits with a constant phase shift are cascaded and either utilized or by-passed by switches. The digital phase shifters have a high and phase-shift-dependent insertion loss. Furthermore they do not provide continuous phase shifting which results in high side lobe level in the

radiation pattern of the antenna, and beam pointing error. On the other hand, the analog phase shifter shifts the phase continuously, which results in better side lobe levels and lower beam pointing errors. The main drawback of the analog phase shifters is the insertion loss variation in the various phase states. In following, we will explain some of the well-known phase shifters, such as *the switched transmission lines, High-pass/Low-pass*, *All-pass*, *Distributed*, *Vector summing* and *reflective-type phase shifters* which have been used in various microwave and mm-wave integrated circuits [59, 102, 107–116].

In the design of RF phase shifting phased-array systems, in order to steer the front-end beam, the active or the passive beamforming method are the two approaches that can be followed. In the active approach, the antenna is connected to the LNA and the amplified signals will be phase shifted through the phase shifters. The output of the different branches are combined in the power combiner and will be downconverted to the IF signal through the mixer. In the passive beamforming, the high performance phase shifters are connected to the antenna array. The received signals from the antennas are phase shifted through the phase shifter and the combined signal will be amplified by the low noise amplifier. In this approach the radio structure will be simplified. The Butler matrix structure [117] or Rotman lens [118] are examples of the passive beamformers. The insertion loss and hence noise figure of the phase shifter is critical in this type of phase shifter for the overall performance of the system. In this chapter, the first two phase shifters in CMOS technology for active beamforming method are designed. Next, a MEMS-based reflective-type phase shifter for the passive beamforming application is introduced. This design is intended to integrate with the antenna for a passive beamformer.

5.2.1 Switched transmission lines phase shifters

In the switched transmission lines, multiple constant phase shifting bits are cascaded and separated by switched CMOS transistors in between. Fig. 5.4 shows a single bit of a switched transmission line. Each bit is designed using a low-pass π-network which consists of a series inductor (L_s) and two shunt capacitors (C_p). Arranging the MOSFET switches as shown in Fig. 5.4 permits the switching between a phase shift (delay) state and a bypass state. When S_i is low, M_1 is off and M_2 is on, hence the π-network makes certain there is a phase delay in the transmission path. Conversely, when S_i is high, M_1 is on and by passes the signal. In practice the parasitic capacitors in M_2 can affect the off state of the transistor. Therefore, in practice a parallel inductor is taken into account for making a parallel resonance at the operation frequency. Although, the linearity of this type of phase shifter is acceptable, the main drawback of the switched transmission line phase shifter is the loss associated with the MOSFET switches [109, 119]. On the other hand, this class of phase shifters does not provide continuous phase shifting which

results in a high side lobe level in the radiation pattern of the antenna, and beam pointing error.

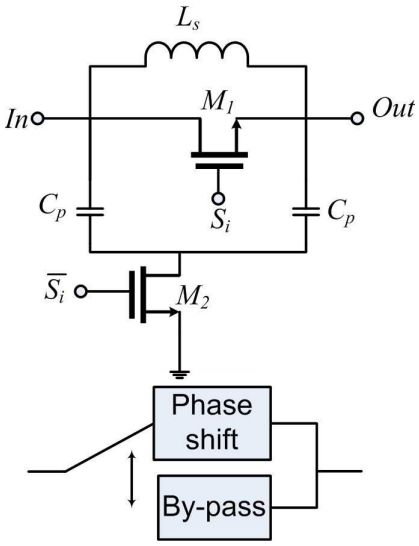

Figure 5.4: A stage of a switched transmission lines.

5.2.2 High pass/low pass phase shifter

Fig. 5.5 shows the general block diagram of the high pass/low pass phase shifter. The high-pass/low-pass phase shifter is basically functioning by taking the difference between the phase from the high-pass filter path and the low-pass filter path of a particular bit. By arranging the CMOS switches to permit switching between low-pass and high-pass, it is makes it possible to create a certain phase shift between the two states [59,120,121]. Like the switched transmission line phase shifter however, the linearity of the phase shifter is well, but the insertion loss of the overall phase shifting is quite high. Nonetheless, the discrete phase shifting can affect the side lobe levels and leads to higher beam pointing error.

5.2.3 All-pass phase shifters

In the all-pass phase shifter, typically an active configuration is employed with a variable resonant circuit with second order all-pass network characteristics in Eq. (5.4) .

$$H(s) = \frac{s^2 - \frac{\omega_0}{Q}s + \omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{5.4}$$

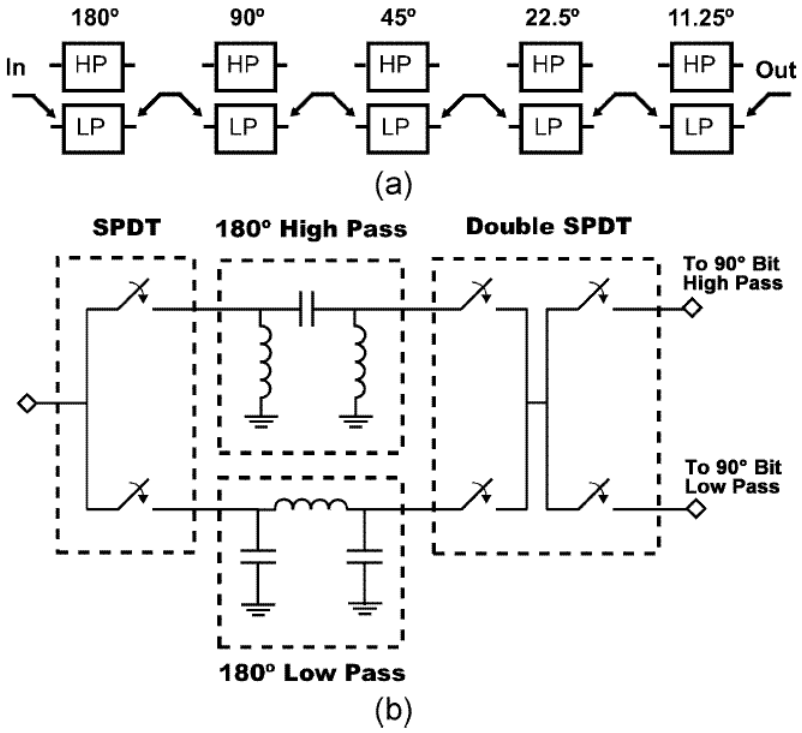

Figure 5.5: (a) Block diagram of a 5-bit high-pass/low-pass phase shifter. (b) Generalized schematic of the first SPDT switch, the filter sections for the initial bit, and the back-to-back SPDT switches that separate adjacent bits [120].

Therefore, the phase of the transmission response can be changed by varying the capacitance or the inductance of the resonant circuit without changing the amplitude [114, 115]. The main drawback of this type of phase shifter is the narrow-band response and also power consumption of the circuit.

5.2.4 Distributed phase shifters

The operation concept of this phase shifter is based on the changing the propagation constant of the propagated wave. For a forward travelling wave over a transmission line, if the voltage at the input port is V_0, the voltage at any point on the transmission line is $V(z) = V_0 e^{-j\gamma z}$, where γ is the propagation constant. . In a tuneable transmission line or a phase shifter changing the physical length of the line or the propagation constant of the traveling wave can a produce phase shift. The varactor loaded circuit shown in Fig. 5.6, is an example of a phase shifter where the output phase can be controlled by changing the value of the capacitances by tuning the DC bias applied to the varactors.

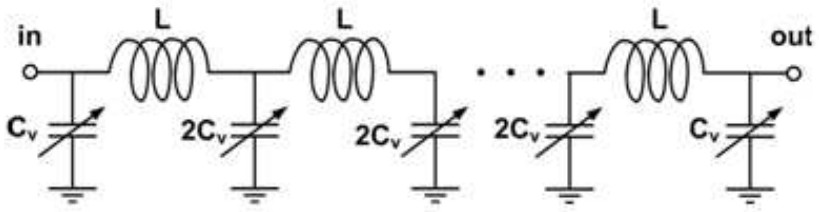

Figure 5.6: The distributed phase shifter using varactors as the tuning elements

5.2.5 Vector-sum phase shifters

Fig. 5.7 depicts the block diagram of a vector summing phase shifter. In the vector summing phase shifters, the input signal is divided into two quadrant components through a 90-degree hybrid. The quadrant components will be amplified by two Variable Gain Amplifiers (VGA) and combined, consequently. A phase shift in the range of 0 to 90 ° can be simply set by choosing proper gains for the VGAs. For achieving a full 360 degree phase shift, two 0/180° phase inverters can be placed after the VGAs to extend the phase shift range up to 360°. The linearity performance is poor due to the active phase shifting, and a large power consumption is also usually required to achieve a high dynamic range [59, 111, 121–125].

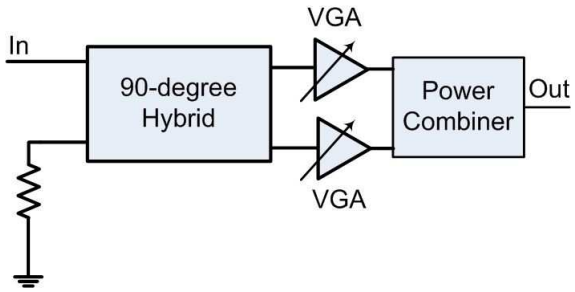

Figure 5.7: The block diagram of the vector summing phase shifter

5.2.6 Reflective-type phase shifters (RTPS)

One of the most common types of phase shifters is the reflective-type phase shifter which employs a 4-port 90° hybrid and two similar purely imaginary (reflective) loads [107,108,122,126,127]. Fig. 5.8 shows the general block diagram of the RTPS. The *through* and *coupled* ports of the hybrid are terminated with the reflective terminations and the isolated port is used as the output.

The reflection coefficient at the reflective load (Γ) is:

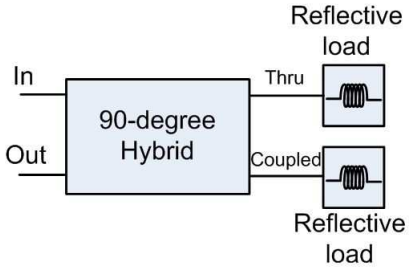

Figure 5.8: General block diagram of the reflective-type phase shifter

$$\Gamma = \frac{jB - Z_0}{jB + Z_0} = 1\angle\phi$$
$$\phi = -2\tan^{-1}\frac{B}{Z_0} \tag{5.5}$$

The incident signal at the input reaches the output after reflection back from the imaginary loads in phase, and they will be added up. The reflective loads can be altered electronically, optically, mechanically or magnetically. Therefore, the phase of the reflection coefficient at the through and coupled ports changes, which results in the phase shift of the output signal. The amount of phase shift is dependent on the load type. Several passive terminations are proposed for the reflective loads. Fig. 5.9 shows four common types of the various reflective loads. A single varactor (Fig. 5.9a) cannot provide a phase shift more than 75° degree in practice [128]. Adding a series inductor can increase the phase shift up to 180° degree (Fig. 5.9(b)). The inductor must resonant with the capacitor at the operation frequency of the phase shifter.

$$L_r = \frac{\omega_0^2}{\left(\frac{C_{r,min} + C_{r,max}}{2}\right)} \tag{5.6}$$

For having a complete 360° degree phase shift one should use dual resonated loads to achieve a phase variation more than 360° degree [112, 128, 129]. Fig. 5.9c depicts the schematic of the dual-resonance load. In this design, L_{r1} is chosen such that it resonates with $C_{r,min}$ and L_{r1} resonates with $C_{r,max}$. The phase of each series' resonance is 0° and therefore, this design guarantees a 360° phase shift when the varactors are biased from C_{min} to C_{max}. The input impedance of the parallel resonant load is:

$$
\begin{aligned}
Z_{in} &= \frac{\left(j\omega L_1 + \frac{1}{j\omega C}\right)\left(j\omega L_2 + \frac{1}{j\omega C}\right)}{j\omega L_1 + \frac{1}{j\omega C} + j\omega L_2 + \frac{1}{j\omega C}} \\
&= j\frac{\left(\omega L_1 - \frac{1}{\omega C}\right)\left(\omega L_2 - \frac{1}{\omega C}\right)}{\omega L_1 + \omega L_2 - \frac{2}{j\omega C}}
\end{aligned} \tag{5.7}
$$

Therefor, the magnitude of the reflection coefficient is 1 and the phase is:

$$
\angle\Gamma = -2\tan^{-1}\frac{\left(\omega L_1 - \frac{1}{\omega C}\right)\left(\omega L_2 - \frac{1}{\omega C}\right)}{Z_0\left(\omega L_1 + \omega L_2 - \frac{2}{j\omega C}\right)} \tag{5.8}
$$

It can be seen that the phase of Γ at $C = C_{min}$ and $C = C_{max}$ is 0. If we set the denominator of the term inside the inverse-tangent of the phase phrase to zero we have:

$$
\begin{aligned}
C &= \frac{2}{\omega^2(L_1 + L_2)} \\
&= \frac{2C_{min}.C_{max}}{C_{min} + C_{max}}
\end{aligned} \tag{5.9}
$$

which means at this certain value of C, the phase would be 180°. This shows that by using this parallel resonant load, one can achieve a full 360° phase shift in the reflection coefficient and consequently in the total phase shifter structure. The main drawback of the parallel resonant load is that its performance will deteriorate with resistive losses in the inductor or capacitor. It can be shown that the magnitude of the reflection factor shows significant variations in this case, resulting in large changes in the insertion loss. An LC transformation network can be added to decrease these variations of the magnitude and the resulting loss variations of the RTPS. This will reduce the maximum loss is reduced [112]. Fig. 5.9(d) shows the schematic of the dual resonant load with the transformer.

The RTPS, being fundamentally passive, shows excellent linearity characteristics. The main challenge in integrating the CMOS-based RTPS design is the loss. The two main sources of loss in a RTPS are the transmission-line losses in the 90° hybrid and the loss in the reflective terminations. To reduce phase shifter loss, active negative resistance circuits have been used in RTPS designs [113].This, however, limits the linearity and noise performance of the RTPS. The insertion-loss variation can also be minimized by using an equalization resistance, and by modifying the

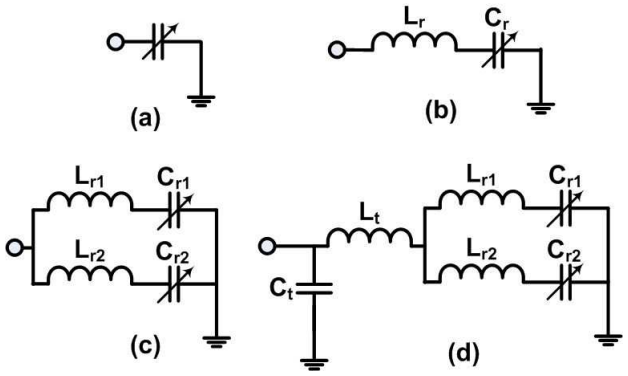

Figure 5.9: Different proposed reflective loads

90° hybrid [130]. In the following, the design of two RTPS in CMOS technology will be explained.

5.3 Proposed Reflective-type phase shifter in CMOS 90 nm technology

In this part, the design of a RTPS with dual resonated loads in CMOS 90 nm technology is explained. As mentioned earlier the two main parts of the phase shifter are 90° hybrid and the reflective loads.

5.3.1 Broadband 90° hybrid

For a relatively broadband 90° hybrid a broadside coupler is used instead of the edge coupled coupler. The gap of an edge coupled coupler should be very small to have a 3 dB coupling to the coupled port is not practical. The broadside couplers are composed of two parallel microstrip lines which are positioned at the different layers in a multi-layers transmission line. They show a very wide bandwidth behavior where they are used as 90° Hybrids [131]. To analyze a symmetric broadside coupler, as shown in Fig. 5.10, the structure can be decomposed into even and odd modes and for each case one can define an associated characteristic impedance which is Z_e or Z_o. The coupling factor can be determined from [132]:

$$k = \frac{Z_e - Z_o}{Z_e + Z_o} \tag{5.10}$$

For a symmetric structure there are closed form expressions [133] for the even mode and odd mode characteristic impedances.

$$Z_{0e} = \frac{188.3}{\sqrt{\varepsilon_r}} \frac{K(k')}{K(k)} \tag{5.11}$$

$$Z_{0o} = \frac{296.1}{\sqrt{\varepsilon_r} \frac{b}{s} \tanh^{-1} k} \tag{5.12}$$

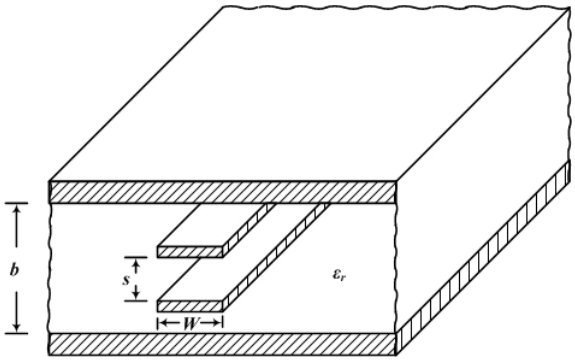

Figure 5.10: The symmetrical broadside coupled line.

where b is the vertical spacing between the ground planes, s is the signal line spacing, w is the signal linewidth, k is a parameter related to w, b and s. $k' = \sqrt{1-k^2}$ and $K(k)$ and $K(k')$ are complete elliptic integrals of the first kind [134].

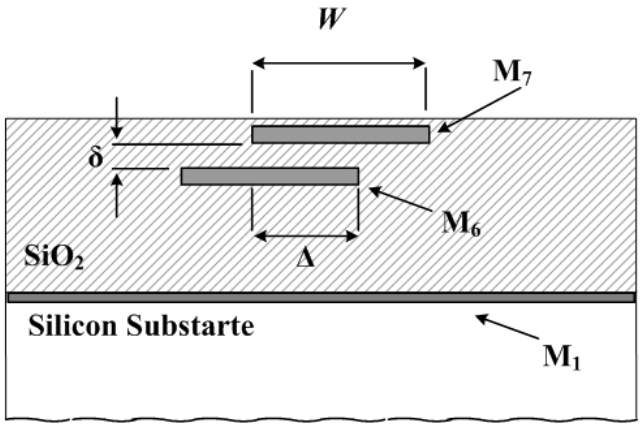

Figure 5.11: The cross section of the meandered shape broadside coupler implemented in CMOS 90 nm technology

For a broadband 90° hybrid, a broadside coupler is utilized. This structure has broadband behavior and is shielded from the lossy silicon substrate, which is the main source of loss for passive devices in CMOS. As shown in Fig. 5.11, a broadside coupler consists of two parallel microstrip lines positioned at different layers in a multi-layers transmission line structure.

Fig. 5.11 shows the cross section of the meandered shape broadside coupler. The broadside structure is implemented on thick metals in the CMOS 90 nm process. The coupler is designed and meandered to have a more compact size. The parameters W and Δ are optimized in the 60 GHz band using HFSS. The phase difference between the coupled and through port and insertion loss of the through and coupled port are shown in Fig. 5.12.

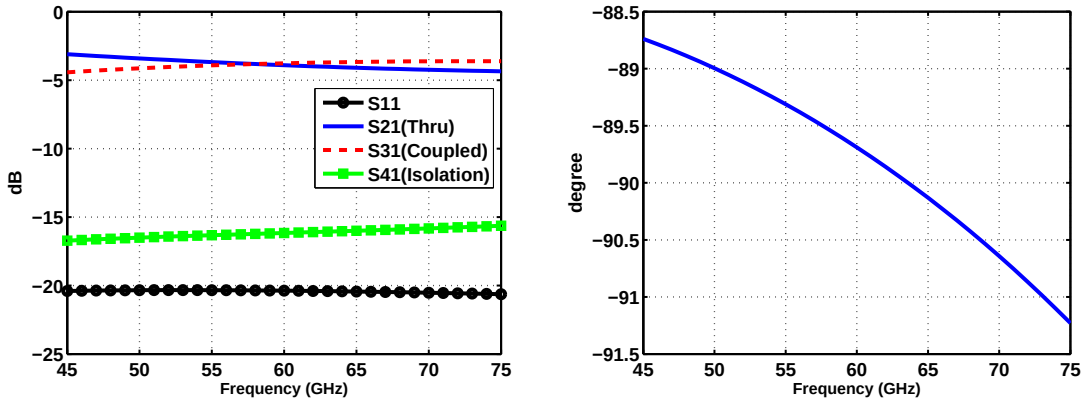

Figure 5.12: The phase difference between the coupled and through port and insertion loss of the through and coupled port of the broadside coupler.

5.3.2 Lumped element reflective load

In the integrated RTPS design, the reflective loads are designed by employing varactors. Varactors can be implemented in CMOS technology by using a regular CMOS transistor in which the source and drain terminals that are connected together. Applying a variable voltage between gate and drain/source of this structure generates a variable capacitor. Assuming a transistor with W=7 μm and L=0.37 μm where W and L are width and length of the transistor respectively. The high-frequency device simulation demonstrates that at 60 GHz frequency by varying the applied DC voltage from 0 to 1V, the transistor can work as a varactor with a minimum capacitance ($C_{v,min}$) of 49 fF and a tuning ratio of 3. The proposed reflective load is shown in Fig. 5.13. This load contains two inductors, a capacitor and a varactor. The input impedance of this load, where the inductors and capacitors are ideal elements with pure imaginary impedance, is given by Eq. 5.13

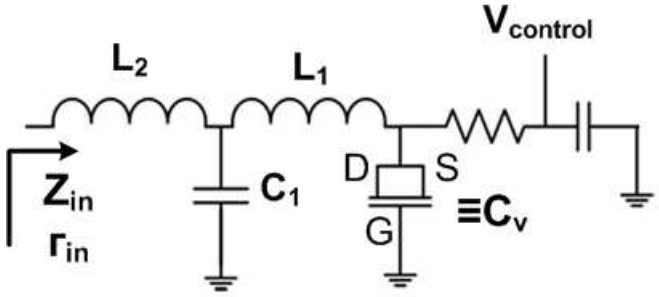

Figure 5.13: The proposed reflective load.

$$Z_{in} = j\omega L_2 + \left(\frac{-j}{\omega C_1}\right) \parallel \left(j\omega L_1 - \frac{j}{\omega C_v}\right) \tag{5.13}$$

$$= j\left(\frac{\omega L_1 - \frac{1}{\omega C_v}}{1 + \frac{C_1}{C_v} - \omega^2 C_1 L_1} + \omega L_2\right) \tag{5.14}$$

C_v denotes the varactor capacitance and C_1, L_1 and L_2 are the capacitance and inductance of the matching elements shown in Fig. 5.13. The reflection coefficient can be expressed as:

$$\Gamma_{in} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} = 1\angle\theta \tag{5.15}$$

where,

$$\theta = -2\arctan\left(\frac{\Im(Z_{in})}{Z_0}\right) \tag{5.16}$$

When the varactor capacitance varies the phase of the reflection coefficient of the load will changes accordingly. As a result, the output phase of the phase shifter changes by θ in Eq.5.16. By setting $L_1 = (\omega^2 C_{v,min})^{-1}$, $C_1 = C_{v,max}/(\omega^2 L C_{v,max} - 1)$ and $L_2 = 0$, the output phase changes from 0-180 °. In practice, the inductors and capacitors are not purely reactive loads. The resistive part has two major effects. It limits the overall phase shift of the phase shifter and increases the insertion loss.

5.3.3 Developed phase shifter

The die micrograph of the fabricated phase shifter is shown in Fig. 5.14, where the chip area excluding the pads is $0.3 \times 0.25mm^2$. Using Cascade on-wafer measurement setup, the phase shifter was tested for a wide range of frequencies from 50 to 65 GHz and the S-parameters of the two-port network w measured.

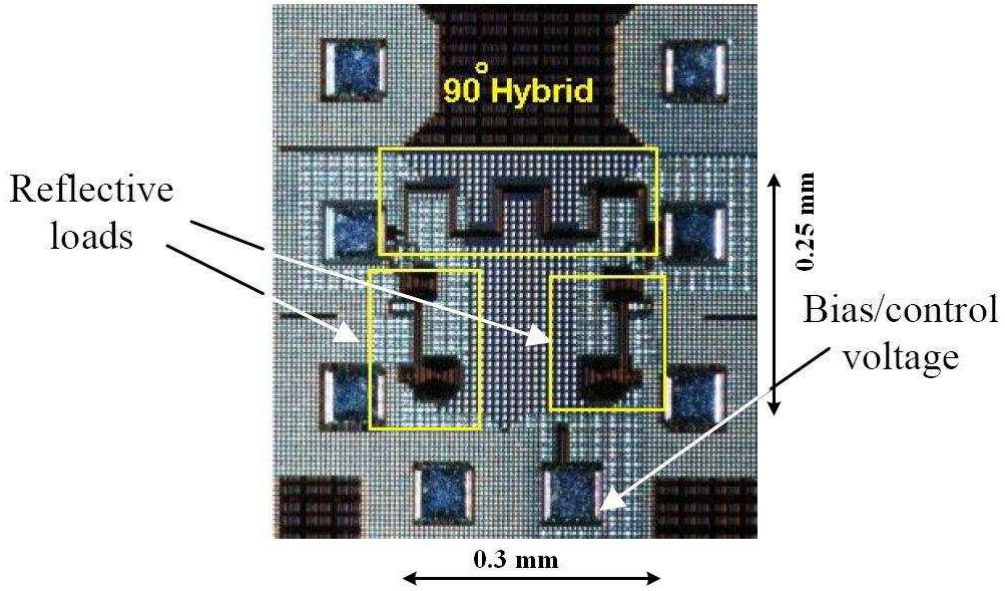

Figure 5.14: The die micrograph of the RTPS phase shifter implemented in 90 nm-CMOS technology.

Fig. 5.15 shows the relative phase shift and insertion loss versus the tuning voltage of the phase shifter. The fabricated phase shifter provides 90° of continuous phase shift for the tuning voltage between 0-0.8V. The insertion loss variation of the phase shifter is about 3.5 dB over this wide range of frequencies. Fig. 5.16 shows the measured output phase of the phase shifter for different tuning voltages. The phase shifter shows a linear behavior over the 50-65GHz frequency range while maintaining a 90° continuous phase shift.

Fig. 5.17 depicts the insertion loss and input matching of the phase shifter over the entire bandwidth of 15GHz. The maximum insertion loss is 8 dB which is the lowest value for the phase shifters reported in the CMOS technology at the mm-wave range. The return loss of the phase shifter is more than 12 dB at all phase states. The summary of performance of the phase shifter is shown in Table 5.3.

Table 5.2: Summary of the performance of the phase shifter

Technology	ST CMOS 90 nm
Frequency Range	50-65 GHz
Phase Shifter Type	RTPS/Continuous phase shifting
Maximum Phase Shift	90°
Die Area	$0.3 \times 0.25 mm^2$
Power Consumption	0 Watts
Insertion Loss	6.25 ± 1.75

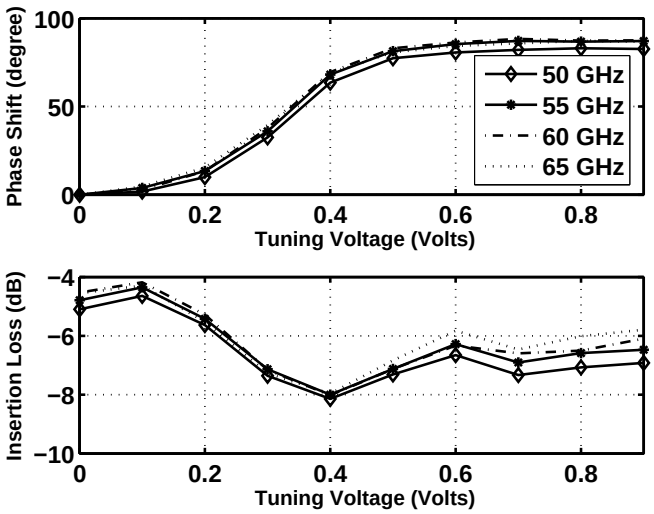

Figure 5.15: Relative phase shift and insertion loss of the phase shifter versus tuning voltage at 50, 55, 60 and 65 GHz.

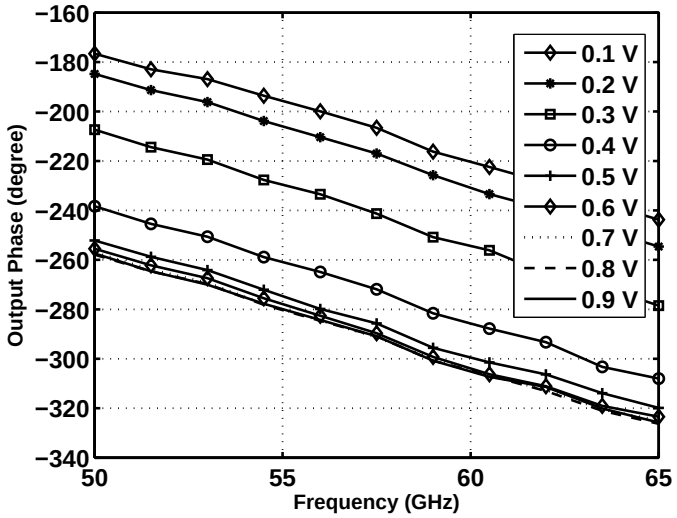

Figure 5.16: Measured output phase of the phase shifter versus frequency for various tuning voltages.

5.4 A transmission-line-based reflective-type phase shifter in CMOS 0.13 μm technology

Since, the CMOS 90 nm technology was no longer offered by CMC for the Canadian universities, we should have chosen another technology to pursue the research. The

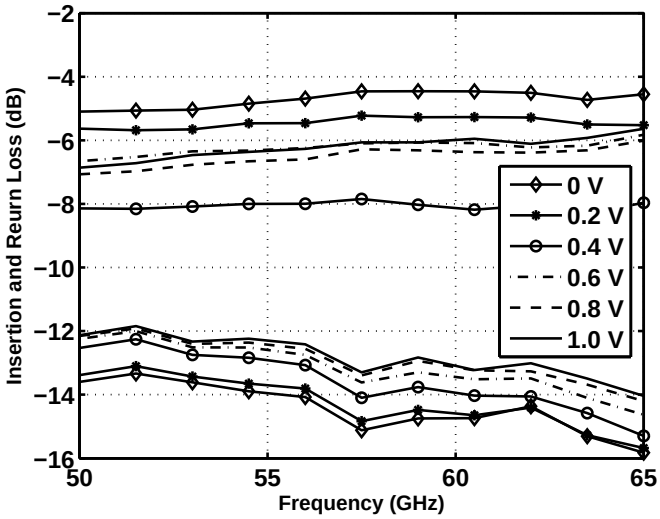

Figure 5.17: Measured insertion loss and input return loss of the phase shifter versus frequency for various tuning voltage.

only available option at the time of the design was CMOS 0.13 μm technology. The second phase shifter was designed and fabricated on standard IBM CMOS 0.13 μm. The offered technology has 7 metal layers with two thick top metal layers. As discussed earlier in section 5.1.2, the phase shifter with a phase shifting range more than 180° can provide almost 80% of the ideal phase shifter with a full phase shifting range. Therefore, in this design we did our best to have minimum 180° phase shift.

5.4.1 90° hybrid

In this design, the broadside coupler is employed as the 90° hybrid to benefit the broadband behavior and better performance of it. As it is depicted in Fig 5.18, the two top thick metal layers of the CMOS process were utilized for the design of the broadside coupler.

The thicknesses of the two thick metals are 4 μm and 3 μm, respectively. The bottom metal layer is chosen as a ground to isolate the signal from the lossy silicon substrate. The length of the broadside coupler is 640 μm, where the width of the top and bottom lines are 10 μm and 8 μm, respectively. The structure is meandered to fit in a 335 μm $\times$ 85 μm rectangle. The simulation results are shown in Fig. 5.19. The simulation results show that the designed hybrid has a wide range of operation around 60 GHz. The insertion loss at 60 GHz is 0.3 dB and the return loss and isolation are better than 16 dB and 17 dB, respectively.

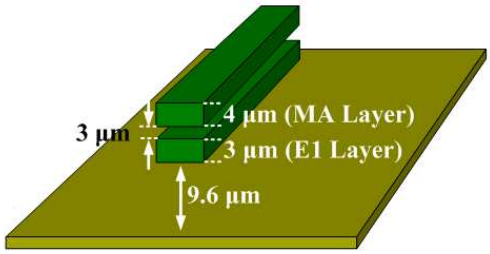

Figure 5.18: Broadside 90° hybrid on the multilayer metals on CMOS 0.13 μm technology.

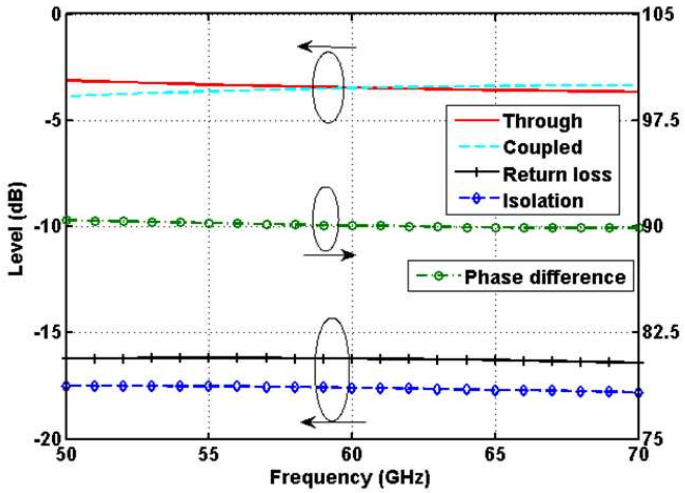

Figure 5.19: Phase difference between I and Q signals, coupling, isolation and return loss level of the designed broadband 90° hybrid.

5.4.2 Reflective load

NMOS varactor was used as the tuning element of the phase shifter. A source-to-gate connected transistor with W=2.4 μm and L=0.24 μm was chosen as a varactor. By reverse biasing this transistor and varying the applied DC voltage from -0.5 to $1V$ a varactor with a minimum capacitance 45 fF and tuning ratio of 3 can be achieved. The models provided by the foundry show that the typical Q of these varactors in this technology is not higher than 3 at 60 GHz. In order to achieve as much phase shift with minimum insertion loss variation, one should use the proper impedance transformers to achieve maximum phase shift. The Dual Resonant Reflective Load (DRRL) with transformation can provide a 360° phase shift [135]. Implementing such a load with low-Q lumped inductors will result in huge insertion loss of the phase shifter. Therefore, the microstrip transmission lines are employed to implement the DRRL. The proposed DRRL is shown in Fig. 5.20. The transmission lines with an electrical length θ_1 and θ_2 are chosen as the

impedance transformers. If the varactor is lossless, then by choosing θ_1 and θ_2 as below, one can achieve full 360° phase shift.

$$\theta_1 = \arctan\left(\frac{1}{\omega Z_0 C_{v,min}}\right) \& \theta_2 = \arctan\left(\frac{1}{\omega Z_0 C_{v,max}}\right) \tag{5.17}$$

Where $C_{v,min}$ and $C_{v,max}$ are the minimum and maximum values of the varactor. As mentioned earlier, in practice the Q of the varactor is very low. The effect of a limited Q is the lowering the phase shift. This not only increases the overall insertion loss, but also enlarges the insertion loss variation of the phase shifter versus tuning voltage, which are undesirable [55]. An impedance transformer has been used to minimize the insertion loss variation. The impedance transformer uses a transmission line with an electrical length of θ_S and a parallel capacitor (C_p). After optimization the best possible performance, we came up with θ_S=31° and $C_p = 60fF$.

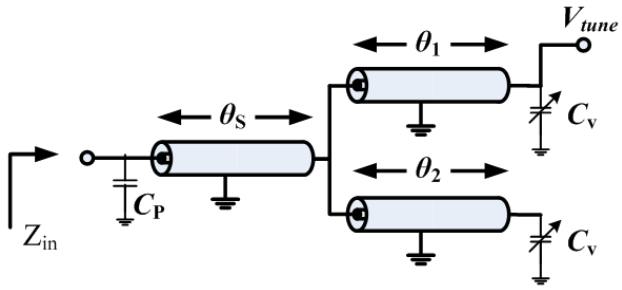

Figure 5.20: Transmission-line based loads on the multilayer metals on CMOS 0.13 μm technology.

5.4.3 Developed phase shifter performance

The die micrograph of the fabricated phase shifter is shown in Fig. 5.14. The chip area excluding pads is $0.3 \times 0.5mm^2$. Fig. 5.22 shows the relative phase shift and insertion loss versus the tuning voltage of the phase shifter. The fabricated phase shifter provides 240° continuous phase shift for the tuning voltage between 0-1.5V at 60 GHz. The phase shifting is maximum 300° and 225° at 55 and 65 GHz, respectively. The insertion loss of the phase shifter is shown in Fig. 5.22. The insertion loss at 60 GHz is 10.2 ± 1.5 dB. The insertion loss is 10.6 ± 1.4 dB and 10.2 ± 1.56 dB at 55 GHz and 65 GHz, respectively. The load has been optimized to minimize the insertion loss variation of phase shifter versus tuning voltage. The insertion loss variation of the phase shifter is about 3 dB at 60 GHz. Fig. 5.23 shows the measured output phase of the phase shifter for different tuning voltages between 0 and 0.9 V.

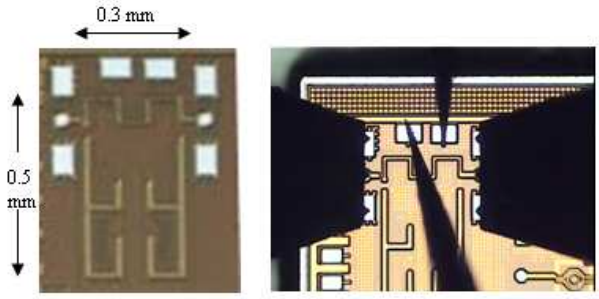

Figure 5.21: The die micrograph of the RTPS phase shifter implemented in CMOS 0.13μm technology.

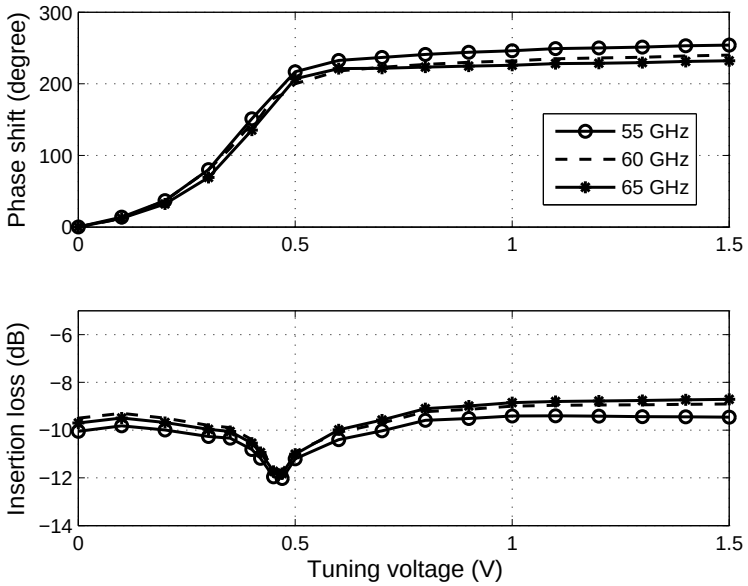

Figure 5.22: Relative phase shift and insertion loss of the phase shifter versus tuning voltage at 55, 60 and 65 GHz.

Table 5.3: Summary of the performance of the phase shifter

Technology	CMOS 0.13 μm
Frequency Range	55-65 GHz
Phase Shifter Type	RTPS/Continuous phase shifting
Maximum Phase Shift	240.0°
Die Area	0.3×0.5 mm^2
Power Consumption	0 Watts
Insertion Loss	10.2 ± 1.5

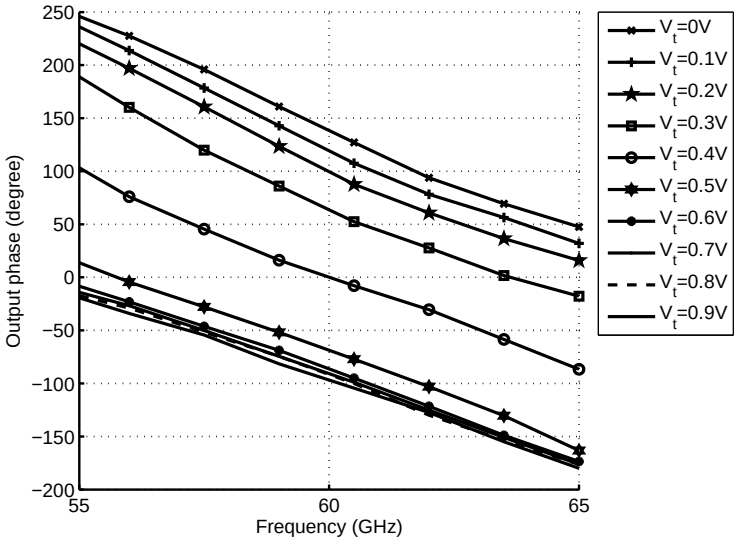

Figure 5.23: Measured output phase of the phase shifter versus frequency for various tuning voltages.

5.5 Proposed MEMS reflective-type phase-shifter

Although CMOS technology offers a low-cost and a moderate performance for a phase shifter, realizing a CMOS-based high performance systems and low loss phase shifter with a full 360° phase variation is quite challenging [107]. On the other hand, the Micro Electromechanical Systems (MEMS) offers better RF performance when low loss materials including gold are used on a low loss substrate such as alumina [136]. In comparison with CMOS technology, the MEMS capacitive switch exhibits lower loss which is encouraging for building digital phase shifters. In [137], a reflective-type phase shifter (RTPS) employing MEMS series-switches was reported. In the following, using variable short circuit transmission lines with shunt MEMS metal to metal contact switches the MEMS-based reflective type phase shifter is designed and implemented [138].

5.5.1 MEMS phase shifter architecture

In the design of digital mm-wave RTPS, PIN diodes [139–141] and MEMS [137] are used as electrical switches. They have used series or shunt switches configurations to add the required phase shift to the reflective load. In the implemented phase shifter in [137], a 90° Hybrid is connected to two reflective loads as it is shown in Fig. 5.24. The switches can increase or decrease the electrical length of the transmission lines connected to the *through* and *coupled* ports of the hybrid. This length variation results in the change of the phase of the reflection coefficient at

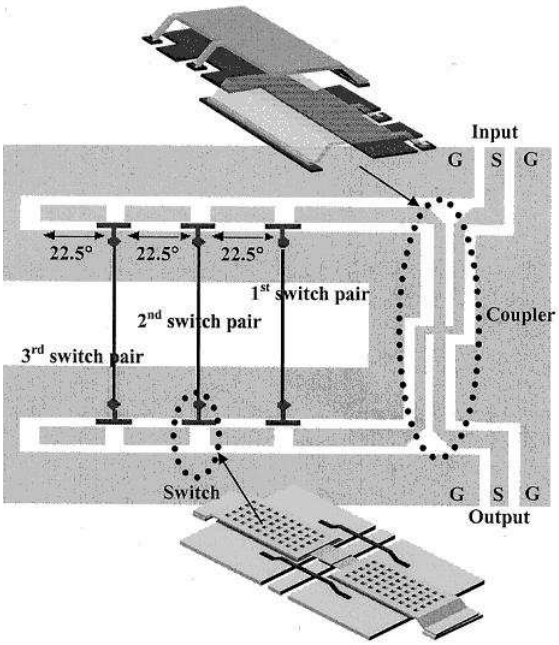

Figure 5.24: Schematic view of the two-bit reflection type phase shifter [137]

each load. Consequently, the phase of the signal passing through the phase shifter could be altered. The main drawback of this design is the 5 dB loss variation of the phase shifter as a function of the phase shift.

In the proposed design, the shunt switches' configuration in the form of short-ended transmission line is used as the reflective loads. Let us consider a transmission line with total length of L which is terminated by a short load which is shown in Fig. 5.25a. If the length of the transmission line is changed from 0 to $\lambda/2$ it can be seen that the load moves over the perimeter of the smith chart as a full imaginary or reflective load (Fig. 5.25b). This simple idea can be implemented using the short-ended Single-Port Single-Through (SPST) switches. Instead of changing the physical layout of the transmission line, by adding the short-ended SPSTs at different locations of the transmission line, one can change the electrical length of the load. This idea is shown in Fig. 5.26, where N switches are located with uniform spacing Δl along the line. For a uniform phase distribution we should have $\Delta l = \frac{L}{N}$. At any time, there is only one switch connected. Hence, the input impedance of the reflective load if the nth switch is 'on' is:

$$Z_{in} = jZ_0 \tan \beta(n\Delta l) \tag{5.18}$$

The magnitude of the reflection coefficient at the input port is always 1, but the phase changes when the switches configuration and consequently the effective electrical length alters.

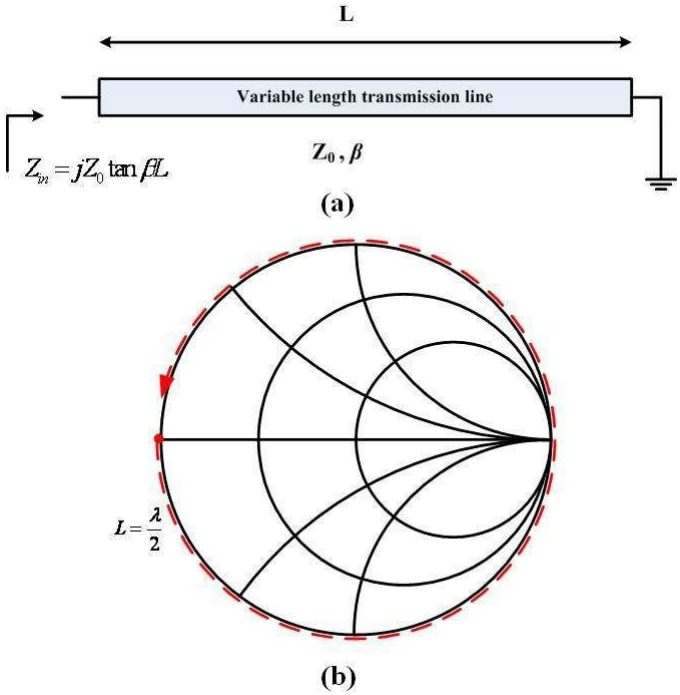

Figure 5.25: (a) A short-ended transmission line (b) The locus of load over the smith chart when the length of transmission line alters

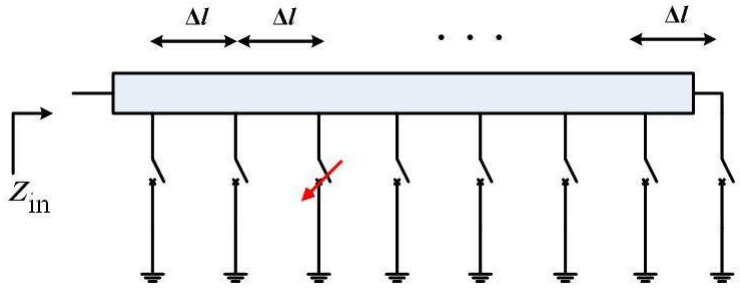

Figure 5.26: The proposed reflective load with the short-ended SPST switches

$$\begin{aligned} \Gamma &= \frac{Z_{in} - Z_0}{Z_{in} + Z_0} = 1\angle\theta \\ \theta &= -2\beta n \Delta l \end{aligned} \tag{5.19}$$

By connecting two similar loads to the through and coupled ports of a 90° hybrid, a RTPS can be implemented with 360° phase shift. The resolution of the phase variation can be determined by the number of switches or in better words the Δl.

The main advantage of the proposed phase shifter is that as we use only one

switch at any phase shifting case, even by using a lossy switch, the insertion loss variation of the phase shifter over the phase shift is minimum. For designing the phase shifter, we need to design a 90° hybrid and low-loss switches. In the following the design of these two blocks will be explained in more details.

5.5.2 90° hybrid

90° hybrid is a key element in the reflective-type phase shifters. For a relatively broadband 90° hybrid, a broadside coupler is utilized. The gap (G) of an edge coupled coupler should be very small to have a 3 dB coupling to the coupled port. Broadside couplers are composed of two parallel transmission lines which are positioned on top of each other. This structure shows a very wide bandwidth behavior where they are used as a 90° Hybrids. Fig. 5.27 shows the proposed

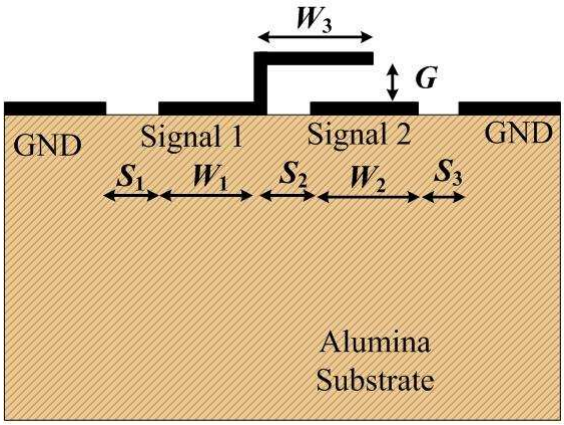

Figure 5.27: Cross section of the broadside coupler in MEMS technology.

co-planar waveguide (CPW) broadside coupler designed in MEMS technology. In the designed broadside coupler, the input signal will go over the coupled line using the cantilever structure. The length of the coupler is essential to realize the 90° phase difference at the coupled and through ports. The closed form equations of the broadside couplers can be used for the initial design of the broadside coupler. The parameters shown in Fig. 5.27 can be optimized to have an optimum hybrid at 60 GHz. The structure is simulated and optimized in Ansoft HFSS [142]. The optimized values are $W_1 = 13\mu m$, $W_2 = 13\mu m$, $W_3 = 22\mu m$, $S_1 = 18\mu m$, $S_2 = 10\mu m$, $S_3 = 10\mu m$ and $G = 2.5\mu m$.

5.5.3 Load design

The next step is the design of the switch for the proposed MEMS RTPS is the switch design. To design a switch, the conventional air bridge is employed to ground the

signal to the side metal platings, in the ON state Fig. 5.28 depicts the simulated switch in Sonnet. In this simulation the switch was analyzed for both ON and OFF states, where the switch terminates the transmission line with ground or open circuit respectively.

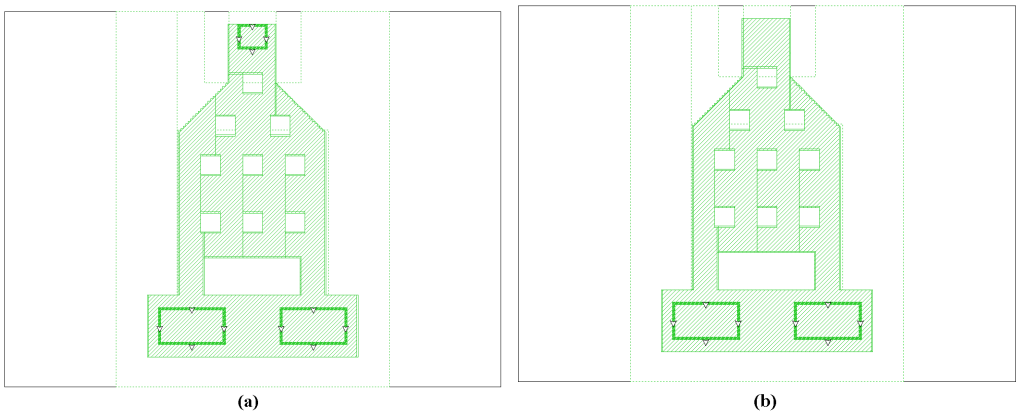

Figure 5.28: Simulation of the MEMS switch in Sonnet (a) ON state (b) OFF State.

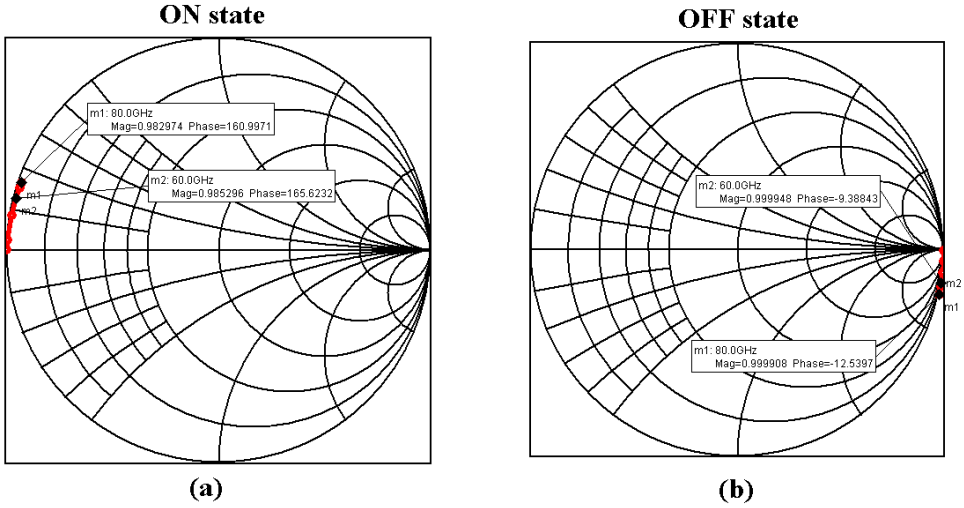

Figure 5.29: Simulation results of MEMS switch in Sonnet (a) ON state (b) OFF State.

The simulation results of the switches are shown in Fig. 5.29 for both ON and OFF states respectively. The switch has 0.15 dB of loss in the short circuit case with less than 15° phase error where in the open circuit case has about 10° of phase error. These results were promising for the implementation a low loss phase shifter in MEMS technology in the mm-wave band.

The next step in the design of the MEMS RTPS is the load design. To design a variable short end load, the air bridge switches are employed where signal can be

shortened to the ground of the CPW when the switch is actuated "ON" state. Fig. 5.30 depicts the layout of the simulated switch in Ansoft HFSS . In this simulation the switch was analyzed for both ON and OFF state where the switch terminates the transmission line with ground or open circuit, respectively.

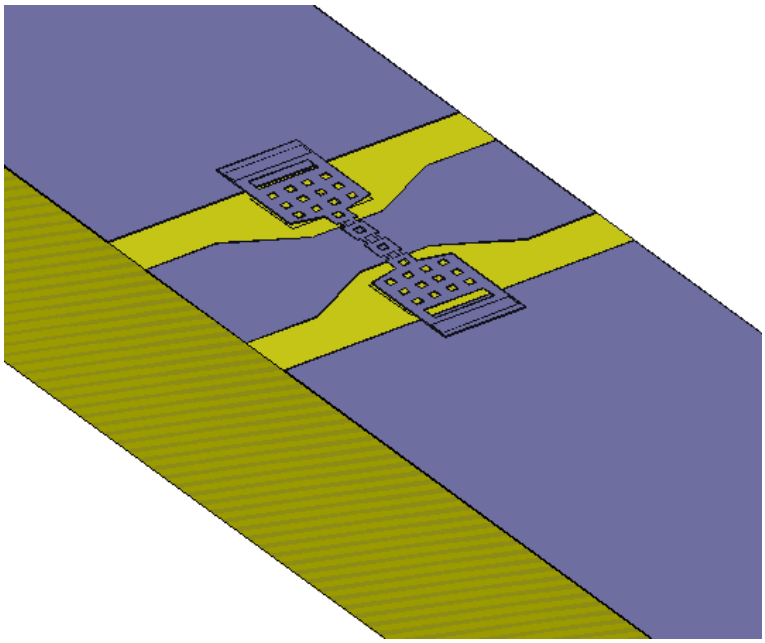

Figure 5.30: The simulated MEMS switch in Ansoft HFSS

The last step in the phase shifter design is the overall load design. By placing multiple switches along the transmission line, we can change the electrical length of a short ended transmission line. Changing the electric length of the short ended line will change linearly, the phase of the input reflection of the transmission line. Therefore, by actuating any of the switches, the output phase of the phase shifter alters. A 50 Ω CPW transmission line on a 25 mil alumina substrate with $W = 190\mu m$ and $G = 72\mu m$ is built as the load transmission line. The switches are placed along this transmission line. The transmission line below each switch has been tapered to compensate for the capacitive load on the CPW due to MEMS shunt switches.

The number and the locations of the switches are chosen based on the resolution of the phase shifter. In this design, in order to have 45° of phase shift steps, 8 switches are placed to realize the full 360° phase shift. Theoretically, the distance between successive switches in this 3-bit phase shifter should be $\lambda_g/8 \approx 200\mu m$. Since the size of each switch is greater than $200\mu m$, the consecutive spacing of the switches is chosen to be $3\lambda_g/8$ to have full 360° phase shift. The layout of the designed load is shown in Fig. 5.31.

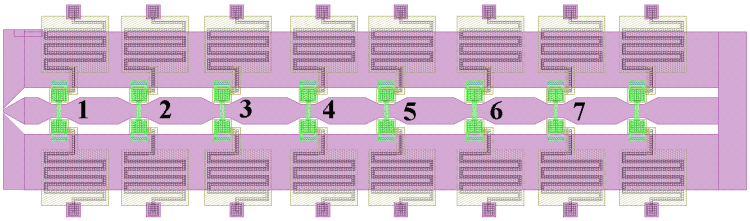

Figure 5.31: Layout of the proposed load

5.5.4 Fabrication process

The phase shifter was fabricated at the clean room of the Center for Integrated RF Engineering (CIRFE) located at the University of Waterloo, using a modified version of the UWMEMS process [143]. The process consists of two structural layers of gold, one biasing layer of chromium, and one insulator layer of silicon dioxide. A low loss ceramic, alumina substrate that is 25 mil and has a dielectric constant of 9.9 was used in our fabrication process. The process starts with an E-beam of the chromium layer and patterning it to form the biasing lines. Then a 0.5 μm silicon dioxide is deposited using Plasma-Enhanced Chemical Vapor Deposition (PECVD). A 40 nm of chromium to work as an adhesion layer, followed by a 50 nm gold seed layer, is deposited and electroplated to form the first structural layer. A sacrificial layer of polyimide PI2562 that has a thickness of 2.5 μm is spin coated and cured at 350°C. A 1.2 μm deep dimple, using a time controlled manner, is etched using oxygen plasma with a Reactive Ion Etching (RIE) tool. Those dimples reduce the contact resistance due to its small contact area and as a result increase the pressure. Anchors were etched for a longer time relying on the first gold layer as an etch stop. An adhesion layer of the chromium was used when the anchors were to be on alumina; however for gold to gold contact no adhesion is needed. Finally, the second structural layer that consists of gold was electroplated after sputtering 200 nm of gold. The targeted thickness of the second gold layer is 1 μm. The fabricated phase shifter is then released by etching the polyimide layer using an Inductively Coupled Plasma (ICP) oxygen plasma. The SEM pictures of the fabricated phase shifter are shown in Fig. 5.32.

5.5.5 Simulation results

Electromechanical simulations

The continuous model of the switch part is built in ANSYS [144]. Fig. 5.33 shows the deformed structure at the pull-in voltage. The pull-in voltage occurs at 30 volts.

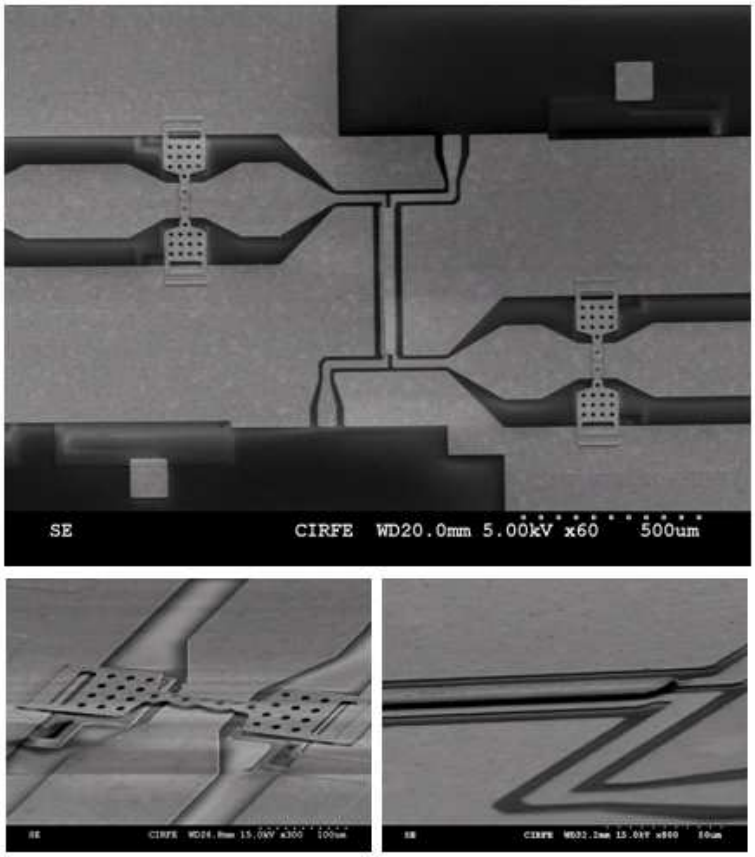

Figure 5.32: SEM picture of the fabricated phase shifter, the broadside coupler and the contact switches

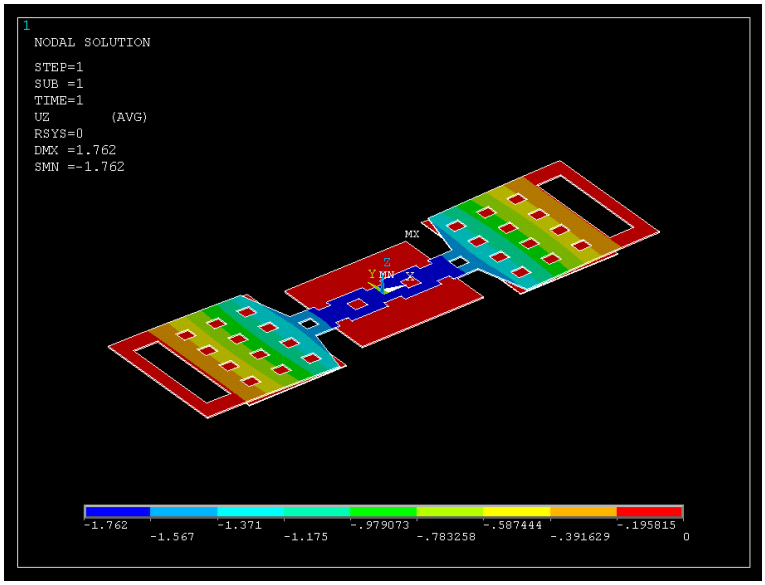

Figure 5.33: The electromechanical modeling of the switch in ANSYS

RF simulations

The simulation results of the broadside coupler in Ansoft HFSS are shown in Fig. 5.34. The structure is optimized to have signals with same magnitude at second (*through*) and third (*coupled*) port with 90° phase difference at 60 GHz. The simulated insertion loss of the broadside coupler is about 0.6 dB at 60 GHz. The isolation and input return loss at 60 GHz are better than 17 and 18 dB, respectively.

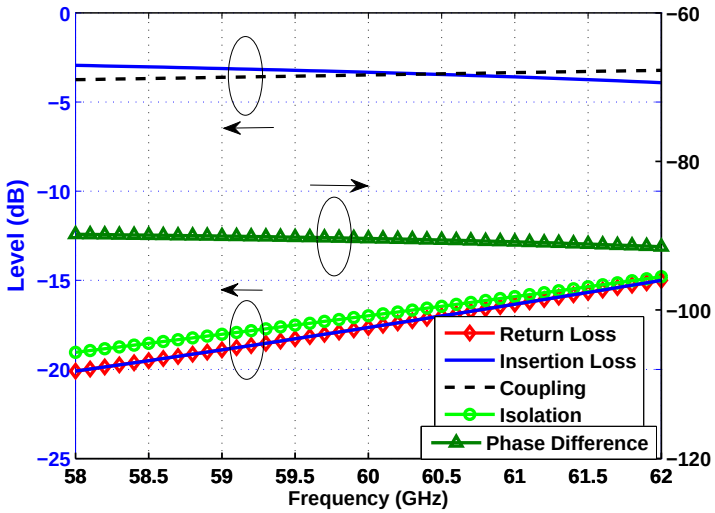

Figure 5.34: Simulation results of the designed broadside coupler in HFSS

The overall load has been simulated in HFSS. The full EM simulations has been done on the load for each of the switches states. The results show that the phase shifter has an average loss of 2.5 dB. The output phase of the phase shifter for different states provide 45 degree phase shift which is 360 degree in total.

5.5.6 Measurement results

The measurement results are shown in Fig. 5.35 and Fig. 5.36, respectively. The phase shifter has been tested for different switch states. As an example for state no. 1, switch number 1 on both loads, as depicted in Fig. 5.31 are being actuated. The S-parameters at 60 GHz have been measured for all 8 states. The S-parameters in dB are shown in Fig. 5.35. The measurement shows that the insertion loss of the phase shifter at 60 GHz is changing between 2.4 dB and 5.5 dB. The loss variation is about 3 dB over all states. The input and output return losses are better than 9 dB for all states.

The phase shift of the S_{21} for the 8 switching states at 60 GHz can be represented in the polar diagram as shown in Fig. 5.36. However the steps are not exactly 45° which could be due to the phase variation of the switches when they are not closed.

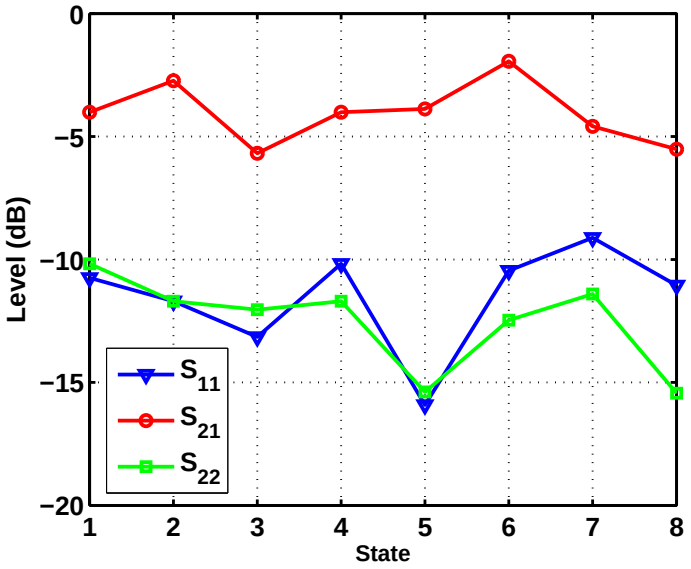

Figure 5.35: The S-parameters of the phase shifter 60 GHz for different switch states in dB

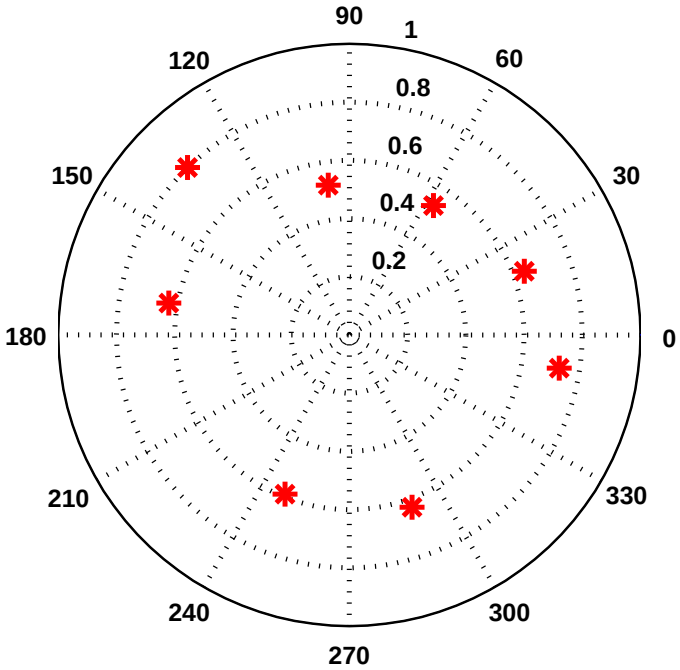

Figure 5.36: The polar representation of s_{21} at 60 GHz for different switch states

5.6 Chapter summary and conclusions

In this chapter, after a short discussion on the phase shifter and its applications in RF systems, an analysis on the effect of the phase shifter's limited phase shift was done. It was shown that a phase shifter with phase shift of more than 180° the average array factor is only 0.5 dB less than ideal phased-array. Then after introducing different topologies for the phase shifters, for the first time A Reflective Type Phase Shifter (RTPS) was chosen for mm-wave phase shifting in CMOS technology. The main advantages of the design are continuous phase shifting and zero power consumption. The two RTPS in CMOS 90 nm and CMOS 130nm were designed and verified. After that, in order to evaluate the performance of MEMS technology for the emerging wireless applications, MEMS-based RTPS was introduced and the design process as well as measurement results were reported.

Chapter 6

Proposed mm-Wave Integrated Phased-Array in CMOS Technology

6.1 Phased array design

As discussed earlier, the RF phase shifting architecture requires less chip area and has the lowest LO routing complexity. However, to design an efficient front-end and low-loss linear phase shifter is challenging. Some of the phased-array systems in literature use low-resolution digital phase shifters, such as 2-bit phase shifters, to steer the antenna beam [145, 146]. Using analog continuous phase shifters increases the beam-space resolution and ERIP [66, 95]. Furthermore, by applying zero-knowledge beamforming algorithms [49], no knowledge/calibration of phase shifters is required which decreases the cost when in mass production. This section discusses the design and experimental verification of the CMOS phased-array receiver front-end architectures for 60-GHz wireless communication.

6.2 Phased-array radio architecture

As the number of array elements in the phased-array grows, the system architecture design become more challenging. The LO routing is more complex, while the chip area and power consumption should be kept at a minimum. According to the discussion in section 3.1.2 the RF-phase-shifting architecture has been used. Let's assume the proposed variable-IF dual-conversion RF-phase-shifting architecture for both receiver and transmitter shown in Fig. 6.1.

Using the system analysis in [95] for this architecture the values chosen for the VCO frequency, frequency of the applied LO to the first mixer, the IF frequency and the image frequency are shown in Table 6.1.

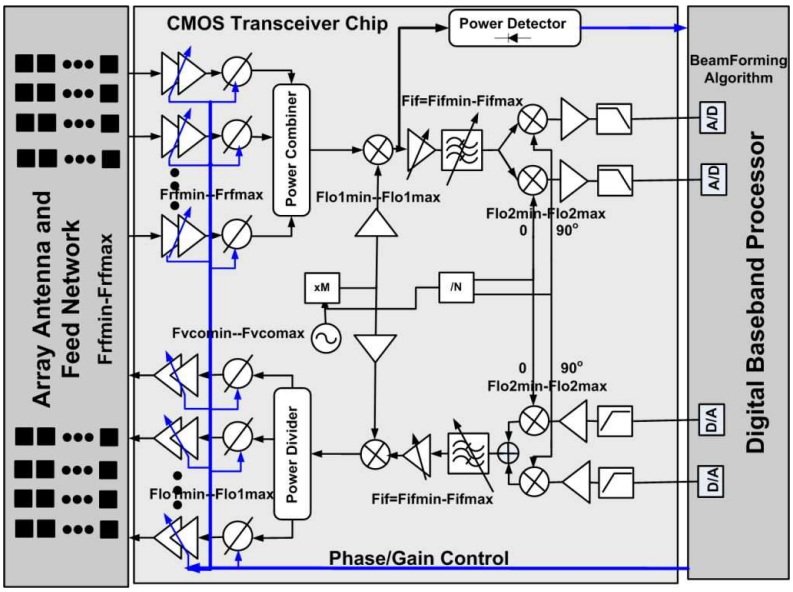

Figure 6.1: The block diagram of proposed phased-array transceiver

Table 6.1: Values chosen for VCO frequency, IF frequency and image frequency.

f_{RF}	M	N	f_{LO1}	f_{Image}	f_{VCO}	f_{IF1}
57-66 GHz	2	2	45.6-52.8 GHz	34.2-39.6 GHz	22.8-26.4 GHz	11.4-13.2 GHz

In the chosen frequency plan, at the receiver side the first mixer down converts the RF combined signals to the first center IF which is between 11.4 and 13.2 GHz. The second down conversion stage, will directly convert the IF level to the baseband. The analog baseband signal will be digitized using the high speed A/D converter after amplification and filtering. A portion of the IF signal will go to the power detector to measure the level of the input signal for beamforming algorithm. The algorithm will control the output phase of the phase shifter and the gain of amplifiers (if needed).

At the transmitter side, the I and Q signals are converted to analog signals through the high speed D/A blocks. The harmonics of the converted signal and also the spurious signals are filtered by the low pass filters. The filtered signal is then up-converted to the 12 GHz IF by the first I and Q up-conversion stage. After another stage of filtering and amplification, the signal is up-converted to 60 GHz. The LO feed-through and generated spurious at the output of the second mixer are filtered out by the band pass filter centered at 60 GHz. The RF signal is divided and distributed into each path. The signal of each path is phase shifted and amplified by the phase shifter and the power amplifier before feeding the transmit antenna array.

6.3 RTPS-based phased-array front-end

6.3.1 Block diagram

Fig. 6.2 shows the multi-element receiver front-end including the down-conversion mixer based on the RTPS to implement in 0.13 μm CMOS technology. In this section, the design of a 2 $\times$ 1 phased-array is explained. The low noise amplifier block consists of a 3-stage cascode amplifier. The RTPS connected to the LNAs rotates the phase of the signals from the antennas. The outputs from the two paths are combined at a Wilkinson power combiner. The combined signal is converted to a differential signal using a balun.

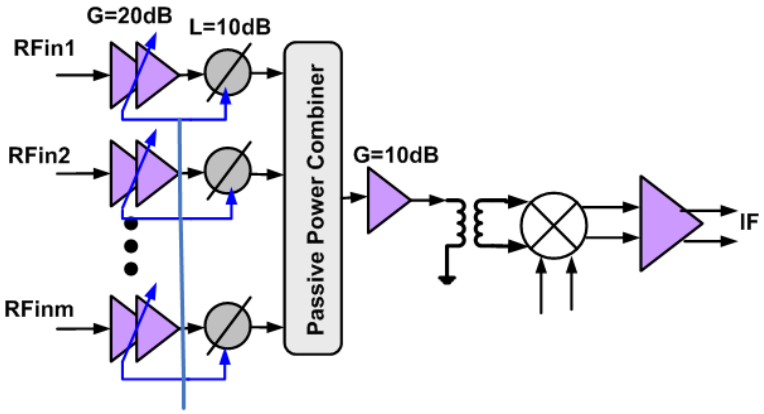

Figure 6.2: RF phase shifting receiver front-end based on passive phase shifting

The advantages of this approach are linearity, lower power consumption and a wideband front-end. The front-end can be easily scaled to a higher number of array elements. In that case, each path is repeated and the power combiner will be scaled accordingly.

6.3.2 Block designs

In this section the design of the blocks of the proposed system is explained.

Low-noise amplifier

Different CMOS LNA topologies such as common-gate [147], common-source, and cascode [5, 148, 149] structures are utilized and implemented for mm-wave receivers including in 60-GHz systems. Fig. 6.3 depicts the transistor-level schematic of a Common-Source (CS) and a Common-Gate (CG) topology. The common-gate amplifier provides a wideband input matching with good reverse isolation, however,

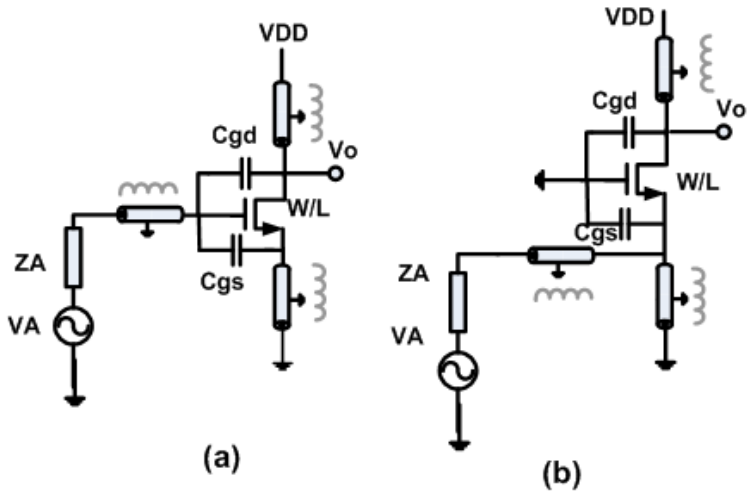

Figure 6.3: Different single transistor CMOS amplifier topologies a) Common Source b) Common Gate

the noise figure of the CG LNA is considerably higher than that of the CS or cascode LNAs.

Compared to the CS and CG topologies, the cascode structure allows for a better stability. A higher gain can also be achieved; however, its noise figure is higher due to the extra noise introduced by the cascode transistor. In fact, the cascode topology can be considered as the cascaded of the CS and CG stages. Fig. 6.4 shows two possible cascode topologies. The first circuit illustrates the commonly cascode with inductive source degeneration. The inductor at the source of the CS device facilitates the input matching; however, it lowers the gain. Inter-stage inductor has been used to improve the matching between the CS and cascode transistors.

Fig. 6.4b shows a topology that provides a higher gain by adding an inductor at the gate of the cascode transistor. The added inductor pushes the achievable gain of the cascode amplifier closer to its limit which is the Maximum Stable Gain (MSG). The biasing of the drain and gate of the transistors is provided through transmission line elements that are also part of the matching circuit. A three stages cascode LNA, as shown in Fig. 6.5, was designed for the proposed front-end. The transmission lines TLG_1, TLG_2 , and TLG_3 are used to increase the gain of cascode amplifier as compared to conventional cascode architectures which connect the gate of cascode transistors to signal ground.

A balance between the stability and the high gain is required in the design. Also, through proper design for good isolation between bias lines and the V_{DD} of the three stages, single V_{DD}, V_G and V_{G-Cas} were used for biasing the amplifier. This reduces the complexity of the biasing circuit required for the amplifier. The transistor size ($W/L = 50\mu m/0.13\mu m$) and bias current are optimized to achieve maximum gain at 60 GHz. Fig. 6.6 shows the die micrograph and two port measurement results

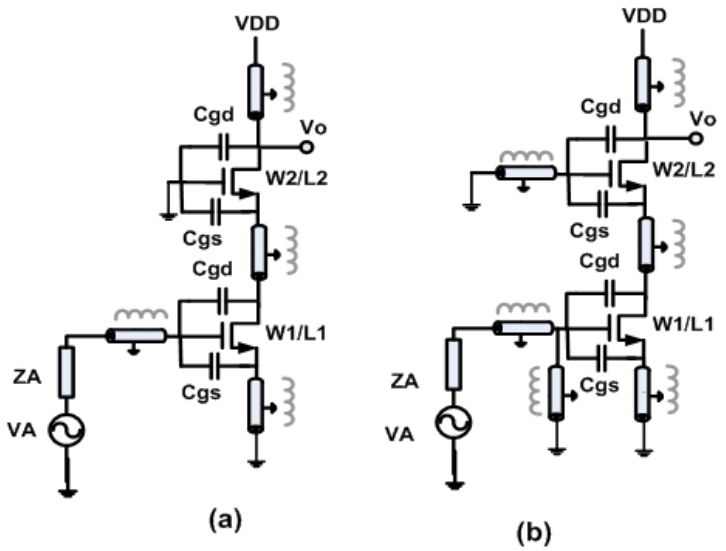

Figure 6.4: Different cascode CMOS amplifier topologies a) most common topology b) optimal topology

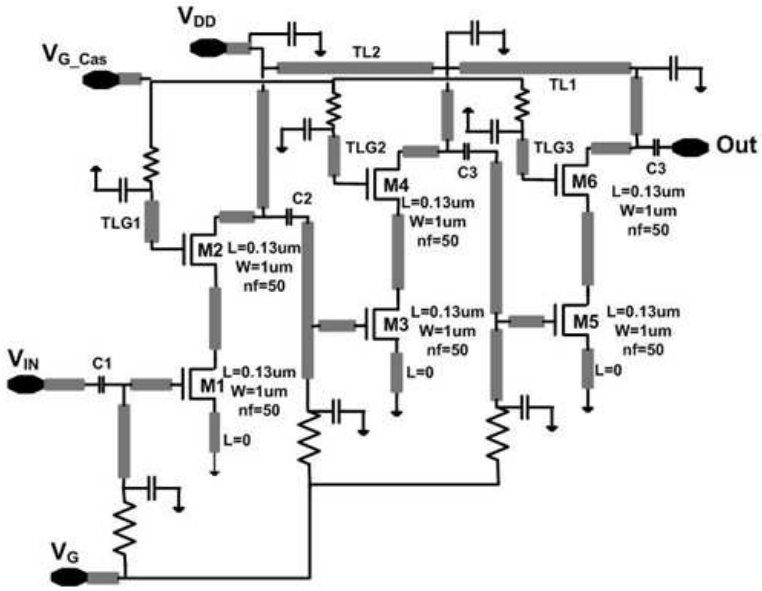

Figure 6.5: A schematic diagram of 3 stages low noise amplifier

of the amplifier. The maximum measured gain of about 19 dB at 59.5 GHz at $V_{DD} = 2V$ was achieved. The measured input and output return loss over 57 to 66 GHz was better than 9 dB. The 3 dB bandwidth of the LNA is about 5 GHz around the center of 59.5 GHz.

The LNA gain control can be used by the beam-forming controller to adjust the gain of each path and compensate the phase shifter insertion loss variation in the

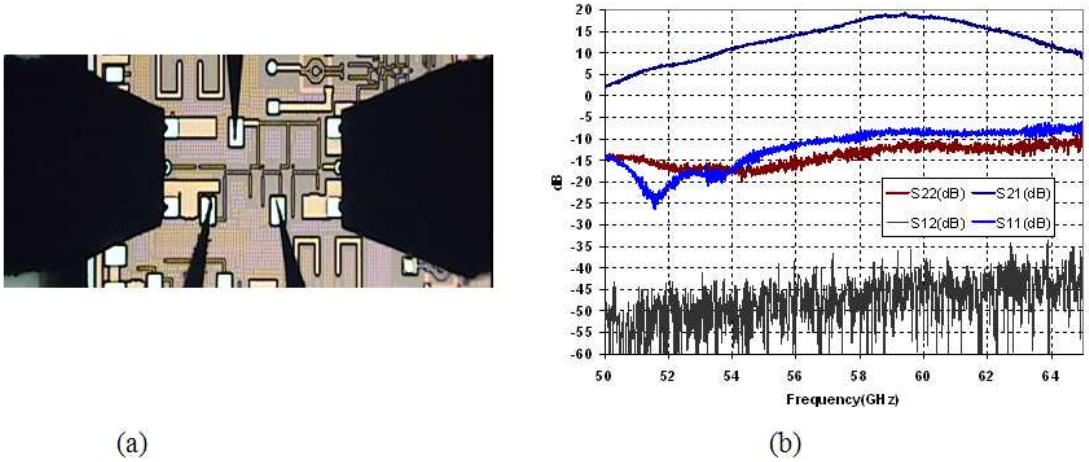

Figure 6.6: (a) Die photo of 60 GHz CMOS amplifier in 0.13um CMOS technology (b) Measured S parameters of the amplifier.

array configuration. The simulation shows that the input P_{1dB} of the amplifier is -16.8 dBm and the saturated output power of the amplifier is about 5 dBm. The simulated noise figure of the amplifier is 6.7 dB under typical process conditions. The simulated IIP3 of the amplifier is -7.13 dBm [95].

Phase shifter design

The detailed design of reflective-type phase-shifter (RTPS) is shown in Chapter 5.

Power combiner design

To combine the two signals coming from the LNAs and phase shifters, the transmission line based microstrip Wilkinson power divider/combiner is designed in the top metal layer of this technology. The bottom metal layer is used as the reference ground plane. For realizing the 100 Ω balance resistor between the arms of combiner, the resistive layer with sheet resistance of 60 Ω/□ was used. The quarter-wavelength 70 Ω lines are meandered to reducing the size. The power combiner was designed and optimized using Ansoft HFSS [142] environment. Fig. 6.7 shows the insertion loss and return loss graphs. The maximum insertion loss in the desired bandwidth is 0.45 dB (considering the loss tangent of 0.01 for all dielectric layers).

Down-conversion mixer

As part of the receiver architecture, a double balanced mixer was designed in CMOS 130 nm technology. More details are provided in [95].

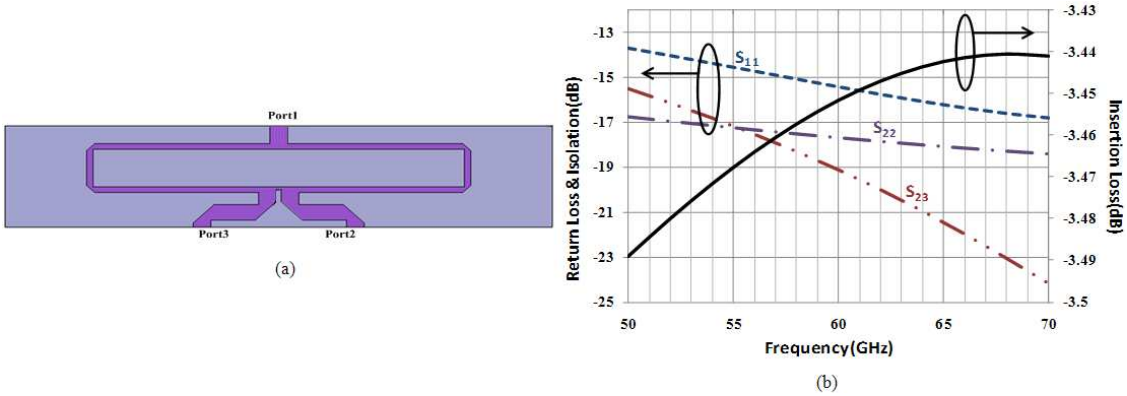

Figure 6.7: (a)Top view of the Wilkinson combiner. (b)Insertion and return loss of Wilkinson combiner/divider.

6.3.3 Phased array performance

The receiver array die block diagram and the chip under testing are shown in Fig. 6.8. A 3-stage cascode amplifier was used as a low noise amplifier block. The LNA block is followed by a RTPS and the outputs of the two paths are combined using a Wilkinson power combiner. The combined signal is converted to a differential signal using a balun. The advantages of this approach are linearity, lower power consumption and a wideband front-end. The front-end is easily scalable to higher number of array elements. The receiver array die under test is shown in Fig. 6.8(b) excluding the pads, the two element front end including the mixer occupies $2.2mm^2$ silicon area.

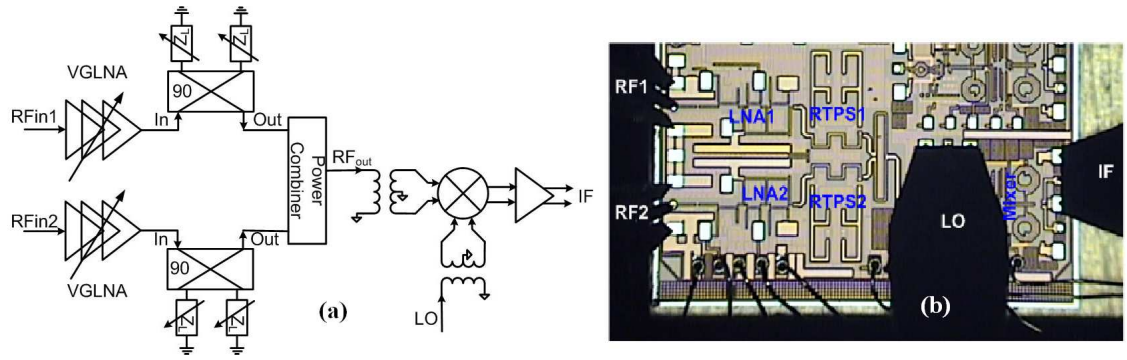

Figure 6.8: A two element phased-array front-end based on RTPS phase shifter (a) block diagram (b) Die micrograph (The occupied area is $2.2mm^2$).

Fig. 6.9 shows the measurement setup used for the characterization of the two element array chip. The 60 GHz signal from the output of the Agilent E8257D PSG analog signal generator is used as the 60 GHz signal source. An external power splitter was used to divide the RF signal between the two inputs. The measured amplitude and phase mismatch between the two outputs of the power divider at 60

GHz are 0.68 dB and 6°, respectively. The RF cable connects the signal generator to the power splitter. The total insertion loss of each cable from the input of the signal generator to the input of RF probes (including power splitter insertion loss and the cable insertion loss from the power split outputs to the probes input) is about 20 dB. The GGB 110H dual probe with adjustable distance between the tips was used to apply the 60 GHz signals to the input pads. The insertion loss of the probe at 60 GHz according to the datasheet is 1.5 dB. The die was mounted on a printed circuit board with the silver epoxy. The bias pads were bonded to the printed circuit board through the gold wirebonds. All the required bias levels for the chip were applied through the printed circuit board and wire bonded pads.

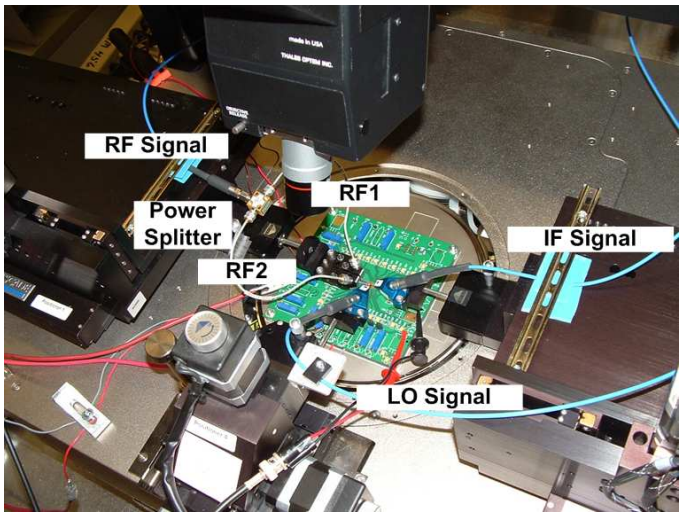

Figure 6.9: Measurement setup at 60 GHz

The 48 GHz LO signal is applied to the LO pads through the i67 infinity CPW probe. Another infinity CPW probe was connected to the spectrum analyzer, that monitors the IF signal. Fig. 6.10 presents the measured combined power at the IF output when two RF signals that are in phase are connected to the RF inputs. For this measurement, the control voltage for one channel was fixed at 0 V and the control voltage for the second channel varied between 0 to 1.5 V. As the voltage control of the channel 2 increases, the power level at IF decreases due to the added phase shift in one path. Out of phase cancelation of about 15 dB was measured. This number is limited to the amplitude mismatch between the two paths as a result of the phase shifter insertion loss variation.

Fig. 6.11 presents the conversion gain versus the RF frequency while the IF was fixed at 12 GHz by sweeping the LO and RF simultaneously. The RF and LO frequencies were swept from 54 to 66 GHz and 42 to 54 GHz respectively. This measurement shows a 3 dB bandwidth of 4.5 GHz for the front-end.

Channel to channel isolation versus the frequency is shown in Fig. 6.12a. The isolation is better than 45 dB over the frequency range of 55 to 66 GHz. Fig. 6.12b illustrates the LO to RF and LO to IF isolation versus the frequency. The LO to

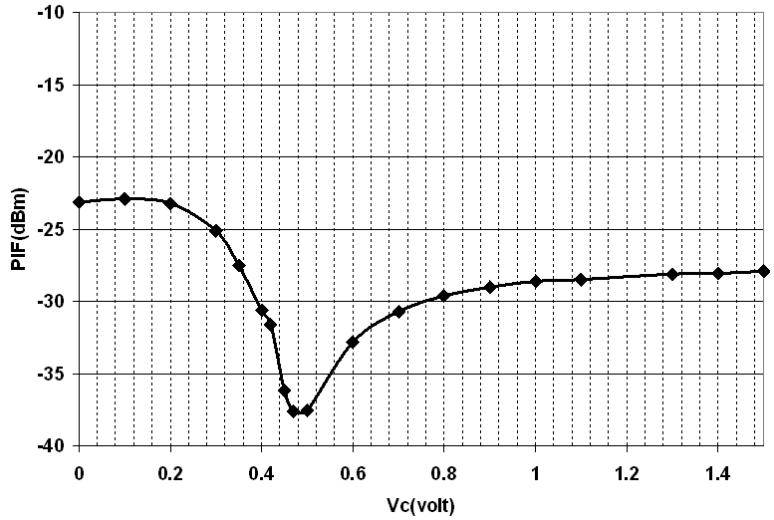

Figure 6.10: Measured IF power versus $V_{C2}(F_{RF} = 60GHz, F_{LO} = 48GHz, P_{RF1} = P_{RF2} = -30dBm, V_{C1} = 0, V_{C2}$ varies from 0 to 1.5 V)

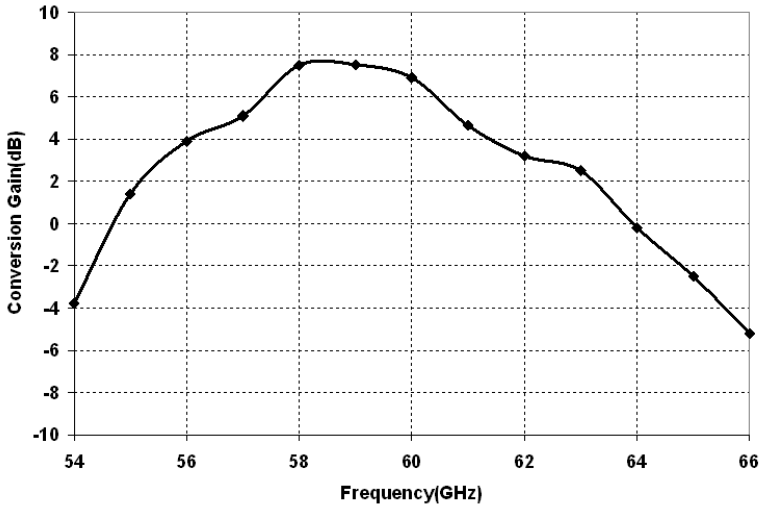

Figure 6.11: Measured maximum receiver conversion gain versus RF frequency ($V_{C1} = V_{C2} = 0V$)

RF isolation is better than 50 dB over the frequency range of 50 to 64 GHz. The LO to IF isolation varies between 17 to 13 dB for the LO frequency range of 45 to 50 GHz. This can be easily filtered out since the receiver IF is centered around 12 GHz.

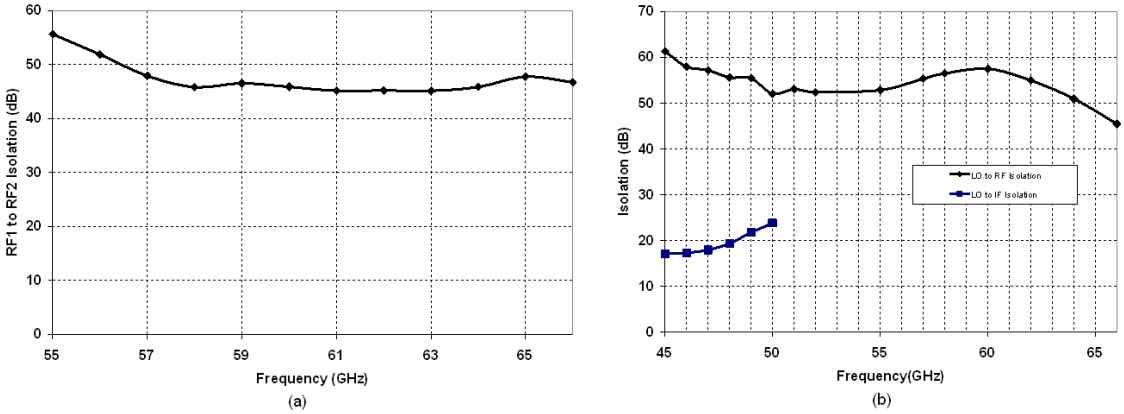

Figure 6.12: (a) Measured On-chip channel to channel isolation (b) Measured LO to RF and LO to IF Isolation versus frequency

6.4 Phased-array with integrated on-chip dielectric resonator antennas

In designing the mm-wave phased-arrays for short range wireless applications with beamforming capabilities, partly or fully on-chip antenna that is integrated with the front-end is a suitable candidate for implementing fully integrated radio systems. In addition, for the applications such as imaging, an integrated high performance antenna and front-end is needed. In this section, in order to evaluate the performance of the mm-wave integrated phased-array with on-chip antennas, a 60 GHz 2-by-1 phased-array with on-chip antenna has been designed and fabricated.

6.4.1 mm-Wave on-chip antennas

An on-chip antenna simplifies the matching between the antenna and the front-end, and improves the performance of the RF systems from a gain and noise figure point of view. At mm-wave band, the size of the antenna which is in the order of the wavelength is comparable to the chip-size. Therefore, implementation of a monolithic integrated mm-wave system on semiconductor substrates become an attractive and practical option. A considerable amount of research has been dedicated to this topic over the last few years [3, 6, 38, 74, 83, 96, 150–162]. Most of the efforts use the low-cost silicon-based semiconductor technologies such as CMOS or SiGe to realize the fully integrated system solutions at mm-wave [161, 163]. Many of the reported on-chip antennas have low radiation gains (below -5 dBi) or low radiation efficiency (below 10%) [74, 96, 155, 156]. Therefore, designing a high-efficiency on-chip antenna is a crucial step towards realizing system-on-chip solutions. The main source of loss in the low-cost silicon technology which is the low resistivity of the silicon substrate (0.01-20 Ω-cm) which deteriorates the performance of passive integrated elements. The leakage through the substrate not

only creates unwanted crosstalk between digital circuits, RF and analog circuits, but also reduces the radiation efficiency of the antenna system. There is also the restriction on the chip area which limits the aperture size, and thereby reducing the radiation gain of antenna.

Fig. 6.13 illustrates the previously developed integrated on-chip antenna configuration in our group for the integrated on-chip antenna [95]. The proposed structure consists of:

- Silicon substrate
- Cavity and shield layer
- H-Slot aperture
- Passivation layer
- Dielectric Resonator

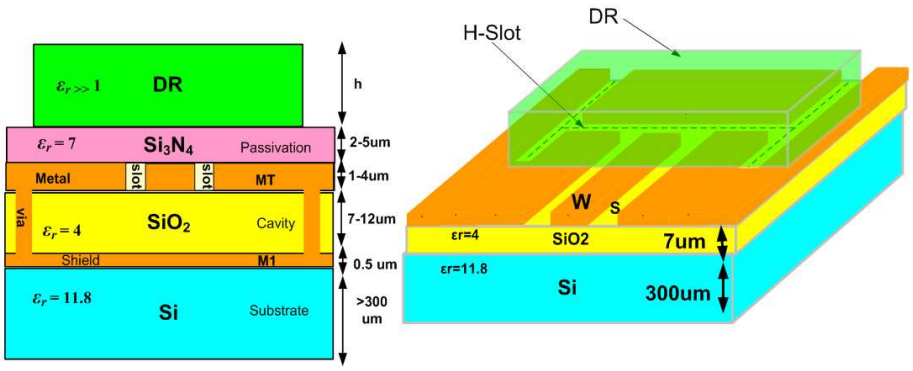

Figure 6.13: On-chip cavity backed slot antenna with dielectric resonator on top. Cross section and 3D structure

The slot aperture is implemented on the top metal layer of the silicon technology. The lowest metal layer (M1) is connected to the top ground plane through via holes and behaves like a shield. By shielding the antenna from lossy silicon substrate, the antenna substrate is limited to silicon dioxide (SiO_2) and the intermediate dielectric layers between the metal layers. Also a cavity is formed under the slot antenna. In integrated silicon technology, usually up to 10 metal layers and a thin film silicon dioxide in between exists for the interconnection and routing. The maximum distance between the top and bottom metal layer depending on the process technology used and the metallization option varies from 7 to 15 μm. Thus the maximum thickness of the cavity in the proposed antenna configuration is limited. Generally, a silicon nitride (Si_3N_4) layer for passivation purposes with the thickness of 1-5 μm is placed on top of all the layers except the input/output pads

to isolate and protect top level interconnections from the outside world. Finally, a dielectric layer with a large permittivity is placed on top of the chip to increase the radiation efficiency and improve the antenna matching. It is shown [164] that the passivation layer can be removed for more efficient coupling to the dielectric resonator. Placing the DR improves the radiation efficiency through the following mechanisms [95]:

- A high dielectric constant material on top changes the field distribution and therefore the field will be concentrated in dielectric material on top.
- A dielectric resonator acts as an antenna excited by slot if designed and configured properly.
- A dielectric resonator with high dielectric constant tends to confine near-field energy inside the dielectric and therefore reduces the field intensity and loss inside the lossy substrate. This feature also reduces the mutual coupling between adjacent elements in an array of such antenna elements.

In designing the integrated phased-array with on-chip antennas, this antenna is scaled and optimized to operate at the 60 GHz band. Fig. 6.14 shows the block diagram of the two-by-one phased-array with an on-chip H-slot antenna. The signals received by two H-slot antennas are amplified by low noise amplifiers and is phase shifted by the reflective-type phase shifters. The two VGAs are to compensate the gain variation of each channel due to the phase shifter imbalance insertion loss. After all that, the two outputs are added at the power combiner. In following paragraphs the design of the blocks are explained.

6.4.2 60 GHz on-chip H-Slot dielectric resonator antenna

The H-slot is an aperture-type electrically small antenna. A slot aperture can be end-loaded to reduce its overall length at a given resonance frequency [165]. For example, the maximum size of the slot antenna to show a resonance at 60 GHz is 0.85 mm. Thus, the overall length of the antenna is almost $\lambda_{g0}/8$, or 4 times smaller than a half-wavelength dipole operating at the same frequency. The radiation efficiency of such an electrically small antenna is negligible (less than 1%) [95]. To improve the radiation efficiency of the integrated antenna, a layer of dielectric constant material with a high permittivity is added on top of the slot aperture to create a rectangular DR antenna [160]. The magnetic current over the slot excites the first order mode of the dielectric resonator. Thus, the integrated antenna can radiate the input power, more efficiently.

In order to design the DRA introduced in [95], we have to first look into the excited modes in the rectangular dielectric resonator. By studying the excited modes, we can find the dimesnsions of the resonator. As mentioned in [95] the

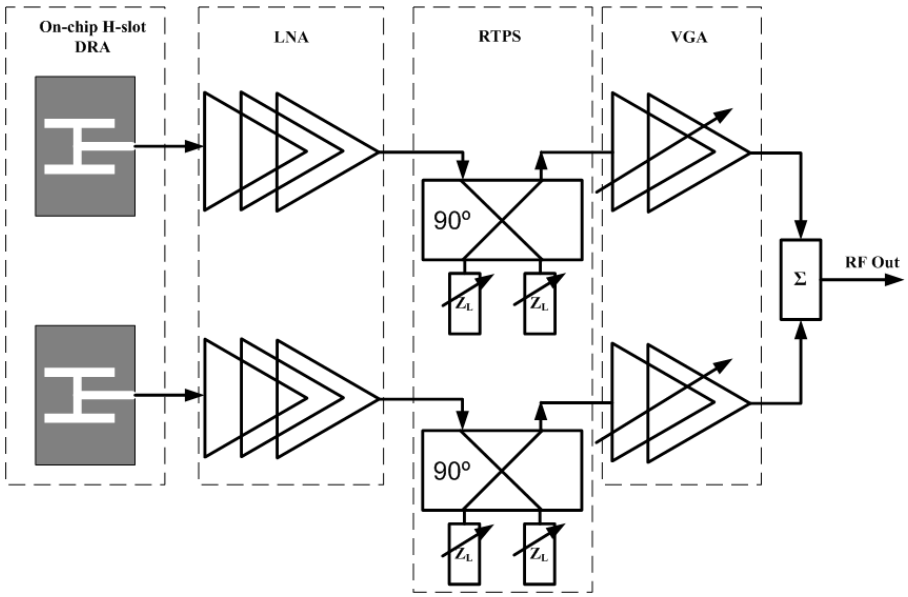

Figure 6.14: The block diagram of the two-by-one phased-array with on-chip H-slot antenna.

relative permittivity of the dielectric resonator should be greater than 10 to increase the efficiency of the antenna. The available ϵ_r options to order the dielectric resonators from our commercial source (TCI Ceramics) are 12 and 36. The benefit of using the material with $\epsilon_r = 12$ is that the antenna with dielectric resonator using this material has a wider operation bandwidth. Not only that, but the fabrication of a highly accurate dielectric resonator with minimum fabrication errors for the single antenna or array of them is feasible through the monolithic fabrication process on high-resistivity silicon substrates. An example of the fabrication of a disk resonator and a dielectric waveguide are shown in [166]. A similar process can be used for fabrication of dielectric resonators. The fabrication process which are shown in Fig. 6.15 are:

- Step 1: Sputtering a 0.1 μm Cr.
- Step 2: Spin coating thick photoresist AZ4620 on the sputtered Cr thin layer
- Step 3: Pattern AZ4620 photoresist with the first mask to define both the DR and DIG. The photoresist thickness is $11 \sim 12$ μm and the smallest features that can be achieved is $> 5\mu m$.
- Step 4: A wet etching of the Cr layer is performed to expose the Si wafer of the SOI. Special care is taken not to over etch the Cr layer in order to define accurately the gap between the DR and DIG.

- Step 5: Using a STS ICP-RIE etcher, the SOI wafer is placed inside the chamber for Deep Reactive Ion Etching (DRIE). The combined Cr layer and photoresist are used as the mask. The oxide layer will serve as a stop layer.
- Step 6: The wafer is cleaned in acetone to remove any photoresist, and then in O_2 plasma to fully remove any residue remaining.
- Step 7: Wet etching of the Cr thin layer to expose the remaining Si that define the DR and DIG.
- Step 8: The wafer will be diced and devices are ready to use.

It is noted that this fabrication method is not used for this design and the potential of the method for this application is introduced.

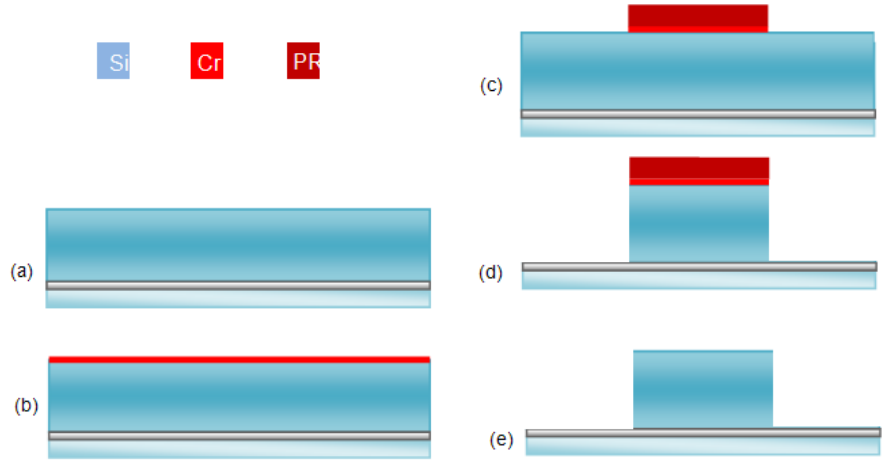

Figure 6.15: The example of fabrication steps of the dielectric resonator on high resistivity silicon wafer

In order to compare the performace of the antennas, both antennas are designed and optimized. Fig. 6.16 shows the distribution of the electric field in the dielectric resonators for both $\epsilon_r = 12$ and $\epsilon_r = 36$. The length, width and height of the DR with $\epsilon_r = 12$ are $1mm \times 0.9mm \times 0.75mm$, respectively. These dimensions for the resonator with $\epsilon_r = 36$ are $0.6mm \times 0.55mm \times 0.5mm$, respectively.

The tangential electric field at the surface of the DRA, acts as the magnetic current source and radiates the electromagnetic energy into space. The H-slot is used to couple the electromagnetic energy from the CPW port into the dielectric resonator. The H-slot is an aperture-type electrically small antenna. The end-loaded slot aperture has an overall smaller length at a given resonance frequency [165]. The magnetic current over the slot excites the first order mode of the dielectric resonator in the dielectric resonator. Adding the DR to the H-slot antenna improves the radiation efficiency due to [164]:

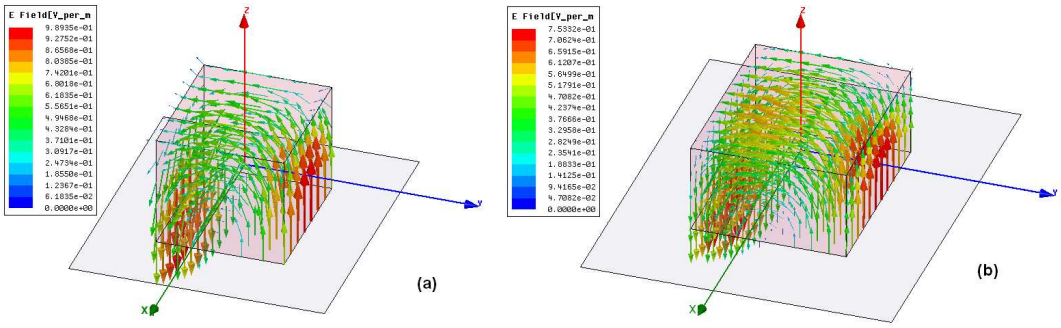

Figure 6.16: Distribution of electric field for simulated eigenmode analysis. (a) Dielectric resonator with $\epsilon_r = 12$ (b) Dielectric resonator with $\epsilon_r = 36$

- The field is mainly concentrated in the high dielectric constant material on the top.
- If the dielectric resonator is excited properly by the slot, it radiates efficiently into space.
- The tendency of confining near-field energy in the dielectric resonator with a high dielectric constant, reduces the field intensity and loss inside the lossy silicon substrate.This feature also reduces the mutual coupling between adjacent elements in the design of an array of such antenna elements.

Fig. 6.17a shows the 3D H-slot structure and the DRA on top of it for $\epsilon_r = 12$. The parameters x_c, y_c, l_1 and l_2 which are the H-slot physical dimensions and the cavity size are depicted in Fig. 6.17b. The dimensions of the DR calculated from the eigenmode analysis and the H-slot physical parameters are optimized to have resonance at 60 GHz band. The simulation results of the H-slot DRA with $\epsilon_r = 12$ are shown in Fig. 6.18. As it can be seen, the impedance bandwidth of this antenna covers more than 7 GHz from 57.5 GHz to 64.5 GHz. The peak gain occurred at $\theta = 0°$ and $\phi = 0°$ which is 4 dBi. The simulated radiation efficiency of this antenna is 78% at 60 GHz.

Fig. 6.19a depicts the 3D view of the H-slot structure and the DRA on top of it for $\epsilon_r = 36$. Similarly, the parameters x_c, y_c, l_1 and l_2 are shown in Fig. 6.19b. The DR dimensions and parameters x_c, y_c, l_1 and l_2 are optimized for both materials are shown in Table 6.2. L_{DR}, W_{DR} and H_{DR} are the dimensions along x, y and z axis, respectively. The simulation results of the H-slot DRA with $\epsilon_r = 36$ are shown in Fig. 6.20. As it is expected, the impedance bandwidth of this antenna is narrower than $\epsilon_r = 12$ case. It only covers 1.5 GHz bandwidth from 58.7 GHz to 60.2 GHz. The peak gain is at $\theta = 0°$ and $\phi = 0°$ which is 4 dBi. The simulated radiation efficiency of this antenna at the center band is 74%.

Between the two studied cases, the antenna with $\epsilon_r = 12$ has a wider operational bandwidth and is suitable for the wireless applications at 60 GHz. The size of the

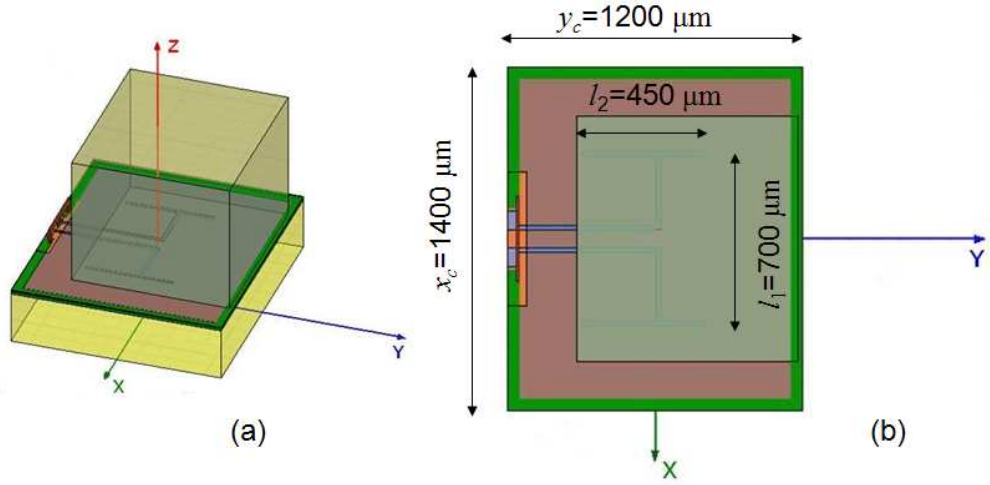

Figure 6.17: On-chip cavity backed H-slot antenna with dielectric resonator with $\epsilon_r = 12$ (a) 3D structure (b) Top view

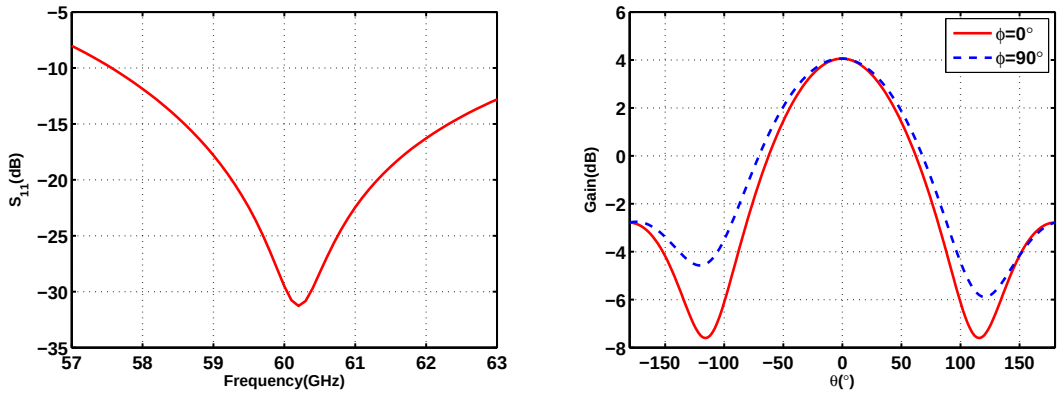

Figure 6.18: Input matching (S_{11}) and Gain of the H-slot DRA with $\epsilon_r = 12$

cavity underneath is very important and has a significant effect on the gain. In order to design the antenna, the dimensions of the cavity x_c and y_c are swept to find the best performance of the array. The simulation results are shown in Fig. 6.21. The gain increases when x_c increases. This means that the more gain required, the more die area is needed. On the other hand, the gain versus y_c has a maximum at 1.2 mm. In order to be able to choose the proper values for x_c and y_c, the simulation shown at Fig. 6.22 is used. The gain of the antenna is swept versus y_c for the different values of x_c. Among the simulated values, x_c =1.4 mm and y_c=1.2 mm are chosen to have the antenna gain more than 4 dBi.

Table 6.2: Values chosen for the dimensions of H-slot antenna and the DR with $\epsilon_r = 12$ and $\epsilon_r = 36$.

	$DR_1(\epsilon_r = 12)$	$DR_2(\epsilon_r = 36)$
x_c	1400 μm	1400 μm
y_c	1200 μm	1200 μm
l_1	700 μm	570 μm
l_2	450 μm	220 μm
L_{DR}	1000 μm	600 μm
W_{DR}	900 μm	550 μm
H_{DR}	750 μm	500 μm

The effect of DR fabrication tolerance on the performance of the antenna

Since the monolithic fabrication introduced in section 6.4.2 for the dielectric resonators was not used for the current design, the dimension errors due to cutting the DRs might become critical. According to the information provided by the manufacturer, the cutting tolerances of the DRs are within ±1 mil. In order to study the cutting tolerances effect on the resonance frequency and gain behavior of the antenna, a statistical analysis on the DR size was done. The dimensions of the dielectric resonator are chosen at random variables with a mean of nominal values and a tolerance of 5%, 7% and 4% for L_{DR}, W_{DR} and H_{DR}, respectively. The statistical analysis shows that the resonance frequency changes within 1.17% of the center frequency which is ±1.02 GHz. The gain also varies within 2.5% of the nominal value which is ±0.1 dBi.

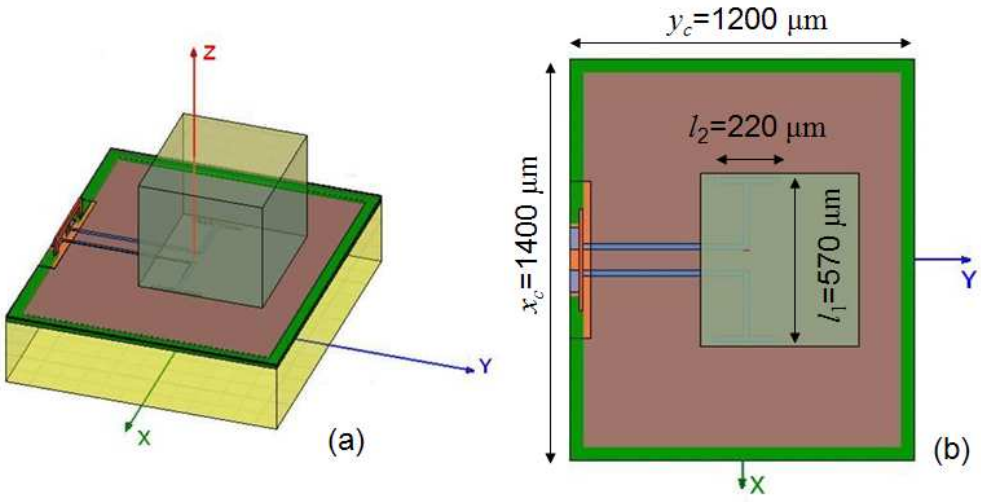

Figure 6.19: On-chip cavity backed H-slot antenna with dielectric resonator with $\epsilon_r = 36$ (a) 3D structure (b) Top view

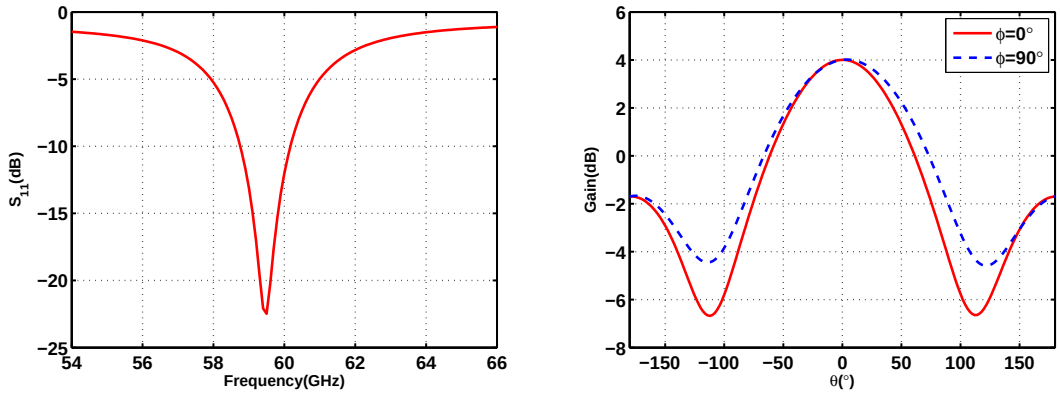

Figure 6.20: Input matching (S_{11}) and Gain of the H-slot DRA with $\epsilon_r = 36$

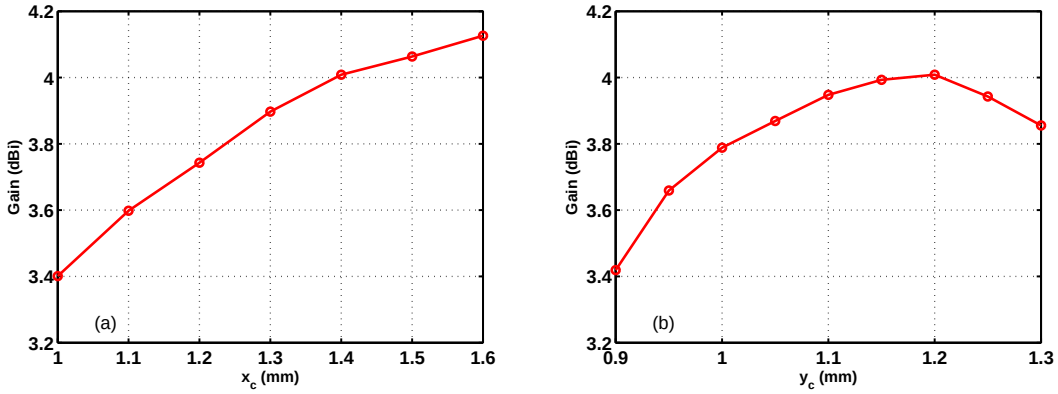

Figure 6.21: (a) Gain of the antenna for different values of x_c when y_c=1.2 mm (b) Gain of the antenna for different values of y_c when x_c=1.4 mm

6.4.3 Low-noise and variable gain amplifiers

Among the different LNA topologies implemented in the 60 GHz band, the common source topology provides the best noise performance. Using the systematic design method presented in [167], it can achieve, a large gain per transistor, a small chip footprint and have stable behavior with optimum noise performance. In this work, the amplifiers introduced by the colleagues at the University of Waterloo in [167] was used for LNA and VGA.Similar structures with 4-stage and 6-stage of amplification are used for the VGA and LNA, respectively.The transistor parameters and biasing voltages were chosen for a minimum noise figure at a current density of 130μ A/μm under a V_d of 1.4V and V_g of 0.65V. The total consumed power is 40mW under this condition.

Fig. 6.23 shows the simulation S-parameters of the 4-stage amplifier. Solid lines are measurement and dashed lines are simulation results. The maximum gain of

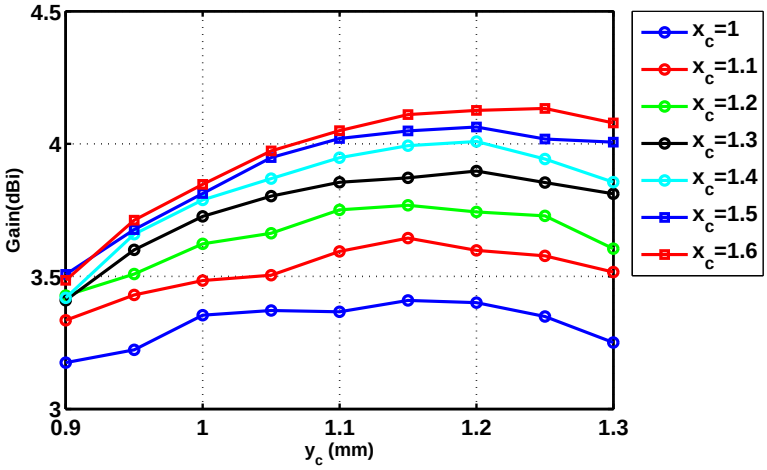

Figure 6.22: Gain of the antenna for different values of x_c and y_c.

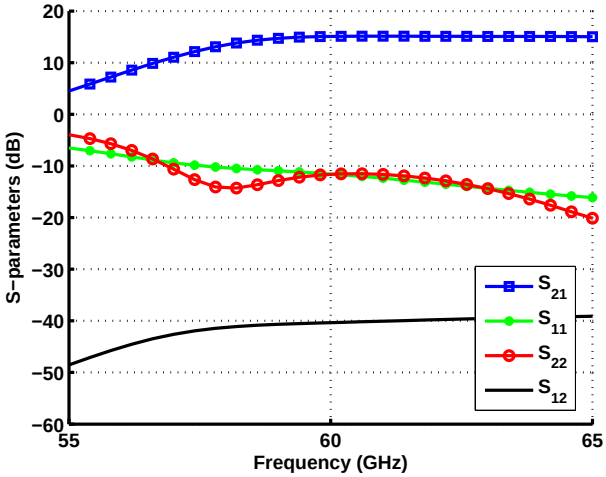

Figure 6.23: Simulated S-parameters of the 4-stage amplifier.

15 dB at 60 GHz can be achieved. This translates to about 4 dB gain per stage where the transistors are used at %65 of their cut-off frequency. The simulated noise figure is less than 6 dB which is close to the minimum noise figure. The 3 dB frequency band is from 57.2GHz to more than 65GHz.

6.4.4 Phase shifter and power combiner

Details of the design of reflective-type phase-shifter and power combiner are previously explained in chapter 5 and section 6.3.2.

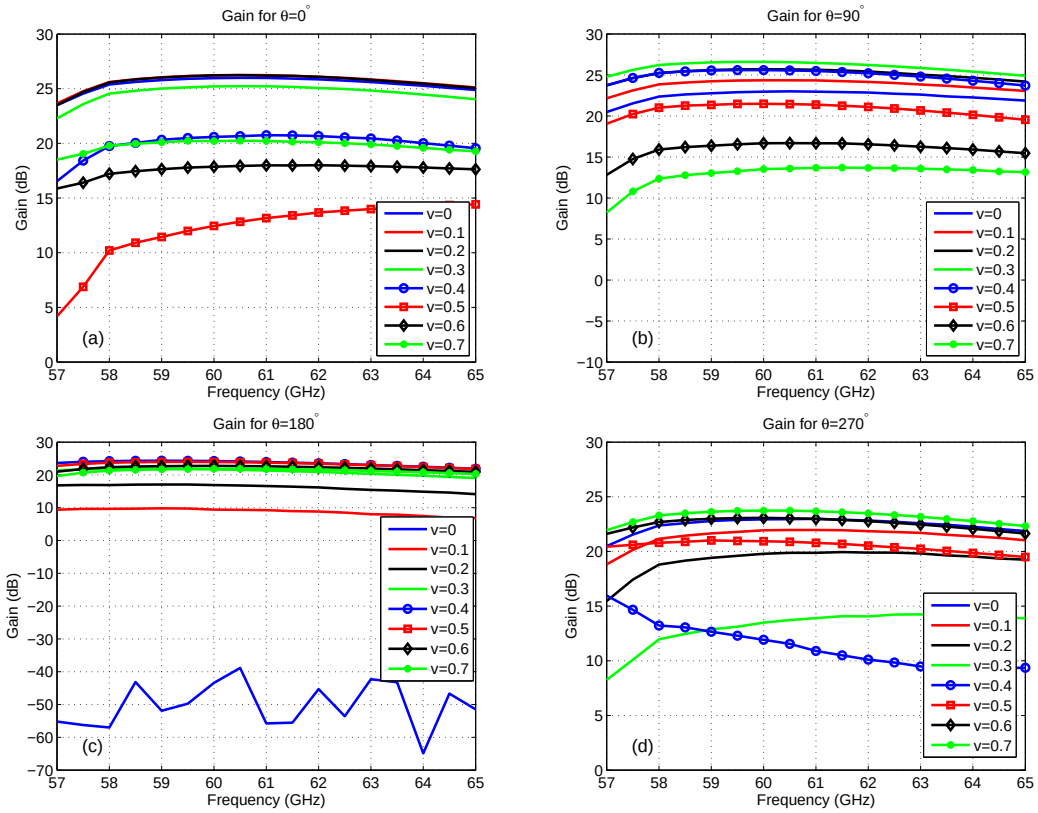

Figure 6.24: Simulation results of the gain of the phased-array for different inputs. In all figures the two inputs of the phased-array have the same magnitude and the phase differences between them are (a) 0°, (b) 90°, (c) 180° and (d) 270°

6.4.5 Phased array simulation results

The block diagram shown in Fig. 6.14 without antennas were simulated in Cadence to characterize the performance of the system. The LNA, phase shifter and the VGA blocks were cascaded and connected to the power combiner block. The simulated S-parameters of power combiner in Ansoft HFSS were imported as a 3-port network. The overall system has been simulated with AC simulation in Analog Design Environment (ADE) in Cadence.

In the simulations of the phased-array performance, two AC sources have been applied at the two inputs of the LNAs. The magnitude of both sources is set to 1. The phase of the source is connected to LNA1 is 0 and θ, the phase of the AC source connected to LNA2, will change from 0 to 270° with intervals of 90°. The gain of the LNAs and VGAs and also the tuning voltage of the RTPS1 are fixed. Then the tuning voltage of the RTPS2 is changed from 0 to 0.7 V with steps of 0.1 V. As it can be seen in Fig. 6.24(a), that the maximum gain which is 26.2 dB occurs at v=0 V. This gain corresponds to phase shift of 0°. In this set of simulations, by increasing the tuning voltage of RTPS2, the gain drops. The maximum gain drop

happens for v=0.5 V in which the gain drops by 14 dB at 60 GHz . This voltage corresponds to the output phase shift of 180°. In the simulation results shown in Fig. 6.24(b), θ is set to 90°. The gain at v=0 V drops by 3-dB which is predictable. The maximum gain occurs at v=0.3 V in this set of simulations. In the simulation results shown in Fig. 6.24(c), θ is set to 180°. Theoretically, the gain at v=0 V should be zero ($-\infty$ dB), and simulator shows a very small value (≤ -40 dB) which makes sense. The maximum gain occurs at v=0.4 V which is 1.8 dB less than the maximum gain of Fig. 6.24(a). In the simulation results shown in Fig. 6.24(d), θ is set to 270°. The gain at v=0 V drops by 3-dB with respect to the θ=0° case. Since the maximum phase shift of the phase shifter is less than 270°, the gain of the array cannot be reached to the maximum possible value (2 dB less than the maximum value).

6.4.6 Phased array measurement setup and experimental results

The block diagram of the test structure of the phased-array is shown in Fig. 6.25. The 60 GHz signal from the output of the Agilent E8257D PSG analog signal generator with a +5 dBm output power was used as the 60 GHz signal source. The RF cable connects the signal generator to the transmitter horn antenna. The total insertion loss of the cable from the input of signal to the input of horn (including the coaxial to waveguide adaptor) is about 18 dB. The horn antenna is set up at 50 cm above the receiver phased-array system to make sure the transmitter and receiver are at far-field radiation zone of each other. The free space loss for this distance is about 62 dB. Gain of the horn antenna is about 22 dBi.

The output of the power combiner on the die is probed by an i67 infinity probe with an insertion loss about 2 dB (including the connector loss) and is connected to the E4448A spectrum analyzer through a cable. The insertion loss of the interconnection cable is 16 dB at 60 GHz. Therefore the overall insertion loss from the output of the signal generator to the input of the spectrum analyzer due to the free-space, cables and interconnections loss is 76 dB. The total conversion gain of the phased-array at 60 GHz can be calculated from $G_{Array} = P_{RX} - P_{TX} + 76$. In our case, since P_{TX} is set to 5 dBm, the equation becomes:

$$G_{Array} = P_{RX} + 71. \tag{6.1}$$

The measurement setup of the phased-array receiver and the receiver phased-array photo with the DRAs are shown in Fig. 6.26 (a) and (b), respectively. The micrograph of the die is shown in Fig. 6.26(c). Since we didn't had access to an on-chip antenna measurement setup at time of measurement, the received signal in a fixed position of transmitter horn antenna on top of the receiver was measured. Although this is not an accurate antenna measurement setup due to the multiple reflections from the metallic chuck and the body of probe station, we still can have

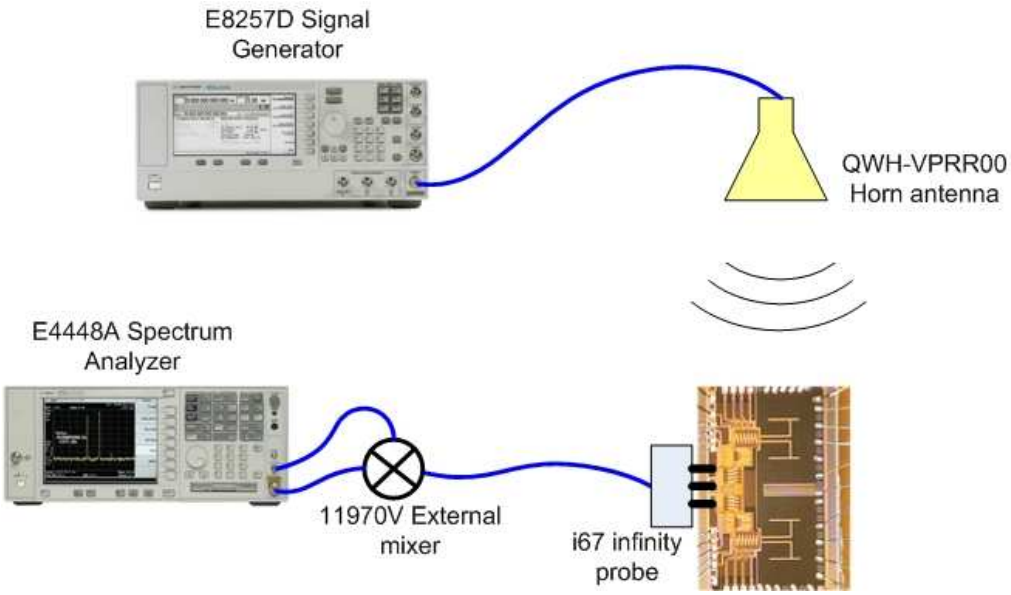

Figure 6.25: The block diagram of the measurement setup.

a good sense of the receiver performance with this measurement. Further radiation pattern of the array as well as accurate antenna characterization needs a specific on-chip antenna setup which is under development in our group.

The measured spectrum of received signal at the output of the 2-by-1 array is shown in Fig. 6.27(a). The level of the received signal is -50.3 dBm at 60 GHz. Using the Eq. 6.1, the gain of the array becomes 20.7 dB at this frequency.

The frequency is also swept manually to measure the gain response of the array between 55 GHz and 65 GHz. The maximum gain happens at 61 GHz which is 20.85 dB. The 3-dB bandwidth is from 56.5 GHz to more than 65 GHz (approximately 66 GHz). The fact that the measured gain of array is less than the simulated values could be due to poor performance of each block of the system with respect to the simulated one. Other than the circuits block, the antennas could have less gain with respect to the simulated one.

In order to test the performance of the phased-array the antenna should have been rotated in different angles to verify the phase shifting response. In the setup we used, which is not an appropriate one for antenna characterization, we didn't have that much flexibility to rotate and align the horn antenna at specific angles. Therefore, in order to test the phased-array performance, the horn is fixed at its position ($\theta = 0°$). Thereafter the tuning voltage of one of phase shifter (V_{C1}) is set to 0 V and the other tuning voltage (V_{C2}) is varied from 0 to 1.5 V. The measured gain of this measurement is shown in Fig. 6.28.

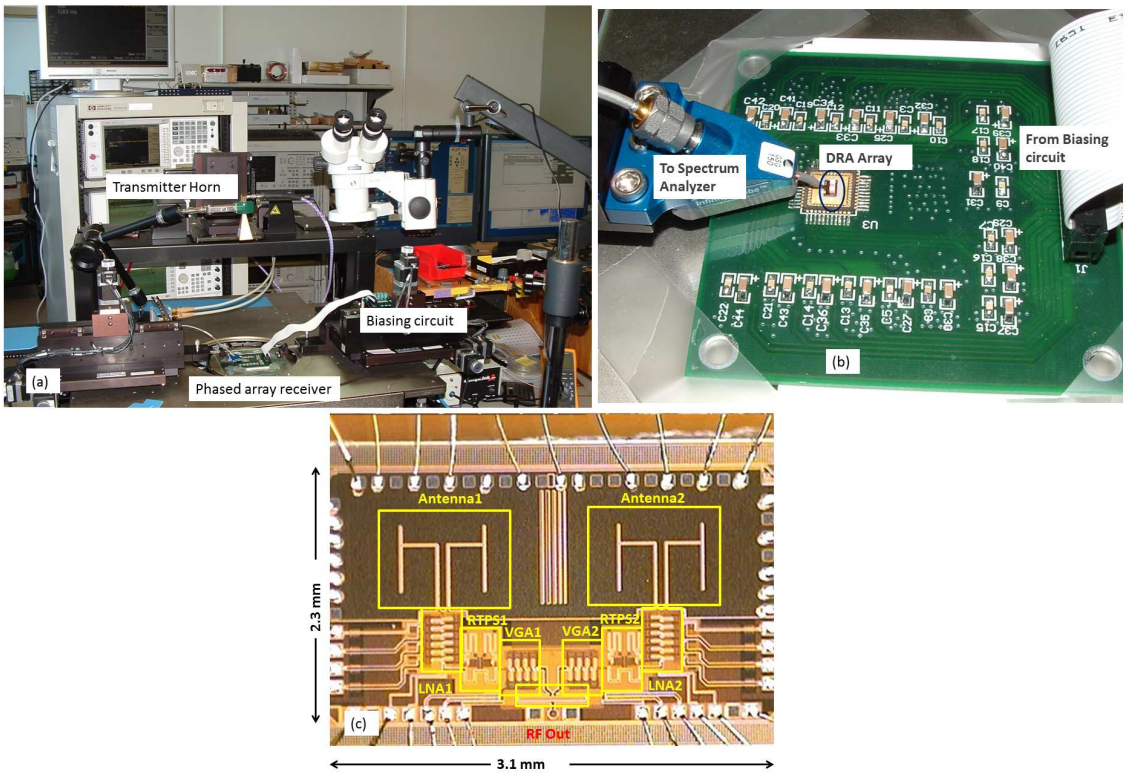

Figure 6.26: (a) Measurement setup of the phased-array receiver on the probe station. (b) The receiver phased-array with DRA array (c) Die micrograph of the two-by-one phased-array receiver.

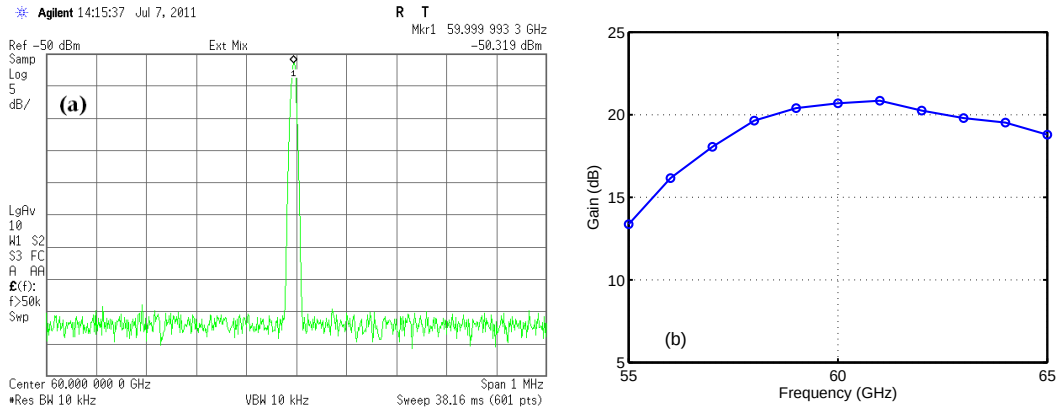

Figure 6.27: (a) The spectrum of the received signal at 60 GHz. The level of received signal is about -50 dBm. (b) The gain of the array versus frequency.

6.5 Chapter summary and conclusions

In this chapter the design of two phased-arrays integrated on CMOS technology was explained. In the first system, the design and development of the key blocks of

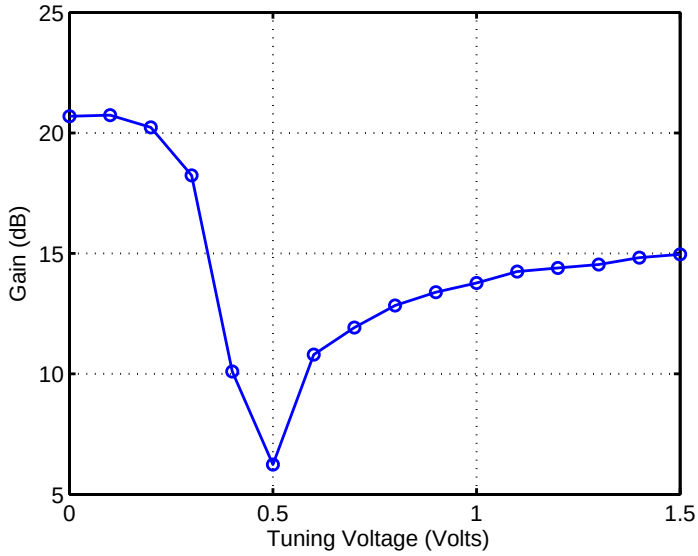

Figure 6.28: Measured received power versus V_{C2}; V_{C1} is set to 0 V while V_{C2} varies from 0 to 1.5 V)

Table 6.3: The performance summary of the phased-array

Parameter	Phased-Array 1	Phased-Array 2	Unit
RF band	57-64	57-64	GHz
Front-end bandwidth	4.5	9	GHz
LNA peak gain	19	18	dB
NF (simulated)	<7	<7	dB
Max front-end gain	7	20	dB
Number of antennas per chip	2 (scalable)	2 (scalable)	-
Front-end power consumption	21	48	mA/path
Phase shifter control voltage	0 to 1.5	0 to 1.5	V
Phase shifter range	240	240	°
Supply voltage	1.5	1.5	V
Chip area	1.12	2.22(including antenna)	mm^2
Technology	CMOS 0.13 μm	CMOS 0.13 μm	

a phased-array front-end was explained. A three stage high gain 60 GHz cascode amplifier was developed. The passive millimeter-wave reflective-type phase shifter was also presented. Two element front-ends were implemented in 0.13 μm CMOS technology. The measurement results of the overall performance of the phased-array were presented. The on-wafer measurements show that this phased-array with

RF-phase shifting architecture has more than 7 dB conversion gain at 60 GHz. In the second system, the phased-array which integrates on-chip DRA slot along with the LNAs, phase shifters, VGAs and power combiner is introduced. This array system shows more than 20 dB gain at 60 GHz. These prototypes show the feasibility of the integration of the phased-arrays on silicon. Table 6.3 lists the performance summary of the two phased-arrays.

Chapter 7

Conclusion, Future Works and Directions

7.1 Conclusion and contributions

In this thesis, we have studied and investigated the integrated mm-wave phased-array architecture and its enabling technologies. Low-cost integration technology is the key to widespread usage of mm-wave in numerous innovative applications, which are currently being conceptualized. This report began with a brief study on the mm-wave band and the emerging applications for this band. Then, the propagation of the mm-wave signal in an indoor radio-wave propagation environment was analyzed using accurate ray-tracing for LOS and NLOS scenarios, and it was shown that the shadowing loss of a human body can be as high as 40 dB. In view of the severe LOS/NLOS path loss and the fundamental limitations of the current CMOS technology, such as low amplifier gain and output power, which results in a low EIRP per antenna, the adaptive (intelligent) integrated phased-array antenna/radio system (at both ends) is the most viable approach to provide the required SNR for a reliable mobile mm-wave network operation with useful coverage. Then, a low-cost/complexity integrated mm-wave phased-array configuration was proposed along with a number of new ideas for key component technology. A fast beamforming algorithm developed in the Center for Intelligent Antenna and Radio Systems (CIARS) at the University of Waterloo was employed to realize the potential of the phased-arrays for both LOS and multi-path signal propagation. The beamforming algorithm shows that the imbalanced insertion loss of phase shifters results in a margin between the ideal and practical beamforming gain. Moreover, the beamforming gain depends on the input SNR, and reduces for a lower input SNR. In the case of shadowing, the proposed beam-forming algorithm seeks for the strongest ray, hence an excess gain up to 14 dB can be obtained. The key circuit blocks of the mm-wave radio front-end such as the antenna, while the phase shifters were discussed in separate chapters. Based on the system analysis in Chapter 2, three kinds of antennas were designed and implemented.

The patch antenna on low-loss substrate, the slot antenna with IPD technology and the slot on-chip DRA antenna were introduced. In Chapter 5, different passive reflective-type phase shifters in CMOS and MEMS technology was designed and verified.

In Chapter 6, the design of the two phased-arrays integrated on CMOS technology was explained. In the first system, the design and development of the key blocks of a phased-array front-end was explained. The second design, integrates the on-chip H-slot antenna with the phased-array antenna. The two element phased-array front-ends were implemented in 0.13 μm CMOS technology.

In Summary the major contributions of the author can be listed as follow:

- The design of passive reflective-type phase shifters in CMOS technology.
- The channel study and systematic analysis of the wave propagation in the mm-wave band.
- The implementation of efficient high gain antennas in a new passive silicon technology at 60 GHz.
- The design of efficient on-chip antennas.
- The extensive measurement and characterization of on-chip antennas and millimeter-wave circuit blocks.
- The implementation of a high gain CMOS amplifier at 60 GHz.
- The implementation and demonstration of a two element 60 GHz phased-array front-end in low-cost CMOS technology.
- The implementation and demonstration of a two element 60 GHz phased-array front-end integrated with on-chip antenna in CMOS technology.

7.2 Future research directions

The integrated mm-wave transceiver is an important part in the future of wireless communications and radar and sensing systems. The multi-antenna systems are able to overcome the high free space propagation and intrinsic material's loss as well as technology limits. With the advancement of integrated silicon technology toward the THz band, mm-wave transceivers will be a hot research area for the next coming years. Based on the outcomes of this research the direction of future research in this area can be:

- **Developing novel on-chip antennas, with integration with the front-end at the mm-wave/sub mm-wave band.**

According to the unwanted parasitic effects of the interconnection between the antenna and front-end in package at mm-wave specifically above 100 GHz, the design of on-chip antenna with high-performance and high-efficiency is desirable. An efficient on-chip antenna improves the noise figure and system performance significantly and is desirable for different sensing and imaging applications. According to the outcomes of this research the methods developed for the having efficient on-chip antennas can be scaled for higher frequencies.

- **The polymer-based dielectric resonators for post processing on-chip antennas.**

  The post processing of the polymer-based shapes over the radiators such as metallic and slot antennas, low-profile and planar antennas with improved radiation performance can be attained. Recently, the polymers have been widely used at higher frequencies for antenna applications due to their low-cost and soft nature which facilitates accurate machining. By adding additives materials, the permittivities of the polymers such as Liquid Crystal Polymer (LCP), Polydimethylsiloxane (PDMS), and Polyoxymethylene (POM) can increase up to 10 and even more which are ideal for antenna on-chip applications.

- **Novel active and passive circuits and systems for wireless communications and imaging applications above 100 GHz.**

  mm-Wave imaging can be used for remote sensing, security surveillance, and nondestructive inspection for medical and environment field. Employing the benefits of silicon technology scaling, the integration of high-performance mm-wave systems in a single-die is possible. Moreover, high packing density technologies for CMOS realizes the possibility of building low-cost multi-pixel focal plane array for mm-wave imaging. Another interesting research topic would be the development of novel wafer-level sub-mm-wave integration of passive imagers with zoom-in capability.

- **Developing characterization techniques for on-chip device and antenna characterizations at sub-mm-wave.**

  As we know, the characterization of devices and antennas at the very high frequency bands is critical due to unwanted effects of the excitation probes. The fundamental research on the characterization and de-embedding the probe effects on mm-wave and sub-mm-wave radiators can be another direction of future research. CIARS at UW with the unique measurement capabilities up to 500 GHz is one of the best places for pursuing this topic.

- **The development of ultra-high-data rate mm-wave/sub-mm-wave wireless communication for chip-to-chip wireless interconnections**

  The circuits and systems developed here can be scaled and used in the other CMOS or BiCMOS technologies where the cut-off frequency of transistor can

go beuond 200 GHz. Therefore, development of high performance transceivers at mm-wave/sub-mm-wave band is feasible.

- **Novel mm-wave/sub-mm-wave waveguide and packaging techniques.**

  Using the developed fabrication process on the high resistivity Silicon-On-Insulator (SOI) substrate in our group for antenna and waveguide applications at mm-wave, we can develope novel waveguides and interconnections for the packaging of mm-wave/sub-mm-wave chips and systems.

APPENDICES

Appendix A

Noise in Phased-Arrays

A.1 Introduction

In addition to beam steering, phased-arrays are capable of improving receiver sensitivity. In a typical phased-array, consisting of N antennas, the received signals will have a power gain N^2 in the direction of peak gain. The N noise signals, received from the antennas will be added incoherently and the resulted noise power gain would be N. This uncorrelated noise combination leads to SNR improvement in the system by the factor N. This SNR improvement is valid as long as there are no correlated noise sources in the system. Typically, in cold environments such as space where the noise temperature is about $70°K$ [71] the received noise is negligible as compared with the antenna noise temperature and the noise added by the lossy feeds or the amplifiers. In the hot environments, such as small offices where the noises from the florescent lamps [17] provides much higher background noise.

The effect of the correlated noises can also influence the output received noise. Assume a noise signal from a point noise source is received by two antenna elements as shown in Fig. A.1. When the time delay between the signals is being compensated after phase shifting and combining, the noises are added coherently and result in much higher received noise power. Correlation radiometers exploit input noise correlation to detect the temperature of the objects [168].

In case of extended noise sources such as sky or wall, the received noise would be uncorrelated and hence the noise behavior can be modeled by the brightness temperature parameter. T_b, the brightness temperature can be found from [71] :

$$T_b = \frac{\int_{\phi=0}^{2\pi} \int_{\theta=0}^{\pi} T_B(\theta,\phi) D(\theta,\phi) \sin\theta \, d\theta \, d\phi}{\int_{\phi=0}^{2\pi} \int_{\theta=0}^{\pi} D(\theta,\phi) \sin\theta \, d\theta \, d\phi} \tag{A.1}$$

where $T_B(\theta,\phi)$ is the distribution of the background temperature, and $D(\theta,\phi)$ is

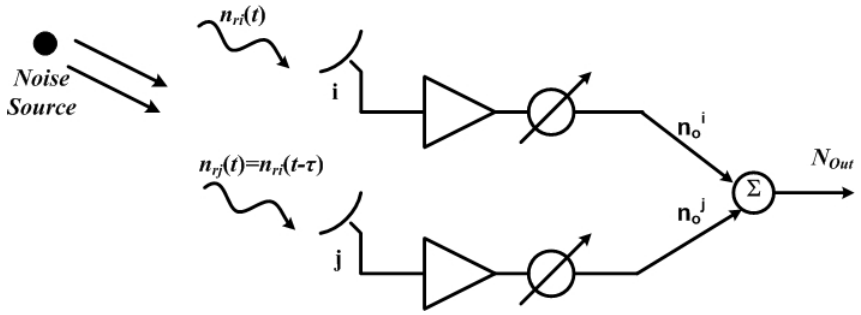

Figure A.1: Correlation of received noises at different antennas from a point source

the directivity of the antenna.

A.2 Calculation of received noise in phased-arrays

Let us consider the general phased-array system architecture with RF phase-shifting shown in Fig. A.2. There are three main sources of noise in each branch; the received noise at the antenna from the background, the thermal noise generated by the antenna losses and the noise generated by the LNA. The aforementioned noises contribute to the total output noise after the combiner. In following, some parameters are introduced to formulate the system noise analysis rigorously. $\mathbf{S}_{ANT}$ is the $N \times N$ scattering matrix of the array of N antennas. The 2×2 scattering matrix of each amplifier in ith branch is denoted by $\mathbf{S}^i_{AMP}$. The phase shifters are modeled by $N \times N$ matrix as following:

$$\mathbf{\Theta} = \begin{pmatrix} |s^1_{21,ps}(\phi_1)|e^{j\phi_1} & & 0 \\ & \ddots & \\ 0 & & |s^N_{21,ps}(\phi_N)|e^{j\phi_N} \end{pmatrix} \tag{A.2}$$

$\mathbf{N}_{ANT}$, $\mathbf{C}_A$ and $\mathbf{C}_B$ are the noise vectors wave generated by the antennas, amplifiers toward the antenna and amplifiers toward the receiver, respectively.

$$\mathbf{N}_{ANT} = \begin{pmatrix} n^1_{ant} \\ \vdots \\ n^N_{ant} \end{pmatrix}, \mathbf{C}_A = \begin{pmatrix} c^1_a \\ \vdots \\ c^N_a \end{pmatrix}, \mathbf{C}_B = \begin{pmatrix} c^1_b \\ \vdots \\ c^N_b \end{pmatrix} \tag{A.3}$$

The noise elements of an amplifier can be found from its s-parameters, Γ_{opt} and R_n

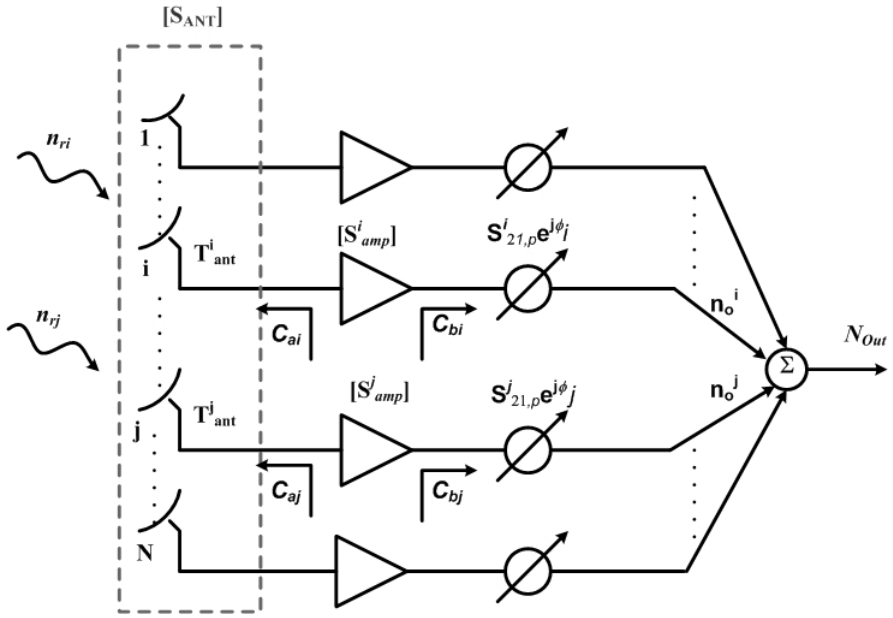

Figure A.2: Block diagram of a phased-array system and the noise waves

as following [169]:

$$\begin{aligned}
\overline{|c_1|^2} &= KT_{min}\big(|s_{11}|^2-1\big)+\frac{kt|1-s_{11}\Gamma_{opt}|^2}{|1+\Gamma_{opt}|^2} \\
\overline{|c_2|^2} &= |s_{11}|^2\big(KT_{min}+\frac{kt|\Gamma_{opt}|^2}{|1+\Gamma_{opt}|^2}\big) \\
\overline{c_1c_2^*} &= \frac{-s_{21}^*\Gamma_{opt}kt}{|1+\Gamma_{opt}|^2}+s_{11}s_{21}^*\big(\frac{kt|\Gamma_{opt}|^2}{|1+\Gamma_{opt}|^2}+kT_{min}\big)
\end{aligned} \tag{A.4}$$

where

$$kt=\frac{4kT_0R_n}{Z_0}$$

A.2.1 Received noise calculation for the lossless antenna

If we assume the antenna cascaded by an amplifier as shown in Fig. A.3, for the incident and reflected waves a and b, from the noise wave models in circuit analysis [170], we have:

$$\mathbf{B}=\mathbf{S}_{ANT}\mathbf{A}+\mathbf{N}_{ANT} \tag{A.5}$$

where

$$\mathbf{B}=\begin{pmatrix}b_1\\ \vdots\\ b_N\end{pmatrix},\mathbf{A}=\begin{pmatrix}a_1\\ \vdots\\ a_N\end{pmatrix}$$

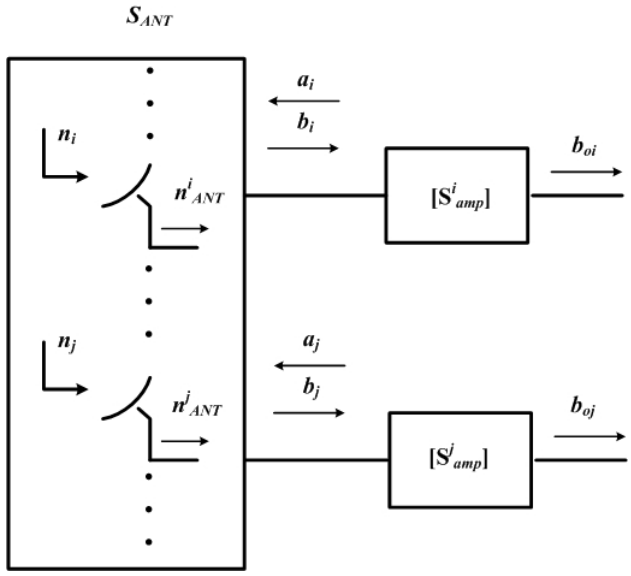

Figure A.3: Array of antennas cascaded by the amplifiers and the noise waves of the antennas

The input reflection coefficient at the amplifier if the amplifier output is loaded by a load with Γ_l is:

$$\Gamma_{in} = s_{11} + \frac{s_{12}s_{21}\Gamma_l}{1 - s_{22}\Gamma_l}$$

Here, we assume $s^i_{12,amp} \approx 0$ for each amplifier which means $\Gamma_{in} = s_{11}$ or $a_i = b_i s^i_{11,amp}$. Therefore, if we define matrix $\mathbf{\Gamma}$ as:

$$\mathbf{\Gamma} = \begin{pmatrix} s^1_{11,amp} & & 0 \\ & \ddots & \\ 0 & & s^N_{11,amp} \end{pmatrix}$$

$\mathbf{A}$ and $\mathbf{B}$ can be related by $\mathbf{\Gamma}$ as follow:

$$\mathbf{A} = \mathbf{\Gamma B} \tag{A.6}$$

Replacing A.6 into A.5, we have:

$$\mathbf{B} = \left(\mathbf{I} - \mathbf{S}_{ANT}\mathbf{\Gamma}\right)^{-1}\mathbf{N} = \mathbf{\Lambda N} \tag{A.7}$$

The available noise power from the antenna at the antenna ports can be found from A.7. For analyzing the contribution of the amplifier noise in the output noise, the wave and noise vectors at the amplifiers and the antenna ports are included simultaneously as it is shown in Fig. A.4. This configuration consists of $2N$ internal and N external ports. The internal ports consist of antenna ports as well as the

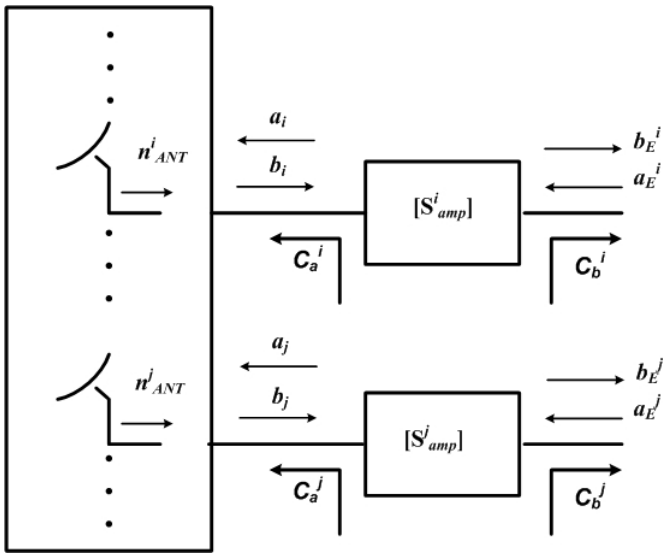

Figure A.4: Array of antennas cascaded by the amplifiers and the noise waves of both antennas and amplifiers

input ports of the amplifiers. It is clear that the output ports of the amplifiers are considered as the external ports. The internal and external wave and noise wave vectors can be related by the following matrix equation.

$$\begin{pmatrix} \mathbf{b}_E \\ \mathbf{b}_I \end{pmatrix} = \begin{pmatrix} \mathbf{S}_{EE} & \mathbf{S}_{EI} \\ \mathbf{S}_{IE} & \mathbf{S}_{II} \end{pmatrix} \begin{pmatrix} \mathbf{a}_E \\ \mathbf{a}_I \end{pmatrix} + \begin{pmatrix} \mathbf{n}_E \\ \mathbf{n}_I \end{pmatrix} \tag{A.8}$$

$\mathbf{S}_{EE}$, $\mathbf{S}_{EI}$, $\mathbf{S}_{IE}$ and $\mathbf{S}_{II}$ can be defined as follow:

$$\mathbf{S}_{EE} = \mathbf{S}_{22,amp} \tag{A.9}$$

$$\mathbf{S}_{EI} = \begin{pmatrix} [0]_{N\times N} & \mathbf{S}_{21,amp} \end{pmatrix} \tag{A.10}$$

$$\mathbf{S}_{IE} = \begin{pmatrix} [0]_{N\times N} \\ \mathbf{S}_{12,amp} \end{pmatrix} \tag{A.11}$$

$$\mathbf{S}_{II} = \begin{pmatrix} \mathbf{S}_{ANT} & [0]_{N\times N} \\ [0]_{N\times N} & \mathbf{S}_{11,amp} \end{pmatrix} \tag{A.12}$$

where $\mathbf{S}_{i,j,amp}$ are diagonal matrices defined as follow :

$$\mathbf{S}_{i,j,amp} = \begin{pmatrix} s^1_{i,j,amp} & & 0 \\ & \ddots & \\ 0 & & s^N_{i,j,amp} \end{pmatrix}$$

The wave vectors $\mathbf{b}_I$ and $\mathbf{a}_I$ are related to each other through a $2N \times 2N$ matrix $\mathbf{\Gamma}'$. If we assign indices 1 to N to the internal ports connected to the antenna ports

and indices $N+1$ to $2N$ to the internal ports connected to the amplifiers, we can see that $b_I^i = a_I^{i+N}$ and $b_I^{i+N} = a_I^i$. Therefore, $\mathbf{\Gamma}'$ can be written as follow:

$$\mathbf{\Gamma}' = \begin{pmatrix} [0]_{N\times N} & [\mathbf{I}]_{N\times N} \\ [\mathbf{I}]_{N\times N} & [0]_{N\times N} \end{pmatrix} \tag{A.13}$$

From (A.8) and (A.13) $\mathbf{a}_I$ in terms of $\mathbf{a}_E$, $\mathbf{n}_E$ and $\mathbf{n}_I$ can be obtained as follow:

$$\begin{aligned} \mathbf{b}_I &= \mathbf{S}_{IE}\mathbf{a}_E + \mathbf{S}_{II}\mathbf{a}_I + \mathbf{c}_I \\ \mathbf{\Gamma}'\mathbf{a}_I &= \mathbf{S}_{IE}\mathbf{a}_E + \mathbf{S}_{II}\mathbf{a}_I + \mathbf{c}_I \\ \mathbf{a}_I &= \big(\mathbf{\Gamma}' - \mathbf{S}_{II}\big)^{-1}\mathbf{S}_{IE}\mathbf{a}_E + \big(\mathbf{\Gamma}' - \mathbf{S}_{II}\big)^{-1}\mathbf{c}_I \end{aligned} \tag{A.14}$$

Then we can replace $\mathbf{a}_E$ from (A.14) in (A.8) and calculate $\mathbf{b}_E$.

$$\mathbf{b}_E = \Big(\mathbf{S}_{EE} + \mathbf{S}_{EI}\big(\mathbf{\Gamma}' - \mathbf{S}_{II}\big)^{-1}\mathbf{S}_{IE}\Big)\mathbf{a}_E + \mathbf{S}_{EI}\big(\mathbf{\Gamma}' - \mathbf{S}_{II}\big)^{-1}\mathbf{c}_I + \mathbf{c}_E \tag{A.15}$$

Equation (A.15) shows the output noise due to both amplifiers and antennas, which can be written as:

$$\mathbf{N}_{out,A} = \mathbf{S}_{EI}\big(\mathbf{\Gamma}' - \mathbf{S}_{II}\big)^{-1}\mathbf{c}_I + \mathbf{c}_E \tag{A.16}$$

$\mathbf{c}_I$ and $\mathbf{c}_E$ in (A.16) are:

$$\begin{aligned} \mathbf{c}_I &= \big(\mathbf{N}_{ANT}^T | \mathbf{C}_A^T\big)^T \\ \mathbf{c}_E &= \mathbf{C}_B \end{aligned} \tag{A.17}$$

where $\mathbf{N}_{ANT}$, $\mathbf{C}_A$ and $\mathbf{C}_B$ were introduced before as antennas and amplifiers noise waves in (A.3). In (A.16), we need to calculate $\big(\mathbf{\Gamma}' - \mathbf{S}_{II}\big)^{-1}$. The inverse of the aforementioned matrix is [171]:

$$\big(\mathbf{\Gamma}' - \mathbf{S}_{II}\big)^{-1} = \begin{pmatrix} \mathbf{S}_{11,amp}^1\mathbf{\Lambda} & \mathbf{\Lambda} \\ \mathbf{\Lambda} & \mathbf{S}_{ANT}\mathbf{\Lambda} \end{pmatrix} \tag{A.18}$$

Where $\mathbf{\Lambda}$ is defined in (A.7). Replacing A.18 into A.17 and A.16, the total noise vector can be written as:

$$\mathbf{N}_{out,A} = \mathbf{S}_{21,amp}\mathbf{\Lambda}\mathbf{N}_{ANT} + \mathbf{S}_{21,amp}\mathbf{S}_{ANT}\mathbf{\Lambda}\mathbf{C}_A + \mathbf{C}_B \tag{A.19}$$

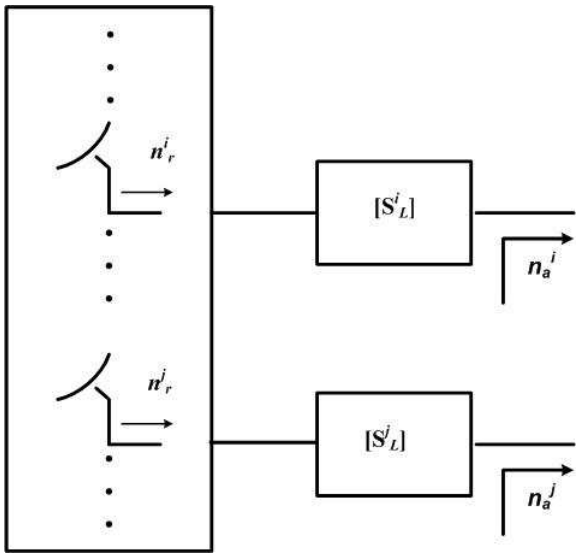

Figure A.5: Array of antennas cascaded by the two-port lossy networks to model the efficiency of the antennas

A.2.2 Received noise calculation for a lossy antenna

As mentioned earlier, the antenna noise consists of the received background noise and the antenna thermal noise for a lossy antenna. For the noise calculation in the lossy antenna case, the method used in [168] is applied here to calculate the lossy antenna noise waves. In this method, the loss of the antenna and the feed network are assumed as those in a 2-port network shown in Fig. A.5. The noise wave vectors from the background and the loss network shown in Fig. A.5 will satisfy following equations [170]:

$$\begin{aligned} \overline{|n_a^i|^2} &= = KT_{ant}^i = K(1-\eta_i)T_0 \\ \overline{|n_r^i|^2} &= KT_b \end{aligned} \tag{A.20}$$

T_{ant} is the antenna temperature noise and T_b, the background temperature, can be found from [71] :

$$T_b = \frac{\int_{\phi=0}^{2\pi}\int_{\theta=0}^{\pi} T_B(\theta,\phi)D(\theta,\phi)\sin\theta\, d\theta\, d\phi}{\int_{\phi=0}^{2\pi}\int_{\theta=0}^{\pi} D(\theta,\phi)\sin\theta\, d\theta\, d\phi} \tag{A.21}$$

where $T_B(\theta,\phi)$ is the distribution of the background temperature, and $D(\theta,\phi)$ is the

directivity of the antenna. The noise vectors $\mathbf{N}_r$ and $\mathbf{N}_A$ are defined as following:

$$\mathbf{N}_r = \begin{pmatrix} n_r^1 \\ \vdots \\ n_r^N \end{pmatrix}, \mathbf{N}_A = \begin{pmatrix} n_a^1 \\ \vdots \\ n_a^N \end{pmatrix} \tag{A.22}$$

The scattering matrix of the equivalent lossy network shown in Fig. A.5 can be written as follow:

$$S_L^i = \begin{pmatrix} S_{11,amp}^i & \sqrt{\eta_i} \\ \sqrt{\eta_i} & S_{11,ANT}^i \end{pmatrix} \tag{A.23}$$

Equation (A.19) can be used here to calculate the output noise power. The only change is that the amplifier should be replaced by the equivalent lossy network. The antenna noise vector, $\mathbf{N}_{ANT}$, then becomes:

$$\mathbf{N}_{ANT} = \mathbf{E}^{\frac{1}{2}} \mathbf{\Lambda} \mathbf{N}_R + \mathbf{N}_A \tag{A.24}$$

where $\mathbf{E}$, which can be called the "efficiency matrix" of the antenna, is:

$$\mathbf{E} = \begin{pmatrix} \eta_1 & & 0 \\ & \ddots & \\ 0 & & \eta_N \end{pmatrix}$$

The output noise vector waves before the phase shifters can be found by substituting noise calculated from (A.24) in the expression for $\mathbf{N}_{ANT}$ in (A.19). In order to calculate the output noise waves before the combiner, the resulted noise vector waves should be multiplied by phase shifting matrix introduced in (A.2). The output noise correlation matrix would be:

$$\mathbf{N}_{out} = \mathbf{\Theta} \mathbf{N}_{out,A} \mathbf{N}_{out,A}^{\dagger} \mathbf{\Theta}^{\dagger} \tag{A.25}$$

where † is the Hermitian conjugate of the matrix. The resulted output noise is the spectral density of the received noise at a certain frequency. In order to determine the output power noise, these spectral density functions in (A.25) should be integrated over the frequency [17].

A.3 An example of a practical system

In order to examine the effect of beamforming on the received noise power, a 60 GHz phased-array system as an important example in this section is considered. This system works in an office environment where the background temperature changes from $270°K$ to $420°K$ linearly [17]. The system is a 2-element phased-array. Each branch consists of an amplifier with a typical gain of 20 dB and an impedance matching better than 15 dB. The antenna is an array of two patches with half

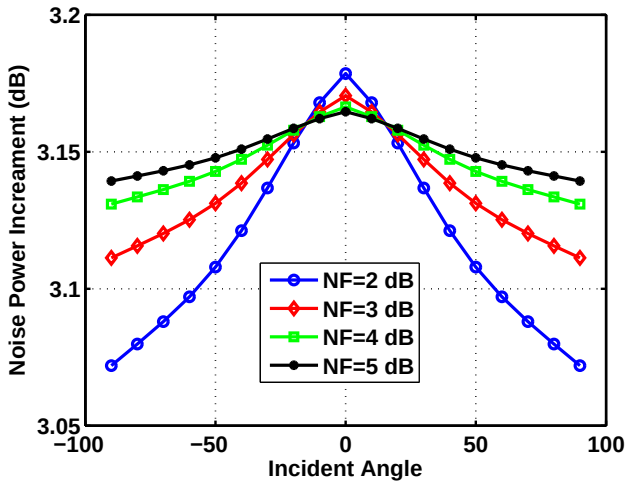

Figure A.6: Increment in received noise power for a 2-element phased-array

wavelength spacing. The simulation of the array shows 15 dB return loss at each port and more than 20 dB isolation between the adjacent antennas. The efficiency of the antennas are 80%. The system is simulated for various NFs of the LNAs and the increased received noise with respect to a single antenna element is calculated and plotted for different incident angles.

Fig. A.6 shows the simulation results of the system. As it can be seen in the graph, for the incident angle 0° where the background noise is maximum the level of the received noise is maximum. By increasing the incident angle, since the background noise temperature decreases the dominant portion of the output noise is the noise from the LNA. By increasing the noise figure of the LNA, it can be seen that the beam forming has a minor effect on the received signal since the noise of LNA is much higher than the received signal by the antennas. This analysis shows that the noise figure of the LNAs has a critical role in the received noise of system. For the systems with high noise figure, the background noise temperature has a minor effect on the output noise power.

Appendix B

Beamforming Algorithms for mm-Wave Receiver Phased-Array

B.1 Signal Model

This part is derived from [49]. Let $\mathbf{X}(t) = [x_1(t)\ x_2(t) \cdots x_N(t)]$ denote the received signals by all elements. Then it consists of three parts: source signal $\mathbf{x}_S(t)$, interference $\mathbf{x}_I(t)$, and background noise $\mathbf{n}(t)$,

$$\mathbf{x}(t) = \mathbf{x}_S(t) + \mathbf{x}_I(t) + \mathbf{n}(t)\ . \tag{B.1}$$

The background noise is assumed to be spatially white. Assume the source (transmitter) is located at direction $\overrightarrow{\mathbf{r}} = (\theta_T, \phi_T)$ in the receiver array coordinate system transmitting RF signals at frequency f_0. The RF signal received by an element of the array located at (x_n, y_n, z_n) is given by

$$x_s^n(t) = s_0(t)G_e(\overrightarrow{\mathbf{r}}) \times \exp\left[jk_0(x_n \sin\theta_T \cos\phi_T + y_n \sin\theta_T \sin\phi_T + z_n \cos\theta_T)\right] \tag{B.2}$$

where k_0, and $s_0(t)$ are respectively the RF wave number and the source waveform. The path loss is included in $s_0(t)$. The array output for a single receiver array (Fig. 3.3(a)) is

$$y(t) = \mathbf{w}^H \mathbf{X}(t) \tag{B.3}$$

where $\mathbf{w}$ is the array weights vector and ^{H} denotes the Hermitian operator. If analog phase shifters, such as the one shown in Fig. **??**, were used to adjust the array weights for beamforming the wight vector would be

$$\mathbf{w}(v_1, v_2, \cdots v_N) = [f(v_1)e^{j\psi(v_1)}\ f(v_2)e^{j\psi(v_2)} \cdots f(v_N)e^{j\psi(v_N)}] \tag{B.4}$$

where v_i is the control voltage of the i^{th} phase shifter, and f and ψ denote the amplitude (insertion loss) and phase-shift functions of the phase shifter shown in

Fig. **??**(b) and (c). The total received power by the array is then

$$P(t) = y^H y \tag{B.5}$$

B.2 Statement of the problem

In the absence of co-channel interference, beamforming for a mm-wave receiver array is a constrained optimization problem with the objective of maximizing the total received power by the array. The voltage dependent characteristics of the phase shifters form the constrains of the problem. Hence, the beamforming problem can be stated as:

$$\begin{aligned} &maximize \quad P(w_1, w_2, \cdots, w_N) \\ &subject\ to: w_i = f(v_i)\exp(j\psi(v_i)) \qquad for\ each\ phase\ shifter \\ &\qquad v_{min} \leq v_i \leq v_{max} \qquad for\ each\ phase\ shifter \end{aligned} \tag{B.6}$$

An efficient method to solve this problem is to use gradient estimation methods such as zero-knowledge beamforming algorithm [172]- [173]. In this case the control voltages are updated in an iterative manner

$$\mathbf{v}(n+1) = \mathbf{v}(n) + 2\mu\nabla_{\mathbf{v}}P(n) \tag{B.7}$$

where μ is an internal algorithm parameter called the *step size*, and $\nabla_{\mathbf{v}}P(n)$ is the gradient of power with respect to $\mathbf{v}$. Since the exact calculation of the gradient is not practical it is replaced by an estimated vector:

$$\nabla_{\mathbf{v}}P(n) \ \simeq \ [\hat{g_1}(n)\ \hat{g_2}(n)\ \cdots\ \hat{g_N}(n)] \tag{B.8}$$

where each component $\hat{g_k}(n)$ is the approximate partial derivative of $P(n)$ w.r.t. $v_k(n)$.

B.3 Reverse-channel aided Beamforming

The size and cost constrains of the receiver do not allow for incorporating a complex processor in the portable node, however the access point (fixed node) can handle more elaborate signal processing tasks. Moreover, in mm-wave networking standards such as WPAN 50MHz of the spectrum is reserved for the reverse channel to carry the control signals between the access points and mobile nodes. Access point can be equipped with direction-of arrival (DOA) estimation unit, which can calculate the relative position of the mobile nodes and send this information to them. The mobile node can use this information to adjust its beam. Although this

method is very fast but in the case of shadowing it is not efficient. In this case the beamformer, using Least Mean Square (LMS) algorithm [174]- [175] can maintain the array beam on the direction of the strongest component of the multipath signal.

Bibliography

[1] K. Ohata, et al., "Sixty-GHz-band ultra-miniature monolithic T/R modules for multimedia wireless communication systems," *IEEE Trans. Microwave Theory Tech.*, vol. 44, no. 12, pp. 2354–2360, Dec 1996.

[2] S. Reynolds, et al., "A silicon 60GHz receiver and transmitter chipset for broadband communications," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2820–2830, Dec 2006.

[3] Sten E. Gunnarsson, et. al, "60 GHz single-chip front-end MMICs and systems for multi-Gb/s wireless communication," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1143–1157, May 2007.

[4] T. Mitomo, et. al, "A 60-GHz CMOS receiver front-end with frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 1030–1037, April 2008.

[5] C.H. Doan, S. Emami, A.M. Niknejad, and R.W. Brodersen, "Millimeter-wave CMOS design," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144–155, Jan. 2005.

[6] A. Babakhani, et al., "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Receiver and antennas," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2795–2806, Dec. 2006.

[7] B. Razavi, "Gadgets gab at 60 GHz," *IEEE Spectrum*, vol. 45, no. 2, pp. 46–58, Feb. 2008.

[8] A. Kamerman and L. Monteban, "WaveLAN-II: A high-performance wireless LAN for the unlicensed band," *Bell Labs Technical Journal*, pp. 118–133, summer 1997.

[9] Y. Takimoto, "Recent Activities on Millimeter-Wave Indoor LAN System Development in Japan," *in Proceedings of IEEE Microwave System Conference*, pp. 7–10, 1995.

[10] P. Smulders, "Exploiting the 60 GHz band for local wireless multimedia access: prospects and future directions," *Communications Magazine, IEEE*, vol. 40, no. 1, pp. 140–147, Jan 2002.

[11] C. Park and T. Rappaport, "Short-range wireless communications for next-generation networks: UWB, 60 GHz millimeter-wave WPAN, and ZigBee," *IEEE Wireless Commun.*, vol. 14, no. 4, pp. 70–78, Aug. 2007.

[12] A. Natarajan, A. Komijani, X. Guan, A. Babakhani, and A. Hajimiri, "A 77-GHz Phased-Array Transceiver With On-Chip Antennas in Silicon:Transmitter and Local LO-Path Phase Shifting," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2807–2819, Dec. 2006.

[13] J. Y. Park, S. S. Jeon, Y. Wang, and T. Itoh, "A 60-GHz Planar Integrated Phased Array," *European Microwave Conference, 2003. 33rd*, pp. 837–840, 2003.

[14] S. Xiao M. Zhou, Y.Zhang, *Millimeter Wave Technology in Wireless PAN, LAN, and MAN*. CRC Press, 2008.

[15] F. C. C. (FCC), *Millimeter-Wave Propagation: Spectrum Management Implications*. FCC document, 1997.

[16] C. Shannon, "A mathematical theory of communications," *Bell Systems Technical Journal*, vol. 27, p. 79423 and 623656, Jul. 1948.

[17] Arun Natarajan, *Millimeter-Wave Phased Arrays in Silicon*. PhD thesis, California Institute of Technology, 2007.

[18] *Wireless Gigabit Alliance*, uRL:http://wigig.org/specifications.

[19] *Wireless HD*, uRL:http://http://www.wirelesshd.org.

[20] " IEEE 802.15 WPAN Task Group 3c (TG3c) ," Sept. 2009. [Online]. Available: http://www.ieee802.org/15/pub/TG3c.html

[21] T. Baykas, C.-S. Sum, Z. Lan, J. Wang, M. Rahman, H. Harada, and S. Kato, "Ieee 802.15.3c: the first ieee wireless standard for data rates over 1 gb/s," *Communications Magazine, IEEE*, vol. 49, no. 7, pp. 114 –121, july 2011.

[22] ECMA, "Standard ECMA-387: High Rate 60 GHz PHY, MAC and HDMI PAL ," Dec. 2008, 1st Edition. [Online]. Available: http://www.ecma-international.org/publications/files/ECMA-ST/Ecma-387.pdf

[23] *Defining the Future of Multi-Gigabit Wireless Communications*. Online white paper, July 2010, uRL:http://wirelessgigabitalliance.org/?getfile=1510.

[24] H. Singh, J. Hsu, L. Verma, S. Lee, and C. Ngo, "Green operation of multi-band wireless LAN in 60 GHz and 2.4/5 GHz," in *Consumer Communications and Networking Conference (CCNC), 2011 IEEE*, jan. 2011, pp. 787 –792.

[25] L. Gilreath, V. Jain, and P. Heydari, "Design and Analysis of a W-Band SiGe Direct-Detection-Based Passive Imaging Receiver," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 10, pp. 2240 –2252, oct. 2011.

[26] D. Le Vine, A. Griffis, C. Swift, and T. Jackson, "Estar: a synthetic aperture microwave radiometer for remote sensing applications," *Proceedings of the IEEE*, vol. 82, no. 12, pp. 1787 –1801, dec 1994.

[27] J. Lovberg, C. Martin, and V. Kolinko, "Video-rate passive millimeter-wave imaging using phased arrays," in *Microwave Symposium, 2007. IEEE/MTT-S International*, june 2007, pp. 1689 –1692.

[28] L. Zhou, C.-C. Wang, Z. Chen, and P. Heydari, "A W-band CMOS Receiver Chipset for Millimeter-Wave Radiometer Systems," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 2, pp. 378 –391, feb. 2011.

[29] E. Laskin, M. Khanpour, S. Nicolson, A. Tomkins, P. Garcia, A. Cathelin, D. Belot, and S. Voinigescu, "Nanoscale CMOS Transceiver Design in the 90 170-GHz Range," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 57, no. 12, pp. 3477 –3490, dec. 2009.

[30] I. Sarkas, E. Laskin, J. Hasch, P. Chevalier, and S. Voinigescu, "Second generation transceivers for d-band radar and data communication applications," in *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International*, may 2010, pp. 1328 –1331.

[31] Tapan K. Sarkar, Robert Mailloux, Arthur A. Oliner, Magdalena Salazar-Palma, Dipak L. Sengupta , *History of Wireless.* Wiley-IEEE Press, 2006.

[32] T. Iida, *Satellite Communications: System and Its Design Technology.* IOS Press, 2000.

[33] M. I. Skolnik, *Radar Handbook.* McGraw-Hill, 2008.

[34] B. F. Burke and F. Graham-Smith, *An Introduction to Radio Astronomy*, 2002.

[35] J. G. Webster, *Wiley Encyclopedia of Electrical and Electronics Engineering.* Cambridge University Press, 1999.

[36] K. Finkenzeller and K. Finkenzeller, *RFID Handbook: Fundamentals and Applications in Contactless Smart Cards and Identification.* John Wiley and Sons, 2003.

[37] M.R. Nezhad-Ahmadi, G.H. Rafi,and S. Safavi-Naeini, "An efficient integrated antenna structure on low-resistivity silicon substrtate," pp. 4353–4356, July 2006.

[38] M.-R. Nezhad-Ahmadi, M. Fakharzadeh, B. Biglarbegian, and S. Safavi-Naeini, "High-Efficiency On-Chip Dielectric Resonator Antenna for mm-Wave Transceivers," *Antennas and Propagation, IEEE Transactions on*, vol. 58, no. 10, pp. 3388 –3392, oct. 2010.

[39] M. Fakharzadeh, M.-R. Nezhad-Ahmadi, B. Biglarbegian, J. Ahmadi-Shokouh, and S. Safavi-Naeini, "CMOS Phased Array Transceiver Technology for 60 GHz Wireless Applications," *Antennas and Propagation, IEEE Transactions on*, vol. 58, no. 4, pp. 1093 –1104, april 2010.

[40] Y. Hamada, M. Tanomura, M. Ito, and K. Maruhashi, "A high gain 77 ghz power amplifier operating at 0.7 v based on 90 nm cmos technology," *Microwave and Wireless Components Letters, IEEE*, vol. 19, no. 5, pp. 329 –331, may 2009.

[41] M. Aust, A. Sharma, O. Fordham, R. Grundbacher, R. To, R. Tsai, and R. Lai, "A 2.8-W Q-Band High-Efficiency Power Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 10, pp. 2241–2247, 2006.

[42] T. Manabe,and Y. Miura, and T. Ihara, "Effects of Antenna Directivity and Polarization on Indoor Multipath Propagation Characteristics at 60 GHz," *IEEE J. Selec. Area Commun.*, vol. 14, no. 3, pp. 1441–448, Apr. 1996.

[43] C.-P. Lim, M. Lee, R. J. Burkholder, J. L. Volakis and R. J. Marhefka, "60 GHz Indoor Propagation Studies for Wireless Communications Based on a Ray-Tracing Method," *EURASIP Jour. Wireless Commun. and Net.*, 2007, article ID 73928.

[44] P. F. M. Smulders, C. F. Li, H. Yang, E. F. T. Martijn and M. H. A. J. Herben, "60 GHz Indoor Radio Propagation Comparison of Simulation and Measurement Results," 2004.

[45] B. Langen, G. Lober and W. Herzig, "Reflection and Transmission Behaviour of Building Materials at 60 GHz," pp. 505–509, 1994.

[46] L. M. Correia and Paul O. Frances, "Estimation of Materials Characteristics from Power Measurements at 60 GHz," pp. 510–513, 1994.

[47] C. M. Alabaster, "Permittivity of Human Skin in Millimetre Wave Band," *Electron. Letters*, vol. 39, no. 21, pp. 1521–1522, Oct. 2003, article ID 73928.

[48] D. Tse, and P. Viswanath, *Fundamentals of Wireless Communication.* Cambridge University Press, 2005.

[49] Mohammad Fakharadeh, *Optical and Microwave Beamforming for Phased Array Antennas.* PhD thesis, University of Waterloo, 2008.

[50] Ali M. Niknejad, and Hossein Hashemi, *mm-Wave Silicon Technology 60 GHz and Beyond.* Springer, 2007.

[51] Robert J. Mailloux, *Phased Array Antenna Handbook- Chapter 1*, 2nd ed. Artech House, 2005.

[52] H. Hashemi, X. Guan, A. Komijani, and A. Hajimiri, "A 24-GHz SiGe Phased-Array ReceiverLO Phase-Shifting Approach," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 2, pp. 614 – 626, Feb. 2005.

[53] S. Raman, N. Barker, and G. Rebeiz, "A W-band dielectric-lens-based integrated monopulse radar receiver," *IEEE Trans. Microwave Theory Tech.*, vol. 46, no. 12, pp. 2308–2316, Dec. 1998.

[54] R. Miura, T. Tanaka, I. Chiba, A. Horie, and Y. Karasawa, "Beamforming experiment with a DBF multibeam antenna in a mobile satellite environment," *Academic Press*, vol. 45, no. 4, pp. 707–714, Apr 1997.

[55] M. Fakharzadeh, P. Mousavi, S. Safavi-Naeini, and S.H. Jamali, "The Effects of Imbalanced Phase Shifters Loss on Phased Array Gain," *IEEE Letters on Antennas and Wireless Propagation*, vol. 7, pp. 192–196, July 2008.

[56] G. E. Moore, "Cramming more components onto integrated circuits," *Proceedings of the IEEE*, vol. 86, no. 1, pp. 82–85, Jan. 1998.

[57] D. Johns, *Analog Integrated Circuit Design.* John Wiley and Sons, 1997.

[58] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for si-based rf ics," *IEEE Solid-State Circuits*, vol. 33, no. 5, pp. 743–752, May 1998.

[59] S. Alalusi and R. Brodersen, "A 60GHz Phased Array in CMOS," pp. 393–396, Sep. 2006.

[60] X. Guan, H. Hashemi, and A. Hajimiri, "A fully integrated 24-GHz eight-element phased-array receiver in silicon," *IEEE Solid State Circuits*, vol. 39, no. 12, pp. 2311–2320, Dec. 2004.

[61] A. Natarajan, A. Komijani, and A. Hajimiri, "A fully integrated 24-GHz phased-array transmitter in CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2502–2514, Dec. 2005.

[62] J. Buckwalter, A. Babakhani, A. Komijani, and A. Hajimiri, "An integrated subharmonic coupled-oscillator scheme for a 60-GHz phased-array transmitter," *IEEE Trans. Microwave Theory Tech.*, vol. 54, no. 12, part2, pp. 4271–4280, Dec. 2006.

[63] Koh Kwang-Jin, G. M. Rebeiz, "A Q -Band Four-Element Phased-Array Front-End Receiver With Integrated Wilkinson Power Combiners in $0.18\mu m$ SiGe BiCMOS Technology," *IEEE Trans. Microwave Theory Tech.*, vol. 56, no. 9, pp. 2046–2053, Sep. 2008.

[64] C.-S. Wang, J.-W. Huang, K.-D. Chu, and C.-K. Wang, *Circuits and Systems I: Regular Papers, IEEE Transactions on.*

[65] S. Kishimoto, N. Orihashi, Y. Hamada, M. Ito, and K. Maruhashi, "A 60-GHz band CMOS phased-array transmitter utilizing compact baseband phase shifters," in *Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE*, june 2009, pp. 215 –218.

[66] A. Natarajan, S. Reynolds, M.-D. Tsai, S. Nicolson, J.-H. Zhan, D. G. Kam, D. Liu, Y.-L. Huang, A. Valdes-Garcia, and B. Floyd, "A Fully-Integrated 16-Element Phased-Array Receiver in SiGe BiCMOS for 60-GHz Communications," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 5, pp. 1059 –1075, may 2011.

[67] W. Chan and J. Long, "A 60-GHz Band 2x2 Phased-Array Transmitter in 65-nm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 12, pp. 2682 –2695, dec. 2010.

[68] E. Cohen, C. Jakobson, S. Ravid, and D. Ritter, "A thirty two element phased-array transceiver at 60GHz with RF-IF conversion block in 90nm flip chip CMOS process," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2010 IEEE*, may 2010, pp. 457 –460.

[69] M. Tabesh, J. Chen, C. Marcu, L. Kong, S. Kang, A. Niknejad, and E. Alon, "A 65 nm CMOS 4-Element Sub-34 mW/Element 60 GHz Phased-Array Transceiver," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 12, pp. 3018 –3032, dec. 2011.

[70] J.J. LEE, "G/T and Noise Figure of Active Array Antennas," *Academic Press*, vol. 41, no. 2, pp. 241–244, Feb. 1993.

[71] David M. Pozar, *Microwave Engineering*, 3rd ed. John Wiley and Sons, 2005.

[72] C. Karnfelt, P. Hallbjorner, H. Zirath, and A. Alping, "High gain active microstrip antenna for 60-GHz WLAN/WPAN applications," *IEEE Trans. Microwave Theory Tech.*, vol. 54, no. 6, pp. 2593–2603, June 2006.

[73] I.-S. Chen, H.-K. Chiou, and N.-W. Chen, "V-band on-chip dipole-based antenna," *Antennas and Propagation, IEEE Transactions on*, vol. 57, no. 10, pp. 2853–2861, Oct. 2009.

[74] Y. Zhang, M. Sun, and L. Guo, "On-chip antennas for 60-GHz radios in silicon technology," *Electron Devices, IEEE Transactions on*, vol. 52, no. 7, pp. 1664 – 1668, july 2005.

[75] Y. P. Zhang, M. Sun, K. M. Chua, L. L. Wai, and D. Liu, "Antenna-in-Package Design for Wirebond Interconnection to Highly Integrated 60-GHz Radios," *Antennas and Propagation, IEEE Transactions on*, vol. 57, no. 10, pp. 2842–2852, Oct. 2009.

[76] K.-C. Huang and D. Edwards, "60 GHz Multibeam Antenna Array for Gigabit Wireless Communication Networks," *Academic Press*, vol. 54, no. 12, pp. 3912–3914, Dec. 2006.

[77] A. Rosen, R. Amantea, P. Stabile, A. Fathy, D. Gilbert, D. Bechtle, W. Janton, F. McGinty, J. Butler, and G. Evans, "Investigation of active antenna arrays at 60 GHz," *IEEE Trans. Microwave Theory Tech.*, vol. 43, no. 9, pp. 2117–2125, Sep 1995.

[78] A. Lamminen, J. Saily, and A. Vimpari, "60-GHz Patch Antennas and Arrays on LTCC With Embedded-Cavity Substrates," *Academic Press*, vol. 56, no. 9, pp. 2865–2874, Sept. 2008.

[79] B. Pan, Y. Li, G. Ponchak, J. Papapolymerou, and M. Tentzeris, "A 60-GHz CPW-Fed High-Gain and Broadband Integrated Horn Antenna," *Academic Press*, vol. 57, no. 4, pp. 1050–1056, April 2009.

[80] A. Patrovsky and K. Wu, "Active 60 GHz front-end with integrated dielectric antenna," *Electronics Lett.*, vol. 45, no. 15, pp. 765–766, 16 2009.

[81] Y. Murakami, T. Kijima, H. Iwasaki, T. Ihara, T. Manabe, and K. Iigusa, "A switchable multi-sector antenna for indoor wireless LAN systems in the 60-GHz band," *IEEE Trans. Microwave Theory Tech.*, vol. 46, no. 6, pp. 841–843, Jun 1998.

[82] P. Smulders and M. Herben, "A shaped reflector antenna for 60-GHz radio access points," *Academic Press*, vol. 49, no. 7, pp. 1013–1015, Jul 2001.

[83] P. Bijumon, Y. Antar, A. Freundorfer, and M. Sayer, "Dielectric resonator antenna on silicon substrate for system on-chip applications," *Antennas and Propagation, IEEE Transactions on*, vol. 56, no. 11, pp. 3404 –3410, nov. 2008.

[84] J.R. James, and P.S. Hall, *Handbook of Microstrip Antennas.* Institution of Electrical Engineers (IEE), 1989.

[85] J. Laskar, "60GHz CMOS low power single chip radio: The intersection of gaming and connectivity," in *Radio and Wireless Symposium, 2009. RWS '09. IEEE*, jan. 2009, pp. 654 –657.

[86] B. Biglarbegian, M. Fakharzadeh, D. Busuioc, M.-R. Nezhad-Ahmadi, and S. Safavi-Naeini, "Optimized microstrip antenna arrays for emerging millimeter-wave wireless applications," *Antennas and Propagation, IEEE Transactions on*, vol. 59, no. 5, pp. 1742 –1747, may 2011.

[87] N. Hoivik, D. Liu, C. Jahnes, J. Cotte, C. Tsang, C. Patel, U. Pfeiffer, J. Grzyb, J. Knickerbocker, J. Magerlein, and B. Gaucher, "High-efficiency 60 GHz antenna fabricated using low-cost silicon micromachining techniques," in *Antennas and Propagation Society International Symposium, 2007 IEEE*, june 2007, pp. 5043 –5046.

[88] M. Nezhad Ahamdi and S. Safavi-Naeini, "On-chip antennas for 24, 60, and 77ghz single package transceivers on low resistivity silicon substrate," in *Antennas and Propagation Society International Symposium, 2007 IEEE*, june 2007, pp. 5059 –5062.

[89] [Online]. Available: http://www.onsemi.com/

[90] B. Biglarbegian, M. Nezhad-Ahmadi, C. Hoggat, S. Hose, M. Fakharzadeh, and S. Safavi-Naeini, "A 60 GHz on-chip slot antenna in silicon integrated passive device technology," in *Antennas and Propagation Society International Symposium (APSURSI), 2010 IEEE*, july 2010, pp. 1 –4.

[91] C. Calvez, C. Person, J. Coupez, F. Gallee, H. Ezzeddine, A. Cathelin, and D. Belot, "New millimeter wave packaged antenna array on ipd technology," in *Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2010 Topical Meeting on*, jan. 2010, pp. 96 –99.

[92] Titz, D. and Pilard, R. and Ferrero, F. and Gianesello, F. and Gloria, D. and Luxey, C. and Brachat, P. and Jacquemod, G., "60GHz antenna integrated on High Resistivity silicon technologies targeting WHDMI applications," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2011 IEEE*, june 2011, pp. 1 –4.

[93] F.-J. Huang, C.-M. Lee, C.-Y. Kuo, and C.-H. Luo, "Mmw antenna in ipd process for 60-ghz wpan applications," *Antennas and Wireless Propagation Letters, IEEE*, vol. 10, pp. 565 –568, 2011.

[94] W. Heinrich, "The flip-chip approach for millimeter wave packaging," *Microwave Magazine, IEEE*, vol. 6, no. 3, pp. 36 – 45, sept. 2005.

[95] Mohammad-Reza Nezhad-Ahmadi, *Integrated Circuit and Antenna Technology for Millimeter-Wave Phased Array Radio Front-End.* PhD thesis, University of Waterloo, 2010.

[96] S.-S. Hsu, K.-C. Wei, C.-Y. Hsu, and H. Ru-Chuang, "A 60-GHz Millimeter-Wave CPW-Fed Yagi Antenna Fabricated by Using 0.18-μm CMOS Technology," *Electron Device Letters, IEEE*, vol. 29, no. 6, pp. 625 –627, june 2008.

[97] M. Kahrizi, T. Sarkar, and Z. Maricevic, "Analysis of a wide radiating slot in the ground plane of a microstrip line," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 41, no. 1, pp. 29 –37, jan 1993.

[98] K. Mohammadpour-Aghdam, S. Brebels, A. Enayati, R. Faraji-Dana, G. Vandenbosch, W. DeRaedt , "RF probe influence study in millimeter-wave antenna pattern measurements," *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 21, no. 4, pp. 413–420, july 2011.

[99] K. Hettak, L. Talbi, G. Delisle, and G. Morin, "A low profile polarization diversity 60 GHz CPW fed patch antenna for fading mitigation," in *Antennas and Propagation Society International Symposium (APSURSI), 2010 IEEE*, july 2010, pp. 1 –4.

[100] A. Buerkle, K. Sarabandi, and H. Mosallaei, "Compact slot and dielectric resonator antenna with dual-resonance, broadband characteristics," *Antennas and Propagation, IEEE Transactions on*, vol. 53, no. 3, pp. 1020 – 1027, march 2005.

[101] R. Kumar Mongia and A. Ittipiboon, "Theoretical and experimental investigations on rectangular dielectric resonator antennas," *Antennas and Propagation, IEEE Transactions on*, vol. 45, no. 9, pp. 1348 –1356, sep 1997.

[102] F. Ellinger, U. Mayer, M. Wickert, N. Joram, J. Wagner, R. Eickhoff, I. Santamaria, C. Scheytt, and R. Kraemer, "Integrated adjustable phase shifters," *Microwave Magazine, IEEE*, vol. 11, no. 6, pp. 97 –108, oct. 2010.

[103] N. Pothecary, *Feedforward linear power amplifiers*, ser. Artech House microwave library. Artech House, 1999.

[104] J. Breitbarth and J. Koebel, "Additive (Residual) Phase Noise Measurement of Amplifiers, Frequency Dividers and Frequency Multipliers ," June 2008.

[105] T. Lee, K. Donnelly, J. Ho, J. Zerbe, M. Johnson, and T. Ishikawa, "A 2.5 v cmos delay-locked loop for 18 mbit, 500 megabyte/s dram," *Solid-State Circuits, IEEE Journal of*, vol. 29, no. 12, pp. 1491 –1496, dec 1994.

[106] M. Fakharzadeh, P. Mousavi, S. Safavi-Naeini, and S.H. Jamali, "The Effects of Imbalanced Phase Shifters Loss on Phased Array Gain," *IEEE Antenna Wireless Propag. Lett.*, vol. 7, pp. 192–196, 2008.

[107] B. Biglarbegian, M. Nezhad-Ahmadi, M. Fakharzadeh, and S. Safavi-Naeini, "Millimeter-Wave Reflective-Type Phase Shifter in CMOS Technology," *Microwave and Wireless Components Letters, IEEE*, vol. 19, no. 9, pp. 560–562, 2009.

[108] A. Natarajan, M. Tsai, and B. Floyd, "60GHz RF-path phase-shifting two-element phased-array front-end in silicon," in *VLSI Circuits, 2009 Symposium on*, 2009, pp. 250–251.

[109] Byung-Wook Min, and Gabriel M. Rebeiz, "Ka-Band BiCMOS 4-Bit Phase Shifter with Integrated LNA for Phased Array T/R Modules," pp. 479–482, June 2007.

[110] G. M. R. T. M. Hancock, "A 12-GHz SiGe phase shifter with integrated LNA," *IEEE Trans. Microwave Theory Tech.*, vol. 53- part1, no. 3, pp. 977–983, Mar. 2005.

[111] Pei-Si Wu; Hong-Yeh Chang,; Ming-Fong Lei,; Bo-Jr Huang,; Huei Wang,; Cheng-Ming Yu,; Chern, J.G.J., "A 40-74 GHz amplitude/phase control MMIC using 90-nm CMOS technology," pp. 115–118, Oct 2007.

[112] R. V. F. Ellinger and W. Bchtold, "Ultracompact Reflective-Type Phase Shifter MMIC at C-Band With 360° Phase-Control Range for Smart Antenna Combining," *IEEE J. Solid States Circuits*, vol. 37, no. 4, pp. 481–486, Apr. 2002.

[113] H. Zarei and D. J. Allstot, "A low-loss phase shifter in 180 nm CMOS for multiple-antenna receivers," pp. 382–534, Feb 2004.

[114] H. Hayashi and M. Mauraguchi, "An MMIC active phase shifter using a variable resonant circuit [and MESFETs]," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 47, no. 10, pp. 2021 –2026, oct 1999.

[115] M. Chu, D. J. Allstot, "CMOS phase-shifting circuits for wireless beamforming transmitters," *Journal of Analog Integrated Circuits and Signal Processing*, vol. 54, no. 1, pp. 45–54, Jan. 2008.

[116] R. Lahiji, L. Katehi, and S. Mohammadi, "A Distributed Analogue CMOS Phase Shifter with Shielded Transmission Line," in *Microwave Conference, 2008. EuMC 2008. 38th European*, oct. 2008, pp. 817 –820.

[117] C.-H. Tseng, C.-J. Chen, and T.-H. Chu, "A Low-Cost 60-GHz Switched-Beam Patch Antenna Array With Butler Matrix Network," *Antennas and Wireless Propagation Letters, IEEE*, vol. 7, pp. 432 –435, 2008.

[118] W. Lee, J. Kim, C. S. Cho, and Y. J. Yoon, "A 60 GHz Rotman lens on a silicon wafer for system-on-a-chip and system-in-package applications," in *Microwave Symposium Digest, 2009. MTT '09. IEEE MTT-S International*, june 2009, pp. 1189 –1192.

[119] R. V. Garver, "Broad-band diode phase shifters," *IEEE Trans. Microwave Theory Tech.*, vol. 20, no. 5, pp. 314–323, May 1972.

[120] J. D. C. M. M. M. Morton, J. P. Comeau and J. Papapolymerou, " Sources of Phase Error and Design Considerations for Silicon-Based Monolithic High-Pass/Low-Pass Microwave Phase Shifters," *IEEE Trans. Microwave Theory Tech.*, vol. 54, no. 12, pp. 4032–4040, Dec. 2006.

[121] Kwang-Jin Koh and Gabriel M. Rebeiz, "An X- and Ku-Band 8-Element Linear Phased Array Receiver," pp. 761–764, Sep. 2007.

[122] M.-D. Tsai and A. Natarajan, "60GHz passive and active RF-path phase shifters in silicon," in *Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE*, june 2009, pp. 223 –226.

[123] I. Sarkas, M. Khanpour, A. Tomkins, P. Chevalier, P. Garcia, and S. Voinigescu, "W-band 65-nm CMOS and SiGe BiCMOS transmitter and receiver with lumped I-Q phase shifters," in *Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE*, june 2009, pp. 441 –444.

[124] K.-J. Kim, K. Ahn, T. Lim, H. Park, and J.-W. Yu, "A 60 GHz Wideband Phased-Array LNA With Short-Stub Passive Vector Generator," *Microwave and Wireless Components Letters, IEEE*, vol. 20, no. 11, pp. 628 –630, nov. 2010.

[125] J.-C. Wu, J.-C. Kao, J.-J. Kuo, K.-Y. Kao, and K.-Y. Lin, "A 60-GHz single-ended-to-differential vector sum phase shifter in CMOS for phased-array receiver," in *Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International*, june 2011, pp. 1 –4.

[126] P. Vadivelu, P. Sen, S. Sarkar, D. Dawn, S. Pinel, and J. Laskar, "Integrated cmos mm-wave phase shifters for single chip portable radar," in *Microwave Symposium Digest, 2009. MTT '09. IEEE MTT-S International*, june 2009, pp. 565 –568.

[127] M. Tabesh, A. Arbabian, and A. Niknejad, "60GHz low-loss compact phase shifters using a transformer-based hybrid in 65nm CMOS," in *Custom Integrated Circuits Conference (CICC), 2011 IEEE*, sept. 2011, pp. 1 –4.

[128] M. El-Tanani and G. Rebeiz, "C-band low-loss phase shifter 360° for wlan applications,," pp. 1503–1506, 2007.

[129] J. I. Upsur and B. D. Geller, "Low loss 360 x-band phase shifter,," pp. 487–490, June 1990.

[130] C.S. Lin, S.F. Chang, C.C. Chang, and Y.H. Shu, "Design of a Reflection-Type Phase Shifter With Wide Relative Phase Shift and Constant Insertion Loss," *IEEE Trans. Microwave Theory Tech.*, vol. 55, no. 9, pp. 1862–1868, Sept. 2007.

[131] Hiroshi Okazaki and Tetsuo Hirota, "Multilayer mmic broad-side coupler with a symmetric structure," *IEEE Microwave and Guided Wave Letters*, vol. 7, no. 6, pp. 145–146, Jun. 1997.

[132] Rajesh Mongia, and Inder Bahl, and Prakash Bhartia, *RF and Microwave Coupled-Line Circuits*. Artech House, 1999.

[133] S. B. Cohn, "Characteristic impedances of broadside-coupled strip transmission lines," *IEEE Transactions on Microwave Theory and Techniques*, vol. 8, no. 6, pp. 633–637, Nov. 1960.

[134] F. Oberhettinger and W. Magnus, *Applications of Elliptic Functions in Physics and Technology.* New York: Springer, 1949.

[135] R. V. F. Ellinger and W. Bchtold, "Ultracompact Reflective-Type Phase Shifter MMIC at C-Band With 360° Phase-Control Range for Smart Antenna Combining," *IEEE J. Solid States*, vol. 37, no. 4, pp. 481–486, Apr 2002.

[136] Gabriel M. Rebeiz, *RF MEMS: Theory, Design, and Technology.* John Wiley and Sons, 2003.

[137] J. Park, H. Kim, W. Choi, Y. Kwon and Y. K. Kim, "V-Band Reflection-Type Phase Shifters Using Micromachined CPW Coupler and RF Switches," *IEEE Journal of Microelectromechanical Systems*, vol. 11, no. 6, pp. 808–814, Dec. 2002.

[138] B. Biglarbegian, M. Bakri-Kassem, R. Mansour, and S. Safavi-Naeini, "MEMS-based reflective-type phase-shifter for emerging millimeter-wave communication systems," in *Microwave Conference (EuMC), 2010 European*, sept. 2010, pp. 1556 –1559.

[139] D. S. A. W. Jacomb-Hood and J. D. Merrill, "A three-bit monolithic phase shifter at V-band," *"in IEEE MTT-S International Microwave Symposium Digest"*, pp. 81–84, June 1987.

[140] S. D. S. Weinreb, W. Berk and N. Byer, "Monolithic varactor 360° phase shifters for 75 110 GHz," *"in International Semiconductor Device Research Conference, Charlottesville, VA"*, Dec 1993.

[141] K. Zuefle, F. Steinhagen, W. H. Haydl, and A. Hulsmann, "Coplanar 4-bit HEMT phase shifters for 94 GHz phased-array radar systems," *"in IEEE MTT-S International Microwave Symposium Digest, Anaheim, CA"*, pp. 303–306, June 1999.

[142] [Online]. Available: http://www.ansoft.com/hfss

[143] URL:http://cirfe.uwaterloo.ca/documents/UWMEMSDesignHandbookv2.3.pdf.

[144] [Online]. Available: http://www.ansys.com/

[145] S. Kishimoto, N. Orihashi, Y. Hamada, M. Ito, and K. Maruhashi, "A 60-GHz band CMOS phased-array transmitter utilizing compact baseband phase shifters," in *Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE*, june 2009, pp. 215 –218.

[146] E. Cohen, C. Jakobson, S. Ravid, and D. Ritter, "A bidirectional TX/RX four element phased-array at 60GHz with RF-IF conversion block in 90nm CMOS process," in *Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE*, june 2009, pp. 207 –210.

[147] B. Razavi, "A 60GHz direct-conversion CMOS receiver," in *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, feb. 2005, pp. 400 –606 Vol. 1.

[148] T. Yao, M. Gordon, K. Tang, K. Yau, M.-T. Yang, P. Schvan, and S. Voinigescu, "Algorithmic Design of CMOS LNAs and PAs for 60-GHz Radio," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 5, pp. 1044 –1057, may 2007.

[149] B. Heydari, P. Reynaert, E. Adabi,M. Bohsali, B. Afshar, M.A. Arbabian and A.M. Niknejad, "A 60-GHz 90-nm CMOS cascode amplifier with interstage matching," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2893–2904, Dec. 2007.

[150] T. Zwick, D. Liu, and B. Gaucher, "Broadband planar superstrate antenna for integrated millimeterwave transceivers," *Antennas and Propagation, IEEE Transactions on*, vol. 54, no. 10, pp. 2790 –2796, oct. 2006.

[151] K. Kim, H. Yoon, and K. O, "On-chip wireless interconnection with integrated antennas," in *Electron Devices Meeting, 2000. IEDM Technical Digest. International*, 2000, pp. 485 –488.

[152] C. Cao, Y. Ding, X. Yang, J.-J. Lin, A. Verma, J. Lin, F. Martin, and K. O, "A 24-GHz Transmitter with an On-Chip Antenna in 130-nm CMOS," in *VLSI Circuits, 2006. Digest of Technical Papers. 2006 Symposium on*, 0-0 2006, pp. 148 –149.

[153] K. Kim and K. O, "Characteristics of integrated dipole antennas on bulk, SOI, and SOS substrates for wireless communication," in *Interconnect Technology Conference, 1998. Proceedings of the IEEE 1998 International*, jun 1998, pp. 21 –23.

[154] R. Li, W. Bomstad, J. Caserta, X. Guo, and O. Kenneth, "Evaluation of integrated antennas for wireless connection between an integrated circuit and an off-chip antenna," in *Interconnect Technology Conference, 2003. Proceedings of the IEEE 2003 International*, june 2003, pp. 120 – 122.

[155] N. Behdad, D. Shi, W. Hong, K. Sarabandi, and M. Flynn, "A 0.3mm^2 Miniaturized X-Band On-Chip Slot Antenna in 0.13 μm CMOS," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2007 IEEE*, june 2007, pp. 441 –444.

[156] Shamim, A.; Roy, L.; Fong, N.; Tarr, N.G., "24 GHz On-Chip Antennas and Balun on Bulk Si for Air Transmission," *Academic Press*, vol. 56, no. 2, pp. 303–311, Feb. 2008.

[157] T. Yao, L. Tchoketch-Kebir, O. Yuryevich, M. Gordon, and S. Voinigescu, "65GHz Doppler Sensor with On-Chip Antenna in 0.18 μm SiGe BiCMOS," in *Microwave Symposium Digest, 2006. IEEE MTT-S International*, june 2006, pp. 1493 –1496.

[158] C.-S. Wang, J.-W. Huang, S.-H. Wen, S.-H. Yeh, and C.-K. Wang, "A CMOS RF front-end with on-chip antenna for V-band broadband wireless communications," in *Solid State Circuits Conference, 2007. ESSCIRC 2007. 33rd European*, sept. 2007, pp. 143 –146.

[159] R. van Dijk, A. Neto, J. Akkermans, and J. Mills, "EBG-Based 60 GHz On-Chip Antenna in Passive Silicon," in *Microwave Conference, 2008. EuMC 2008. 38th European*, oct. 2008, pp. 682 –685.

[160] M.R. Nezhad-Ahmadi,and S. Safavi-Naeini, "On-chip antennas for 24, 60, and 77GHz single package transceivers on low resistivity silicon substrate," pp. 5059–5062, June 2007.

[161] E. Ojefors, H. Kratz, K. Grenier, R. Plana, and A. Rydberg, "Micromachined Loop Antennas on Low Resistivity Silicon Substrates," *Academic Press*, vol. 54, no. 12, pp. 3593–3601, Dec. 2006.

[162] E. Ojefors , F. Bouchriha , K. Grenier and A. Rydberg, "24 GHz ISM-band antennas on surface micromachined substrates for integration with a commercial SiGe process," *Proc. Eur. Conf. Wireless Technology*, 2003, munich, Germany.

[163] R. Alhalabi and G. Rebeiz, "High-efficiency angled-dipole antennas for millimeter-wave phased array applications," *Antennas and Propagation, IEEE Transactions on*, vol. 56, no. 10, pp. 3136 –3142, oct. 2008.

[164] M.-R. Nezhad-Ahmadi, M. Fakharzadeh, B. Biglarbegian, and S. Safavi-Naeini, "High-efficiency on-chip dielectric resonator antenna for mm-wave transceivers," *Antennas and Propagation, IEEE Transactions on*, vol. 58, no. 10, pp. 3388 –3392, oct. 2010.

[165] B. Porter and S. Gearhart, "Impedance and polarization characteristics of H and IHI slot antennas," *Antennas and Propagation, IEEE Transactions on*, vol. 48, no. 8, pp. 1272 – 1274, aug 2000.

[166] M. Basha, B. Biglarbegian, M. Neshat, S. Gigoyan, and S. Safavi-Naeini, "Low-cost, monolithic and integrated whispering gallery mode ring resonator for sensing applications," in *Microwave Conference (EuMC), 2011 41st European*, oct. 2011, pp. 515 –518.

[167] M. Fahimnia, M. Mohammad-Taheri, Y. Wang, M. Yu, and S. Safavi-Naeini, "A 59-66 GHz Highly Stable Millimeter Wave Amplifier in 130 nm CMOS

Technology," *Microwave and Wireless Components Letters, IEEE*, vol. 21, no. 6, pp. 320 –322, june 2011.

[168] R. Sorace, "Analysis of correlation and total power radiometer front-ends using noise waves," *"IEEE Trans. on Geoscience and Remote Sensing"*, vol. 43, no. 11, pp. 2452–2459, Nov. 2005.

[169] S. W. Wedge, *Computer-aided design of low noise microwave circuits.* PhD thesis, California Institute of Technology, 1991.

[170] S. W. Wedge and D. B. Rutledge, "Wave techniques for noise modeling and measurement," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 2004–2012, 1992.

[171] J. P. Weem and Z. Popovic, "A method for determining noise coupling in a phased-array antenna," *Microwave Symposium Digest, 2001 IEEE MTT-S International*, 2001.

[172] M. Fakharzadeh, S. Safavi-Naeini, S.H. Jamali and P. Mousavi, "Zero-knowledge beamforming of phased-array antennas based on simultaneous perturbation gradient approximation ," pp. 537–540, July 2006.

[173] P. Mousavi, M. Fakharzadeh, S.H. Jamali, K. Narimani, M. Hossu, and H. Bolandhemmat, and G. Rafi, and S. Safavi-Naeini, "A Low-Cost Ultra Low Profile Phased Array System for Mobile Satellite Reception Using Zero-Knowledge Beam-forming Algorithm," *IEEE Trans. Antennas Propag., Accepted for future publication*, June 2008.

[174] L. C. Godara, "Application of Antenna Arrays to Mobile Communications, Part II: Beam-Forming and Direction of Arrival Considerations," *Proceedings of IEEE*, vol. 85, no. 8, pp. 1195–1254, Aug. 1997.

[175] Simon Haykin, and Bernard Widrow, *Least-Mean-Square Adaptive Filters.* John Wiley and Sons, 2003.