Design of a Power Amplifier and Envelope Amplifier for a Multi-band Multi-standard Envelope Tracking System

by

Yushi Hu

A thesis
presented to the University of Waterloo
in fulfillment of the
thesis requirement for the degree of
Master of Applied Science
in
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2012

AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Yushi Hu

Abstract

This thesis presents the design of a Power Amplifier (PA) and envelope amplifier for an Envelope Tracking (ET) system that is aimed at meeting emerging radio standards in terms of power efficiency and linearity. The class J mode of operation, as well as the efficiency and power contours from load pull was exploited to develop an adequate procedure for the design of a broadband and high efficiency radio frequency PA. An in-depth study has also been conducted for a hybrid envelope amplifier topology in order to optimize it for power efficiency through proper setting of its switching stage supply. Two separate proof of concept prototypes of the PA and envelop amplifier were designed, fabricated and tested. The PA designed was able to achieve an average drain efficiency of 73.6%, average output power of 45.89dBm, and an average gain of 18dB between 650MHz and 1.050GHz (48% bandwidth). The envelope amplifier achieved close to 74.6% efficiency for a 5MHz bandwidth LTE signal envelope with 6.4dB peak to average power ratio.

Acknowledgements

I would like to take this opportunity to say how grateful I am to Dr. Slim Boumaiza for giving me the wonderful opportunity to study and learn during my time as a master's student under his supervision. His insights, lessons, and patience with me have really helped me grow in the past two years. I would like to thank him, Dr. Ajoy Opal, Dr. Vincent Gaudet and Hassan Sarbishaei for reading my thesis, and giving their valuable comments.

Throughout my time as a master's student, I have been blessed to have friends that have been there for me, and have given me much laughter in my life. Their encouragements, advices, and our times together are all treasured by me. I want to especially thank my girlfriend Sharon Liang for being patient with me even when I became difficult to deal with, and for helping me become a better person.

I have been extremely blessed with a family who have brought me up with great food, and more importantly with much love. I can never thank them enough. Last, but certainly not least, I want to thank God for His grace and guidance throughout my life. I pray that I will continue to grow in my walk with Him.

Table of Contents

List of Figures

List of Tables

List of Acronyms

AC: Alternating Current

ADS: Advanced Design Software

DC: Direct Current

DE: Drain Efficiency

EER: Envelope Elimination and Restoration

ET: Envelope Tracking

EVM: Error Vector Magnitude

FET: Field Effect Transistor

IMD: Intermodulation Distortion

LTE: Long Term Evolution

MATLAB: Matrix Laboratory

OFDM: Orthogonal Frequency-Division Multiplexing

PA: Power Amplifier

PAE: Power Added Efficiency

PAPR: Peak to Average Power Ratio

PUF: Power Utilization Factor

RF: Radio Frequency

SRFT: Simplified Real Frequency Technique

TPG: Transducer Power Gain

Chapter 1
Introduction

1.1 Motivation

Wireless communication has become critical in our lives. As its application becomes broader and more diverse, the demand for higher bandwidths increases as well. This together with the scarcity of wireless spectrum has led to the emergence of high spectral efficiency radio standards like Long Term Evolution (LTE). It is now a challenge for the wireless operators to accommodate the diversity of these new emerging communication standards together with legacy standards. Since current radio systems are optimized for only a given standard and centre frequency, the trivial solution is to use one set up for each standard. This forces the operator to obtain and maintain a very broad product spectrum [1]. The alternate method is to use multi-standard and multi-band transmitters which are flexible, and can support standards with different requirements of dynamic range, bandwidth, and center frequency. This saves costs as well as power consumption for the operator. This thesis will focus on the RF front end. Specifically, a design is presented aimed at improving the efficiency of the Power Amplifier (PA) for this multi-standard multi-band transmitter. The PA is responsible for using DC power to amplify a low power input signal to an output with enough power required to drive the antenna for long distance transmission. As the PA is one of the largest consumers of power in the transmitter system, any efficiency degradation will lead to serious problems such as thermal issues, compromised reliability, and higher operating costs.

1.2 Challenges

For multi-band operation, the PA must be capable of broadband operation to support signals with different centre frequencies and bandwidth. However, obtaining good performance from the PA at a wide range of frequencies comes with added complexities in its design. Meeting the requirements of the different standards is another challenge for the new design. LTE, for example, uses Orthogonal Frequency-Division Multiplexing (OFDM) to achieve higher bandwidth. However, the Peak to Average Power Ratio (PAPR) of OFDM signals are larger than previous standards [2], placing stricter demands on the Power Amplifier's (PA) linearity. This also degrades its efficiency since traditional PA designs obtain the highest efficiencies at maximum operating power only. In Figure 1.1, a class B amplifier's efficiency versus output power is plotted. As output power is backed off by 10dB, we see the efficiency drop by more than 53%.

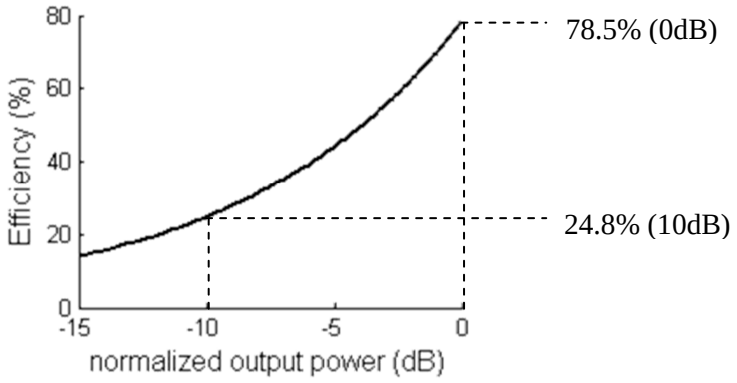


Figure 1.1 Class B efficiency versus output power

1.3 Potential solutions

For broadband operation of the PA, the introduction of the class J design space has lessened the requirement on the fundamental and harmonic terminations at the load, making matching across a wide bandwidth easier to achieve. Efficiency enhancement techniques at back-off power have also been developed to make the deployment of high PAPR standards more realistic. The Doherty power amplifier [4] and the Envelope Tracking (ET) system [10-12] are two popular efficiency enhancement techniques that have been heavily investigated. This thesis will focus on the development of the envelope tracking system as it is not inherently bandwidth limited like the Doherty, and is therefore a more promising technology for multi-band and multi-standard operation. The two components that make up the envelope tracking system will be developed and improved independently in this thesis with a focus on their efficiency.

1.4 Thesis organization

The thesis is organized as follows. First a review of classical PA design is done in chapter 2, with discussions about their efficiency, power, gain, and linearity. Efficiency enhancement techniques are also introduced. In chapter 3, the systematic design method used for the broadband PA is documented, and in chapter 4, the design and optimization of envelope amplifier is presented. Finally, conclusion and future works is presented in chapter 5.

Chapter 2
Efficiency Enhancement of Power Amplifier

PA is a critical part of every communication system. It is responsible for bringing the input signals to a power level suitable for transmission. It is also one of the biggest consumers of power in the transmission system, so keeping the PA efficient is of vital importance. Different operation classes and techniques have been utilized in PA designs in the past. Some of the classic modes of operation will be reviewed in this chapter. An idealized voltage controlled current source model for a Field Effect Transistor (FET) will be used for analysis, shown in Figure 2.1.

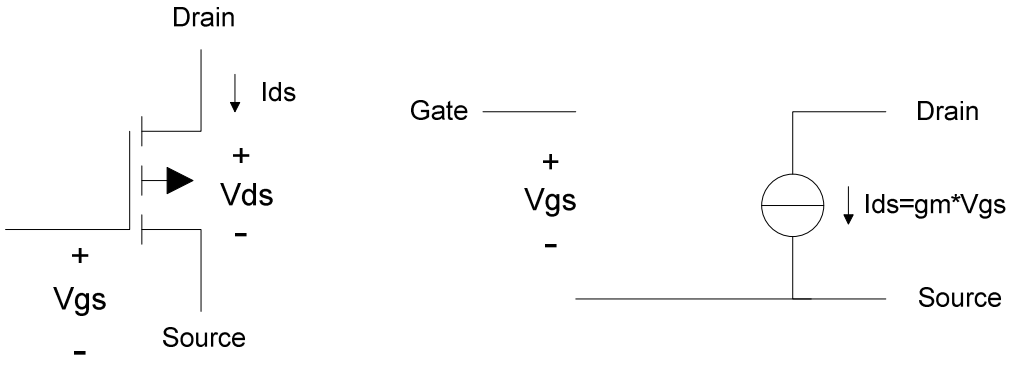
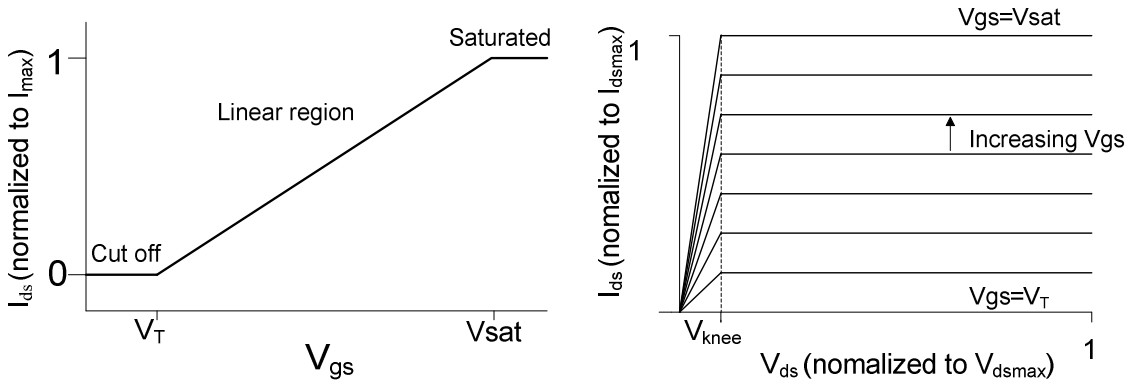


Figure 2.1 FET transistor with its ideal model

The ideal transistor's gate source voltage (V_{gs}) versus the drain source current (I_{ds}) characteristics are shown in Figure 2.2. In the linear region, it is assumed that the transconductance (gm) stays constant, and I_{ds} increases linearly with V_{gs}. There is also an abrupt cutoff once the transistor enters into the saturation or cutoff regions. However, a more realistic model would not have a linear region that is perfectly linear, and there would be a softer transition between the different regions of operation. In this ideal model the knee voltage (V_{knee}), or the turn on voltage will be assumed to be zero. In reality, its value is usually a significant portion of V_{dsmax}.



(a) (b)

Figure 2.2 Transistor's (a) I_{ds} versus V_{gs} and (b) I_{ds} vs. V_{ds}

2.1 Classical operation modes of the PA

Before introducing the classical operation modes of the PA, it is important to define the transistor's conduction angle. The conduction angle defines the portion of the signal period when the transistor is conducting current, or operating in the linear region. The gate bias of the transistor can be adjusted so that its conduction angle is equal to or less than 360 degrees. For conduction angles less than 360 degrees, it is implied that the transistor is operating in cutoff for parts of the signal. This is illustrated with a sine wave input plotted in Figure 2.3. The sine wave is biased at the gate so that part of the input voltage waveform goes below the threshold voltage, V_t. When V_{gs} goes below V_t the transistor is in cut-off operation.

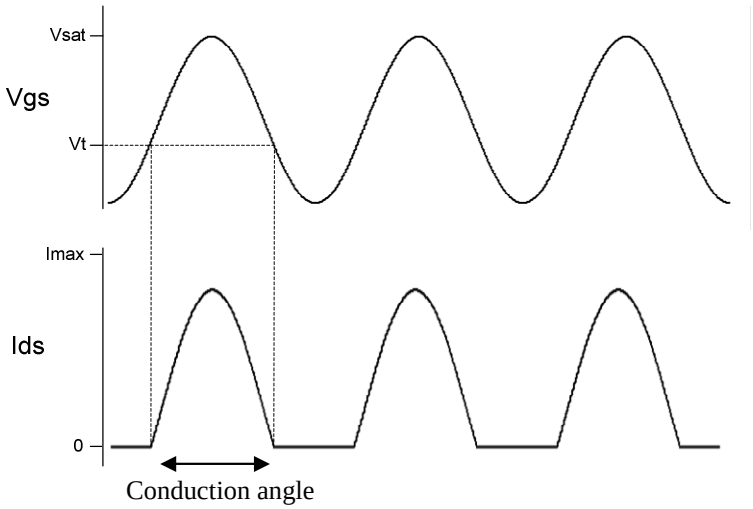


Figure 2.3 Vgs and Ids waveform illustrating conduction angle

The classes of operation of an amplifier can be differentiated according to their conduction angles. The bias point, quiescent current, and conduction angles for each class is given in Table 1, assuming that $V_t = 0$, and $V_{sat} = 1$.

Table 1. Class of Operation and Their Conduction Angles

Class of operation	Bias point	Quiescent Current	Conduction Angle
A	0.5	0.5	2π
AB	0 – 0.5	0-0.5	π-2π
B	0	0	π
C	< 0	0	0-π

The load lines for the different classes are drawn out in Figure 2.4 with their biasing points. The biasing point determines the conduction angle. The lower the biasing point, the lower the conduction angle. The load resistance, represented by the slope of the load line, is assumed to be R_{OPT}, which is the resistance that enables the PA to reach its maximum power. It can be observed that R_{OPT} decreases with the conduction angle as well.

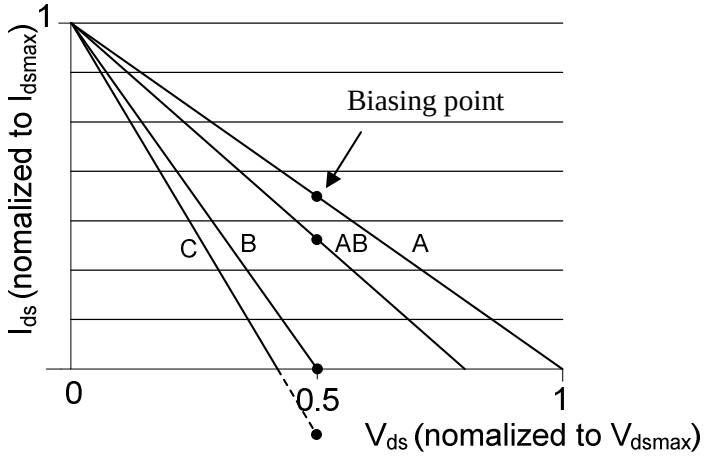


Figure 2.4 Class A, AB, B and C load line

To get an idea about how the output current changes with different conduction angles, Fourier analysis can be used to separate the output current into its DC, fundamental, and harmonics components [3]. The current waveform will be analyzed from - π to π radians for a cosine input. The total conduction angle is represented by α, and the RF current waveform can thus be written as

$$i_d(\theta) = I_q + I_{peak}\cos(\theta) \qquad \text{for} -\frac{\alpha}{2} < \theta < \frac{\alpha}{2}, \tag{2.1}$$

and

$$i_d(\theta) = 0 \qquad \text{for} -\pi < \theta < -\frac{\alpha}{2}, \qquad \frac{\alpha}{2} < \theta < \pi. \tag{2.2}$$

The DC component of the output current will be

$$I_{DC} = \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2}(I_q + I_{peak}\cos(\theta))\,d\,\theta = \frac{1}{2\pi}\left(I_q\alpha + 2I_{peak}\sin\left(\frac{\alpha}{2}\right)\right) \tag{2.3}$$

and the nth harmonics are given by

$$I_n = \frac{1}{\pi}\int_{-\alpha/2}^{\alpha/2}\left(I_q + I_{peak}\cos(\theta)\right)\cos(n\theta)\,d\,\theta \tag{2.4}$$

with the amplitude of the first harmonic being

$$I_1 = \frac{2}{\pi}I_q\sin\left(\frac{\alpha}{2}\right) + \frac{1}{2\pi}I_{peak}\left(\alpha + 2\sin\left(\frac{\alpha}{2}\right)\cos\left(\frac{\alpha}{2}\right)\right). \tag{2.5}$$

In order to express this equation as a function of the conductance angle, the relationship between the quiescent current and the peak current can be used. They can be written as a function of the conduction angle and the maximum current given by

$$\frac{I_q}{I_{peak}} = -\cos(\alpha) \tag{2.6}$$

where

$$I_{peak} = I_{max} - I_q. \tag{2.7}$$

The DC, fundamental, and harmonic currents are plotted in Figure 2.5. The DC component and the fundamental component will be the focus of later analysis on efficiency and power. However, it is important to realize that different classes will produce different harmonic components. So properly designed matching networks with proper harmonic termination in the output matching network is essential.

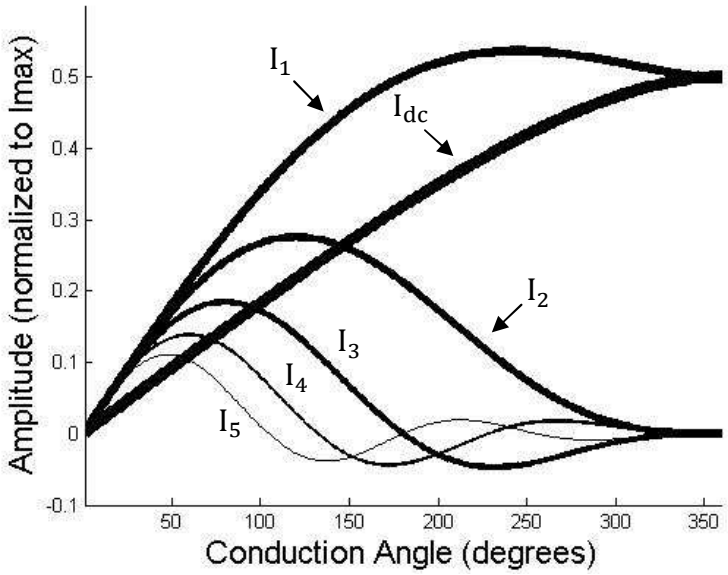


Figure 2.5 Current waveforms vs. conduction angle (Reproduced from [3])

Now that the classical classes of operation for the PA has been briefly introduced, we can take a look at the impact reduced conduction angles will have on the amplifier's efficiency, gain, power, and linearity. The following analysis on efficiency and power are done assuming that the harmonics are properly dealt with at the load for the different classes, and the optimal load impedance for maximum voltage swing is chosen.

2.1.1 Efficiency

One way to define the efficiency of the power amplifier is by its drain efficiency (DE). This is the ratio of RF output to DC input power at the drain of the transistor. The power added efficiency (PAE) on the other hand takes into consideration the input power as well. If the gain of the PA was low, then PAE will be significantly smaller than DE. Their expressions are given as

$$\mathrm{DE} = \frac{\mathrm{P_1}}{\mathrm{P_{dc}}}, \qquad \mathrm{PAE} = \frac{\mathrm{P_1} - \mathrm{P_{in}}}{\mathrm{P_{dc}}}. \tag{2.8}$$

The drain efficiency will be looked at in this section's analysis. The drain efficiency for max power, when $\mathbf{V_{1max}} = \mathbf{V_{dc}}$ can be found as

$$DE = \frac{P_1}{P_{dc}} = \frac{I_{1rms}V_{1rms}}{V_{dc}I_{dc}} = \frac{0.5I_{1max}V_{1max}}{V_{dc}I_{dcmax}} = \frac{0.5I_{1max}}{I_{dcmax}}. \quad 2.9$$

The drain efficiency of the amplifier versus changing conduction angle is plotted in Figure 2.6. The efficiency increases with a decreasing conduction angle. The lowest efficiency is class A, with 360 degrees conduction angle, and maximum 50% operating efficiency. Class C amplifier achieves the highest efficiency with the lowest conduction angle. These results are not surprising considering the current curves in Figure 2.5. The drain efficiency of the amplifier is determined by how small the DC part of the output current is in comparison to the fundamental current. Looking at the trend for these two currents, the DC component of the output current always decreases with conduction angle, while the fundamental component of the output current actually increases (during class AB operation) for a period before dropping with the conduction angle, leading to higher efficiencies.

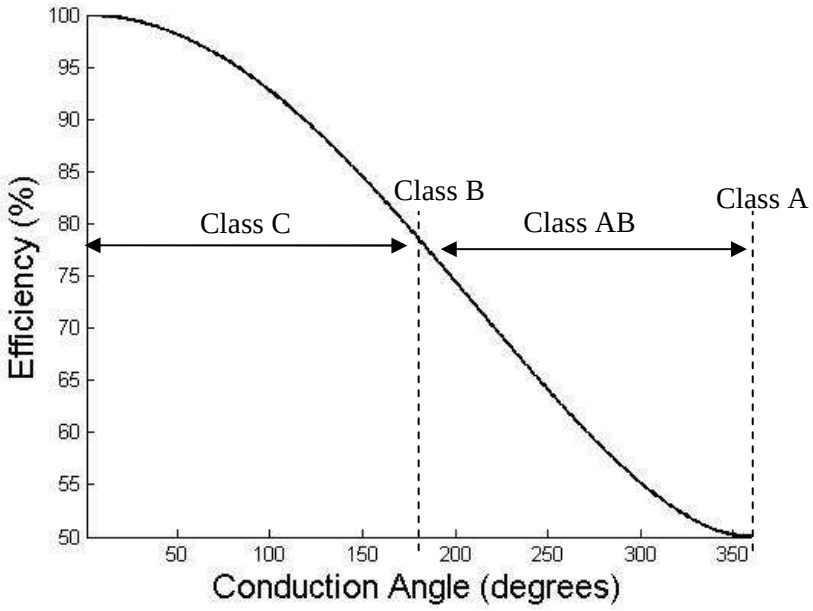


Figure 2.6 Drain efficiency vs. conduction Angle

Next we want to look at how drain efficiency changes at back-off operation for each class of operation. Efficiency at back off operation can be found by varying the value of I_{peak}, and then looking at the change in fundamental RF and DC power. Assuming that the load stays constant at $R_L = R_{OPT} = \frac{V_{dc}}{I_{1max}}$, drain efficiency is

$$DE = \frac{P_1}{P_{dc}} = \frac{I_{1rms}V_{1rms}}{V_{dc}I_{dc}} = \frac{0.5{I_1}^2 R_L}{I_{dc}V_{dc}} = \frac{0.5{I_1}^2 \frac{V_{dc}}{I_{1max}}}{I_{dc}V_{dc}} = \frac{0.5{I_1}^2}{I_{dc}I_{1max}}. \quad 2.10$$

Recall from equation 2.5 that I_1 is a function of the conduction angle. The conduction angle stays constant for class A and B biased amplifiers throughout its entire operation at 2π radians and π respectively. For class AB, α is equal to 2π radians when $I_{peak} < |I_q|$, and α stays constant at 0 for class C when $I_{peak} < |I_q|$. When $I_{peak} > |I_q|$, class AB and C will both have conductance angles that are a function of input drive given in equation 2.6.

The efficiencies at back-off power are plotted in Figure 2.7 for different biases. First thing to note is that none of the classical class of operation maintains its efficiency at back off. In general, as the conduction angle increases, so does the rate at which efficiency drops. Class A's efficiency drops the quickest at higher power, while class C and class B drops at much slower rates for most of the output power range. For example, class B's efficiency changes linearly with I_{peak}, while class A's efficiency has a quadratic relationship with I_{peak}.

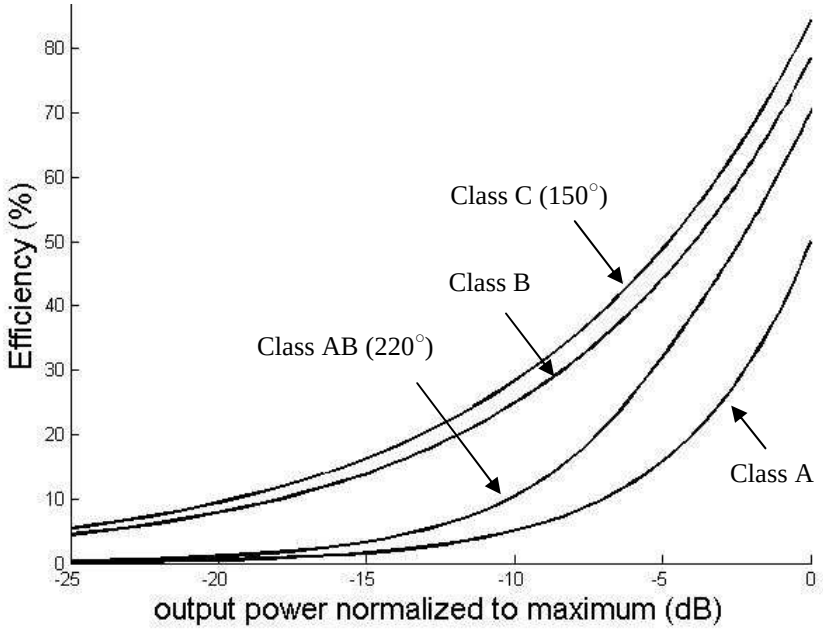


Figure 2.7 Drain efficiency vs. output power

2.1.2 Fundamental RF Power

The change in fundamental power is looked at with changing conduction angle. This will give a better idea of the power utilization factor (PUF), gain, and linearity of each class of operation. PUF is the RF power delivered by a device in a given mode of operation in comparison to the power it would have delivered in class A operation. It is plotted in Figure 2.8. Class AB's maximum fundamental RF output power is highest among the different classes. Class B gives the same output power as class A, and class C's output power decreases with conduction angle.

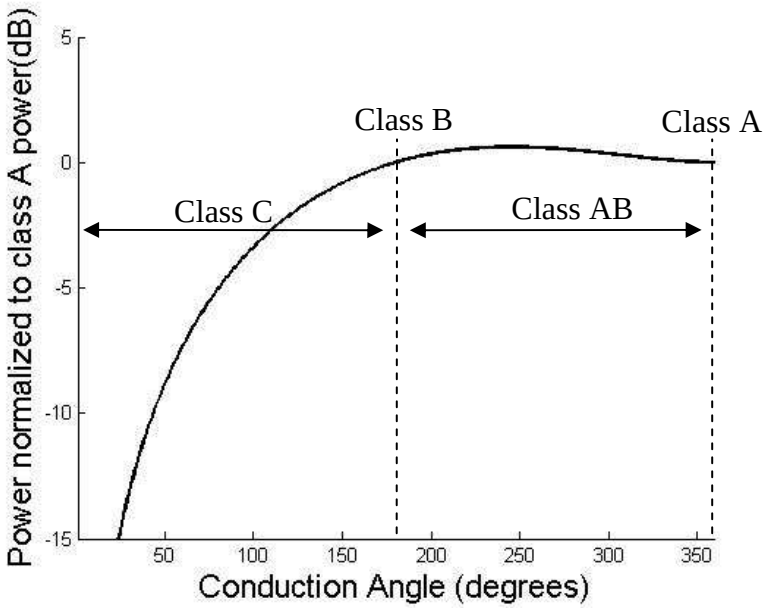


Figure 2.8 Output Power vs. Conduction Angle

The change of fundamental output currents with varying fundamental input voltage is plotted in Figure 2.9, and its squared relationship is plotted in Figure 2.10 to get a better sense of the output power. A point worth noting is the linearity of each class of amplifier. Class A and class B will operate with constant conduction angle throughout its back off. Class AB and class C's conduction angle will be a function of input voltage once $I_{peak} > |I_q|$. Differentiating the output fundamental current with respect to I_{peak}, which is a function of the input voltage, results in

$$\frac{dI_1}{dI_{peak}} = \frac{1}{2\pi}\left(\alpha + 2\sin\left(\frac{\alpha}{2}\right)\cos\left(\frac{\alpha}{2}\right)\right). \qquad 2.11$$

When the conduction angle is constant, $\frac{dI_1}{dI_{peak}}$ is a constant, output current increases linearly with the input voltage, leading to a linear input to output power relation. However, if conduction angle is not constant through its operation, then the output current is no longer just a linear function of the input voltage, leading to nonlinear input to output power relations. The gain is another thing to notice here. Power gain will go down with conduction angle. Class A, with the highest conduction angle has the highest power gain, while class C, with the lowest conduction angle will have the lowest power gain.

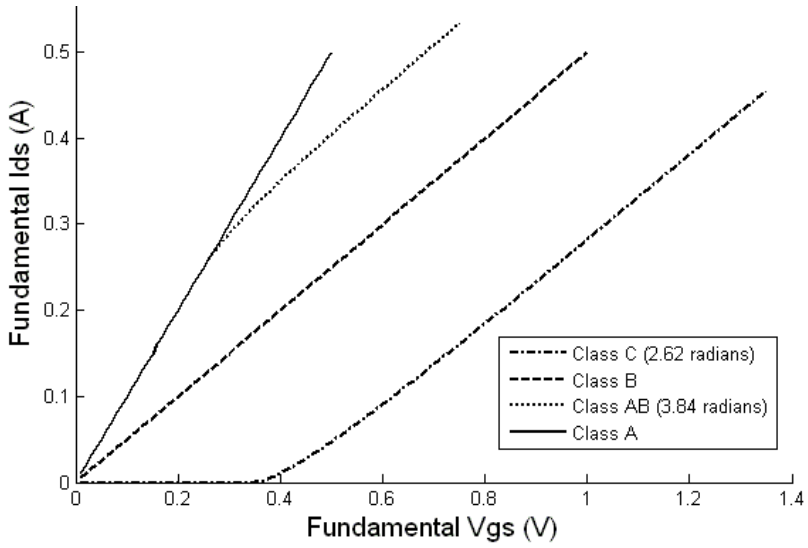


Figure 2.9 Fundamental Output current vs. Fundamental Input voltage

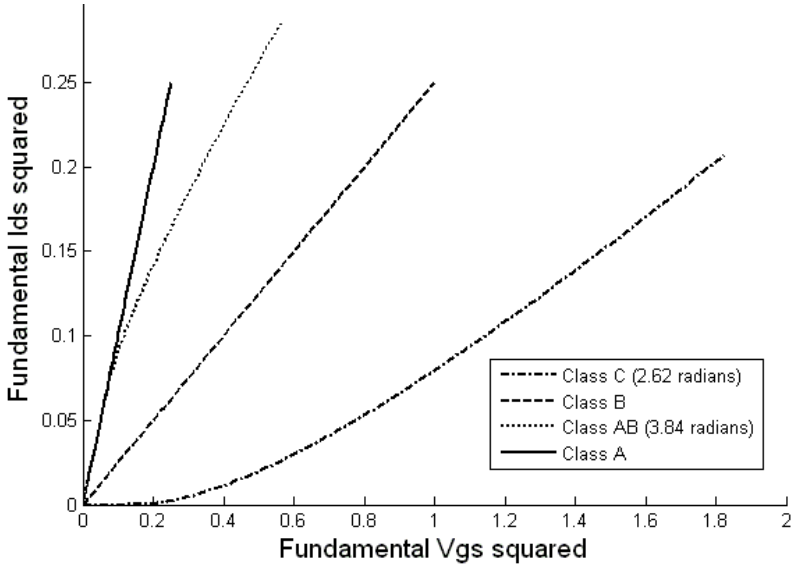


Figure 2.10 Fundamental output current squared vs. Fundamental input voltage squared

A short summary of the above analysis on efficiency, gain, max power, and linearity is given in table 2. By reducing the conduction angle of the transistor, efficiency is improved at both maximum operating power, and most power back off. However, sometimes the tradeoff is in the form of linearity, gain or max power. One thing to keep in mind is that these conclusions were made with the assumption that the ideal model of the FET transistor is valid. For example, class B would be considered a non-linear mode of operation if the transition between cut off and linear region of the transistor was not assumed to be abrupt.

Table 2 Summary of the classes of operation

Class of operation	**Efficiency**	**Gain**	**Max power**	**Linearity**
A	Poor	Excellent	Good	Excellent
AB	Satisfactory	Good	Excellent	Satisfactory
B	Good	Satisfactory	Good	Excellent
C	Excellent	Poor	Poor	Poor

2.2 Back-off Efficiency Enhancement Techniques

One important observation from the last section was that the efficiency the power amplifier degrades when the power is backed off from its maximum point. Let's look at the drain efficiency of class B in particular, given by

$$\mathrm{DE} = \frac{0.5\mathrm{I}_1\mathrm{V}_1}{\mathrm{I}_{\mathrm{dc}}\mathrm{V}_{\mathrm{dc}}} \tag{2.12}$$

where I_1 and I_{dc} for a conduction angle of π are

$$\mathrm{I}_1 = \frac{2}{\pi}\mathrm{I}_{\mathrm{q}} + \frac{1}{2}\mathrm{I}_{\mathrm{peak}}, \tag{2.13}$$

$$\mathrm{I}_{\mathrm{dc}} = \frac{1}{2}\mathrm{I}_{\mathrm{q}} + \frac{1}{\pi}\mathrm{I}_{\mathrm{peak}}. \tag{2.14}$$

Dividing equation 2.13 by 2.14, and setting I_q= 0 for class B operation gives

$$\frac{\mathrm{I}_1}{\mathrm{I}_{\mathrm{dc}}} = \frac{\pi}{2}. \tag{2.16}$$

So the relationship between the fundamental and dc current is fixed no matter what the peak current is. With that in mind, the drain efficiency at back-off can be written as

$$DE = \frac{0.5 I_1 V_1}{I_{dc} V_{dc}} = \frac{\pi}{4}\left(\frac{V_1}{V_{dc}}\right) \quad 2.17$$

In order to maintain the drain efficiency at its maximum, the ratio $\frac{V_1}{V_{dc}}$ should be maintained close to unity. V_{dc} is the maximum output voltage swing possible at the drain, so the relationship implies that in order to maintain efficiency, the amplifier has to have maximum voltage swing at all input voltage. This ensures that the DC power is as small as possible in comparison to the RF power. Two ways of achieving this will be discussed next: Load modulation, and drain modulation.

2.2.1 Load Modulation

Continuing with the analysis with class B operation, if R_L stayed constant at back-off, then V_1 would decrease linearly with the input RF voltage, and so will the amplifier's efficiency. However, if R_L is varied at back-off power with respect to the input voltage with the relationship

$$R_L^* = \frac{2V_{DC}}{I_{max}}\left(\frac{V_{in}}{V_{in\,max}}\right), \quad 2.18$$

then V_1 can be manipulated to maintain operation efficiency. In Figure 2.11, the load line for a class B amplifier operating in back off is shown for a more visual illustration of this efficiency improvement. The load impedance is originally set to R_{OPT}, but this leads to losses as not all of the possible voltage swing is used. To remedy this, one can increase the load resistance. This causes the load line to decrease its slope, and the output once again has the maximum possible voltage swing. However, adjusting the load impedance to be R_L^* to maintain efficiency at back off would result in a non-linear amplifier. The Doherty Amplifier as an implementation of load modulation has been able to avoid this linearity problem through its design.

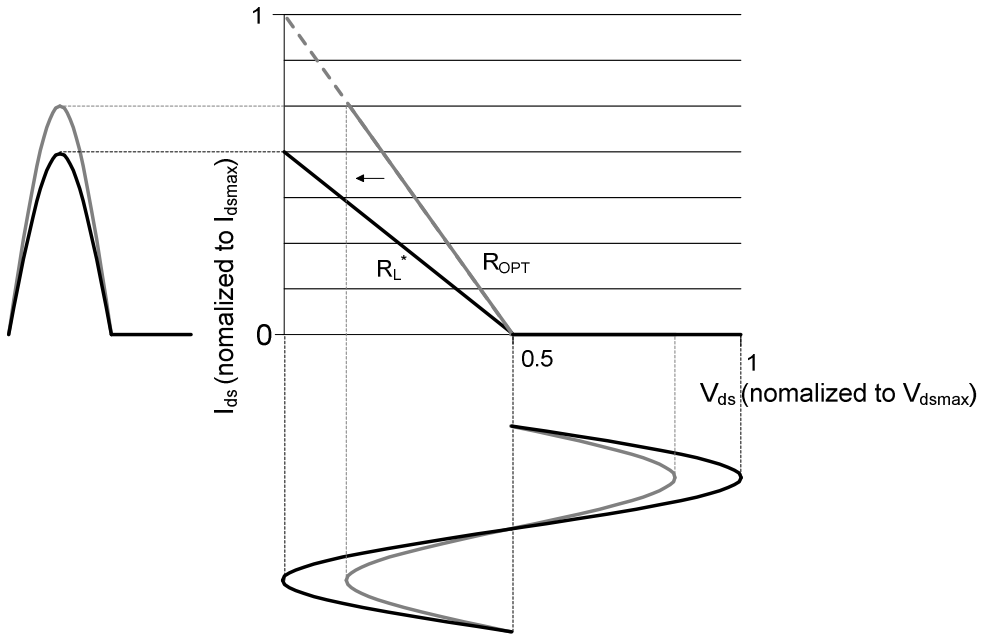
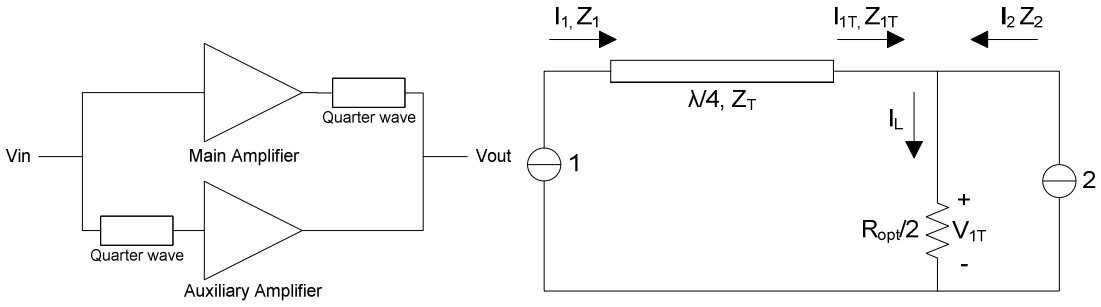


Figure 2.11 Load modulation load line

2.2.2 The Doherty Amplifier

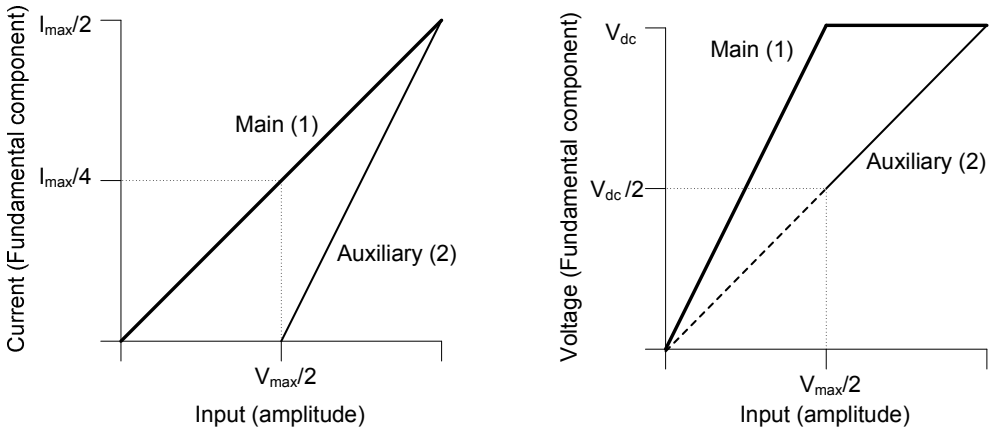
The Doherty Technique was proposed by William H. Doherty in 1936 [4]. The Doherty configuration can be represented with the following topology and equivalent schematic drawn in Figure 2.12. This analysis has been presented before by Cripps [3]. The main and auxiliary amplifiers are modeled as controlled current sources 1 and 2 respectively with V_{1T} being the output voltage.



(a) (b)

Figure 2.12 (a) Simplified Doherty topology (b) with equivalent schematic

The ideal current and voltage profile for a Doherty amplifier optimized for 6dB back-off power is shown in Figure 2.13 for the main and auxiliary amplifiers.



(a) (b)

Figure 2.13 (a) Current and (b) voltage profile for a Doherty Amplifier [3]

The voltage and currents before and after the quarter wave impedance transformer can be related in the following relationships

$$V_{1T}I_{1T} = V_1I_1 \tag{2.19}$$

$$\frac{V_{1T}V_1}{I_{1T}I_1} = Z_T^2. \tag{2.20}$$

If Z_T is set to R_{OPT}, through these two equations, it can be worked out that

$$V_{1T} = I_1R_{OPT}. \tag{2.21}$$

Since I_1, the current of the main amplifier, has a linear relationship with the input voltage throughout the amplifier's operating range, the output will maintains its linearity for all of the input range, and the problem of non-linearity faced by load modulation is avoided.

Assuming class B operation for both main and auxiliary amplifiers, efficiency of the Doherty amplifier at back-off is calculated as follows. When the input voltage is less than $\frac{V_{max}}{2}$, the efficiency of the whole Doherty amplifier is determined by the main amplifier. After the input increases above $\frac{V_{max}}{2}$, the overall efficiency of the system becomes a function of both the main and auxiliary amplifier. Assuming that the auxiliary amplifier is also biased in class B, the drain efficiency of the Doherty amplifier for when $V_{in} > \frac{V_{max}}{2}$ is given by

$$DE(V_{in}) = \frac{v_{in}^2 \pi}{2V_{max}(3v_{in} - V_{max})}. \quad 2.22$$

Taking these two relationships, the ideal efficiency curves for a Doherty amplifier is plotted in Figure 2.14, notice the characteristic efficiency peaks at input voltages of $\frac{V_{max}}{2}$ and V_{max}.

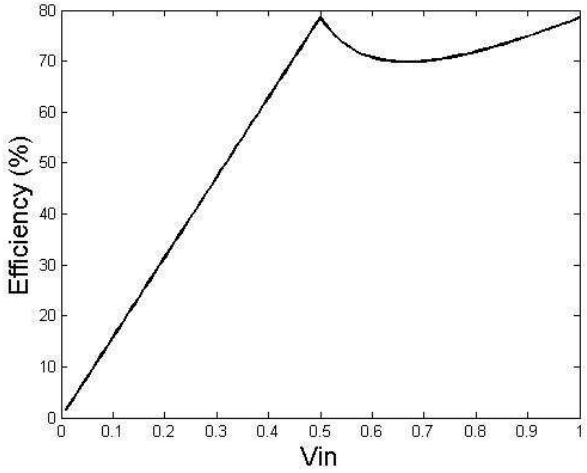


Figure 2.14 Ideal Doherty efficiency plot

In the classical Doherty design, the optimal efficiency point at back-off is around 6dB. For optimal operation with signals of different PAPR, asymmetric Doherty amplifiers [5], and multistage Doherty amplifiers [6] have been designed to improve the efficiency of signals operating lower than 6dB back-off power. However, one of the inherent problems of Doherty technique is the use of the quarter wave transformer, which limits its broadband capabilities.

2.2.3 Drain Modulation

In the previous sub section, load modulation techniques were briefly looked at as a method used to maintain efficiency in power back-off operation. An alternate way to operate efficiently at back-off is to modulate the drain bias of the transistor. Recall the relationship given in equation 2.17. By decreasing the drain bias V_{DD} as V_1 decreases the same effect can be achieved. One can maintain $\frac{V_1}{V_{dc}}$ at a factor of one if

$$V_{DD}^* = V_{dc} = V_1 \quad 2.23$$

A more visual picture of this can be obtained from a load line analysis. In Figure 2.15, the load line for a class B amplifier operating in back off is presented. Once again we see that it is not using all the possible voltage swing at the output. If the whole load line is shifted to the left by changing V_{DD} to be equal to output voltage swing V_1, then the whole voltage swing will be utilized, and efficiency maintained.

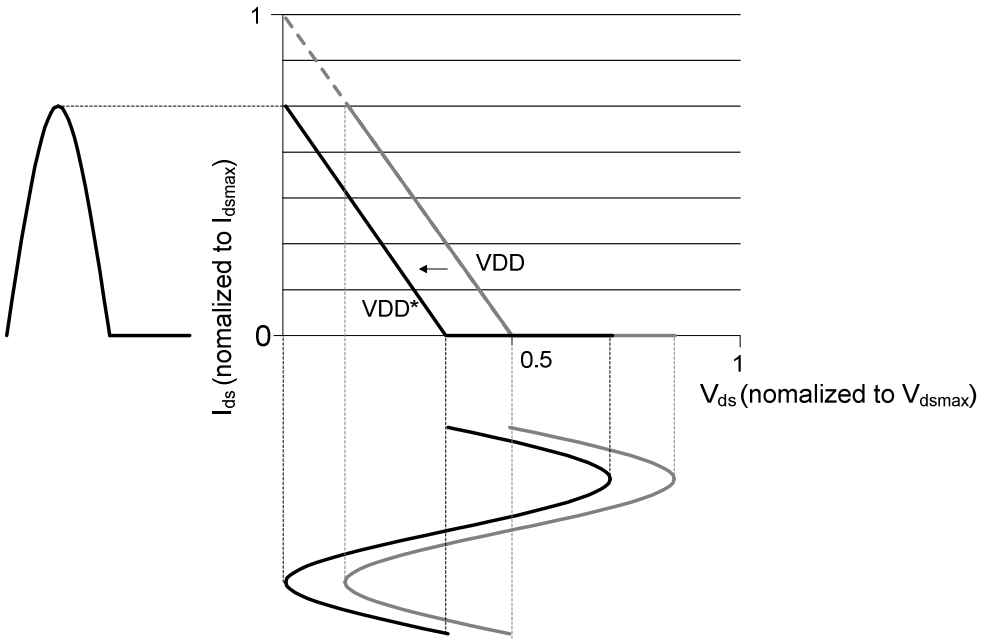


Figure 2.15 Drain modulation load line

Two popular techniques for drain modulation will be looked at, including the envelope elimination and restoration technique (EER) and the envelope tracking technique (ET). Both methods significantly improve the amplifier's efficiency at back-off.

2.2.4 Envelope Elimination and Restoration

EER was developed by Khan [7] in 1952. The system he proposed used an efficient but non linear class C amplifier to amplify a limited signal with only phase information. The signal envelope is detected at the input, amplified, and then modulates the amplified phase only signal at the output,

producing an amplified copy of the input signal. The following is a typical simplified schematic for EER systems

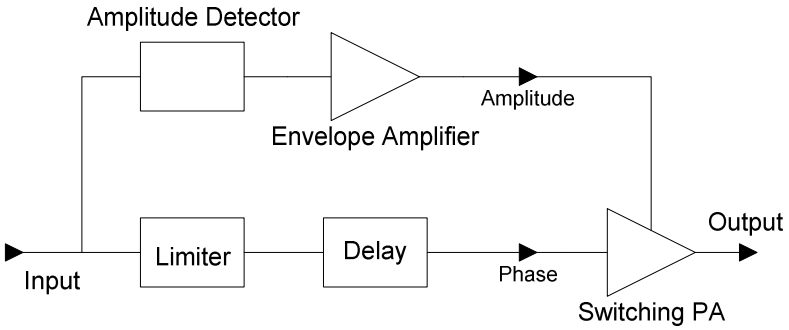


Figure 2.16 EER system [8]

In modern implementations, the magnitude and phase components are generated in the baseband domain and up-converted to RF [8]. The complex baseband signal $s_{base}(t)$ can be written in its vector form as

$$s_{base}(t) = I(t) + jQ(t) = A(t)\phi(t) \tag{2.24}$$

where

$$A(t) = \sqrt{I(t)^2 + Q(t)^2}, \qquad \phi(t) = e^{j\arctan\left(\frac{Q(t)}{I(t)}\right)}. \tag{2.25}$$

The nonlinear transformation for both the amplitude and phase signals increases the required bandwidth on the amplifier. The linearity of the EER amplifier does not depend upon on the RF transistor, but rather the envelope amplifier's finite bandwidth, and the delay between the phase and amplitude signals when they combine [9]. These strict requirements on bandwidth and alignment have confined the EER system to be more suitable for narrowband signals. Another drawback of EER is its power leakage at low power, making it unsuitable for signals with high dynamic range.

2.2.5 Envelope Tracking

ET method is similar to EER in the sense that the drain of the PA tries to follow the output envelope signal. However, the accuracy, or linearity of the tracking is relaxed because the input to the gate of the transistor still contains amplitude information. The linearity of the output signal is now more

dependent on the linearity of the PA rather than the envelope amplifier. It has been shown that ET systems are less sensitive to path mismatch between the envelope signal and the RF signal at the drain and gate of the power transistor [10], but this comes with a tradeoff in efficiency. A simplified schematic of the ET system is given in Figure 2.17

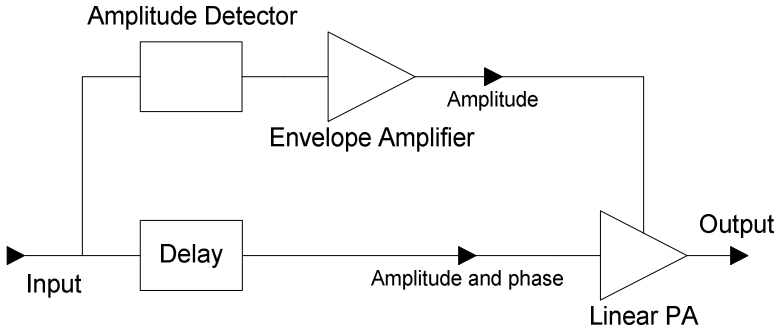


Figure 2.17 ET system [8]

With the relaxed requirements on the drain modulation, the envelope signal can be shaped and altered. This can lead to a few advantages. The bandwidth and dynamic range of the envelope can be reduced to lessen the requirements on the envelope amplifier. Secondly, shaping the envelope can also work to avoid the non-linear knee region of the power transistor, as well as track the Intermodulation Distortion (IMD) sweet spot for better linearity [11].

In both the ET and EER technique, the performance of the envelope amplifier is critical to overall efficiency since

$$\eta_{\text{overall}} = \eta_{\text{PA}}\eta_{\text{EA}} \qquad 2.26$$

Much research has been done to improve the efficiency of the envelope amplifier, while still maintaining an acceptable amount of signal fidelity. The envelope tracking system has been a very promising candidate for multi-standard, multi-band operation, and has been demonstrated to work with a wide variety of standards with different centre frequencies [12]. This thesis will work on further development of this technology.

Chapter 3
Broadband Power Amplifier

In order to support signals with wide bandwidth and different centre frequencies, the PA should achieve good RF performance across a broad frequency range. A simplified PA is shown in Figure 3.1. The DC bias of the transistor and the input output matching networks are the important design parameters for the PA. While the bias level determines the class of operation, as discussed in chapter 2, the matching networks matches the 50Ω load or source to the gate and drain of the transistor, and presents impedances at the fundamental and harmonics for optimal power or efficiency at all the frequencies within the design bandwidth.

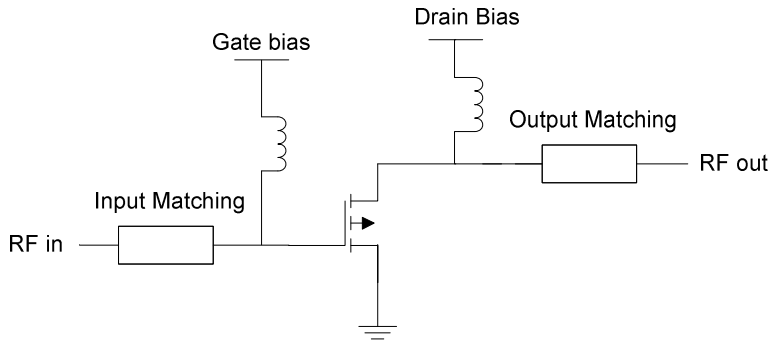


Figure 3.1 Simplified schematic of a PA

3.1 Class J

Amplification of broadband signals with the classical modes of operation, such as class B, is hard to achieve as they require harmonics to be properly shorted. Short terminations are usually narrowband in nature, and presenting the short right at the drain could be impossible due to package parasitic. Also, with a wide enough bandwidth, the second harmonics of the lower bandwidth could be close to, or within the design bandwidth itself. However, with the concept of class J operation and class B/J design space [3], it is shown, in theory, that several solutions gave efficiency performances similar to that of a class B amplifier. These solutions are usually terminated with reactive components in the fundamental load, and a phase shifted, highly reactive second harmonic. This relieves the need for a harmonic short at all frequencies, and lessens the requirement on the fundamental and harmonic termination, making broadband matching more realistic [13].

3.2 Load and Source Pull

For every frequency within the design bandwidth, there is a set of optimal impedance combination at the load and source for either maximum efficiency or output power. One of the simplest ways to find these impedances is through load and source pulls. During this process, first the frequency of operation, input drive as well as the biasing point for the gate and drain are determined and set. The source and load impedance are then varied, and the performance of the device under test is measured. From these measurements, a combination of impedance values for acceptable power and maximum efficiency can be found. The load and source pull procedure can be a tedious and time consuming method. However, if accurate enough model of the transistor is provided, load and source pull through simulation can save much time and energy. Agilent's Advanced Design Software (ADS) will be used to carry out the load and source pull on a 45W GaN HEMT transistor from Cree is used. Transistor is biased for a drain quiescent current of 400mA for class AB operation for its good power, efficiency, as well as linearity performance. While expansive square-law characteristics in the transistor's turn on will degrade class B's linearity, it will work to counter the compressive effects of class AB, making it a more linear class of operation [3]. Ideal DC blocks are used to keep the DC from the RF source, and Ideal DC feed is used to keep the RF away from the DC source as shown in Figure 3.2.

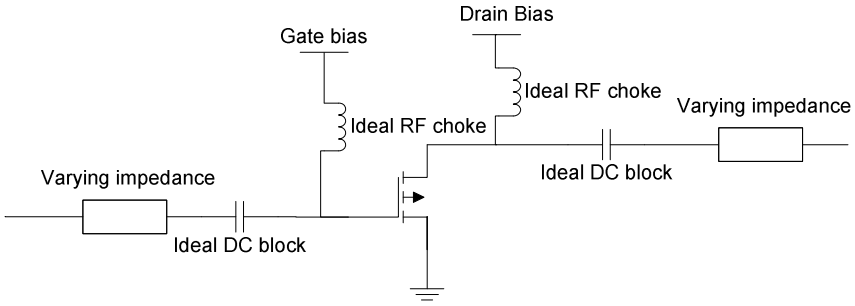


Figure 3.2 Simplified Load and source pull set up

The impedances for optimal efficiency at three frequency points, 650MHz, 850MHz and 1050MHz were found to cover the targeted frequency range. The result of the load pull is efficiency and power contours. Each contour goes through all the impedance points that present a particular efficiency or power. Figure 3.3 shows the load-pull results for the two frequencies at the edges of the targeted band, 650MHz and 1050MHz. The chosen optimal impedances are represented by a black dot on the Figure

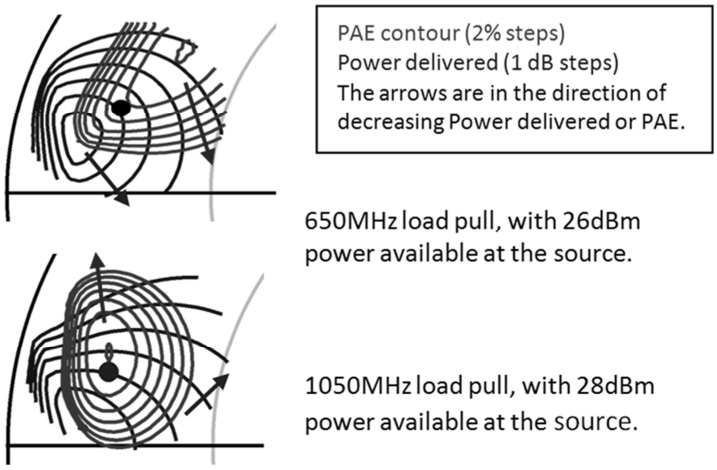


Figure 3.3 Load pull contours

Load pull results show that there is a compromise between power and efficiency in the selection of the matching impedance. In light of this, impedances were chosen so that first they met a specific power level, or a specific power contour. Then, the maximum efficiency possible for that power level was found. This is a unique point. The impedance points were found up to the third harmonic for the load and source side, and listed in table 3 and 4 respectively. The harmonics are given as reflection coefficients. The results of the load and source pull are shown in table 5. A fairly consistent output power was achieved, as well as excellent efficiencies.

Table 3 Optimal load impedance

Frequency	650 MHz	850 MHz	1050 MHz
Fundamental impedance	7.085+j7.801	7.579+j7.241	6.402+j5.715
2nd harmonic reflection coefficient	$0.99\, e^{j\pi\frac{30}{180}}$	$0.99\, e^{j\pi\frac{30}{180}}$	$0.99\, e^{j\pi\frac{30}{180}}$
3rd harmonic reflection coefficient	$0.99\, e^{j\pi\frac{120}{180}}$	$0.99\, e^{j\pi\frac{270}{180}}$	$0.99\, e^{j\pi\frac{270}{180}}$

Table 4 Optimal source impedance

Frequency	650 MHz	850 MHz	1050 MHz
Fundamental impedance	1.282+j5.599	1.013+j3.481	0.892+j1.566
2nd harmonic reflection coefficient	$0.99\, e^{j\pi}$	$0.99\, e^{j\pi\frac{210}{180}}$	$0.99\, e^{j\pi\frac{210}{180}}$
3rd harmonic reflection coefficient	$0.99\, e^{j\pi}$	$0.99\, e^{j\pi\frac{210}{180}}$	$0.99\, e^{j\pi\frac{210}{180}}$

Table 5 Power and efficiency gotten from load pull impedances

Frequency	Power (dBm)	Efficiency (%)
650MHz	46.87	77.52
850MHz	46.55	87.71
1050MHz	46.69	85.05

3.3 Matching network design

The Simplified Real Frequency Technique (SRFT) can now be used to produce LC ladder elements that will yield a good match to this set of optimal impedances [14]. SRFT will maximize the Transducer Power Gain (TPG) of the matching network as a Figure of merit to minimize mismatch across the design bandwidth. Higher TPG, and therefore better matching, is more easily gotten if the impedances have a smaller spread, and are closer to the centre of the Smith chart. For this reason, it is only applied to the fundamental matching, and not the harmonics. Another reason SRFT is not used for harmonic matching is that they are not very sensitive to mismatches. Figure 3.4 shows the load-pull results at 1050 MHz where the second harmonic is kept reactive, with a reflection coefficient magnitude of 0.99, and the reflection coefficient angle is swept from 0 to 360 degrees. The angle of reflection coefficient for the third harmonic was fixed at 270 degrees during the sweep.

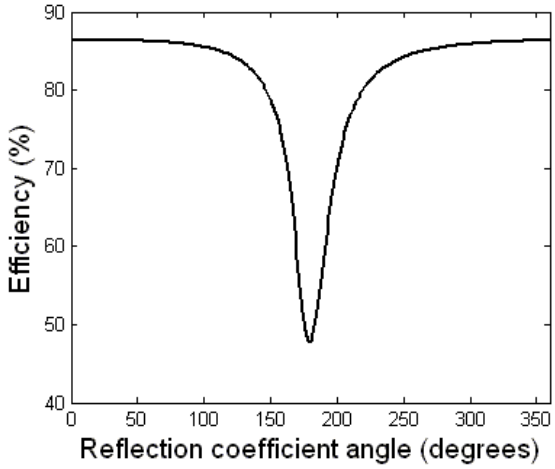


Figure 3.4 reflection coefficient angle versus drain efficiency for the second harmonic load

It shows that efficiency is insensitive to the second harmonic matching as long as it is not close to 180 degrees. The third harmonic had similar behavior, except the efficiency drop around 180 degrees is not as dramatic. The efficiency dropped only by 15% at 190 degrees reflection coefficient angle for the third harmonic. Load pulls at different frequencies showed similar behavior.

3.4 Matching network realization through stepped impedances

The SRFT method outputs a LC matching network, these L and C values can be realized with micro strip lines using the stepped impedance technique [15]. This method uses alternating sections of very high and very low characteristic impedance lines called stepped-impedance, or hi-Z, low-Z filters. They are comparatively easy to design, occupy less space compared to stubs, and has been proven to be effective for broadband matching networks [14]. The inductors and capacitors can be realized by short transmission lines, where $\beta\ell < \frac{\pi}{2}$, with the following electrical lengths

$$\beta\ell = \frac{LR_0}{Z_h} \qquad \beta\ell = \frac{CZ_l}{R_0} \tag{3.1}$$

where Z_h and Z_l are the high and low impedance transmission lines, R_0 is the filter impedance, $\beta\ell$ is the electrical length and the L and C are the normalized element values of the low-pass filter. With this we can implement the LC network given by SRFT with micro strip lines of the correct length and width for each section.

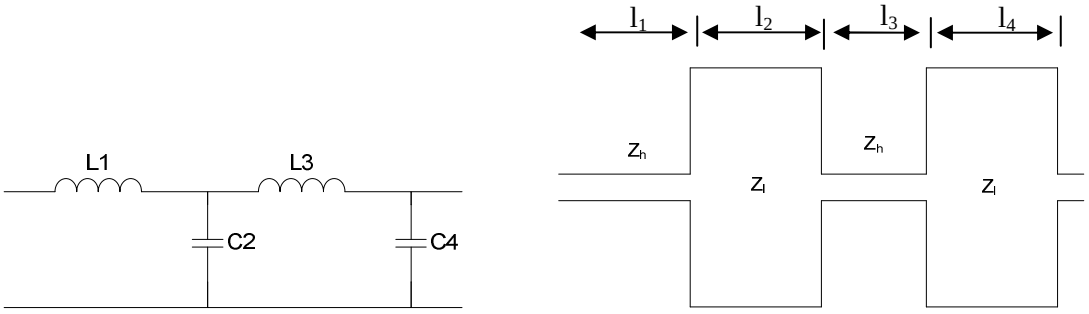


Figure 3.5 Stepped impedance implementation of LC network

3.5 Biasing

The DC bias for both the gate and the drain needs to be isolated from the RF path so that the DC sources and the coupling capacitors will not short out the RF signals. During load and source pull this was realized with an idea RF choke. This can be realistically implemented using quarter wave

transmission lines. The quarter wave transmission line will present an open circuit to the fundamental as well as odd order frequency components. However, for even harmonics, the same length of transmission line will appear as a half wave transmission line. So for even harmonics the biasing line will present a short circuit termination. This can be used to tune the even harmonics, namely the second harmonic in the matching network.

3.6 Stability

The stability of the amplifier can be analyzed using stability circles. Stability circles mark out the range of reflection coefficients looking towards the source impedance and reflection coefficient looking towards the load impedance that will give a magnitude of reflection coefficient looking into the PA at the source and load a value greater than one [15]. This range of values can produce a potentially unstable circuit due to the implication that there are negative real impedances at the input or output, and should be avoided.

3.7 Optimization

The LC network obtained from the SRFT technique and its realization through stepped impedances will have unavoidable mismatches due to the limitations of a physically realizable network. So it is important to adjust them during optimization for maximum efficiency and adequate power. The optimization proposed here tries to consider the shape of the load-pull efficiency contours. The efficiency and power contours are often shaped like the intersection of two circles with different radii as explained in [3] [16]. For an output power level of $P = \frac{P_{opt}}{p}$, with P_{opt} being the maximum power level, there exist two possible load values, $\frac{R_{opt}}{p}$ (R_{LO}) and pR_{opt} (R_{HI}), that produce the same power with reduced voltage swing, or current swing respectively at the output. Series reactance can also be added to R_{LO} without affecting the fundamental output power until a complex magnitude of R_{opt} is achieved, while shunt susceptance can be added to R_{HI} until a complex admittance magnitude of G_{opt} is gotten. The shape of the constant power contours therefore follow the curve for constant resistance, and conductance of

$$R = \frac{R_{opt}}{p}, \quad G = \frac{1}{pR_{opt}}. \tag{3.2}$$

The constant resistance and conductance circle intersects to forms the shape seen in the load and source pulls. This is illustrated in Figure 3.6.

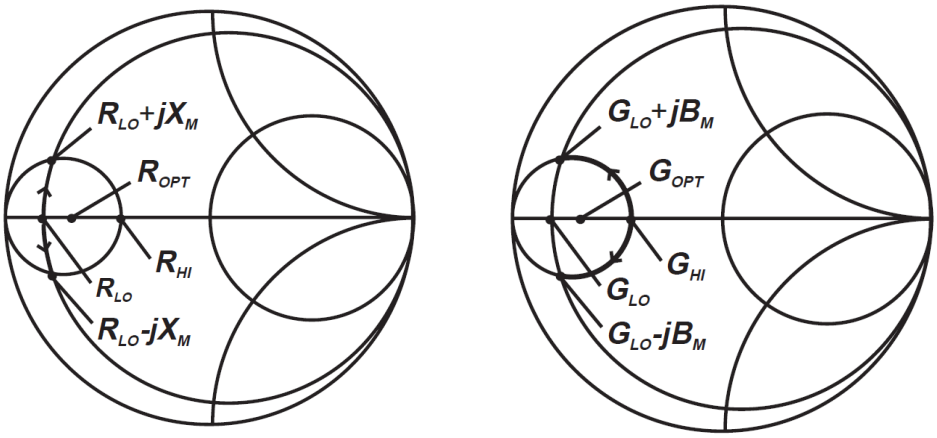


Figure 3.6 Constant power contour for -3dB [3]

The contours are then transformed by the package parasitic to different areas of the Smith chart for different frequencies. Because of the nature of their shape, and the transformation by the package parasitic, areas of clustered efficiency contours can emerge. At the same time, areas with sparse efficiency or power contours take form. So it is important to avoid these highly sensitive areas. For example, Figure 3.7 shows a matching network overlaid on top of the efficiency and power contours at 1050MHz. The black dot denotes the impedance of the matching network at 1050MHz given directly by the SRFT technique. It can be seen that the impedance at 1050MHz is now placed in an area of the Smith chart with dense efficiency contours. Should the impedance change during fabrication process or tuning process to the left, the efficiency of the PA would drop quickly as predicted by the dense concentration of PAE contours there. To counter this, tuning was done to place the impedances in a more insensitive area of the Smith chart. Mismatching below the optimal efficiency can lead to better power, with less efficiency loss.

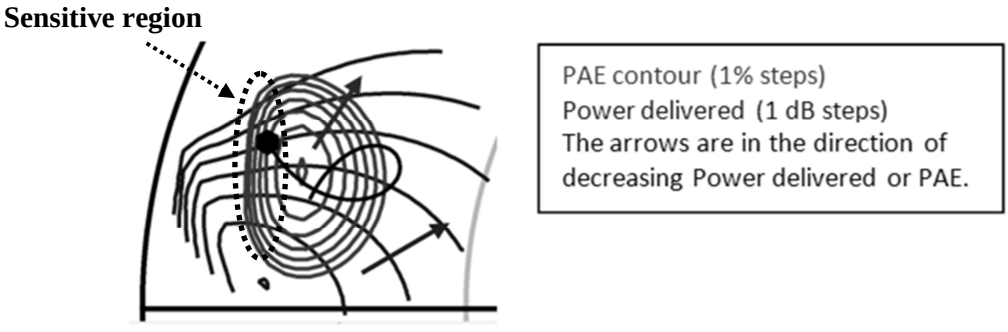


Figure 3.7 SRFT LC matching network load impedance for 1050MHz

As an illustration of this, Figure 3.8 shows the kind of tradeoffs face by a mismatch in each direction. Contours give us a good way to visualize the trade offs of each mismatch. The broad band matching network is different from narrow band matching because one cannot expect to match all the frequency impedance points found through load and source pull, and when designing with the mismatches, it is not just a matter of getting closest to the optimal impedance. It is possible to be closer to the optimal impedance, but still have lower efficiency and power. With the trade offs in mind however, better design decisions can be made when adjusting the broadband matching network.

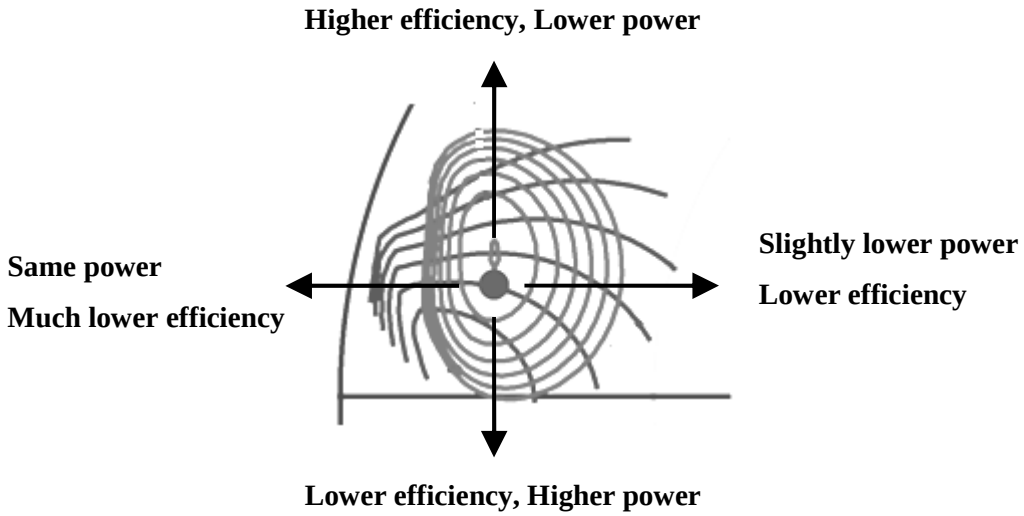
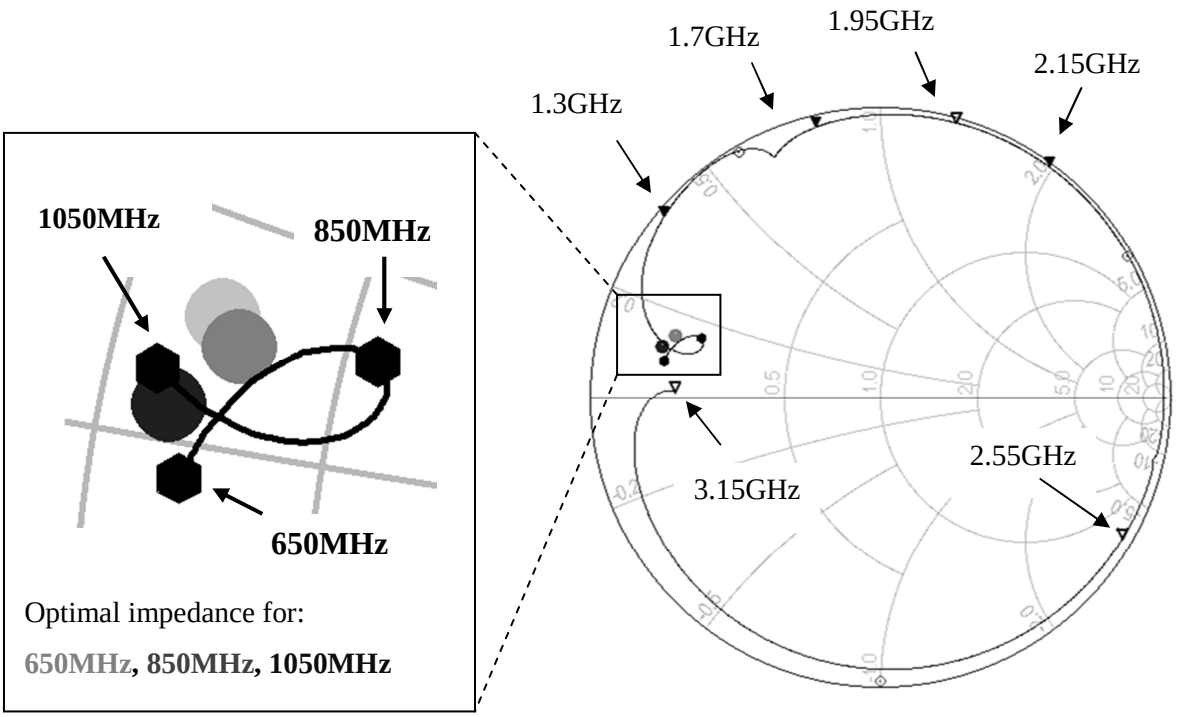
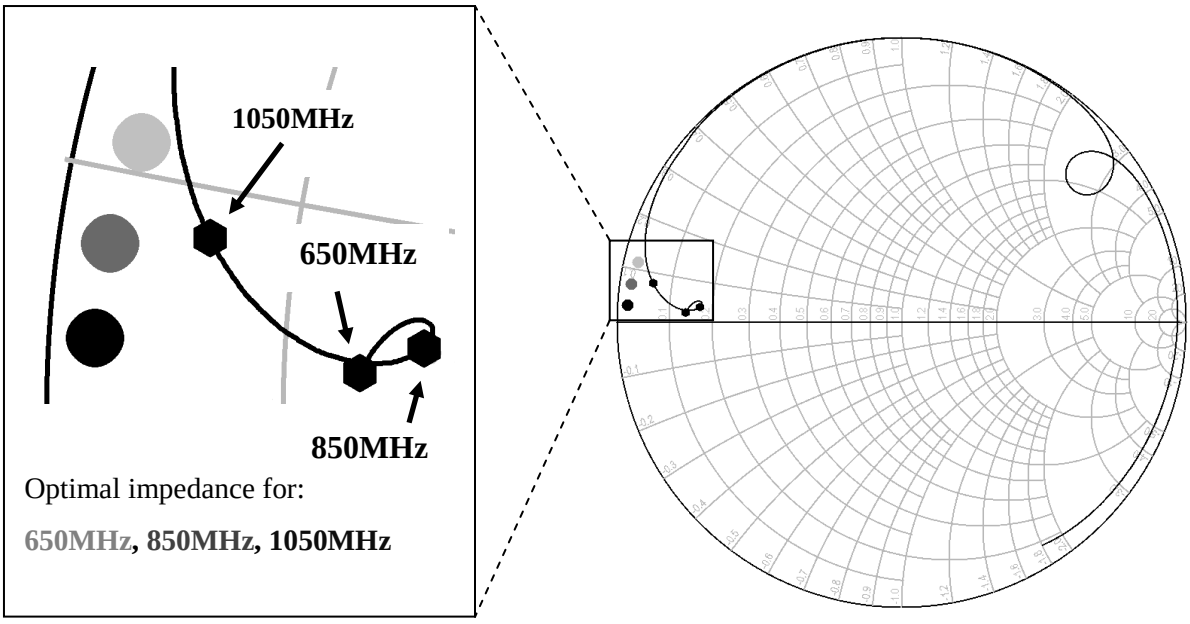


Figure 3.8 Tradeoffs efficiency and power contours for 1050MHz

3.8 Final matching

The final load and source matching network are shown in Figure 3.9. The realized and optimal impedances for 650 MHz, 850 MHz, and 1050 MHz are plotted for the source and the load, as well as the realized harmonic impedances for the load matching network. Few things should be noted about the final matching network. All the fundamental impedances have avoided the sensitive region. They are either mismatched to the right of the optimal impedance (850MHz), or below the optimal impedance (650MHz). The second and third harmonics were kept mostly reactive, on the edge of the Smith chart, and they were tuned to be away from 180 degrees. For impedance matching at the source, the resistance was purposely increase from its optimal value. This was in consideration of the stability of the circuit at the price of very little gain and efficiency deterioration.





(b)

Figure 3.9 Realized and optimal load (a) and source impedances (b)

3.9 Measurement results

The layout with the fabricated PA is shown in Figure 3.10. The input and output matching networks were fabricated on Rogers RT6006 high frequency laminates with 75 mils thickness.

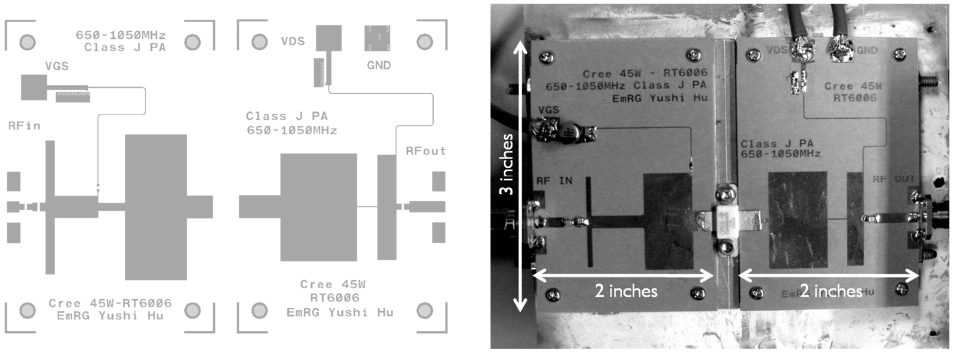


Figure 3.10. Layout and fabricated PA

DC power supplies were used to provide the drain and gate biases. A vector signal generator generated the continuous wave signal that was used in this test at each frequency. The output power was read by a power meter. The efficiency, gain, and output power can then be gotten. The measurement results are compared with the simulation results in Figure 3.11. From the measurement results, an average drain efficiency of 73.61%, average output power of 45.89dBm, and an average gain of 18.12dB was achieved between 650MHz and 1050MHz (48.42% bandwidth).

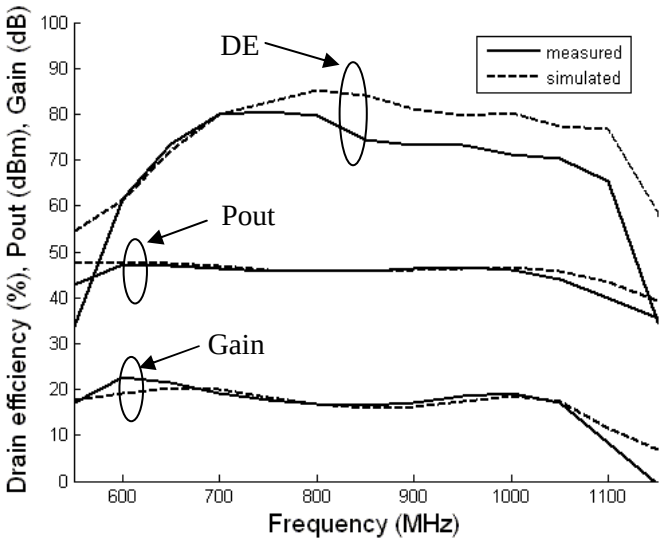


Figure 3.11 Measurement results vs. Simulation results

3.10 Performance with drain modulation

To get an idea of how this PA will perform in the envelope tracking system, the supply is manually adjusted with a single frequency continuous wave input at 800MHz, and the resulting efficiency and gain is plotted below in Figure 3.12. The envelope amplifier is assumed to be 100% efficient for this test. Gain is noticed to decrease as the supply voltage goes closer to the knee voltage of the transistor. This is something that can be avoided with envelope shaping, so that the drain supply no longer tracks the envelope at lower values. The PAE of the PA varies about 20% as the power is backed off by 13.5dB. Compare this with a 58.6% drop in PAE with a fixed supply.

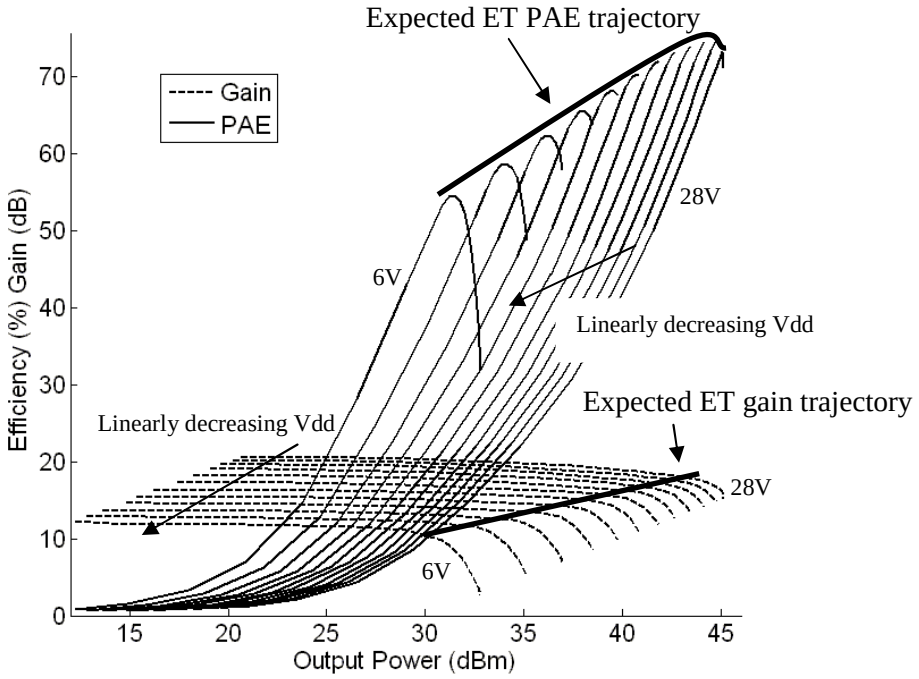
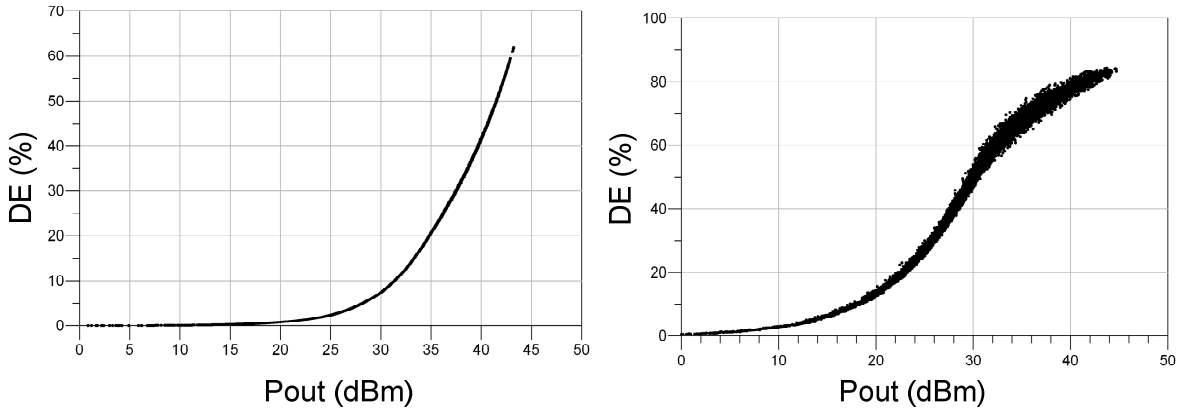


Figure 3.12 PA performance with varying drain bias

A LTE input signal is then simulated with the PA. The envelope is put through the PA with an ideal envelope amplifier with no losses or non-linearity. The signal has a PAPR of 9dB, and a bandwidth of 5MHz. The same input power was applied to the PA with and without envelope tracking. Here the envelope signal was just a linear scaling of the input voltage with a 1V offset added in. The results are given in table 6, and the instantaneous drain efficiencies are plotted in Figure 3.13.

Table 6 PA performance with and without drain modulation

	Without envelope tracking	**With drain modulation**
DE	20%	68.4%
EVM	3.591%	7.17%
Pout average	35dBm	34.9dBm
PAPR out	8.218dBm	9.85dBm
Gain	22.45dB	17.67dB



(a) (b)

Figure 3.13 Drain efficiency without (a) and with (b) drain modulation.

From this analysis, we can notice a few difference between the PA's performance with and without drain modulation. First the gain was reduced with drain modulation. This is expected since the PA is operating close to saturation at all power levels, and the gain of the PA drops as the drain bias comes closer to the knee voltage. This behavior was previously noticed in Figure 12. The Error Vector Magnitude (EVM) also degrades with envelope tracking. These shortcomings can be remedied through envelope shaping, and signal pre-distortion that is beyond the scope of this thesis. The benefit of drain modulation is its efficiency performance. It improved greatly from a fixed supply as expected. An improvement by almost 50% is achieved. Note however, that these efficiencies and results do not take into consideration the envelope amplifier. Its design will be looked at in the next chapter.

Chapter 4
Envelope Amplifier

As discussed in chapter 2, the efficiency of the envelope amplifier is critical to the efficiency of the overall ET system. At the same time though, it should maintain an acceptable level of signal fidelity, and have enough bandwidth to support the envelope signal of the particular standard. While linear regulators, such as the low-dropout regulator, provide excellent linearity and bandwidth at its output, its poor efficiency at low power makes it unsuitable for high PAPR signals. Switching regulators contrarily have excellent efficiency performance, but limited bandwidth and poor signal fidelity [17]. The most popular topology is actually a hybrid amplifier termed class K by its proposers [18]. The topology was originally meant for improving the fidelity of class D switching stage, but has since been adapted for the envelope amplifier [19]. Its combination of switching and linear amplifier makes for a good tradeoff between bandwidth, linearity and efficiency.

4.1 Operating principles

Its simplified schematic is shown in Figure 4.1. It can be seen as comprising of a switching stage and a linear stage. They work together in parallel with a hysteresis control scheme to deliver the envelope signal.

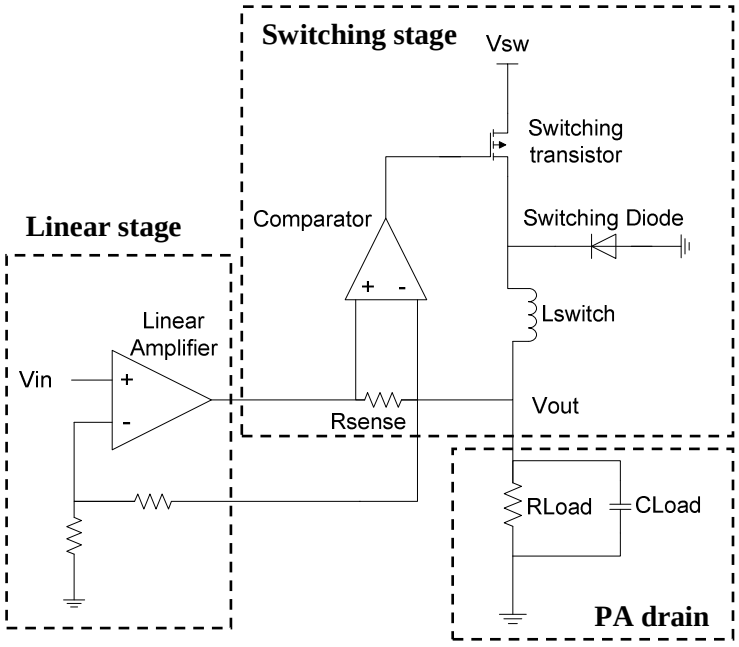
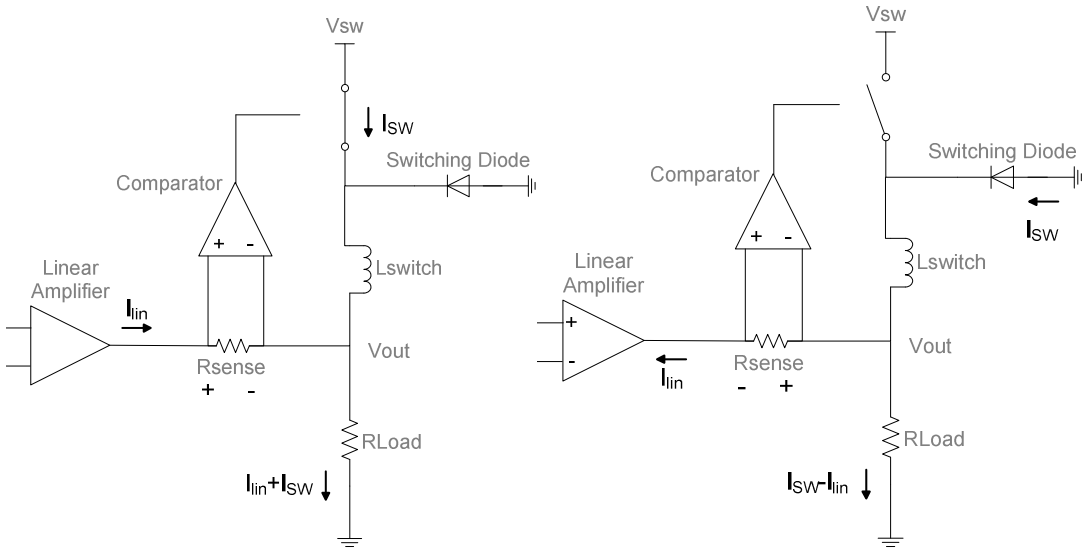


Figure 4.1. Simplified schematic for the hybrid envelope amplifier

The switching stage will efficiently supply most of the output power, since most of the power in the envelope is at low frequencies, while the linear stage will have a much higher bandwidth, and maintains the output signal integrity. The R_{load} and C_{load} here represent a simplified model of the drain of the PA. This model of the PA assumes that the envelope amplifier closely tracks the output envelope, and the value of R_{load} is dependent on the power level. To get a better idea of how the linear stage and the switching stage works together, the whole process can be roughly described with two states.

During state 1, a signal is input into linear amplifier so that it starts to supply current to R_{load}, causing a voltage to form across R_{sense}. This turns on the switching transistor, and a current starts to be drawn from the voltage source V_{switch} into the load through inductor L_{switch} until all of the current is now being supplied by the switching stage.

Once the current flowing through L_{switch} becomes greater than the output current, the amplifier goes into state 2 where the linear amplifier will start to sink current in order to maintain the correct output voltage. This creates a negative voltage across R_{sense} that causes the comparator to turn off, thus closing the switching transistor. The current through L_{switch} now comes from the switching diode, and starts to fall until it is below the actual output current. This whole process is repeated each period.



(a) (b)

Figure 4.2. Hybrid envelope amplifier topology's (a) state 1 and (b) state 2

In Figure 4.3, the current waveforms of the switching stage and the linear stage for a sine wave is plotted. With state 1 and 2 operation marked out. The slew rate of the switching currents will be given by

$$\frac{di}{dt} = \frac{v(t)}{L} \tag{4.1}$$

where $v(t)$ is the voltage across the inductor. When the switching transistor is turned on (state 1), the switching stage current will rise at a rate of $\frac{Vsw-Vout(t)}{L}$. When the switching transistor is turned off (state 2), the switching stage current will fall at a rate of $\frac{Vout(t)}{L}$. $Vout(t)$ is assumed to be constant at the average output voltage for both states. Because of this assumption, the switching stage current can be seen as linearly increasing and decreasing.

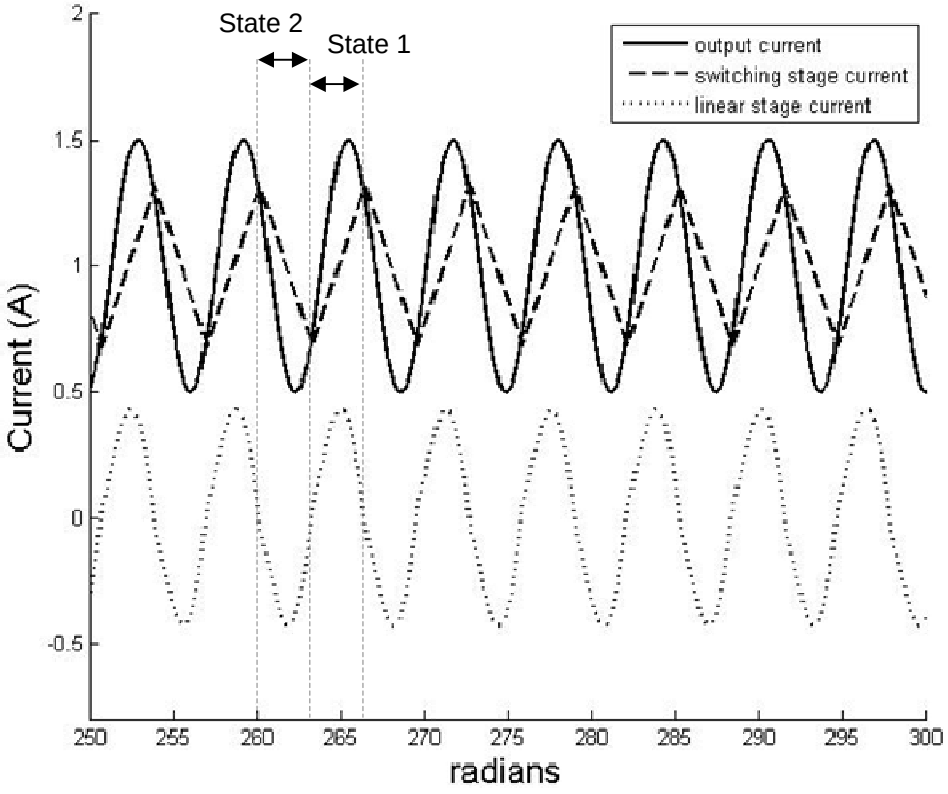


Figure 4.3. Current waveforms in the envelope amplifier

4.2 Optimization of The inductor

When the inductance is changed, the slew rate of the switching current is affected. The rise and falls rates will both change inversely. First the case when the slew rate of the switching stage is reduced will be looked at. To reduce the slew rate of the switching stage, the inductance value should be increased. Taking the same sine wave, and a much slower slew rate, the currents are plotted again in Figure 4.4. The switching current is now looking more and more like a DC current source. It is not able to track much of the output current's AC component, and more stress is put on the linear amplifier to compensate for this discrepancy. This is not desirable as the current coming from the linear stage is much less efficient, so one would want to minimize its contributions to the output current.

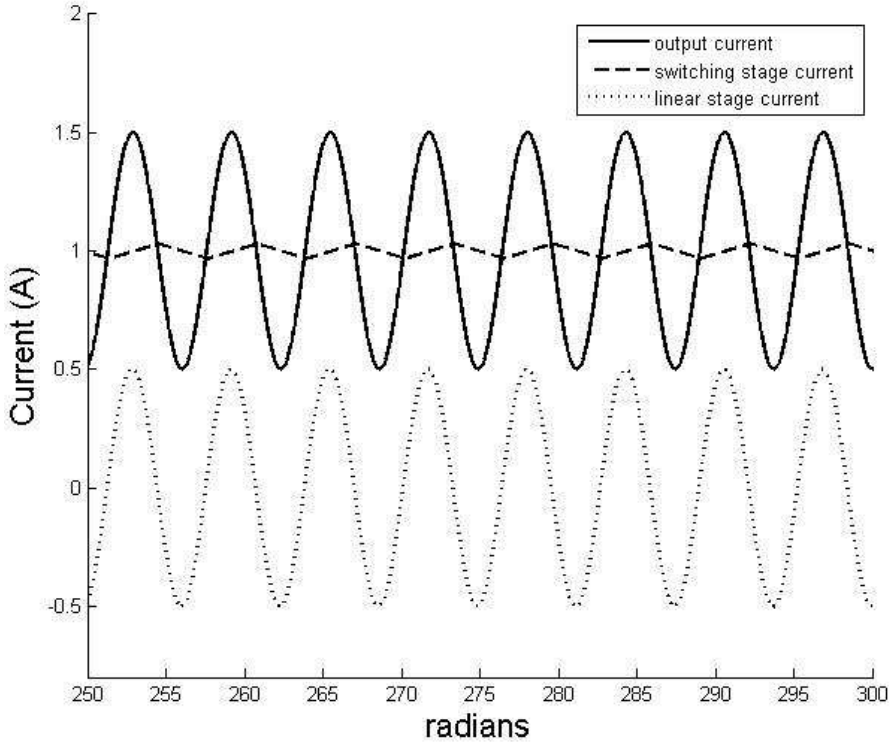


Figure 4.4. Envelope amplifier currents for low switching current slew rate

Note that for lower slew rates the switching frequency of the switching stage is the same as the frequency of the sine wave. However, once the slew rate of the switching stage surpasses the slew rate of the sine wave, the frequency of the switching stage increases as a function of both the slew rate and the hysteresis of the comparator. The current waveforms with a much faster switching

current slew rate are shown in Figure 4.5. The switching stage is now able to follow the output current wave forms more closely. The linear stage only has to supply a small amount of current to make up the difference between the switch and output currents. This comes with an increase in switching frequency. The switching transistor is now turning on and off at a rate much faster than the output sine wave. This can lead to an increase in switching losses.

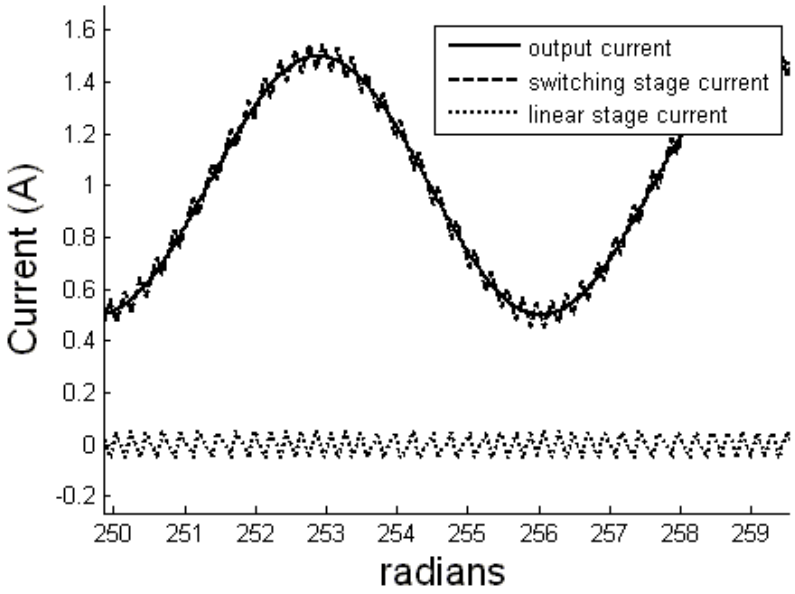


Figure 4.5. Envelope amplifier currents for high switching current slew rate

The analysis of this tradeoff has been looked at by Wang et al [8]. They have classified its operation in three cases shown in table 7. During one part of their analysis, the inductance was varied through the three distinct regions of operation. Changing the switching stage current's slew rate (I_{sw_SR}) and its value in relation to the output current's slew rate (I_{L_SR}). They showed that for best efficiency with a single tone input, a good starting value for the inductance would be the matched slew rate operation point. However, with the modulated signal test, an inductor that was four times larger than the matched slew rate inductance value was found to give the highest efficiency, putting the amplifier in large signal non-linear operating region.

Table 7 Operation modes with different slew rates

Operation modes	Condition	Description
Small signal linear operation	$I_{L\_SR} \ll I_{sw\_SR}$	Switching stage provides most of DC and AC output current, Linear stage filters out switching noise
Matched slew rate	$I_{L\_SR} = I_{sw\_SR}$	
Large signal non-linear operation	$I_{L\_SR} \gg I_{sw\_SR}$	Switching stage provides DC current, linear stage filters out switching noise, and provides most of the AC component of the signal

4.3 Optimizing the Hysteresis Value of the Comparator

The frequency of the switching stage will be a function of the hysteresis value of the comparator once the slew rate of the switching stage current is much higher than the slew rate of the output current. This is when the switching stage current follows closely the actually output current. The switching current will overshoot the output current by the amount of hysteresis in the comparator, and the amount of overshoot together with the slew rate of the fall and rise determines the frequency of the switching stage.

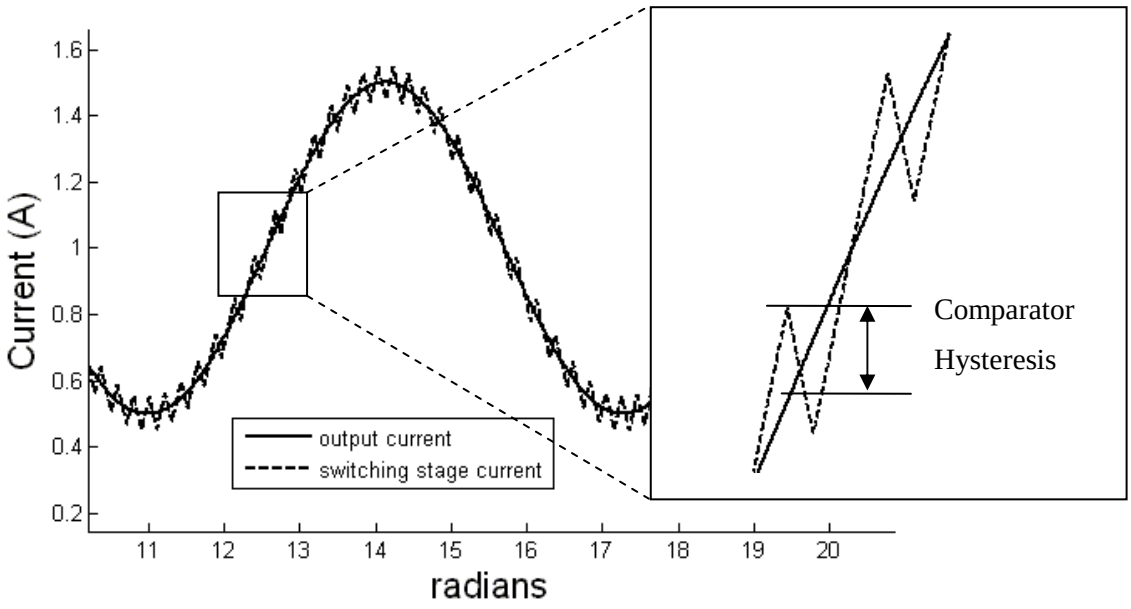


Figure 4.6 Switching stage current with high slew rates

The smaller the hysteresis of the comparator, the less difference between the switching stage current and the output current, thus less stress is placed on the linear stage to cancel the difference. However, we have gained this by increasing the switching frequency of the switching stage. Because of this trade off, there should be an optimal point to have the comparator hysteresis value. This type of analysis has been used to improve the efficiency of low bandwidth signals [20]. They have implemented a comparator with adjustable hysteresis to optimize for the best efficiency during small signal operation as described in table 7.

4.4 Optimizing the Switching Stage Supply Voltage

Generally, the switching stage supply voltage (V_{sw}) uses the same supply as the linear amplifier, but analysis will show that two major sources of loss that could be reduced by having a different value for V_{sw}. They are the conduction losses, and the switching losses. So it is proposed in this work that V_{sw} be looked at as a new parameter of optimization in the hybrid topology.

4.4.1 Conduction Losses

Based on the conduction angle of the switching transistor (Φ), Stauth and Sanders [21] in their analysis derived expressions for the optimum switching current as a function of the supply voltage, average output voltage, and dynamic characteristics of the envelope signal. Their work will be expanded upon in this thesis. All the calculations will be done assuming an input in the form of $v(t) = v_{dc} + A\cos(wt)$. It will also be assumed that the switching stage is a constant DC current source. This assumption is reasonable because the slew rate of the envelope current is usually much greater than the slew rate of the switching stage for high bandwidth signals. The switching cycle of the switching stage can separated into two periods for analysis. The first period is from 0 to Φ radians, and is the period when the switching transistor is conducting. The second period goes Φ to π radians, and is the period when the switching transistor is in cutoff operation. The two periods are illustrated with the current waveforms in Figure 4.7. Notice that only half a period is looked at due to the symmetry in its behavior.

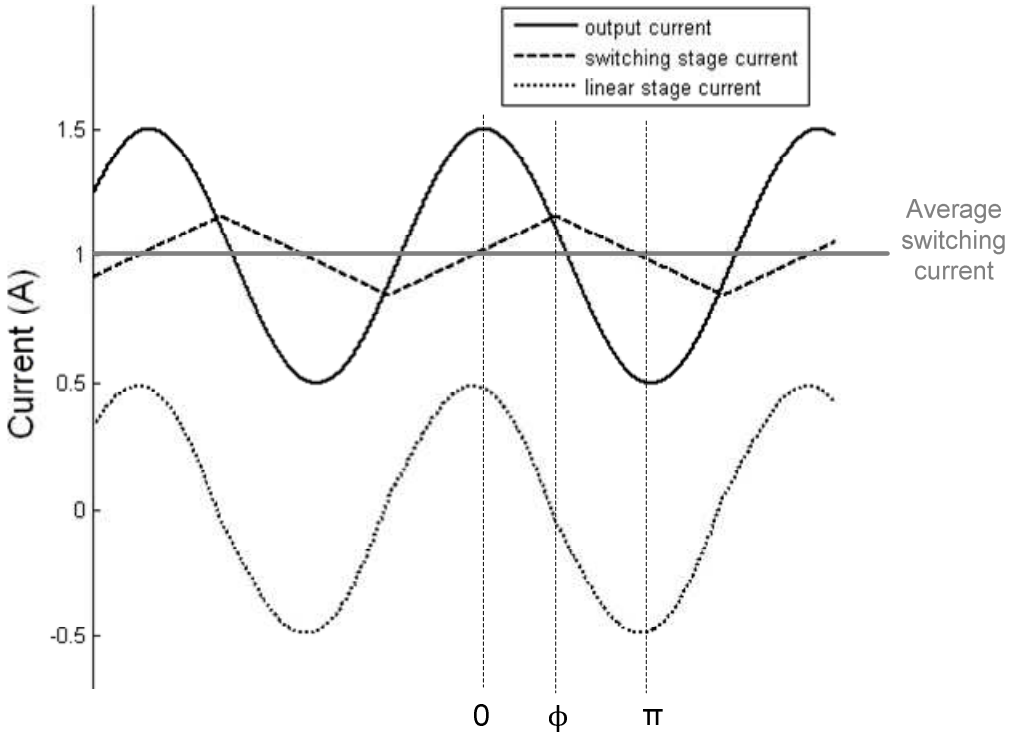


Figure 4.7 Conductance angle

The class AB output stage utilized by the linear stage amplifier is comprised of an NPN transistor that sources current to the output, and a PNP transistor that sinks current from the output. The simplified schematic of the class AB output stage is shown in Figure 4.8.

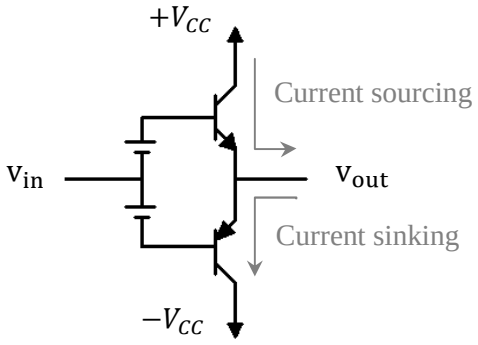


Figure 4.8. Simplified class AB output stage

During the first period, when the switching transistor is conducting, the output current at the load is higher than the average current supplied by the switching stage. So the NPN transistor has to source current to the output in order to maintain linearity. The conduction loss in the NPN transistor during the first period is given by

$$\frac{1}{\pi R_L}\int_0^{\Phi}(V_{DD}-v_{dc}-A\cos\theta)(A\cos\theta-A\cos\Phi)\,d\theta, \tag{4.2}$$

which is essentially the voltage across the NPN transistor multiplied by the current that it sources. After integration it becomes

$$\frac{1}{\pi R_L}\left[(V_{DD}-v_{dc})\sin\Phi A+\frac{A^2}{2}\left(-\Phi-\frac{\sin 2\Phi}{2}\right)-\Phi A\cos\Phi\,(V_{DD}-v_{dc})\ldots\right. \tag{4.3}$$
$$\left.+\sin\Phi A^2\cos\Phi\right].$$

During the second period, the output current at the load is lower than the DC current supplied by the switching stage, and the PNP transistor has to sink current to the output. The power loss during this period is given by

$$\frac{1}{\pi R_L}\int_{\Phi}^{\pi}(v_{dc}+A\cos\theta)(A\cos\Phi-A\cos\theta)d\theta. \tag{4.4}$$

It is essentially the voltage across the PNP transistor multiplied by the current that it sinks. After integration it becomes

$$\frac{1}{\pi R_L}\left[v_{dc}A\sin\Phi+(\pi-\Phi)v_{dc}A\cos\Phi-\sin\Phi\cos\Phi A^2\ldots\right. \tag{4.5}$$
$$\left.-\frac{1}{2}\left(\pi-\Phi-\frac{\sin 2\Phi}{2}\right)A^2\right].$$

If we add the losses for the two periods together, we get the total conduction loss for the class AB output stage over a period of the output signal. The expression is given as

$$P_{LIN}(\Phi)=\frac{1}{\pi R_L}\left(V_{DD}A\sin\Phi-V_{DD}A\Phi\cos\Phi+A\pi v_{dc}\cos\Phi-\frac{\pi A^2}{2}\right). \tag{4.6}$$

If only the losses in the class AB output stage were considered, then by differentiating equation 4.6 with respect to the conduction angle, we can find the optimal conduction angle for lowest loss with the derivative

$$\frac{dP(\Phi)}{d\Phi}=\frac{1}{\pi R_L}(-\pi A v_{dc}\sin\Phi+\Phi\sin\Phi A V_{DD}). \tag{4.7}$$

If we set this derivative equal to zero, we find that the optimal Φ is

$$\Phi^* = \pi \frac{V_{dc}}{V_{dd}}. \tag{4.8}$$

This result is similar to that found by Stauth and Sanders [22]. The analysis will now continue by looking at the conduction losses caused by components in the switching stage, starting with the loss of the switching inductor. While the ideal inductor is lossless, realistic inductor will have a DC series resistor associated with it. Here the loss due to the inductor can be estimated with

$$P_L(\Phi) = \frac{1}{\pi R_L^2} \int_0^{\pi} R_{ind} (A \cos \Phi + v_{dc})^2 \, d\theta \tag{4.9}$$

where R_{ind} is the series resistance associated with the non ideal inductor. It is squaring the average current through the inductor, and multiplying it with the inductor's series resistance. After integration it becomes

$$P_L(\Phi) = \frac{1}{R_L^2} R_{ind} (A \cos \Phi + v_{dc})^2. \tag{4.10}$$

The loss through the switching diode is also related to the conduction angle. This diode is only conducting when the switching transistor is off. This is the same as the period of time when the PNP transistor is sinking current. The loss through the diode can be estimated by

$$P_D(\Phi) = \int_{\theta_1}^{\pi} \left(\frac{\cos \Phi A + v_{dc}}{R_L} \right) V_{Diode} d\theta, \tag{4.11}$$

which becomes

$$P_D(\Phi) = (\pi - \theta_1) \left(\frac{\cos \Phi A + v_{dc}}{\pi R_L} \right) V_{Diode} \tag{4.12}$$

after integration. The final significant conduction loss to consider is the conduction loss through the $R_{DS\ (ON)}$ of the transistor. The average switching current is only flowing through the transistor when it is turned on during the conduction angle, and will produce a loss of

$$P_{RDS}(\Phi) = \int_0^{\theta_1} \left(\frac{\cos \Phi A + v_{dc}}{\pi R_L} \right)^2 R_{DS(ON)} d\theta, \tag{4.13}$$

which becomes

$$P_{RDS}(\Phi) = \frac{1}{\pi R_L^2} \theta_1 R_{DS(ON)} (A \cos \Phi + v_{dc})^2 \tag{4.14}$$

after integration. The losses can now be combined together, and plotted to see what the optimal Φ value is. The Matrix Laboratory (MATLAB) software is used, as differentiating and solving all the power loss equations by hand will be tedious. The particular case when $R_{DS(ON)} = 0.085\Omega$, $V_{DC} = 12V, V_{Diode} = 0.56, R_L = 15, R_{ind} = 0.07\Omega,$ and $A = 4V$ will be looked at. It is plotted in Figure 4.9. Diode losses and inductor losses are shown to decrease with increasing conduction angle, while the conduction loss from the switching transistor increases with conduction angle. However, the conduction loss from the AB output stage was the most significant source of conduction loss in this particular circuit. If the circuit components or input parameters were to change, the significance of each loss will be changed as well. The loss from the AB output stage was minimal around a conduction angle of 1.26 radians, while the total conduction loss was minimum around 1.36 radians.

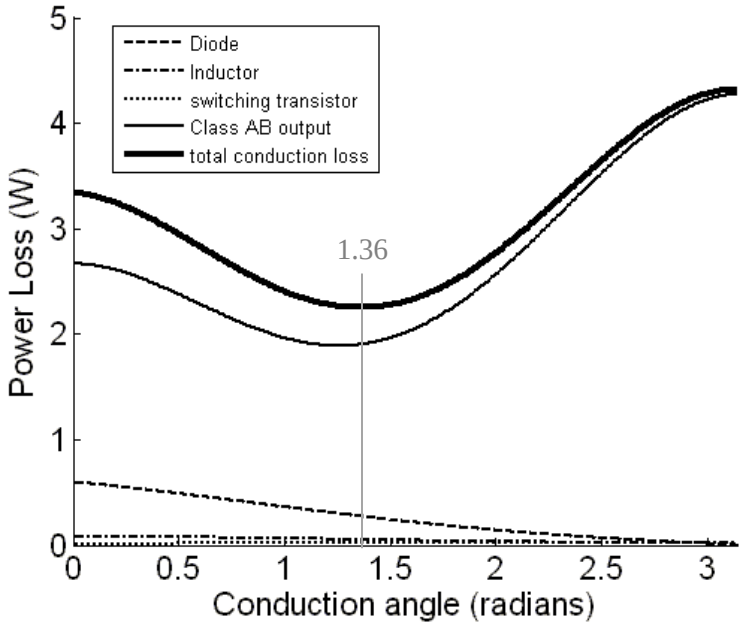


Figure 4.9 Conduction loss versus conduction angle

4.4.2 Actual Conduction Angle

After deriving the optimal conduction angle, the actual conduction angle (Φ) produced by the hysteresis control scheme should be found and compared. First a visual approach will be taken to get an idea of how the slew rates relate to the conduction angle. In Figure 4.10, it is shown that when the switching current slew rates for rise ($S_{Rrise)}$ and fall (SR_{fall}) are changed, the conduction angle and the average current from the switching stage changes. This forces the linear stage to either sink more current than source, or vice versa.

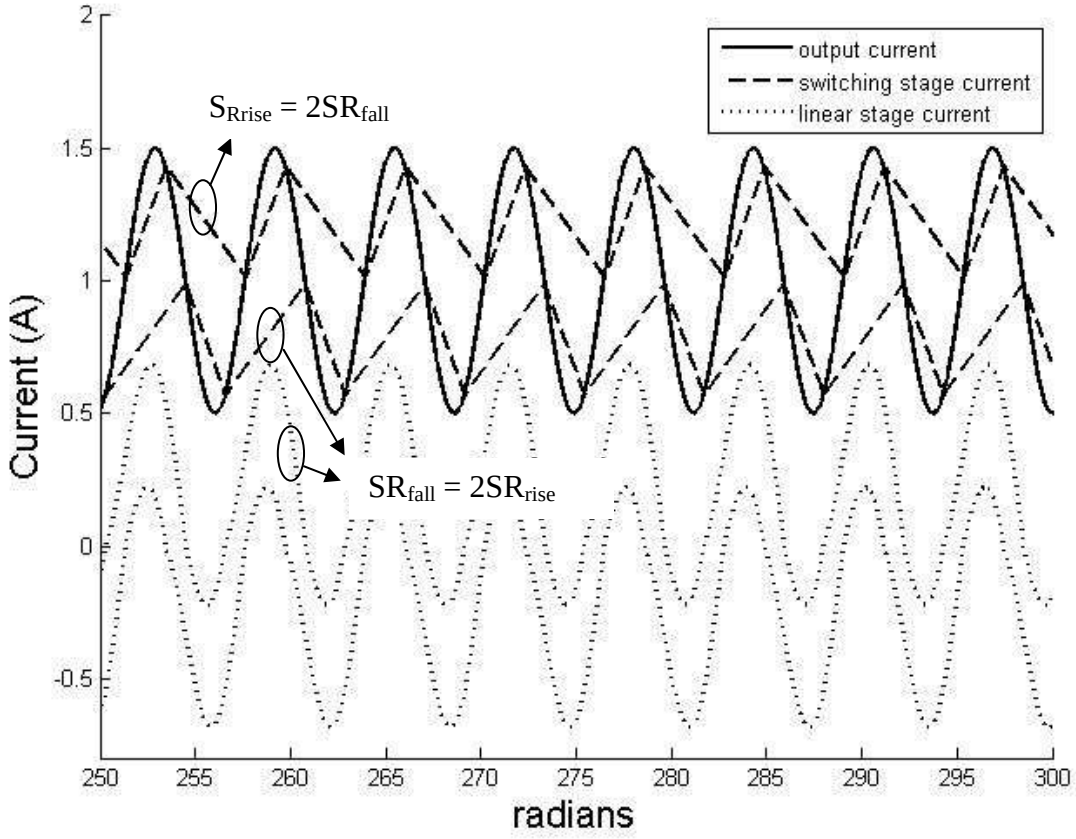


Figure 4.10 Currents for two different slew rate settings

For a more rigorous approach, the actual conduction angle will be numerically derived from the slew rates. The switching current and its important parameters are shown in Figure 4.11.

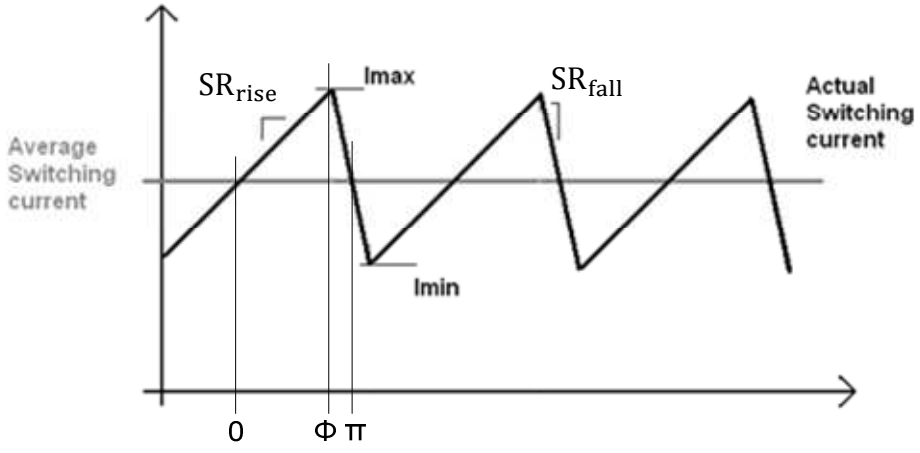


Figure 4.11 Switching current

The parameters can be related as

$$SR_{fall} = \frac{v_{fall}}{L} = \frac{Imax - Iaverage}{\pi - \Phi} \quad 4.15$$

for the falling switching current, and

$$SR_{rise} = \frac{v_{rise}}{L} = \frac{Imax - Iaverage}{\Phi} \quad 4.16$$

for the rising switching current. By dividing equation 4.16 by 4.15, Φ is found to be directly related to v_{fall}, the voltage across the switching inductor when the switching transistor is off, and v_{rise}, the voltage across the switching inductor when the transistor is on as

$$\frac{\Phi}{\pi} = \frac{v_{fall}}{v_{fall} + v_{rise}}. \quad 4.17$$

Where v_{fall} is

$$v_{fall} = v_{dc} - \frac{A}{(\pi - \Phi)} \sin\Phi \quad 4.18$$

and v_{rise} is

$$v_{rise} = V_{SW} - \frac{A}{\Phi} \sin\Phi - v_{dc}. \quad 4.19$$

Substituting equations 4.18, and 4.19 into equation 4.17 gives

$$\frac{\Phi}{\pi} = \frac{v_{dc} - \frac{A}{(\pi - \Phi)} \sin\Phi}{V_{SW} - \frac{A}{\Phi} \sin\Phi - \frac{A}{(\pi - \Phi)} \sin\Phi} \quad 4.20$$

which becomes

$$\frac{\Phi}{\pi} = \frac{v_{dc}}{V_{SW}} \quad 4.21$$

after simplification. Note that in order to maintain this kind of relationship, V_{SW} must not be lower than v_{dc}. Also, recall from equation 4.8 that this is the optimal conductance angle for the class AB output stage. So the hysteresis control method with V_{SW} the same as the linear stage supply voltage automatically gives the optimal conductance angle for the least loss in the class AB output stage.

4.4.3 Control of conductance angle

From the analysis done with the optimal and actual conductance angle, it was concluded that the envelope amplifier's control system is not able to provide the optimal conduction angle for the lowest power loss. This makes some kind of control of the conduction angle beneficial to the overall efficiency of the system. In the last section, we listed out the equation for actual conduction angle in equation 4.21. One of the variable in that equation, which is not set by the input signal, is V_{SW}. This is the supply of the switching stage, and it's a parameter that the designer can have some freedom with. In Figure 4.12, the change in conduction angle is plotted against the V_{SW} value, and the conduction angle eventually intersects the optimal conduction angle at around 27.7V for this particular setup.

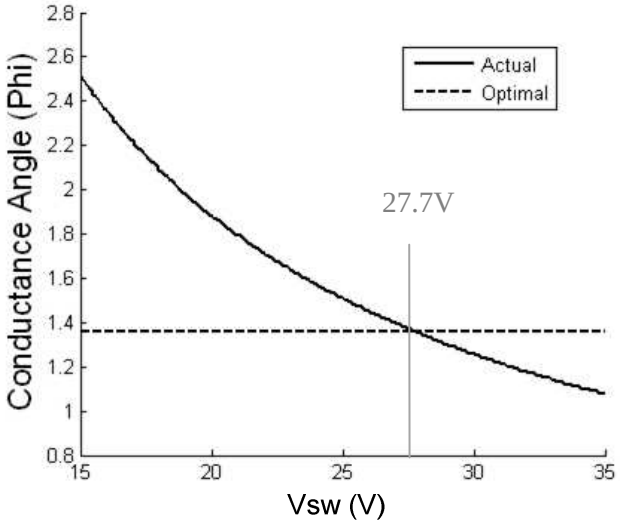


Figure 4.12 Actual and optimal conductance angle vs. V_{SW}

4.4.4 Switching Losses

The second significant source of loss that can be reduced by the setting of V_{SW} is the switching losses from the switching transistor. The switching stage used is a buck converter, and the analysis of the buck converter switching losses will be taken from Erickson [22]. A simplified schematic of the buck converter is shown in Figure 4.13. The diode is kept ideal, and only the switching times of the transistor are considered.

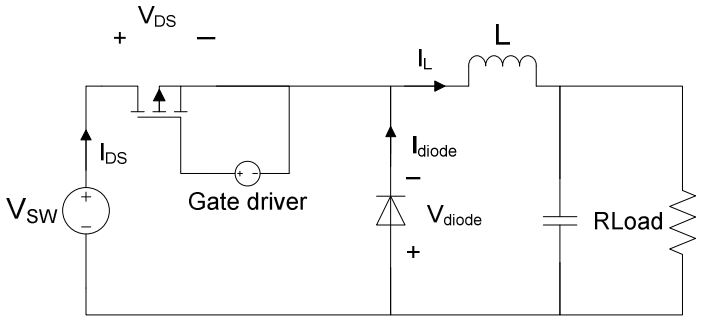


Figure 4.13 Simplified buck converter

The transistor turn-off waveform of the switching transistor is plotted in Figure 4.14. The switching transition time is assumed to be short so that i_L stays constant.

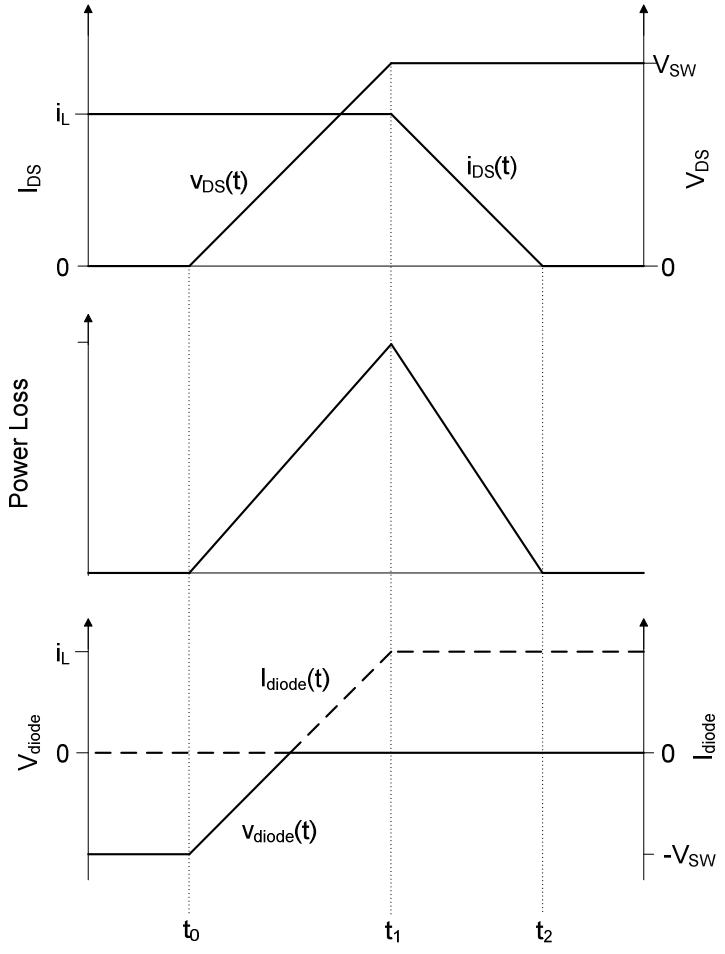


Figure 4.14 Transistor turn-off transition for a buck converter, reproduced from [21]

From t_0 to t_1, the gate driver charges the transistor's gate to drain capacitance. At time t_1 the diode becomes forward biased, and the flow of i_L starts to shift from the diode to the transistor. From t_1 to t_2 the gate driver discharges the transistor's gate to source capacitance, thus turning off the transistor. The total energy loss during the turn off transition can be found by integrating the instantaneous power to get

$$W_{off} = \int i_{DS}(t)v_{DS}(t) = \frac{1}{2}V_{SW}i_L(t_2 - t_0). \quad 4.22$$

The turn on transition for the transistor will lead to the same loss as the turn off transition, but will be dependent upon the turn on time instead of turn off time of the transistor. The average power loss from the turn on and turn off transition behavior will be

$$P_{SW} = \frac{1}{T_s}\int i_{DS}(t)v_{DS}(t) = \frac{1}{2}V_{SW}i_L(t_{off} + t_{on})f. \quad 4.23$$

Notice that the average power loss will be a function of frequency, but it is also be a function of V_{SW} and i_L, with i_L a function of V_{SW}. For the output signal $v(t) = v_{dc} + A\cos(wt)$,

$$i_L = \frac{1}{R_L}\left(A\cos\left(\frac{v_{dc}\pi}{V_{SW}}\right) + v_{dc}\right). \quad 4.24$$

The loss cause by the output capacitance of the switching transistor is another common source of loss. During turn on, the energy stored in C_{DS} and C_j of the diode are dissipated by the transistor, thus adding up to a loss of

$$P_C = \frac{1}{2}(C_{DS}+C_j)V_{SW}{}^2 f. \quad 4.25$$

The important thing to realize from the switching losses analyzed so far is that they are a function of V_{SW}. The switching losses can now be estimated for the particular signal we are looking at versus frequency. The time delays were gotten from the datasheet for the transistor used (ZXMN10A09K from ZETEK).

Table 8 Parameters for ZXMN10A09K transistor

Parameter	Value
Turn-on delay time	6.8ns
Rise time	5.3ns
Turn-off delay time	27.5ns
Fall time	12.3ns
Output capacitance	83pF

The capacitance of the diode used was 100pF. Equation 4.23 and 4.25 was solved and added together with $R_L = 15, v_{dc} = 12, A = 4, f = 1MHz$. To confirm this, SPICE models for the buck converter transistor, diode, and inductor were used in ADS software to plot out the relationship between switching losses and V_{SW}. The loss across the switching transistor can be found by multiplying the voltage across the transistor with the current through the transistor. This loss will also include the conduction loss of the transistor as well. The delay times for calculations are adjusted so that they fit well with simulated results. The calculated and simulated switching losses are plotted in Figure 4.15.

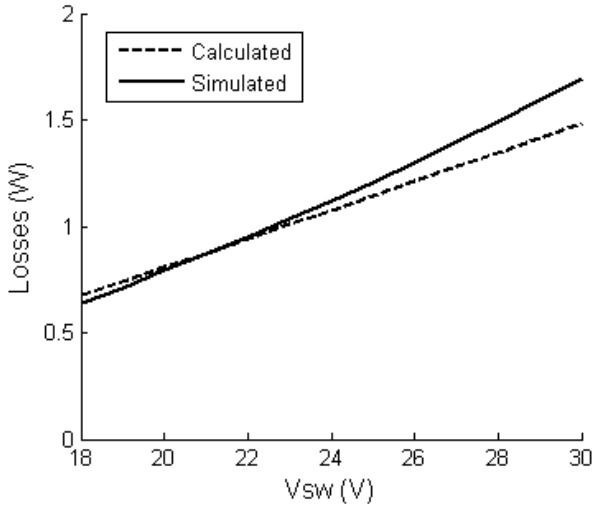


Figure 4.15 calculated versus simulation switching losses

Note that there are other sources of switching loss not considered here. Including the extra switching loss caused by the diode's reverse recovery charge when the switching transistor turns on. This can also lead to ringing with series parasitic capacitances and inductances. However, the diode's reverse recovery charge can be reduced to a negligible amount by using a Schottky diode, which has a very small reverse recovery time.

4.4.5 Combined losses

The conduction losses, as well as the switching losses can now be combined to find a combined power loss as

$$P_{combined} = P_{SW} + P_C + P_{LIN} + P_{diode} + P_L + P_{RDS}. \quad 4.26$$

First the conduction, switching loss, and the combination of the two versus V_{SW} will be looked for a cosine output $v(t) = 12 + 4\cos(2\pi ft)$ where $f = 1MHz$.

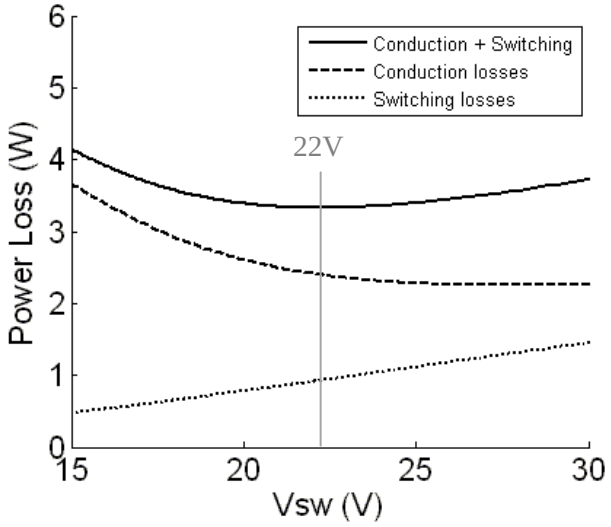


Figure 4.16 Conduction and Switching losses verse Vsw

While the conduction loss is minimum at one point, the switching loss decreases with V_{SW}. They combine together to reveal an optimal V_{SW} (V_{SW}^{*}) of 22V for minimum loss. This result will be confirmed through simulation as well as measurements. A more detailed schematic of the envelope amplifier is given in Figure 4.17.

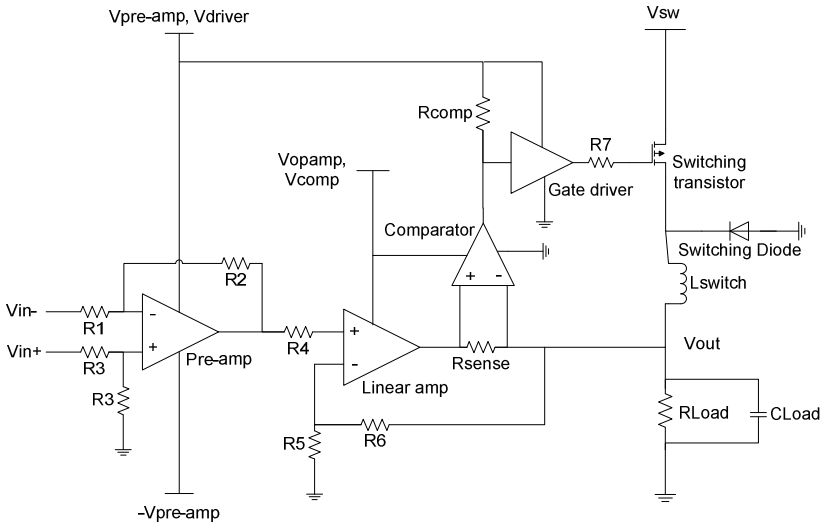


Figure 4.17 Envelope amplifier schematic

The simulation was carried through using the ADS software. Simulation Program with Integrated Circuit Emphasis (SPICE) models were used for each component, with the exception of the gate drive, which is ideally modeled with a voltage controlled voltage source with its expected delay and parasitic. A proof of concept prototype of the envelope amplifier was fabricated using FR4 printed circuit board and discrete components. The efficiency results from simulation and measurement of the fabricated envelope amplifier for an input of $v(t) = 12 + 4\cos(2\pi(1\text{MHz})t)$ are plotted in Figure 4.18. The simulated values follow closely the measurement results. The efficiency improved by 3.4% as V_{SW} was decreased from 30V to 20V. With a good agreement between simulation and measurements, the V_{SW}^{*} can then be analyzed versus amplitude, average output voltage, and frequency.

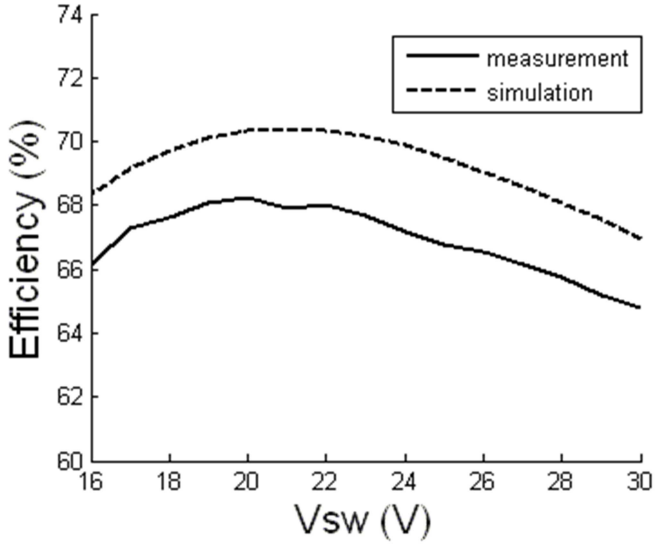


Figure 4.18 Efficiency versus switching stage supply

4.4.6 V_{SW}^{*} versus output signal amplitude

V_{SW}^{*} for lowest loss is plotted versus the amplitude of the output cosine wave in Figure 4.19. The line traces the calculated V_{SW}^{*}, while the asterisk dots are V_{SW}^{*} values gotten from simulation. A good correlation was noticed between the two, confirming calculation results.

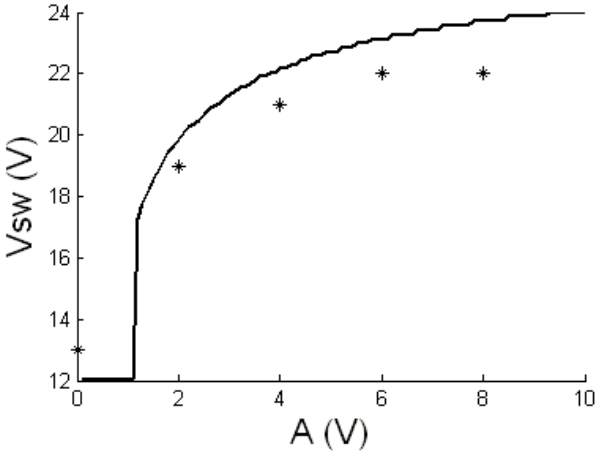
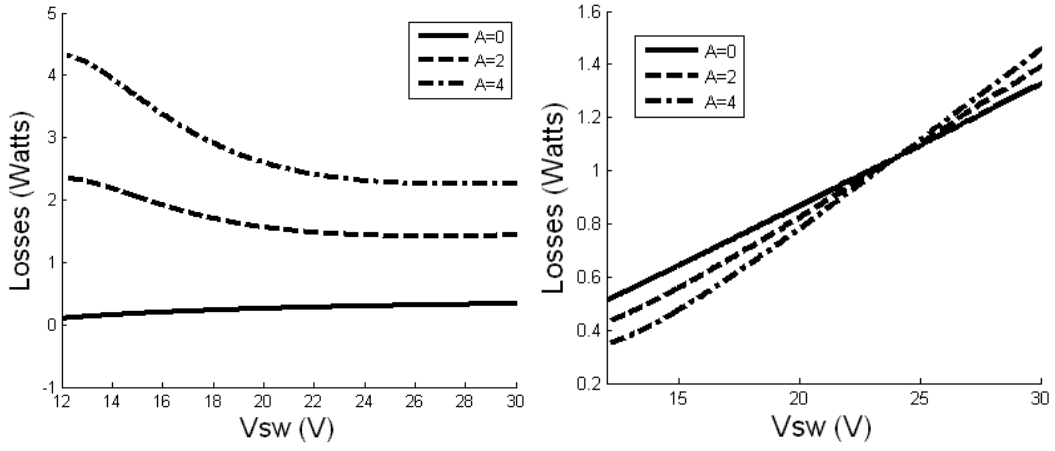
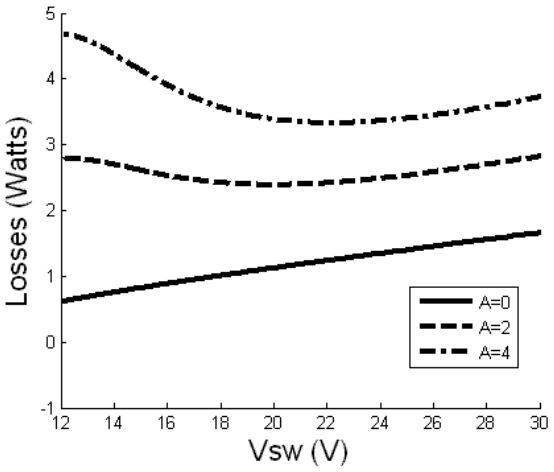


Figure 4.19 V_{SW}^{*} versus amplitude

The trend of V_{SW}^{*} versus amplitude can be explained using the change in conduction loss of the AB output stage. Recall that this analysis has assumed reasonably the switching stage to be a DC current source, while the linear stage supplies some DC and all of the AC output current. If the AC component of the output signal is decreased, less stress will be placed on the inefficient linear amplifier. This leads to a reduction of conduction loss, and the switching losses will become a more significant part of the total power loss. This also means that it will have more of an effect on V_{SW}^{*}. The total conduction loss and the total switching loss are plotted in Figure 4.20 to prove this point. Total conduction loss is shown to decreasing with output amplitude, while the switching stage losses remain almost constants with output amplitude. As the output amplitude decreases, the trend of the combination of these two losses will become more dominated by behavior of the switching loss.





(c)

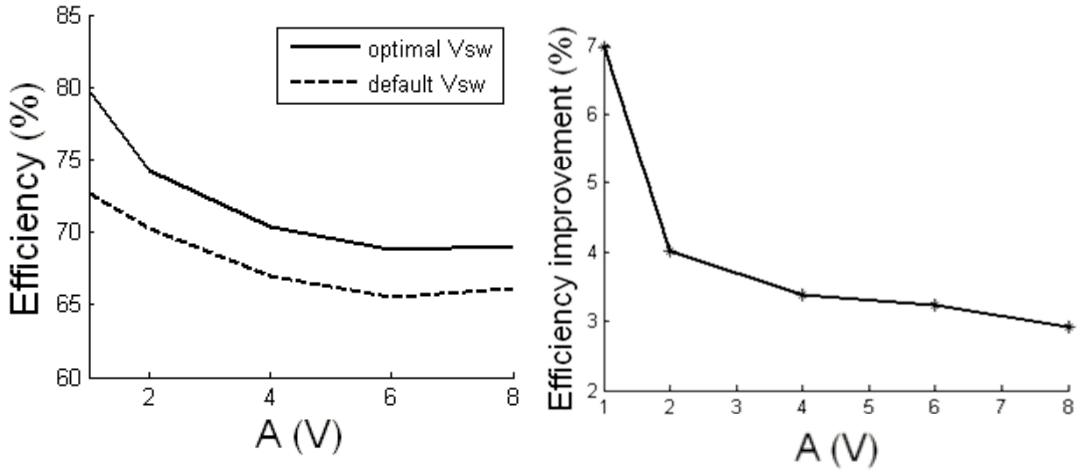
Figure 4.20 Total conduction losses (a), total switching losses (b) and the two combined (c) versus V_{SW} for different output amplitudes

The behavior of conduction and switching losses can be separated into two modes of operation. As V_{SW} is lowered, the combined switching and conduction losses could behave in a way where it first decreases and then increases, leaving a point of minimum loss at the transition. The transition point would determine V_{SW}^*. This type of behavior happens if the rate of increase in total conduction loss becomes greater than the rate of decrease in total switching loss at lower V_{SW} values. This will be called mode 1 operation. The combined loss could also continue to decrease with V_{SW} without increasing at lower V_{SW} values. This happens when the rate of increase in total conduction loss is always lower than the rate of decrease in total switching loss. In this mode the overall trend of the combined loss will be mostly determined by the switching losses. This type of loss behavior will be called mode 2 operation. In mode 2 operation, V_{SW}^* would equal v_{dc}, the minimum V_{SW} allowed. The two modes are summarized in table 9.

Table 9 Modes of loss behavior

Mode	**Condition**	**V_{SW}^***
1	V_{SW}^* is determined by the point where the rate of increase in conduction losses equals the rate of decrease in switching losses.	$> v_{dc}$
2	V_{SW}^* is determined by the point of minimum switching losses.	v_{dc}

In Figure 4.20, when the amplitude is less than 1V, V_{SW}^{*} is kept constant at v_{dc}, and is displaying mode 2 behavior. After the amplitude goes above 1V, V_{SW}^{*} starts to change, and is now operating under mode 1. The efficiency gained with changing from default V_{Sw} to V_{SW}^{*} is plotted in Figure 4.21. There are greater benefits for reducing V_{Sw} when the amplitude is at a low value.



4.21 Simulated efficiency of envelope amplifier versus amplitude under (a) default Vsw setting and V_{sw}^{*} setting with the (b) efficiency improvements from this optimization

4.4.7 V_{SW}^{*} versus average output voltage

V_{SW}^{*} versus v_{dc} is plotted in Figure 4.22. The line traces the calculated V_{SW}^{*}, while the asterisk dots are V_{SW}^{*} values gotten from simulation. Again, a good correlation was noticed between the two.

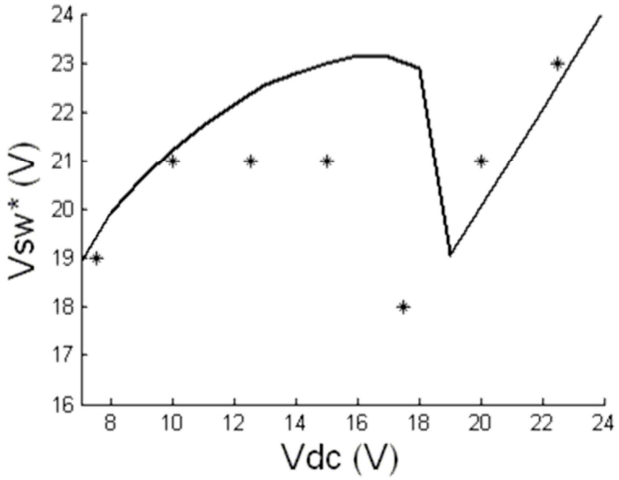


Figure 4.22 V_{SW}^{*} versus output average voltage

Once v_{dc} reaches 19V, V_{SW}^{*} dips down to follow the actual v_{dc} value. This is the point where the losses go from mode 1 behavior into mode 2 behavior. To confirm this change in operation mode, the losses versus V_{SW} is looked at in Figure 4.23 for the v_{dc} output values of 10, 15, and 20V. When v_{dc} is equal to 10V, the change in conduction loss at low V_{SW} is high, and the combined loss is a function of changes in both switching and conduction losses. It is now under mode 1 operation. However, for a v_{dc} of 20V, the rate of increase in total conduction loss is small at low V_{SW} values, and the combined loss is mostly determined by switching losses. The circuit is now operating under mode 2, where the V_{SW}^{*} is equal to v_{dc}.

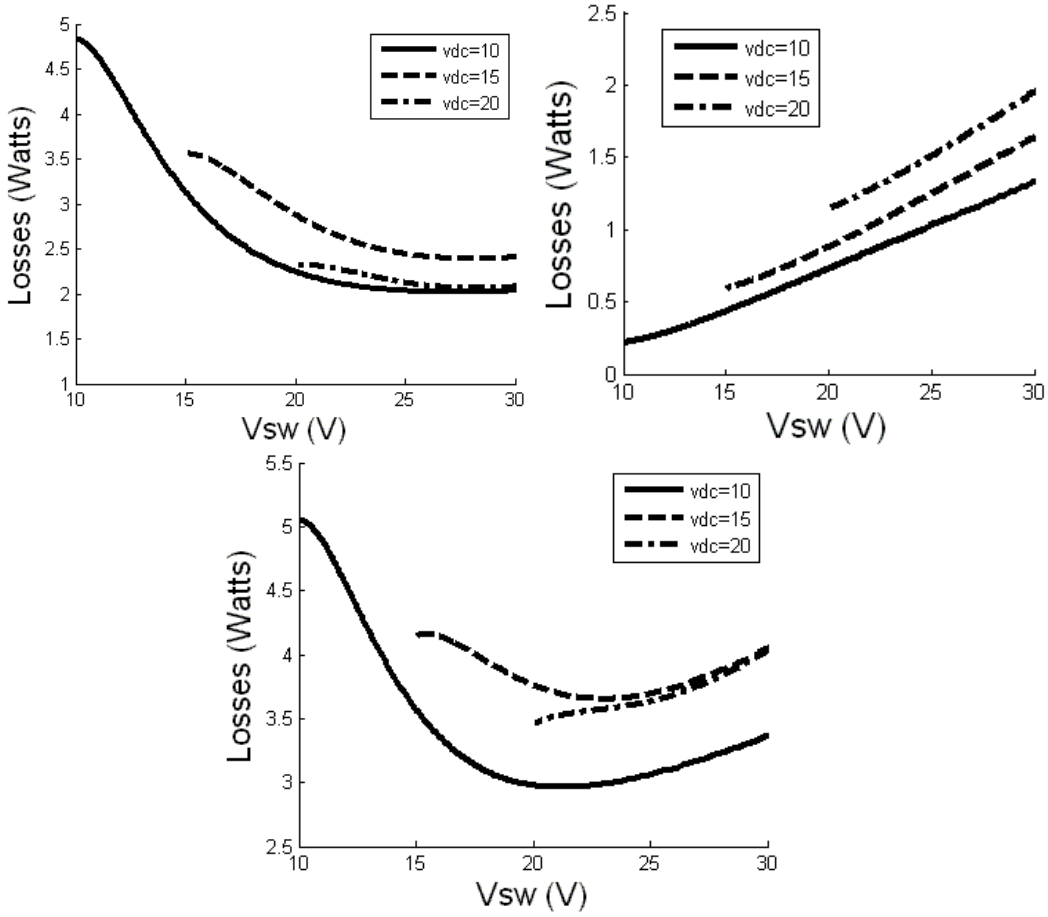
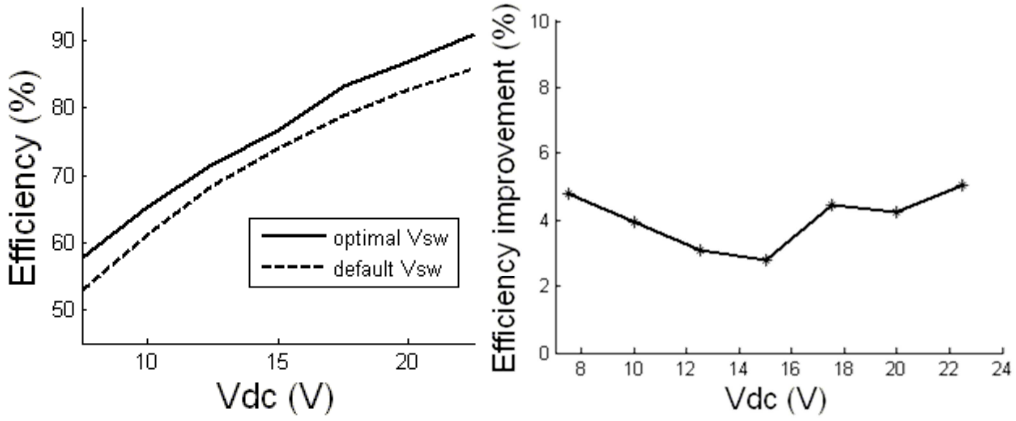


Figure 4.23 (a) Total conduction loss and (b) total switching losses and (c) the two combined versus V_{SW} for different output average voltages

The efficiency benefits of changing from default V_{Sw} to V_{SW}^{*} versus average output voltage is plotted in Figure 4.24. There is an almost constant improvement in efficiency with varying average output voltage.



4.24 Simulated efficiency of envelope amplifier versus average output voltage under (a) default Vsw setting and V_{sw}^{*} setting with the (b) efficiency improvements from this optimization

4.4.8 Optimal switching stage supply versus switching frequency

The switching losses in the switching stage are linearly related to the switching frequency. An increase in total switching loss makes it a more dominant determinant of V_{sw}^{*}, and since total switching loss decreases with V_{sw}, V_{sw}^{*} will decrease with increasing switching frequency. In Figure 4.25, the V_{SW}^{*} values gotten from simulation are plotted. The behavior of V_{sw}^{*} will go from mode 1 into mode 2 at around 2 to 2.5MHz for this particular circuit.

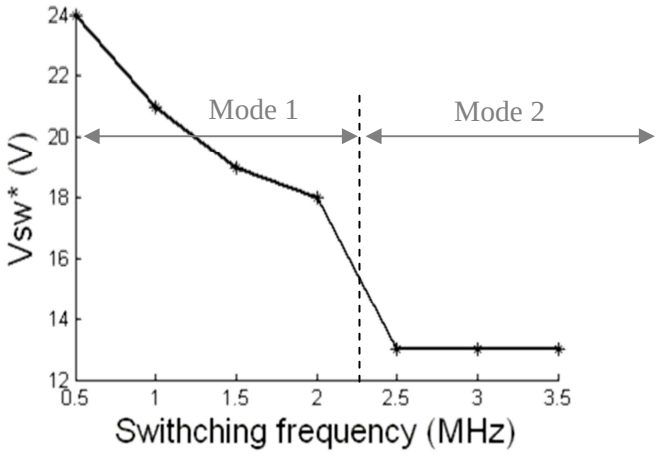
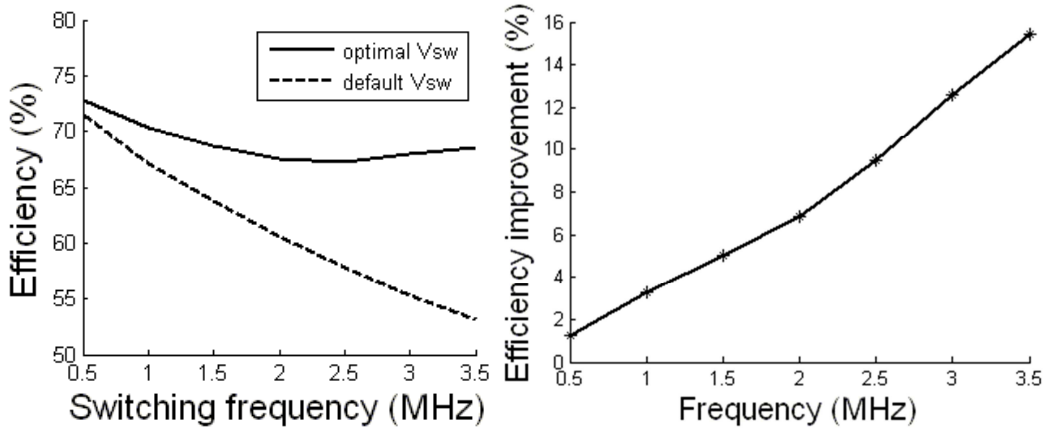


Figure 4.25 V_{sw}^{*} versus output switching frequency

The efficiency benefits of changing from default V_{Sw} to V_{SW}^{*} versus switching frequency is plotted in Figure 4.27. There are greater benefits for reducing V_{Sw} when the switching frequency is at a high value.



4.26 Simulated efficiency of envelope amplifier versus switching frequency under (a) default Vsw setting and V_{sw}^{*} setting with the (b) efficiency improvements from this optimization

The above analysis done for how V_{sw}^{*} changes with amplitude, average output voltage, as well as switching frequency suggests that there is a unique V_{sw}^{*} for every type of input signal.

4.4.9 Modulated signal test

This technique of adjusting V_{sw} to its optimal value is also tried on a more realistic modulated signal to see if the same technique can be applied on modulated signals. The envelope amplifier was tested with the envelope of a 5MHz LTE signal at 6.4dB back-off operation. The average output power was 41.5dB, and a gain of around 33dB was measured. As V_{sw} is varied from 30V down to 16V we see the efficiency improve by roughly 3.2% for a final efficiency of 74.6%.

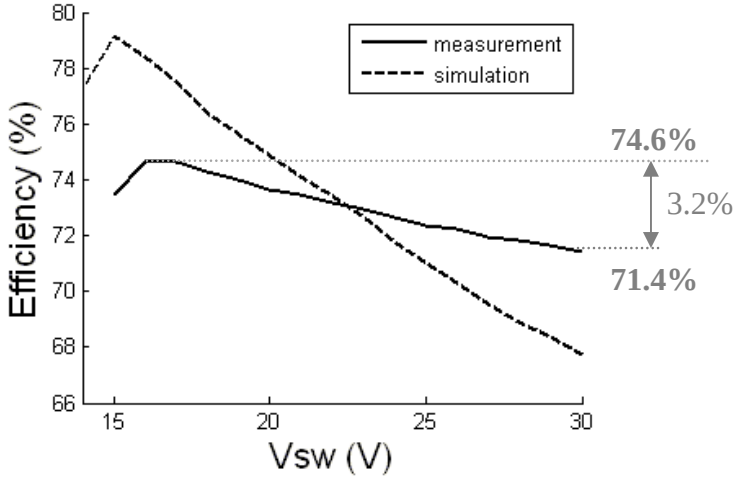


Figure 4.27 Efficiency versus V_{sw} for an LTE 5MHz signal

Chapter 5
Conclusion and Future Work

5.1 Conclusion

The goal of this work has been the development a multi-band multi-standard capable PA to meet the needs of current and future radio standards while supporting legacy standards. Envelope tracking as an efficiency enhancement technique was chosen for its high efficiency at back-off power as well as its potential for broadband operation. Improvements in both the design of the broadband PA and the envelope amplifier for the ET system have been made for power efficiency.

Realizable matching networks at the load of the transistor cannot achieve optimal impedances at all frequencies for a broad frequency range. There will be unavoidable mismatches due to its physical limitations. With this in mind, it is proposed that by taking into consideration the shape and characteristics of the efficiency and power contours, the mismatches can be directed towards a less sensitive region so that its effects on efficiency and power are not as significant. This design method was proven through the design of a broad band power amplifier with an average drain efficiency of 73.6%, average output power of 45.89dBm, and an average gain of 18dB between 650MHz and 1.050GHz (48% bandwidth).

For the envelope amplifier, the supply voltage for the switching stage is looked at as a new design parameter. Its effects on the conduction losses and switching losses were analyzed to reveal an optimal value that is a function of the circuit parameters and the input signal. A test was also done with a 6.4dB PAPR 5MHz LTE signal. The efficiency of the envelope amplifier showed a 3.2% improvement as the switching stage supply was reduced from 30V to 16V, with a final efficiency of 74.6%. Analysis was done to see how the optimal switching stage supply changes with the input signal's amplitude, average voltage, and frequency. Results suggest that there is a different optimal switching stage supply and efficiency benefits for different types of input signal. This efficiency enhancement technique can be used in parallel with other techniques developed in the past for better overall envelope tracking efficiency.

5.2 Future work

While the focus of progress up to now has been on the efficiency of the ET system, future work should be done to try to improve its linearity as well. Many of the non-idealities in the transistor's behavior not taken into consideration here should be designed for in order to improve the PA's linearity. Another potential area of improvement is the bandwidth of the envelope amplifier. To support standards like LTE-A, the envelope amplifier must be capable of supporting up to 100MHz RF bandwidth. Once the two critical parts of the envelope system has been completely developed. The next step is the integration of the broadband PA and the envelope amplifier into a complete envelope tracking system, where design choices such as the envelope shaping function will have to be investigated.

Bibliography

[1] Fischer, G.; Eckl,W.; Kaminski, G.;, “RFMEMS and SiC/GaN as Enabling Technologies for a Reconfigurable Multi-Band/MultiStandard Radio,” *Bell Labs Tech. J.*, vol.7, no.3, pp. 169–189. 2002

[2] Steer, M. “Beyond 3G,” *IEEE Microwave Magazine*, vol. 8, no. 1, pp. 76–82, Feb. 2007.

[3] Cripps, S. C. RF Power Amplifiers for Wireless Communications, Artech House, 2006.

[4] Doherty, W.H.; , "A New High Efficiency Power Amplifier for Modulated Waves," *Proceedings of the Institute of Radio Engineers* , vol.24, no.9, pp. 1163- 1182, Sept. 1936

[5] Iwamoto, M.; Williams, A.; Pin-Fan Chen; Metzger, A.G.; Larson, L.E.; Asbeck, P.M.; , "An extended Doherty amplifier with high efficiency over a wide power range," *IEEE Trans. Microwave Theory & Tech*, vol.49, no.12, pp.2472-2479, Dec 2001

[6] Srirattana, N.; Raghavan, A.; Heo, D.; Allen, P.E.; Laskar, J.; , "Analysis and design of a high-efficiency multistage Doherty power amplifier for wireless communications," *IEEE Trans. Microwave Theory & Tech*, vol.53, no.3, pp. 852- 860, March 2005

[7] Kahn, L.R.; , "Single-Sideband Transmission by Envelope Elimination and Restoration," *Proceedings of the IRE* , vol.40, no.7, pp.803-806, July 1952

[8] Wang, F.; Kimball, D.F.; Popp, J.D.; Yang, A.H.; Lie, D.Y.; Asbeck, P.M.; Larson, L.E.; , "An Improved Power-Added Efficiency 19-dBm Hybrid Envelope Elimination and Restoration Power Amplifier for 802.11g WLAN Applications," *IEEE Trans. Microwave Theory & Tech*, vol.54, no.12, pp.4086-4099, Dec. 2006

[9] Raab, F.H.; "Intermodulation distortion in Kahn-technique transmitters," *IEEE Trans. Microwave Theory & Tech*, vol.44, no.12, pp.2273-2278, Dec 1996

[10] Wang, F.; Yang, A.H.; Kimball, D.F.; Larson, L.E.; Asbeck, P.M.; , "Design of wide-bandwidth envelope-tracking power amplifiers for OFDM applications," *IEEE Trans. Microwave Theory & Tech*, vol.53, no.4, pp. 1244- 1255, April 2005

[11] Kim, D.; Kang. D.; Choi, J.; Kim, J.; Cho, Y.; Kim, B.; , "Optimization for Envelope Shaped Operation of Envelope Tracking Power Amplifier," *IEEE Trans. Microwave Theory & Tech*, vol.59, no.7, pp.1787-1795, July 2011

[12] Moon, J.; Son, J.; Lee, J.; Kim, B.; , "A Multimode/Multiband Envelope Tracking Transmitter With Broadband Saturated Amplifier," *IEEE Trans. Microwave Theory & Tech*, vol.59, no.12, pp.3463-3473, Dec. 2011

[13] Wright, P.; Lees, J.; Benedikt, J.; Tasker, P.J.; Cripps, S.C.; , "A Methodology for Realizing High Efficiency Class-J in a Linear and Broadband PA," *IEEE Trans. Microwave Theory & Tech*, vol.57, no.12, pp.3196-3204, Dec. 2009

[14] Wu, D.Y.-T.; Mkadem, F.; Boumaiza, S.; , "Design of a broadband and highly efficient 45W GaN power amplifier via simplified real frequency technique," *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International* , vol., no., pp.1090-1093, 23-28 May 2010

[15] Pozar, D. M. Microwave Engineering, New York: Wiley, 1998.

[16] Cripps, S.C.; "A Theory for the Prediction of GaAs FET Load-Pull Power Contours," *Microwave Symposium Digest, 1983 IEEE MTT-S International* , vol., no., pp.221-223, May 31 1983-June 3 1983

[17] Hassan, M.; Larson, L.E.; Leung, V.W.; Asbeck, P.M.; , "A Combined Series-Parallel Hybrid Envelope Amplifier for Envelope Tracking Mobile Terminal RF Power Amplifier Applications," *Solid-State Circuits, IEEE Journal of* , vol.47, no.5, pp.1185-1198, May 2012 doi: 10.1109/JSSC.2012.2184639

[18] Jung, N, S.; Kim, N, I.; Cho, G, H.;, "A new high-efficiency and super-fidelity analog audio amplifier with the aid of digital switching amplifier: class K amplifier," *Power Electronics Specialists Conference, 1998. PESC 98 Record. 29th Annual IEEE* , vol.1, no., pp.457-463 vol.1, 17-22 May 1998

[19] Wang, F.; Kimball, D.; Popp, J.; Yang, A.; Lie, D.Y.C.; Asbeck, P.; Larson, L.; , "Wideband envelope elimination and restoration power amplifier with high efficiency wideband envelope amplifier for WLAN 802.11g applications," *Microwave Symposium Digest, 2005 IEEE MTT-S International* , vol., no., pp. 4 pp., 12-17 June 2005

[20] Choi, J.; Kim, D.; Kang, D.; Kim, B.; , "A Polar Transmitter With CMOS Programmable Hysteretic-Controlled Hybrid Switching Supply Modulator for Multistandard Applications," *IEEE Trans. Microwave Theory & Tech*, vol.57, no.7, pp.1675-1686, July 2009

[21] Stauth, Jason T.; Sanders, Seth R.; , "Optimum Bias Calculation for Parallel Hybrid Switching-Linear Regulators," *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE* , vol., no., pp.569-574, Feb. 25 2007-March 1 2007

[22] Erickson, R. W.; Maksimovic, D. Fundamentals of Power Electronics, Second Edition. New York: Springer 2001