

“A Novel Buried-Emitter Photovoltaic Cell for High Efficiency Energy Conversion”

by

Roohollah Samadzadeh Tarighat

A thesis
presented to the University of Waterloo
in fulfillment of the
thesis requirement for the degree of
Doctor of Philosophy
in
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2013

© Roohollah Samadzadeh Tarighat 2013

Author's declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

To address the commonly poor short wavelength response of the conventional solar cell structure which consists of a highly doped thin emitter layer on top of a thicker and less doped base, the novel concept of the Buried-Windowed-Emitter is introduced. This new solar cell structure makes use of a high quality semiconductor layer on top of the traditionally made highly doped emitter and greatly enhances the spectral response of the solar cell by giving the superficially generated carriers a higher chance of collection at the junction. In the proposed BWE structure the emitter is windowed in order to electrically connect the top layer to the base for current collection.

The efficacy of the proposed novel device is proven by computer aided device simulations using the available device simulation tools such as MEDICI. The results of simulation show that the proposed novel Buried-Windowed-Emitter solar cell will not only improve the short wavelength spectral response of the overall cell as expected, but also will boost the spectral efficiency for all the wavelengths. Another exciting conclusion from the results of the computer simulation of the BWE solar cell is that the minority carrier lifetime in the top layer does not need to be very high for a superb performance and values as low as $1\mu\text{s}$ can still boost the short circuit current of the cell to values close to the theoretical limit of the photo-current collectable by a silicon solar cell. This is indeed a good news for manufacturability of this device as it should be practically feasible to achieve epitaxial films with minority carrier lifetime in this range.

In order to increase the understanding about the rather complex structure of the proposed Buried-Windowed-Emitter solar cell, an analytical circuit level model, similar to the case of the standard solar cell, is developed for the proposed device. The developed analytical model helps to understand the importance of the main design parameters such as the dimensions of the pattern of the windowed emitter.

On the path to fabricate the proposed BWE solar cell, great deal of work is done on the development of a low temperature ($<300^\circ\text{C}$) epitaxial silicon technology using the benefits of Plasma Enhanced Chemical Vapor Deposition (PECVD). Highly doped epitaxial silicon layers of up to around $1\mu\text{m}$ thickness are achieved with sheet resistivity as low as $7\Omega/\text{sq}$ which is much lower than what is reported in the literature in similar deposition conditions. Intrinsic, phosphorous doped n-type and boron doped p-type epitaxial films have been developed on silicon substrates. Measurement of reflection spectra of the deposited epitaxial films is proposed as a fast, non-destructive and process-integrate-able method to assess the crystalline quality of the epitaxial films. Effects of higher temperature post deposition annealing have been studied on the developed epitaxial films

A full technology is developed for the fabrication of the proposed novel solar cells. Photo-masks are designed to create 10 different architectures for the design of the windowed emitter in the BWE cell. All

the steps taken in the successful fabrication of the novel BWE cells are presented in detail and the relevant findings are discussed and proposed as future research topics.

Three kinds of cells are fabricated using the developed technology to separately study the effects of partial coverage of the windowed emitter, the optical performance of the developed epitaxial silicon films and the performance and manufacturability of the novel BWE solar cell

The results show that the concept of windowed-emitter by itself (even without the top layer) is capable of enhancing the performance of the solar cell when compared to a standard design. It also promises high conversion efficiency for the BWE solar cell in case a high quality top layer can be deposited on top of the windowed emitter. The results further reveal the lower than expected quality of the low temperature epitaxial films despite the indication of their full crystallinity through other analyses. Use of the epitaxial films as the emitter of the solar cell is proposed as a direct and effective method of studying the photovoltaic performance of the low temperature epitaxial films. Further development of the epitaxial technology will lead to feasibility of a BWE solar cell with very high photovoltaic performance.

Acknowledgments

I am truly thankful:

To my supervisor, Dr. Siva Sivoththaman, for lighting the road of this journey by his excellent academic, moral and scientific support.

To the CAPDS lab manager, Mr. Joseph Street, for his efforts to maintain all the equipment in the CAPDS and for sharing his valuable experience and knowledge in semiconductor processing.

To all the members of the CAPDS who have generously given me the support, thoughtful comments and smiles. Especial thanks to Dr. Bahareh Sadeghi and Lin Tian for their help and collaboration in several stages during this work.

To my PhD defense committee members who have taken the time to evaluate the validity of this work and improved it by their constructive feedback..

To all my friends who have helped my definition of life stay close to its original description

And most importantly to my family especially my mother and father who have nurtured me before and after birth with every bit of unconditional love one can ask for. I will never be able to return anything that can compare.

Table of Contents

Chapter 1- Introduction and literature review	1
1.1 Introduction	1
1.2 Brief history of photovoltaic cells	2
1.3 Targeting high conversion efficiencies.....	3
1.3.1 Effective light absorption and trapping	4
1.3.2 Back surface field	6
1.4 Literature review for new concepts for high efficiency	7
1.4.1 Rear point contact solar cells.....	7
1.4.2 The Passivated Emitter- Rear locally diffused (PERL) solar cell	8
Chapter 2 - Introduction to the proposed novel solar cell structures	12
2.1 Considerations of photon absorption in crystalline silicon	12
2.2 Considerations of the limits of the minority carrier lifetime in crystalline silicon.....	16
2.3 Proposed new solar cell structures.....	17
2.3.1 Three-Terminal solar cell	17
2.3.2 Buried-Windowed-Emitter solar cell	19
Chapter 3 - Computer simulation and proof of concept of the proposed novel solar cells	23
3.1 Simulation tools	23
3.2 Simulation results for the three terminal solar cell	23
3.3 Simulation model for the Buried-Windowed-Emitter solar cell	25
3.4 Simulation results for the Buried-Windowed-Emitter solar cell.....	26
Chapter 4 – Development of an analytical model for the proposed BWE solar cell	32
4.1 Representative model for the BWE structure.....	32
4.1.1 Description of the unit cell.....	33
4.1.2 Methodology used to develop the model	34
4.2- formulation of the model equations	36
Chapter 5 - Technology development for low temperature Silicon epitaxy.....	42
5.1 Theoretical background leading to the new epitaxial silicon process	43
5.1.1 Role of Hydrogen	44
5.1.2 Role of temperature.....	44

5.2 Description of the PECVD system used.....	45
5.3 Chamber preparation prior to film deposition	47
5.4 Results and discussion on the developed process for low temperature silicon epitaxy	48
5.4.1 Variation of the film quality as a function of the distance from the interface	48
5.4.2 N-type silicon epitaxy	51
5.4.3 Findings on the role of Phosphine in enhancing epitaxy	54
5.4.4 Intrinsic silicon epitaxy	55
5.4.5 P-type silicon epitaxy	57
5.4.6 Epitaxy on different substrate orientations.....	57
5.4.7 Control over dopant incorporation.....	59
5.4.8 Quality assessment of the epitaxial films using reflection spectra.....	61
5.4.9- studying the effects of post deposition annealing	64
5.4.10- Potential of the developed deposition techniques for super-lattice formation	70
Chapter 6 – Technology development for the proposed BWE solar cell fabrication	72
6.1 Choice of the technology path.....	72
6.2 Design considerations for photo-masks and cell architectures.....	74
6.2.1 Top Metal contact Design	75
6.3 Detailed fabrication steps and discussion.....	80
Chapter 7 - Results and characterization of the fabricated novel BWE solar cells.....	95
7.1 Characterization methods used:.....	96
7.1.1 Minority carrier lifetime measurements	96
7.1.2 Measurement of reflection spectra	97
7.1.3 External Quantum Efficiency.....	97
7.1.4 Dark and Illuminated current-voltage measurements.....	98
7.2 Characterization and discussions of the cells with windowed emitter and without the top layer	100
7.2.1 Cells with windowed emitter and without the top layer – External Quantum Efficiency	102
7.2.2 Cells with windowed emitter and without the top layer – Reflection Spectra	103
7.2.3 Cells with windowed emitter and without the top layer – Internal Quantum Efficiency.....	105
7.2.4 Cells with windowed emitter and without the top layer – Dark and Illuminated IV.....	110

7.3 Characterization and discussions of the Control experiment cells: standard cell with epitaxial film as emitter.....	113
7.4 Characterization and discussions of the complete BWE solar cells.....	116
7.4.1 Characterization and discussions of the complete BWE solar cells - Quantum Efficiency.....	117
Chapter 8 – Conclusions.....	122
References	124
Appendix A – Medici Code for BWE solar cell simulation.....	128

Chapter 1- Introduction and literature review

1.1 Introduction

A solar cell in its simplest and most popular definition is just a PN junction diode. Figure 1 shows a simplified schematic of a pn junction solar cell.

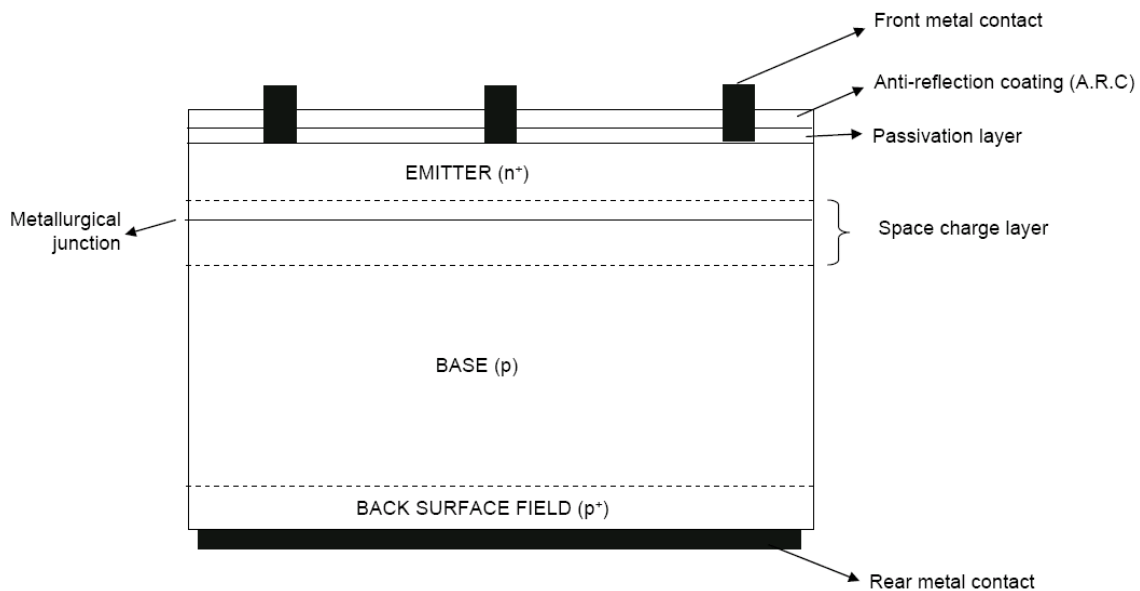


Figure 1, simplified schematic of a pn-junction solar cell. Photo obtained from [9]

Because of asymmetric structure of a diode for electrons and holes, if shone by light of proper energy, the photo-generated electrons and holes can create a current and hence a voltage across an external load. Figure 2 shows a typical IV characteristic curve of a diode with and without illumination. As a first order approximation, the illuminated curve is basically the dark curve pulled down with a value of current which is called photo-current (J_{ph}). One can see that when voltage is positive and current negative, the power consumed by the diode is negative which means the diode is delivering energy and that's where we bias the diode to extract power out of it.

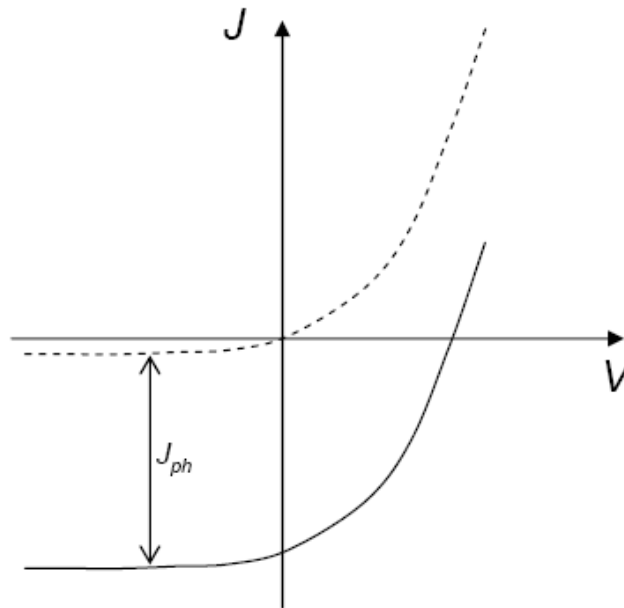


Figure 2, IV curves of a diode with (solid line) and without (dashed line) illumination. Photo obtained from [9]

1.2 Brief history of photovoltaic cells

Edmund Bequerel first in 1839 observed the photovoltaic effect when he saw that light shone on a silver coated platinum electrode immersed in electrolyte produced an electric current. [1]

In 1894, Charles Fritts made the first large area solar cells by sandwiching selenium between gold and some other metals. These structures were basically Schottky barrier thin film devices. Photovoltaic based research was carried on until around 1950 when the high quality silicon wafer production for microelectronic industry gave the opportunity of creating significant power from light. In 1954, the first silicon solar cell was reported by Chaplin, Fuller and Pearson having an efficiency of 6%. Space applications were perhaps among the very few places where the high cost of power generated by these solar cells was tolerated. [10]

The energy crisis in 1970 brought more interest in photovoltaics especially in the modern world. It was after this time that more economic aspects of the solar cells were studied.

1.3 Targeting high conversion efficiencies

To achieve high efficiency in solar energy conversion some techniques can be used from which the choice of material with proper features is the first step. In choosing a material one should consider the band gap energy and structure as well as the quality of the material. For each band gap chosen, there is a theoretical upper limit on the efficiency achievable with a single junction structure. Figure 3 shows this maximum theoretical efficiency value as a function of bandgap. It can be seen that silicon, as the most popular material for solar cells in the current market, is just a bit away from the best band gap energy value.

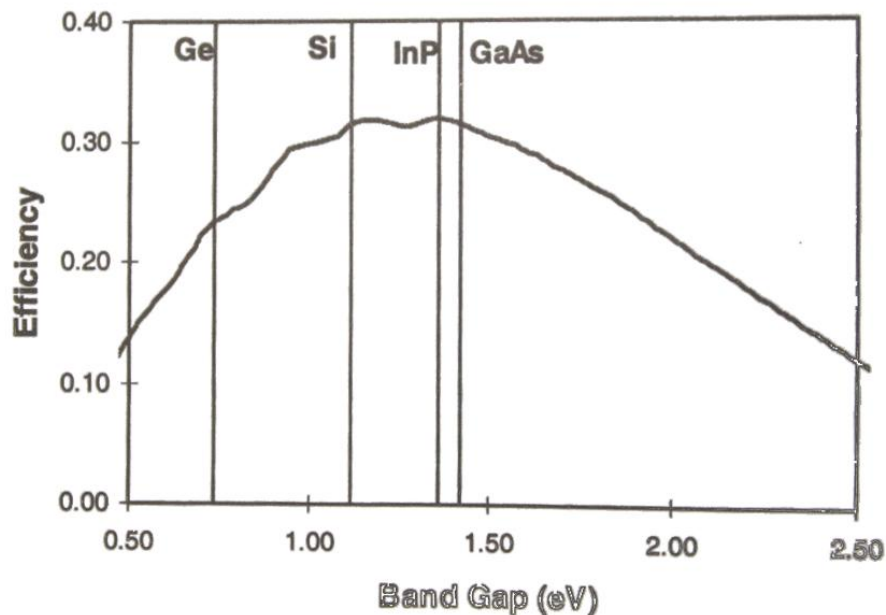


Figure 3, maximum theoretical efficiency for a single material for AM1.5 versus bandgap energy. Photo obtained from [2]

Since most of the semiconductors have their best performance in the single crystalline form, the quality of the material is very important, meaning having less crystal defects will lead to a higher minority carrier lifetime which will benefit the cell with a higher collected photo-current. This is important since the carriers generated far away from the junction will need to diffuse to junction to be collected and they shouldn't be recombined before collection at the junction.

1.3.1 Effective light absorption and trapping

A considerable portion of the incident light can be reflected from the shiny surface of the cell before entering the cell material which will be a loss. To avoid this, an anti-reflection coating is deposited on top of the cell to facilitate the entry of light from air with refractive index close to 1 into the semiconductor with a higher refractive index (around 4 in case of crystalline silicon). For a single layer of anti-reflection coating the refractive index should be the geometric mean of the refractive index of the air and the semiconductor.

In addition to Anti-Reflection-coating, surface texturing is also an important step to enhance light trapping in the semiconductor. Texturing causes the effective thickness of the cell to be larger because causes an angle in the path of the normally entered light beam. Figure 4 illustrates the effect of addition of texturing on photo current of a silicon cell and Figure 5 shows the effect of antireflection coating on the amount of light reflected from the surface of the cell.

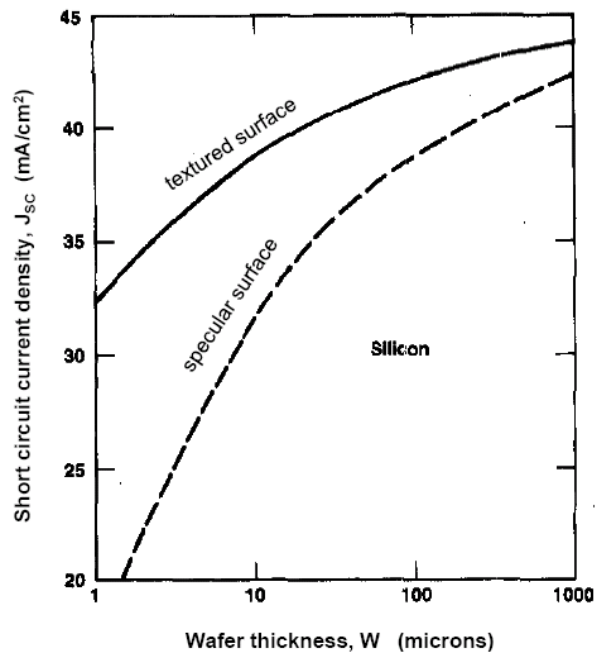


Figure 4, effect of surface texturing on increasing the photo-current of a silicon cell as a function of the cell thickness. Photo obtained from [1]

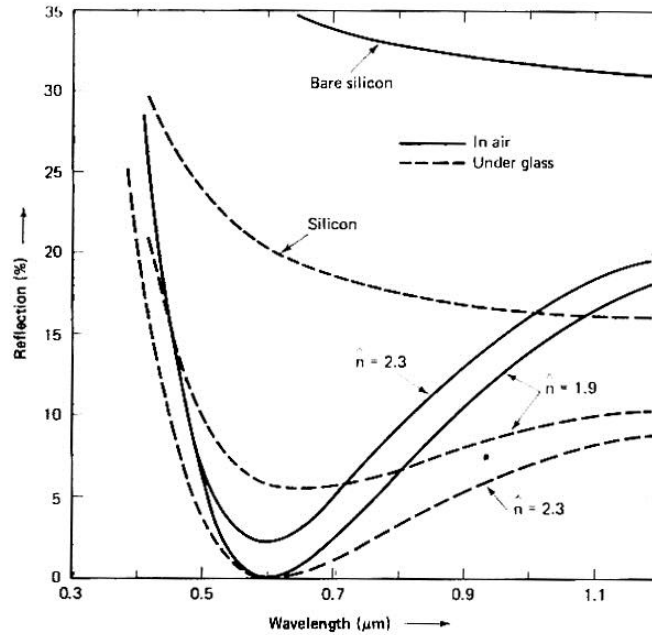


Figure 5, effect of addition of antireflection coating on bare silicon on the reflection of the normally incident light. Photo obtained from [2]

As mentioned before, for each single material cell with a specific bandgap value, there is a theoretical and practical efficiency limit. To pass this limit, the most viable approach is to split the incoming light spectrum based on the photon energy and absorb and convert each portion with a cell made up of the semiconductor with the band gap equal to the minimum photon energy of that portion. The easiest way to implement this idea is to stack cells on top of each other with the cell with highest band gap on top and the least one in bottom. Such a stack of cells are called a tandem structure a schematic of which is shown in Figure 6. With tandem cells one can achieve efficiencies as high as the thermodynamic limit of around 93% [7,17]

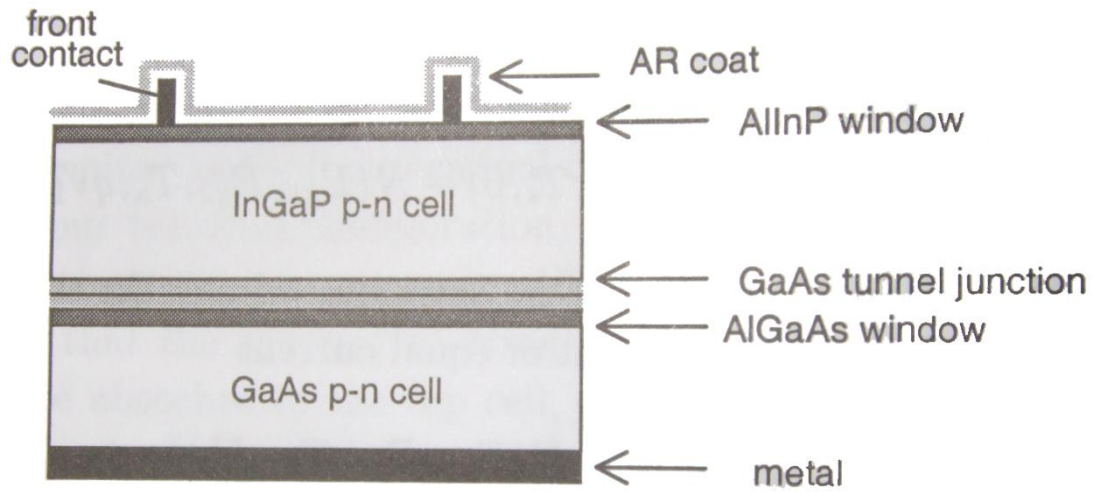


Figure 6, Schematic of a two-step tandem cell. [1]

1.3.2 Back surface field

by introducing a highly doped layer close to the back contact of a simple solar cell, because of formation of a high-low junction close to the back surface, one can achieve more effective surface passivation which will lead to a higher photo-current especially because of the lower energy photons which are absorbed far away from the front surface. Figure 7 shows a diagram representing the collection probability of carriers as a function of distance with and without back surface field.

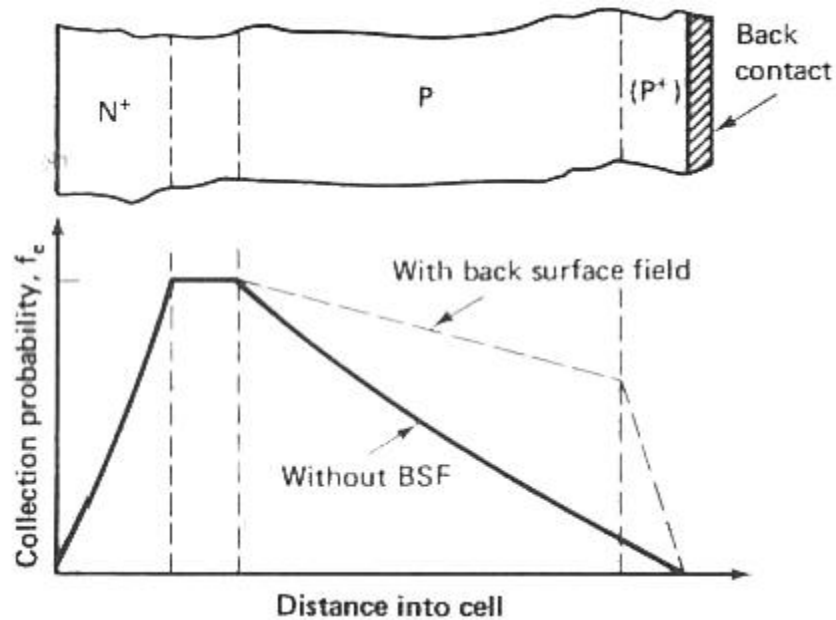


Figure 7, collection probability of carriers as a function of distance in the cell with and without Back Surface Field. [2]

1.4 Literature review for new concepts for high efficiency

To achieve efficiencies close to the theoretical limit one should incorporate many features to maximize light absorption and minimize all sources of loss. As mentioned before surface texturing, surface passivation, anti-reflection coating, back surface field and high quality material are the basic steps. There are few structures reported with the highest efficiencies to which we'll have a quick look below.

1.4.1 Rear point contact solar cells

Rear point contact solar cell is another idea benefiting from no front surface coverage because of metal contacts and also effective back surface passivation. These features are gained with the expense of very high lifetime requirements, but until now this structure has had the record of module level efficiency among industrialized silicon based structures. Figure 8 shows a schematic of this cell which is being produced in Sun Power Corporation.

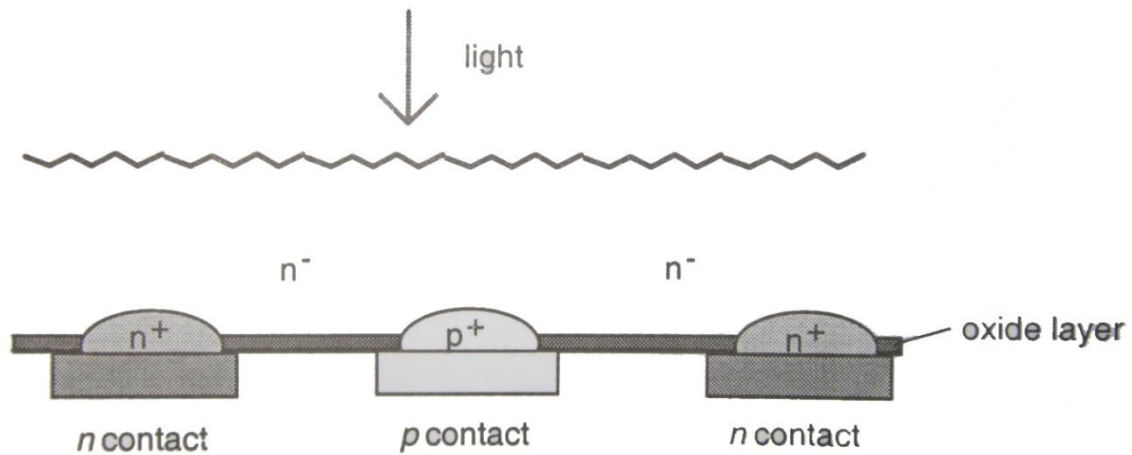


Figure 8, schematic of the Rear Point Contact Solar Cell. Both contacts are in the back so there is no metal coverage in the front letting more light in but since junction is away from the light entering surface, very high lifetime material should be used. [1]

1.4.2 The Passivated Emitter- Rear locally diffused (PERL) solar cell

Figure 9 shows the schematic of this cell. In this structure the rear point contacts lower the area of semiconductor-metal interface which happens to be a very effective recombination centers. This way most of the back surface is covered and hence passivated by the oxide layer. Also the front n layer is differentially higher doped under the metal contact, this way the chance of metal penetrations and shorting to the base reduces and also the thinner layers at the window places improve the high energy photon conversion efficiency. The inverted pyramids are very effective kind of texturing although it needs photolithography to be achieved.

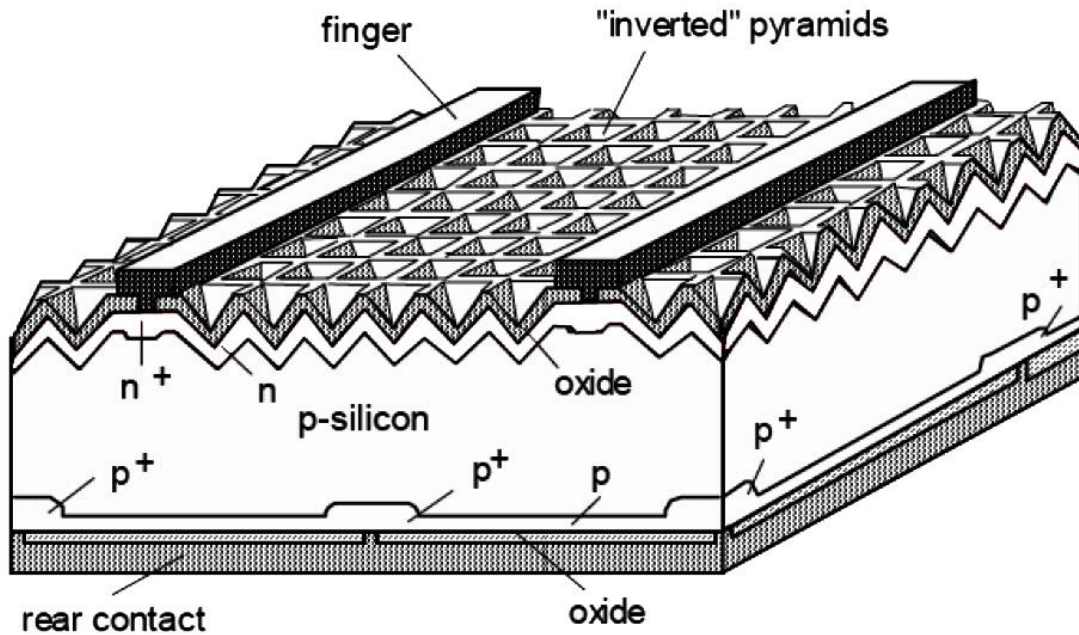


Figure 9, PERL Solar Cell, having the highest reported efficiency for silicon base solar cells (24.4% at AM1.5 direct) [9]

Next chapter we will discuss the novel structure proposed in this thesis which is a three-terminal silicon based solar cell. Below are the two works bearing some similarity to our proposal.

Previously a modeling based on the concept of buried-emitter solar cell has been done by Bouazzi et. al. [3] which has basic analogy with our proposal, although their main purpose has been increasing the junction area which is exactly what we will try to avoid in the last and most sophisticated variation of our proposed structure. Figure 10 shows the schematic of the device Bouazzi et. al. have done the modeling on which is a double facial structure and as a result has the buried emitter on both sides of the device. Furthermore, considering the top layer as p^+ (10^{19} cm^{-3} to solve the series resistance problem) in their work, shows that their intention is not necessarily better high energy photon conversion efficiency but lowering the effective diffusion length of the bulk because of two junctions on each side.

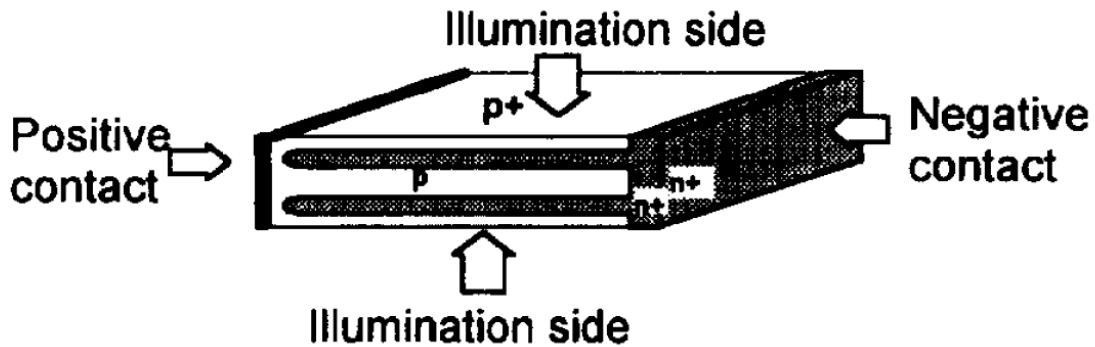


Figure 10, Bouazzi et. al.'s proposed structure for modeling. Two buried emitters are located at each side of the cell [3]

Tandem cells are usually designed in a way that the stacking cells are in series with each other (emitter of one cell is adjacent to base of the other) so there is only the top contact of the top cell and the bottom contact of the bottom cell to be taken care of. Emziane et. al. have done a computer simulation and optimization on a tandem cell with two sub-cells having their emitters in vicinity [4] and hence sharing a similarity with the structure proposed in our work. This structure needs to have a contact to the layer connected to emitter of both cells and as a result has been treated as a three-terminal structure too. Figure 11 shows the structure and corresponding energy band structure of this cell. To optimize the efficiency, Emziane et. al. have tried few combination of bandgaps for the upper and lower cell materials and concluded that the best combination would be 1.2 and 0.74eV for the top and bottom cells respectively. These band gaps can be achieved by proper adjustment of Ga, As or P relative values in Indium based crystals.

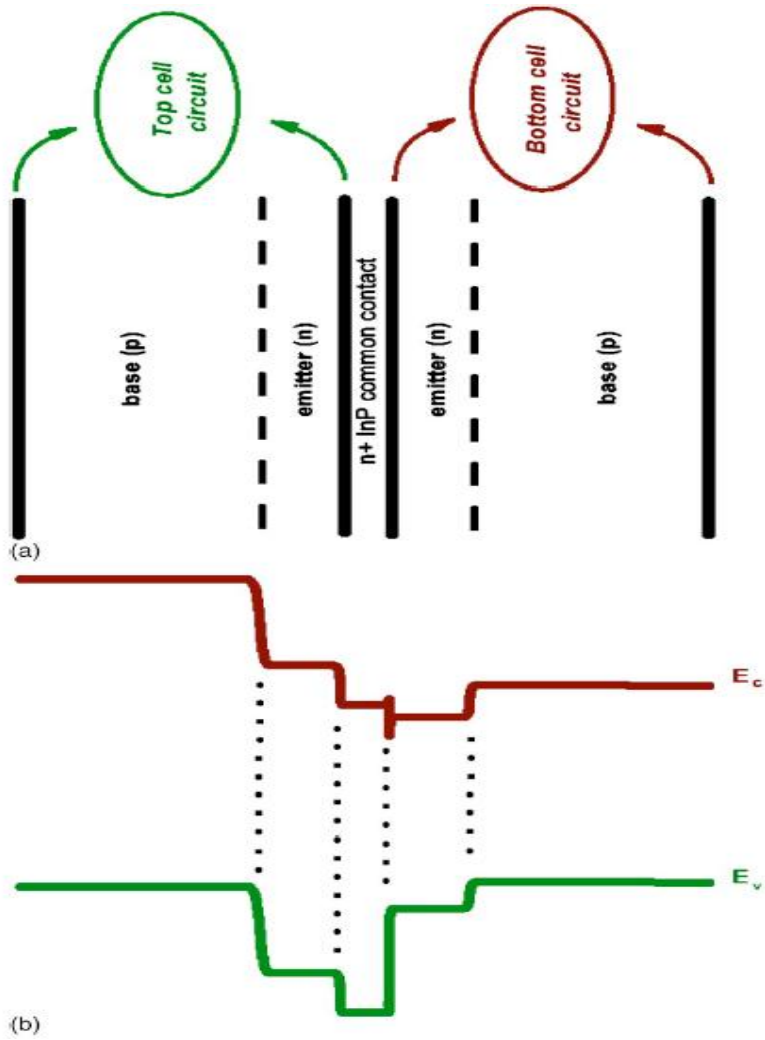


Figure 11, Emziane et. al.'s simulation work on a three terminal tandem structure with two different bandgaps for the top and bottom cells. (a) shows the structure and (b) shows the bandgap structure of the whole cell. [4]

Chapter 2 - Introduction to the proposed novel solar cell structures

This chapter will present the novel solar cell structures proposed by first explaining the idea which leads to justification of the introduction of the novel cell structures. The mechanisms of light absorption in silicon together with the practical limitations of the minority carrier diffusion length in the highly doped silicon layers are the main characters in the introduction of the new solar cell structures.

2.1 Considerations of photon absorption in crystalline silicon

When a number of photons enter the bulk of a semiconductor, due to the statistical nature of the optical absorption, relatively speaking, more photons will be absorbed closer to surface than deeper into the material. [1], [2]. This applies to all the wavelengths which can be absorbed in the semiconductor. Absorption phenomenon for a monochromatic light passing through an attenuating material can be modeled using an exponential function with a negative exponent known as the “absorption coefficient” value of which represents after how much penetration, a photon of that wavelength will be absorbed while traveling through the material. [1] With this model, the carrier generation rate as a function of distance can be expressed as:

$$G(x, \lambda) = (1 - R(\lambda))\alpha(\lambda)N_s(\lambda)e^{-\alpha(\lambda)x} \quad Eq. 1$$

Where $G(x, \lambda)$ is the generation at a distance x from the light entree surface due to absorption of light of wavelength λ , $N_s(\lambda)$ is the flux per unit wavelength at the light entree surface for the light of wavelength λ , $R(\lambda)$ is the reflected fraction and $\alpha(\lambda)$ is the absorption coefficient. This coefficient is mostly an increasing function of the energy of the photon [17, 18], which means even more of the input light will be absorbed closer to the surface, the higher the energy of the photons becomes. Figure 12 shows a plot of the absorption coefficient of light in crystalline silicon as a function of photon energy. The data for the wavelength dependent absorption coefficient of silicon used for this plot is taken from reference [19].

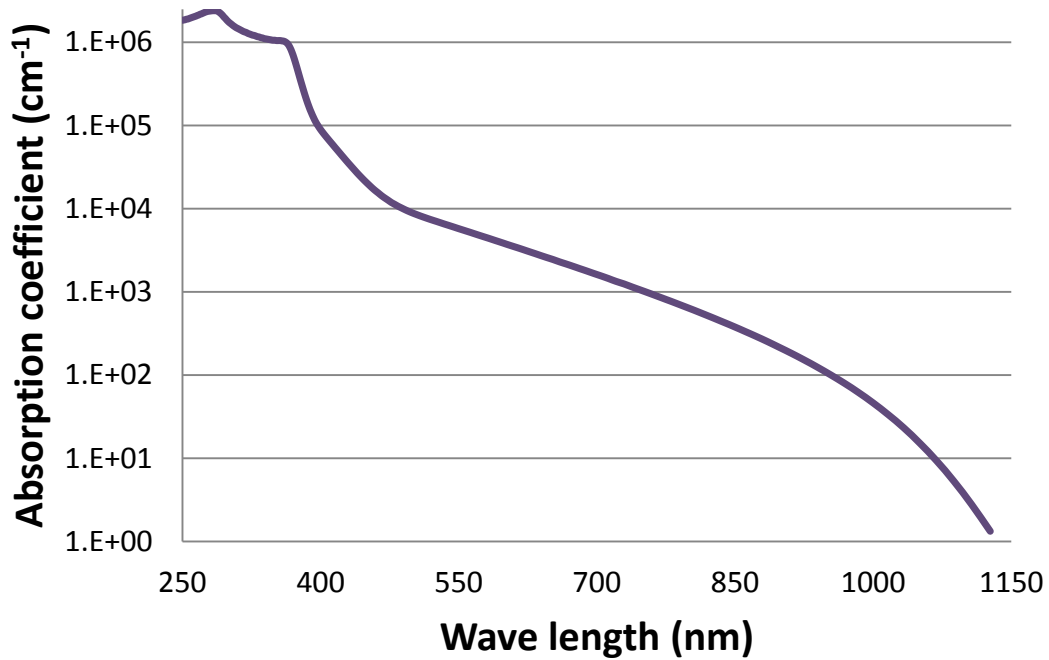


Figure 12, absorption coefficient of light in crystalline silicon as a function of photon wavelength. Higher energy photons absorb much faster than the lower energy ones.

It is well known that the superficial regions of a cell is of utmost importance for light absorption but our goal here is to demonstrate a quantitative measure of how important the surface and immediate subsurface of a solar cell in terms of light absorption. To do so, we can calculate the spatial dependence of absorbed light in a 300 μ m thick slab of crystalline silicon when shone using a light source with the spectrum of the AM1.5 light. Using AM1.5 has the obvious justification that it is the standard of comparison for the performance of the terrestrial solar cells and also very close to what a real solar cell will, on average, receive in terrestrial applications. Figure 13 shows the intensity of AM1.5 light spectrum as a function of photon wavelength. The data for this plot was taken from the National Renewable Energy Laboratory (NREL) website. This data can be used for $N_s(\lambda)$ in Eq.1

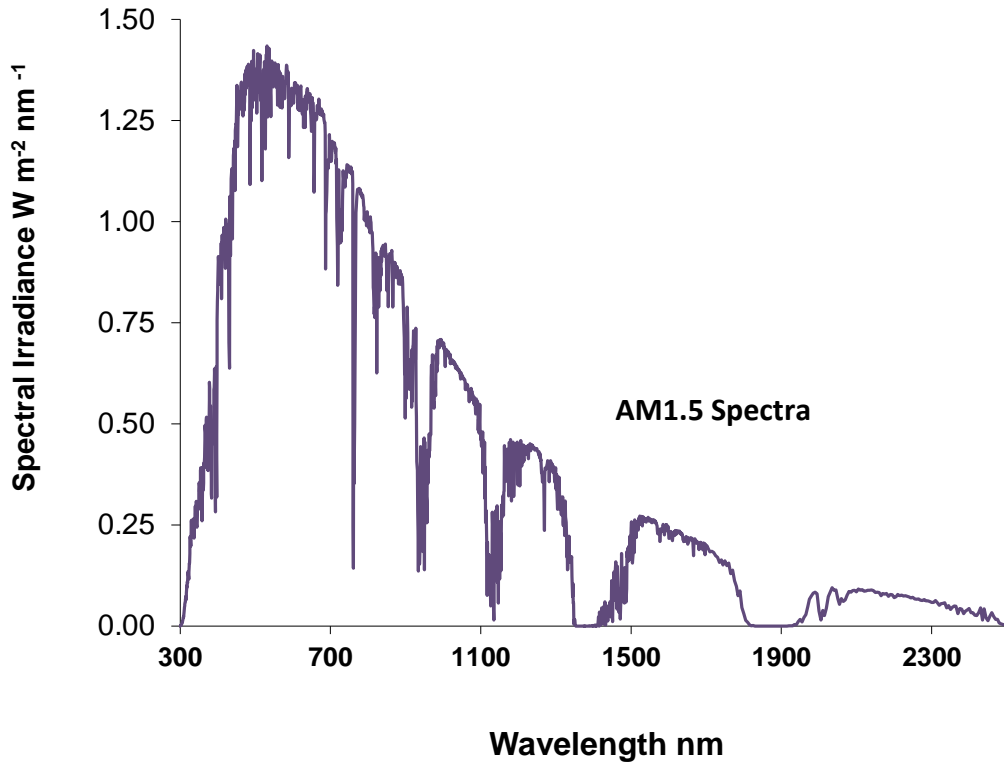


Figure 13, AM1.5 light spectrum used for the evaluation of the spatial distribution of light absorption in a crystalline silicon slab.

Assuming zero reflection from the surface of the silicon surface and integrating Eq.1 over the significantly absorbed part of light spectrum using AM1.5 spectrum as the input light, one can calculate the spatial distribution of light absorption rate in the bulk of the silicon slab. The result is shown in Figure 14.

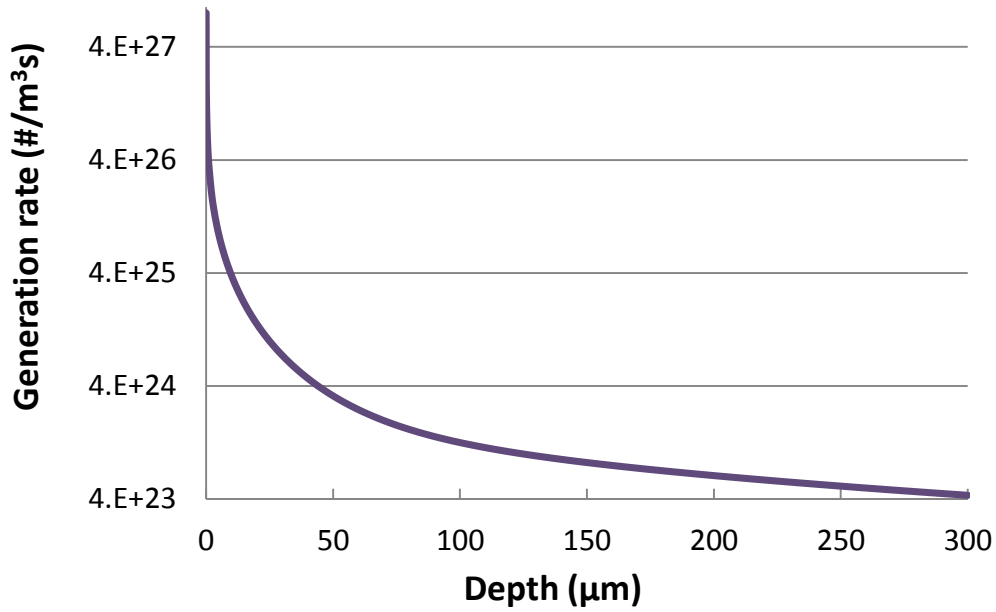


Figure 14, absorption rate of light as a function of distance from the light entrance surface for a crystalline silicon sample when shone by AM1.5 spectrum light and assuming zero reflection from the surface.

Integrating the result one more time from surface to a point in a certain depth will give the number of absorbed carriers per second up to that depth. Figure 15 shows the sketch of this integral normalized to the total number of absorbed photons in a 300μm-thick single crystal silicon assuming zero reflection from surface as shown in Eq.2

$$N_G(x) = 100 \frac{\int_0^x \int_{\lambda_{min}}^{\lambda_{max}} G(x, \lambda) d\lambda dx}{\int_0^{300\mu m} \int_{\lambda_{min}}^{\lambda_{max}} G(x, \lambda) d\lambda dx} \quad Eq. 2$$

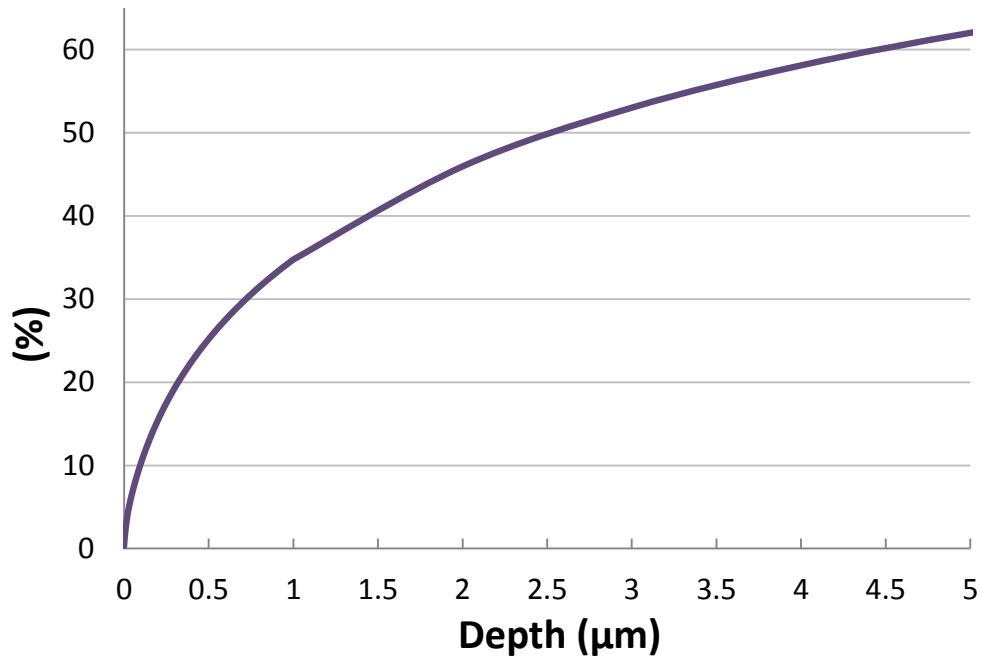


Figure 15 - percentage of the generated carriers between surface and a depth, X, inside the silicon crystal when a 300μm thick silicon crystal is shun by AM1.5 spectrum versus the depth from light entree surface. Only up to the first 5μm of the depth is shown to magnify the importance of the superficial regions in light absorption.

Figure 15 basically shows how important the regions close to surface are for light absorption, e.g. it shows that around 25% of the whole generated carriers in a 300μm crystalline silicon cell are generated in the first 0.5μm close to the surface.

2.2 Considerations of the limits of the minority carrier lifetime in crystalline silicon

To achieve high energy conversion efficiencies in solar cells, one, not only must increase the light absorption but also should make sure the generated carriers can be collected before being lost. Because of this, minority carrier lifetime in solar cells is of great importance to give the generated excess carriers a chance to be collected at the junction before annihilation because of recombination. The most common structure for a crystalline silicon based solar cell is a one sided pn junction (p^+n or n^+p) with emitter having high doping and lower thickness whereas bulk being low-medium doped and with much larger thickness to absorb as much light as possible. High doping of the emitter is necessary to avoid series resistance (including metal contact resistance) whereas the low thickness of it is desired to

minimize the light absorption in the emitter layer. This is due to the fact that by increased doping, because of the defects introduced, the minority carrier lifetime will drop quickly and emitter being the first layer into which light enters, can be a place of low collection efficiency for the generated carriers.

Thick and low doped emitter has fabrication difficulties so is not a common structure also devices like Rear point contact solar cells which have the emitter on the back side rely on the extreme high quality of the used silicon material to ensure a high minority carrier lifetime required for the carriers to diffuse to the backside of the cell before recombining [1], [19].

So as one can see, in the most common design, the best part of the device light absorption-wise, is the worst part regarding the chance of carrier collection. That's why a practical compromise is to minimize the thickness of the emitter and increase its conductivity which still won't completely eliminate the loss in the high energy photons range. To address this issue we are proposing a new device structure which has a high quality medium doped layer on top of the highly doped emitter, so that the region in the immediate vicinity of the light entree surface gives generated carriers higher chance of collection because of increased diffusion length of minority carriers.

2.3 Proposed new solar cell structures

The way we will present the proposed devices is the way the idea developed chronologically. First we will present the Three-Terminal solar cell structure which was first proposed to improve the blue response of the solar cells. We will then present the Buried-Windowed-Emitter cell which was developed to address the short comings of the first proposal.

2.3.1 Three-Terminal solar cell

The significance of introducing the three-terminal solar cell is not because of its high performance but to show its ancestral relation to the Buried-Windowed-Emitter cell. Figure 16 shows the schematic of the basic configuration of the proposed three-terminal solar cell. The principal novelty in this cell is to add a medium doped high quality layer on top of the emitter for the reasons discussed earlier.

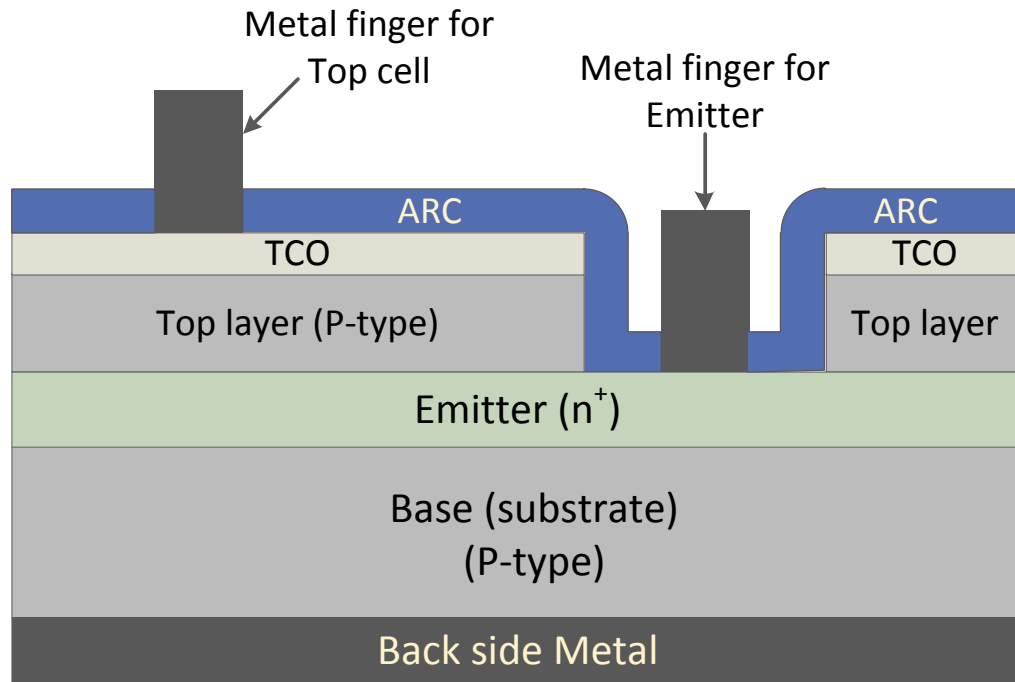


Figure 16 - Schematic of the Three-Terminal solar cell. Emitter is shared between the two emitter-base and emitter-top layer diodes. Top layer is a high quality medium doped layer giving superficially created carriers a higher chance to be collected.

One may see this device as two diodes sharing the emitter hence inherently connected front-to-front (or back-to-back for the device with opposite dopant type); therefore the top layer needs to be electrically connected to outer circuitry for charge extraction and for this, a third metal contact is needed. The purpose is to make the top cell's collector as high quality (medium doped) as possible and since it is the first layer into which the light enters, the top cell is mainly responsible for the conversion of high energy portion of light while the bottom cell absorbs mainly the lower energy portion. . Being medium doped can introduce the series resistance problem for lateral conductivity for which a thin TCO layer or reduced distance between metal contacts can be weak remedies as the former will increase the complexity and cost further and the latter will block more light from entering the device.

Power extraction from this device can be achieved in two ways:

- 1- To connect the top and bottom cells in parallel and use a single power extraction circuit
- 2- To use two separate power extraction circuitries one for the top cell and the other for the bottom cell

The second scheme of power extraction is better in terms of maximum power extraction since the output of each cell can be maximized independently. However it needs a more complicated and thus more expensive power circuitry.

The first scheme, on the other hand, needs only one power extraction circuitry but has some other disadvantages. Among these disadvantages is the doubled area of the junctions and as a result the almost doubled saturation current. This is because of the existence of two junctions (top and bottom cell) with almost the same area of the foot print of the whole cell. Increased saturation current will cause the open circuit voltage of the total cell to drop as in an ideal silicon diode V_{oc} and saturation current are related as follows:

$$V_{OC} \approx \frac{nkT}{e} \ln \left(\frac{J_{SC}}{J_s} + 1 \right)$$

This means that for this device to be actually worth the efforts the gain in the Short circuit current compared to an standard cell structure must be higher than a critical value, otherwise the output power of the whole cell will be even lower than a standard cell. Because of these complexities this structure cannot be considered as a high efficiency cell structure for industrial uses but sets the path for proposing the Buried-Windowed-Emitter solar cell in which connection of the top layer to the base layer is achieved through windows opened in the emitter layer eliminating the need for a third terminal and potentially lowering the junction area. The lateral conductivity problem of the top layer can also be addressed by lowering the width of emitter strips as will be discussed in more detail later on.

2.3.2 Buried-Windowed-Emitter solar cell

In the Buried Windowed Emitter solar cell structure there is a thin high quality layer of semiconductor added on top of the highly doped emitter. Figure 17 shows the 3D and cross sectional schematic of the proposed cell. It is basically composed of a highly doped emitter sandwiched between medium doped base and top layers which have the same dopant type. There are windows opened in the emitter through which the top and base layers are electrically connected. Light enters the device from top surface thus immediately entering in the top layer which is meant to have high minority carrier lifetime and is very close to the junction promising high collection efficiency for at least the portions of the top layer immediately on top of the emitter strips. Highly doped hence defective emitter absorbs much smaller portion of the light (compared to a standard design) therefore can be chosen to be thick and as conductive as possible to eliminate series resistance losses due to lateral conduction within the emitter layer without deteriorating the blue response of the cell.

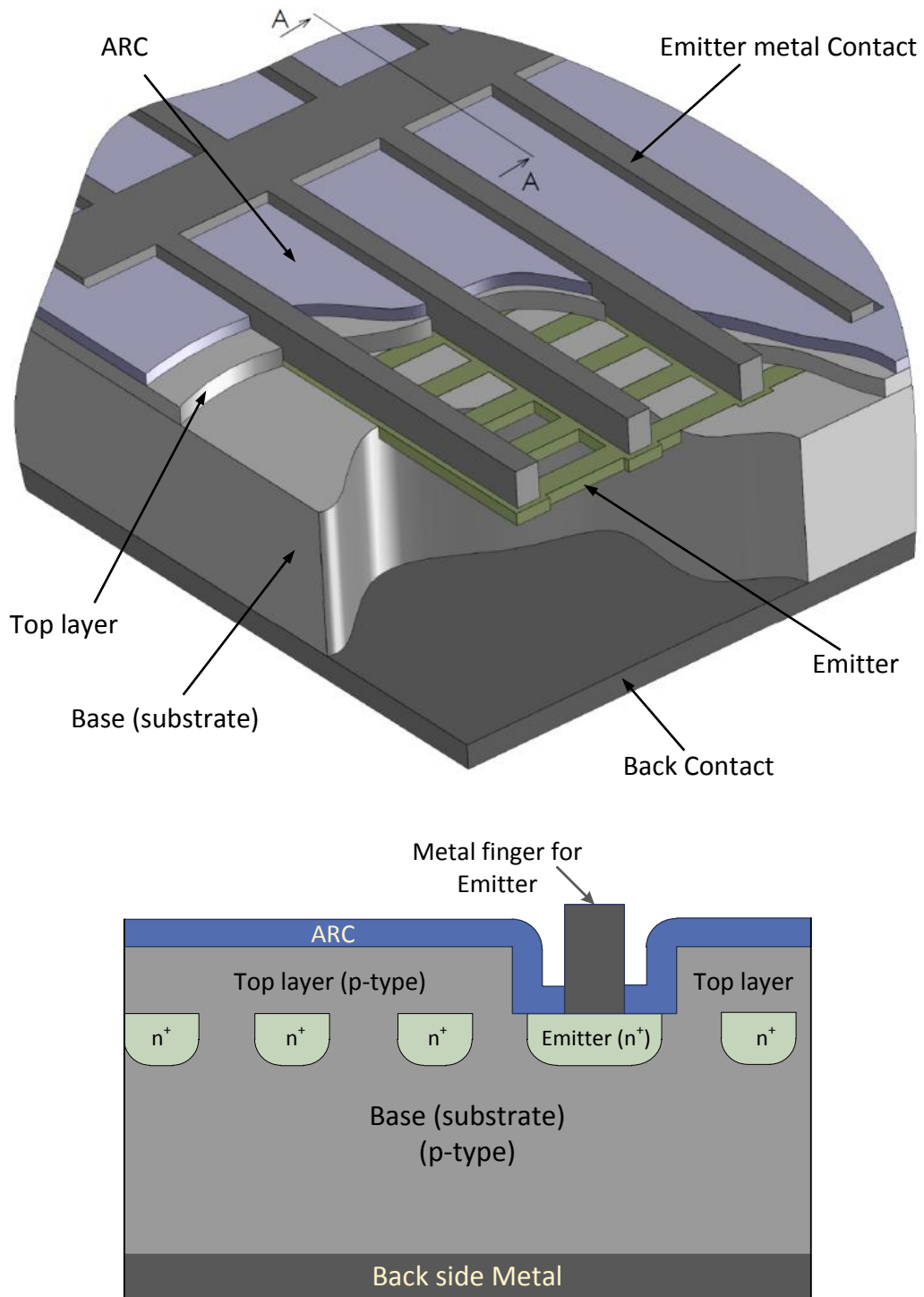


Figure 17 - top: 3D view of the proposed novel Buried-Windowed-Emitter solar cell. Bottom: cross sectional view across the line AA.

Top metal electrode is in contact with the emitter layer by etching the top layer at the appropriate locations and the back contact, similar to a standard design, is covering the whole back side. This structure also offers a better front surface passivation possibility as it is easier to passivate a surface when the top layer has lower doping as opposed to the high doping of an emitter in a conventional cell design. Our focus will be on the areas close to the top surface where the novelty of this structure lies. Other high performance features such as back surface field, surface texturing, front and back surface passivation schemes, etc. are considered obvious optional additions to this device for the best performance and won't be discussed here.

Figure 18 pictorially shows the carrier collection scheme for photovoltaic action in the proposed Buried-Windowed-Emitter solar cell. Depending on the thickness of the top layer and thickness and shape of the emitter, emitter layer will absorb some portion of the light which is best to be minimized for which a thicker top layer and a smaller emitter coverage (defined as the ratio of the total emitter area to the whole device area) is favored. One expects that the generated carriers on a portion of the top layer which is sitting on a patch of emitter to be collected with close to 100% chance since a practical thickness for the top layer will be in the micrometers range.

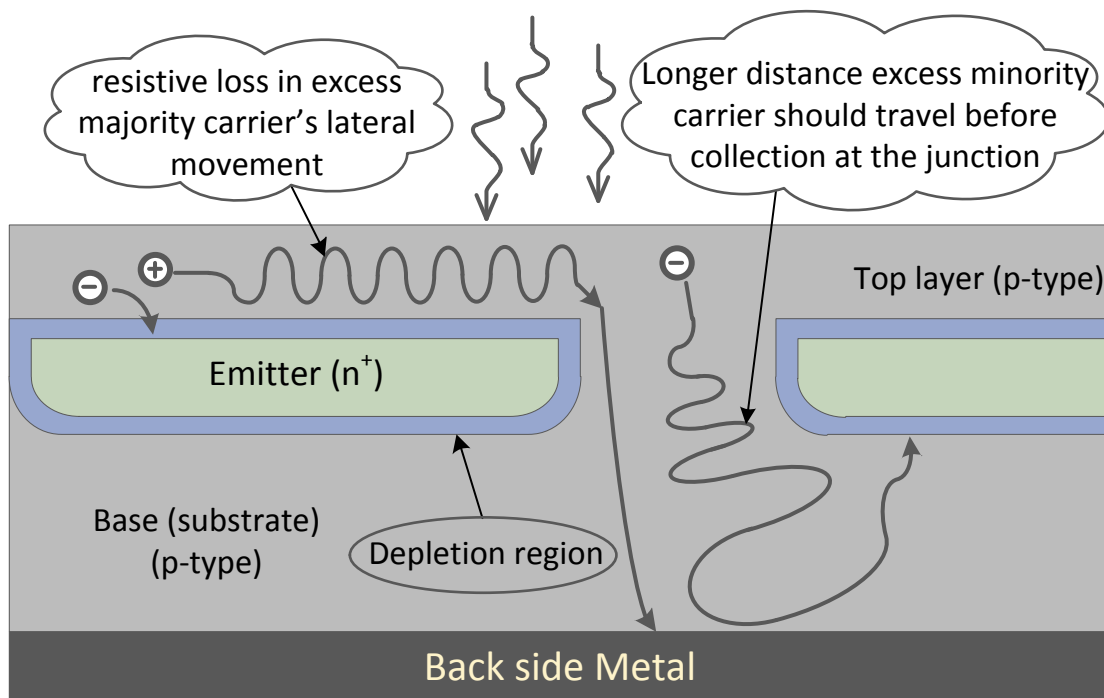


Figure 18 - schematically representation of the carrier collection mechanism and issues in the Buried-Windowed-Emitter structure.

Generated carriers in the other parts of the top layer, however, will need to diffuse a longer distance before reaching a part of the junction to be collected. This structure is optimized for better carrier collection therefore can easily attain high photo currents but for a high energy conversion an optimized

shape and size of the emitter pattern and the thickness of the top layer together with the other device parameters will be required. Excess majority carriers which are generated on top of the emitter patch in the top layer will face some ohmic resistance when moving laterally parallel to the junction until they reach to the window area. To minimize this resistive loss, the top layer's conductivity should be optimized and an emitter design with narrow emitter strips should be used.

In the next chapter we will present the computer simulations of the photovoltaic behavior of the BWE solar cell which will prove the efficacy of the proposed Buried-Windowed-Emitter cell not only for the collection of high energy photons but also for the entire spectrum if designed properly.

Chapter 3 - Computer simulation and proof of concept of the proposed novel solar cells

In order to demonstrate the efficacy of the proposed Buried-Windowed-Emitter solar cell as well as to gain insight about the impact of each design parameter on the performance of such structure, prior to fabrication, we used some computer tools to simulate the photovoltaic behavior of the Buried-Windowed-Emitter solar cell. There are several design parameters which should be optimized to make best use of this structure which include:

- (i) Thickness of the top layer
- (ii) Emitter pattern shape and emitter coverage percentage
- (iii) Emitter strip width
- (iv) Top layer doping

3.1 Simulation tools

Several CAD tools such as COMSOL, MATLAB and MEDICI were used for this simulation but the core device simulator used for the results to be presented is MEDICI. This device simulator offers easier configuration of the device for electronic simulation.

3.2 Simulation results for the three terminal solar cell

MEDICI was used to simulate the photovoltaic performance of the proposed three terminal solar cell. The results showed that using a high quality top layer will lead to increased photo-current compared to a standard cell but whether the energy conversion efficiency would rise or not will depend also on other parameters. Figure 19 shows the result of the comparison of the spectral response of the three terminal solar cells and the standard cell. It shows a boost in the current collection in mainly the short wavelength part of the spectrum and slight gain in the long wavelength part.

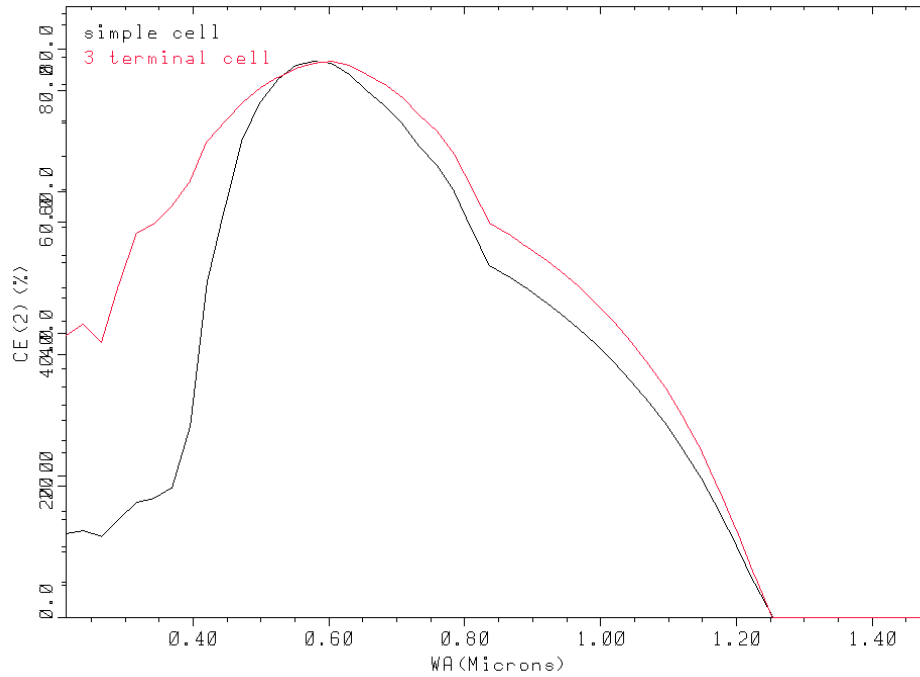


Figure 19 – comparison of the simulated spectral response of the proposed three terminal solar cell and a standard cell.

It should be noted that the energy extraction from the three terminal solar cell can be achieved in 2 ways: (i) by making a parallel connection between the top and bottom cells or (ii) by extracting power from top and bottom cell independently. The second method should give higher overall efficiencies but requires another complete set of power circuitry. Effect of the thickness of the top layer was studied for several cases and the output power was compared to that of the standard cell. Table 1 shows the results of the simulated power and photo-current for the top and bottom cells as a function of various top layer thickness. This data is to be compare to the performance data of a standard cell with similar structure which has a photo-current of $I_{sc}=26.83\text{mA}/\text{cm}^2$ and maximum output power of $P_{max}=8.99\text{ mW}/\text{cm}^2$.

The comparison shows that the overall photo-current of the three terminal cell is always higher than the standard cell but the output power can be less depending on the other parameters.

Thickness μm	I_{ph} upper mA	I_{ph} lower mA	Total I_{ph} mA	Upper cell P_{max} mW/cm^2	Lower cell P_{max} mW/cm^2	Sum of P_{max} for both cells mW/cm^2
0.05	1.05	26.36	27.41	0.1	9.03	9.13
0.1	3.82	24.4	28.25	0.87	8.32	9.19
0.2	5.59	22.77	28.36	1.27	7.72	8.99
0.3	6.1	21.8	27.9	1.26	7.38	8.64
0.5	8.7	20.24	28.95	2.06	6.81	8.87
1	12.41	17.49	29.9	3.59	5.82	9.41

Table 1 – list of the photo-current and output maximum power for the top and bottom cells in the three terminal solar cell.

3.3 Simulation model for the Buried-Windowed-Emitter solar cell

Dark and illuminated behavior of the proposed BWE solar cell structure and also that of a standard cell with very similar parameters were simulated to have the grounds for performance comparison. Figure 20 shows the two structures simulated together with the values for the important parameters used in each. For both devices, a 200 μm of thickness for the whole device is assumed and except for the differences on the top part of the device, the remaining parts are identical. Thickness of the emitter in BWE cell is chosen to be twice the thickness in the standard cell to compensate for the drop in the sheet resistance because of the smaller area. As mentioned before, less sensitivity to emitter thickness is one of the advantages BWE structure offers.

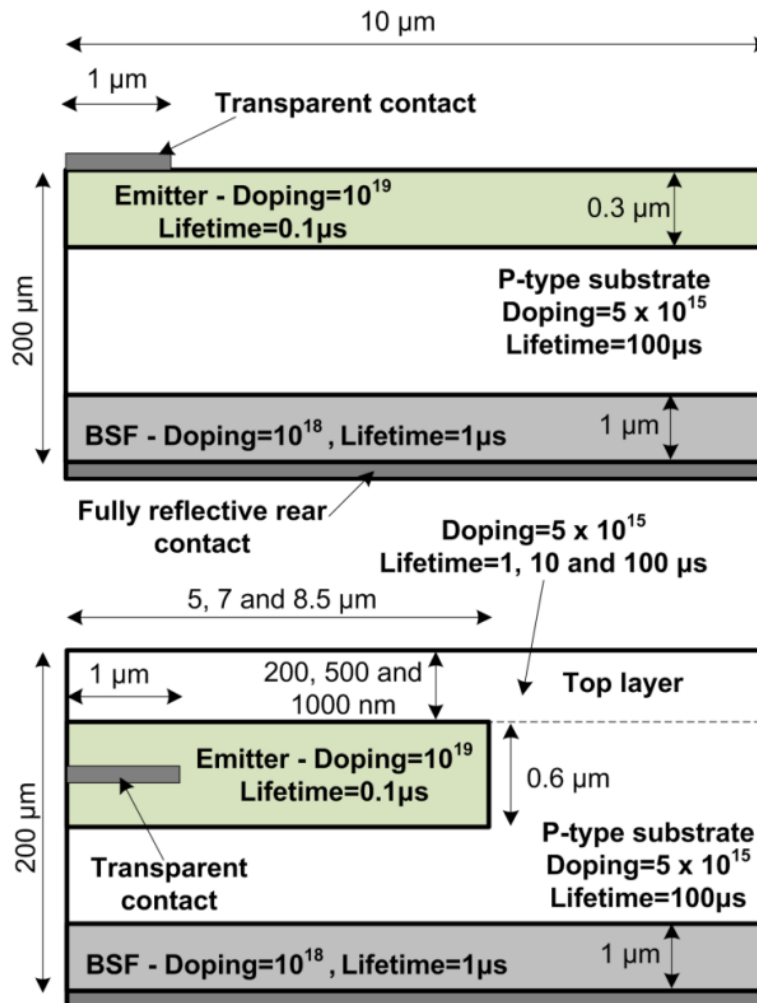


Figure 20 Geometry of the simulated structures. Top: the standard cell. Bottom: the Buried-Windowed-Emitter cell. The standard cell is chosen to have similar parameters, wherever applicable, in order to be used as a comparison basis.

The following three important parameters were swept with the values shown:

- (i) Thickness of the Top layer (200, 500 and 1000nm)
- (ii) Minority carrier lifetime in the top layer (1, 10 and 100 μ s)
- (iii) Emitter coverage percentage (50, 70 and 85%)

Values for these parameters were chosen to cover the high and low extremes of that parameter while still being practically feasible. This makes up 27 combinations of these parameters. Dark IV, illuminated IV and internal quantum efficiency were calculated for each combination of these values and, from the results, efficiency, open-circuit voltage, photo current and fill factor were extracted.

The input MEDICI code written can be found in appendix A. Concentration dependent mobility model, concentration dependent Shockley-Reeds-Hall recombination model and Auger recombination model were used for the simulation. AM1.5 spectrum with 0.1W/cm² intensity was used for illuminated behavior simulation and zero reflection was assumed on the front surface

3.4 Simulation results for the Buried-Windowed-Emitter solar cell

Figure 21 shows the simulated internal quantum efficiency (IQE) for all the devices. Compared to the blue dashed line which is the IQE for the standard cell, significant increase in the IQE is visible at almost all frequencies for all cases except the ones with 85% emitter coverage. The enhancement is more pronounced at higher photon energies as expected for most of the design parameter combinations. Superimposed on this figure is also the AM1.5 spectrum for comparison.

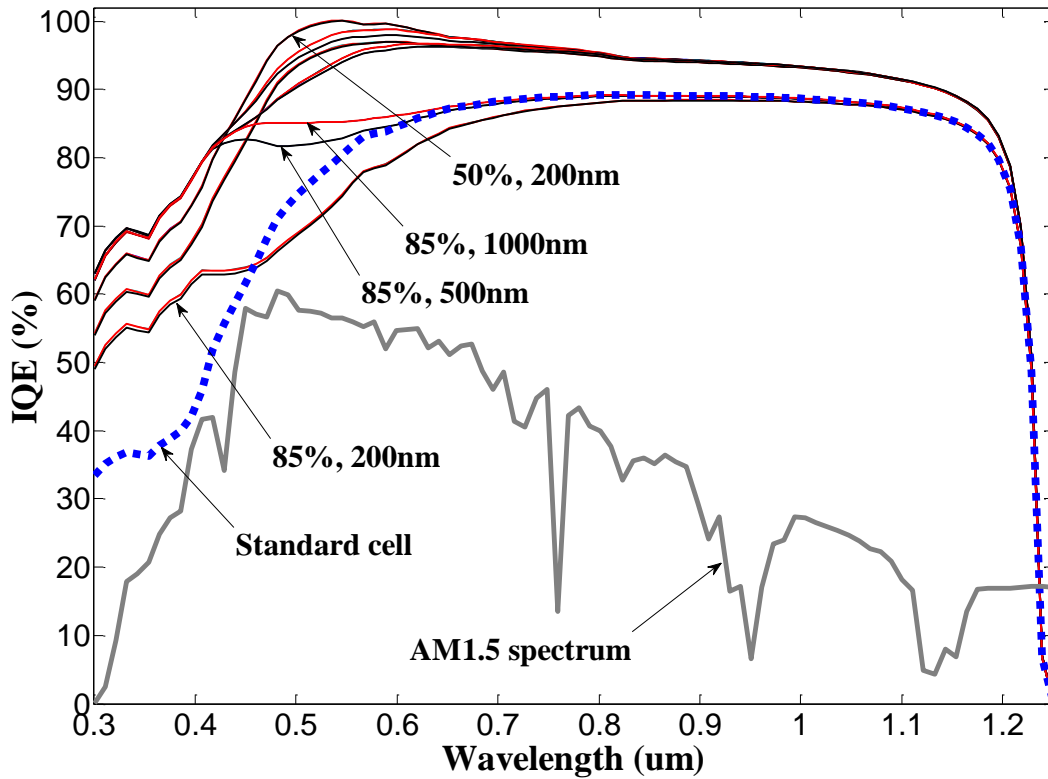


Figure 21, Simulated Internal Quantum Efficiency for the Buried-Windowed-Emitter cell with different design parameters and that of the standard cell for comparison. Am1.5 spectrum is also superimposed on the graph.

The best IQE and hence the highest short circuit current is for the case with 200nm, 50%, 100 μ s top layer, emitter coverage and minority carrier life time for the top layer respectively while the highest efficiency is for the case of (500nm, 50% , 100 μ s) for which the illuminated IV curve is shown in Figure 22. The reason for this difference could be the higher resistive losses in the thin (200nm) top layer especially when one considers the reduced effective thickness because of the extension of the depletion region into the top layer.

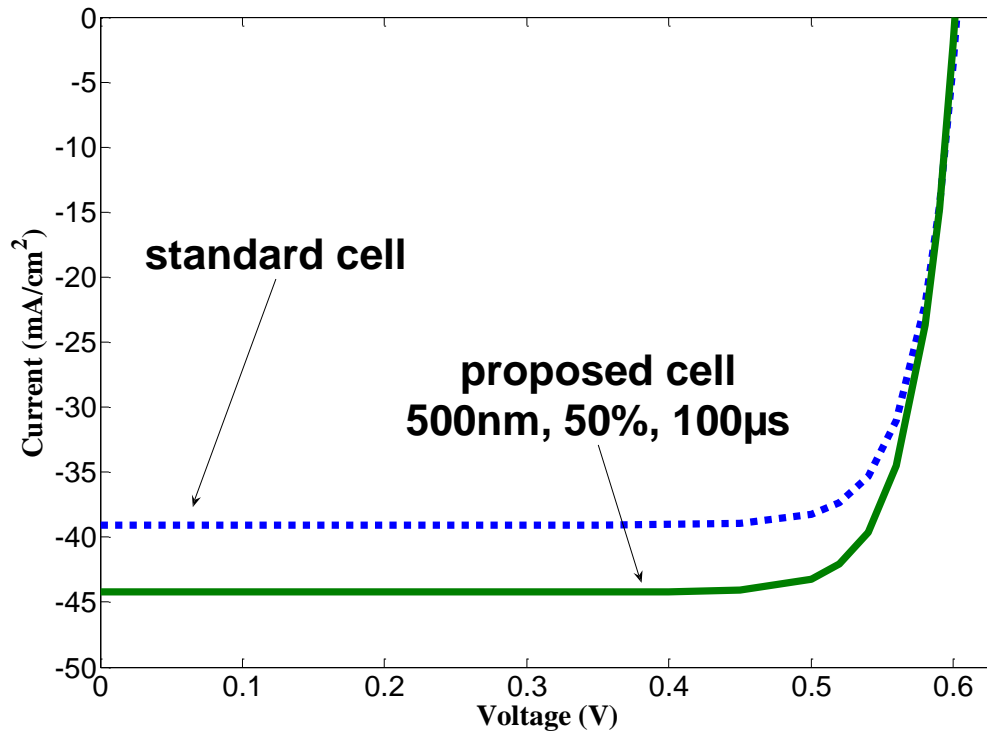


Figure 22 – simulated illuminated IV for a standard cell and a BWE solar cell under AM1.5 spectrum illumination. the predicted short circuit current of the BWE cell is close to the theoretical limit for a silicon solar cell.

Table 2 lists the important illuminated IV parameters such as maximum output power, short circuit current (I_{sc}), open circuit voltage (V_{oc}) and fill factor for all the simulated cases. In each column the highest value is highlighted for easier tracking.

To help to understand the effect of each parameter on the performance, a look at the output maximum powers of each cell separately might be helpful. Figure 23 shows groups of plots of maximum output power versus the changes in only one parameter. Surprisingly, upper layer's minority carrier lifetime is not extremely important and a value as low as $1\mu s$ (which can be easily achieved in reality) leads to satisfactory performance. The more important parameters are the emitter coverage and top layer thickness for each of which there seems to be an optimum value. For very thin thicknesses of the top layer, not only lateral resistivity problem rises but also the light absorption in that layer reduces while at very high thicknesses, lifetime of the top layer would be a limiting factor.

Table 2, list of the important illuminated IV parameters for all the simulated cases. Maximums of each column are highlighted.

Top layer thickness	Emitter coverage	Lifetime in top layer	Max output power (MW/cm ²)	I _{sc} (mA/cm ²)	V _{oc} (V)	FF (%)
200nm	50%	100μs	21.4743	44.4019	0.6004	80.5573
200nm	50%	10μs	21.4668	44.4001	0.6003	80.5418
200nm	50%	1μs	21.3923	44.382	0.5995	80.4035
200nm	70%	100μs	21.0415	43.7718	0.5993	80.216
200nm	70%	10μs	21.0327	43.7681	0.5992	80.2007
200nm	70%	1μs	20.9446	43.7313	0.5983	80.0442
200nm	85%	100μs	18.6109	39.0567	0.5953	80.0511
200nm	85%	10μs	18.6042	39.0511	0.5952	80.0438
200nm	85%	1μs	18.5375	38.9961	0.5944	79.9679
500nm	50%	100μs	21.8853	44.2279	0.6012	82.312
500nm	50%	10μs	21.8698	44.2273	0.601	82.2823
500nm	50%	1μs	21.7144	44.2214	0.5987	82.0146
500nm	70%	100μs	21.7989	44.0915	0.6007	82.303
500nm	70%	10μs	21.7813	44.0913	0.6005	82.2644
500nm	70%	1μs	21.6055	44.09	0.5981	81.9307
500nm	85%	100μs	19.9957	40.6387	0.598	82.2743
500nm	85%	10μs	19.9765	40.6387	0.5978	82.2315
500nm	85%	1μs	19.7847	40.6385	0.5953	81.776
1μm	50%	100μs	21.6339	43.7413	0.6008	82.3163
1μm	50%	10μs	21.6081	43.7402	0.6004	82.2737
1μm	50%	1μs	21.3507	43.7292	0.596	81.9269
1μm	70%	100μs	21.577	43.6603	0.6004	82.3112
1μm	70%	10μs	21.5492	43.6601	0.6	82.2584
1μm	70%	1μs	21.2715	43.6574	0.5954	81.8321
1μm	85%	100μs	20.1704	40.9712	0.5982	82.2993
1μm	85%	10μs	20.1409	40.9712	0.5977	82.2484
1μm	85%	1μs	19.8458	40.9705	0.5933	81.6408
Standard cell			19.4	39.05	0.602	82.2

For very high emitter coverage factors, the electrical connection between the top layer and bulk will face problems and also because of the increased junction area (top and below the emitter layer) and hence the saturation current, open circuit voltage will drop while for very low emitter coverage factors, both top layer and bulk minority carrier lifetime needs to increase to compensate for the increased average distance to the junction. Thicker emitter stripes will also be necessary to compensate for the reduced conductivity of the emitter layer. The parameters used for simulation are not necessarily the optimum values for the highest performance of the solar cell. Typical close to optimum values are chosen only to prove the improvement this structure offers.

Figure 23 shows the conversion efficiency of all the simulated cases in three different plots. Each plot shows the curves for the conversion efficiency as a function of only one variable while the other two variables are considered as plot parameters. This way, it is easier to see the effect of each design parameter on the performance of the Buried-Windowed-Emitter solar cell.

The top plot shows the curves of maximum output power versus emitter coverage. The shape of the curve proposes the lower (among the simulated values) values of coverage for better conversion efficiency. The middle plot shows the curves of maximum output power versus the thickness of the top layer. It proposes that there might be an optimum value for the thickness of the top layer. The bottom plot shows the curves of maximum output power versus the lifetime in the top layer. The interesting fact about these curves is that it shows that the value of the minority carrier lifetime in the top layer is not a very critical value for the performance as long as it is above $1\mu\text{s}$ (the minimum value simulated). This is good news for the fabrication of the BWE solar cell since it is not too difficult to achieve minority carrier lifetime in this range using high performance epitaxial deposition techniques.

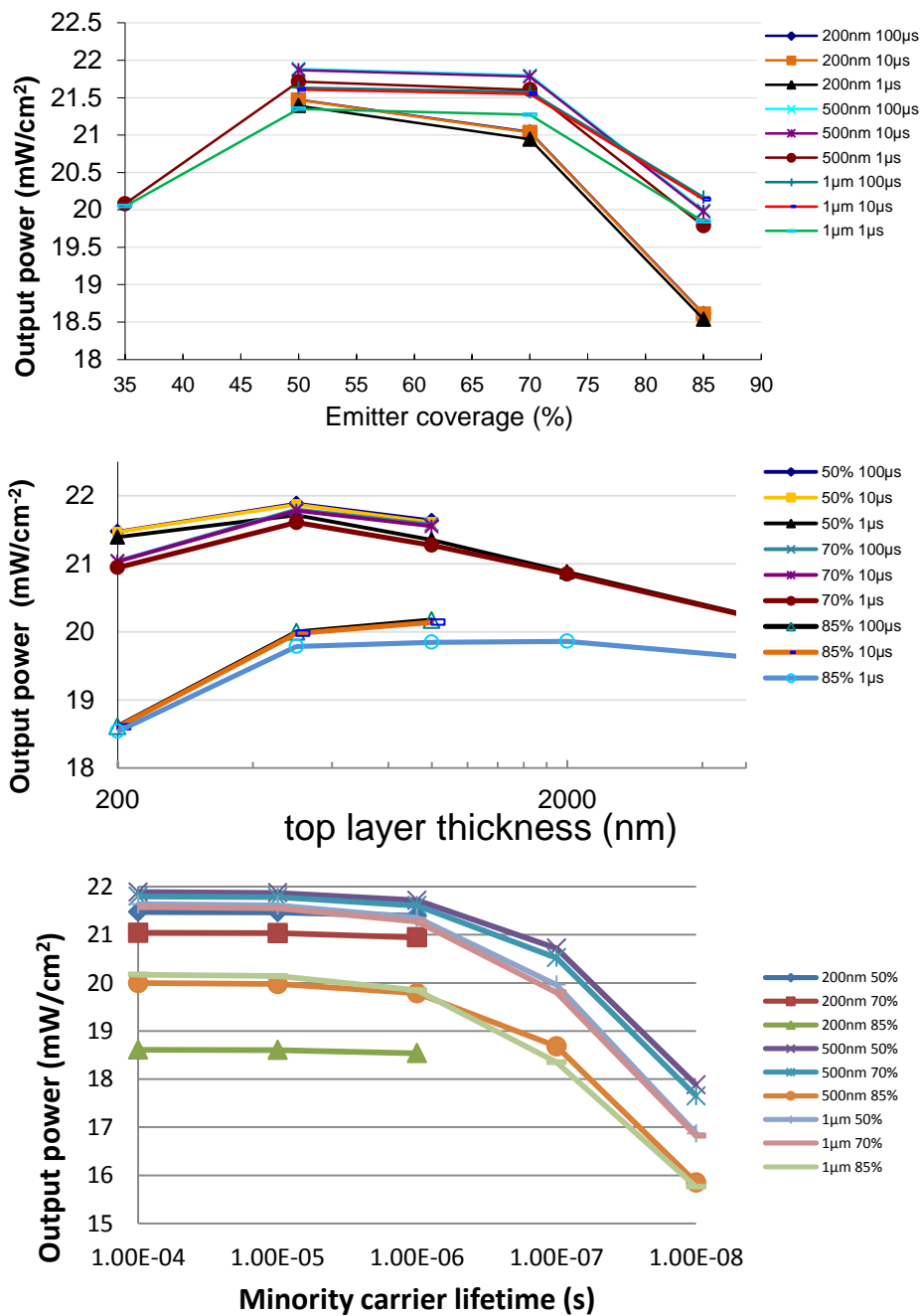


Figure 23, Top: curves of maximum output power versus emitter coverage. Lower coverage percentage seems to be favorable for better conversion efficiencies. Middle: curves of maximum output power versus the thickness of the top layer. Although low thicknesses give rise to better spectral response but because of the series resistance issues due to the limited sheet resistance of the top layer, higher thicknesses end up giving better efficiencies and there seems to be an optimum value for the thickness. Bottom: curves of maximum output power versus the lifetime in the top layer. Very slight drop in the efficiency is observed for the 2 orders of magnitude drop in the lifetime.

Chapter 4 – Development of an analytical model for the proposed BWE solar cell

The Buried-Windowed-Emitter cell structure is a complicated structure for accurate analytical modeling as it is a three dimensional structure and the usual one dimensional method of modeling a PN junction cannot be used directly. However considering the periodicity of the structure, one might be able to create an analytical model for a unit cell of this periodic structure and approximate the whole cell's behavior by a proportional scaling of the behavior of the unit cell. In this chapter, an attempt to analytically model the BWE solar cell structure will be presented based on this periodicity simplification.

4.1 Representative model for the BWE structure

A qualitative description of how BWE cell is operating will give good starting point and direction for the modeling presented. Figure 24 shows the schematic of the cell's cross section. As explained also in chapter-2, one can distinguish two PN junction diodes in this structure sharing the same emitter region. Let's name these two diodes as "top diode" for the diode made of the top layer and the emitter layer and "bottom diode" for the diode made of the emitter layer and the bulk.

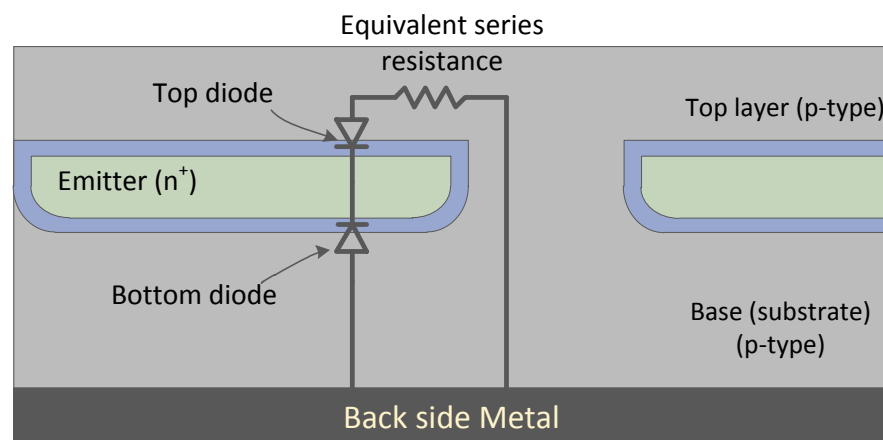


Figure 24 – schematic of the cross section of the BWE solar cell showing the possibility of distinguishing two junctions in the internal structure of it. Super imposed is the representative circuit level model of this structure.

These two diodes are internally interconnected in parallel as they share an emitter and the bases are connected via the windows in the emitter, as a result, the simple circuit diagram shown in Figure 25 will be a proper approximate model. It should be noted that the top diode and the series resistance R_{eq-top} are just lumped equivalents for the spread diode and the series resistance each portion of the diode sees.

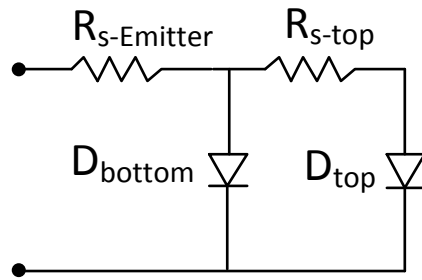


Figure 25 – simple circuit level model extracted from the qualitative explanation of the operation of the BWE solar cell.

4.1.1 Description of the unit cell

To find out how we can find an expression for the parameters of this model, let's first consider the periodic structure of the BWE cell shown in Figure 26 as the pattern of the windowed emitter. Square periodic windows are the same pattern used for cell fabrication which will be discussed in future chapters. A unit cell is highlighted by dashed lines around it and since there is symmetry in each unit cell, one eighth of the cell is enough to be considered. The trapezoid shown in Figure 27 is emitter part of the one eighth of the unit cell. A reasonable assumption is that the lateral resistance will only be considerable in those portions of the top layer which are on top of the emitter. This means that we can assume that as soon as the carriers traveling from on top of the emitter reach to the edge of the window, they won't feel a considerable resistance as they find their way to the back contact.

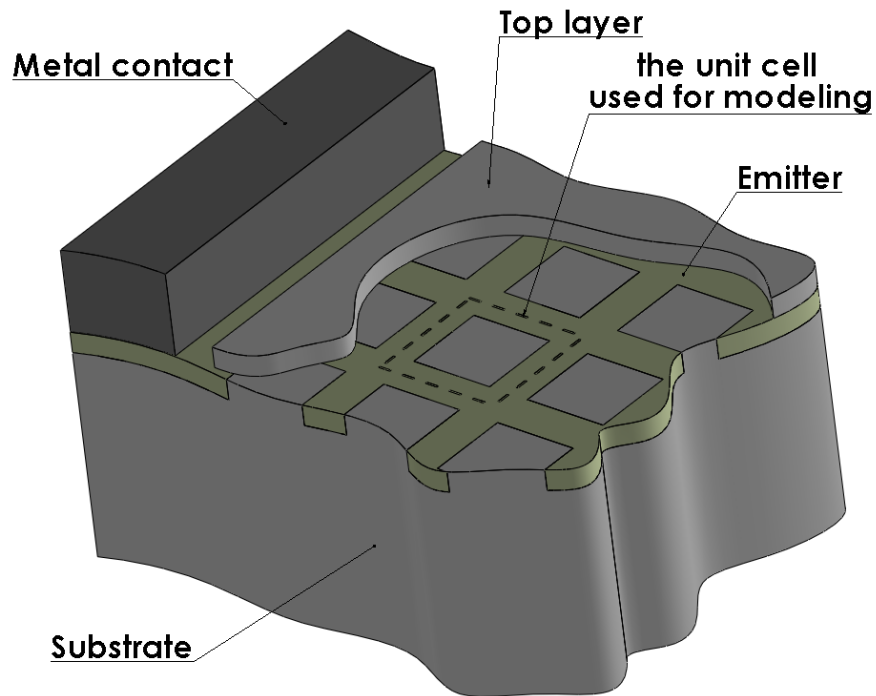


Figure 26 – schematic of the Buried-Windowed-Emitter solar cell used to define the unit cell in the pattern of the emitter.

4.1.2 Methodology used to develop the model

To start the analysis, first consider the infinitesimal portion of width dx at point x indicated in Figure 27. First we do a simplifying assumption which makes a one dimensional analysis possible. It is obvious that the current generated at the top of this slab, sees a different resistance on its way to the edge of the window than what the current generated at the bottom of the slab sees. But equivalently we can lump all the currents from the whole slab and assume that the whole current goes through one resistor. This is equivalent to the assumption that the slab shown in the figure is equipotential which is not far from reality for the low currents at which this photovoltaic device will operate. Later on we will have a more qualitative justification for this equipotential assumption.

This slab is a diode of area A and has a resistance of R for conduction parallel to x axis between the two neighboring slabs at points $x=x_0+dx$ and $x=x_0-dx$.

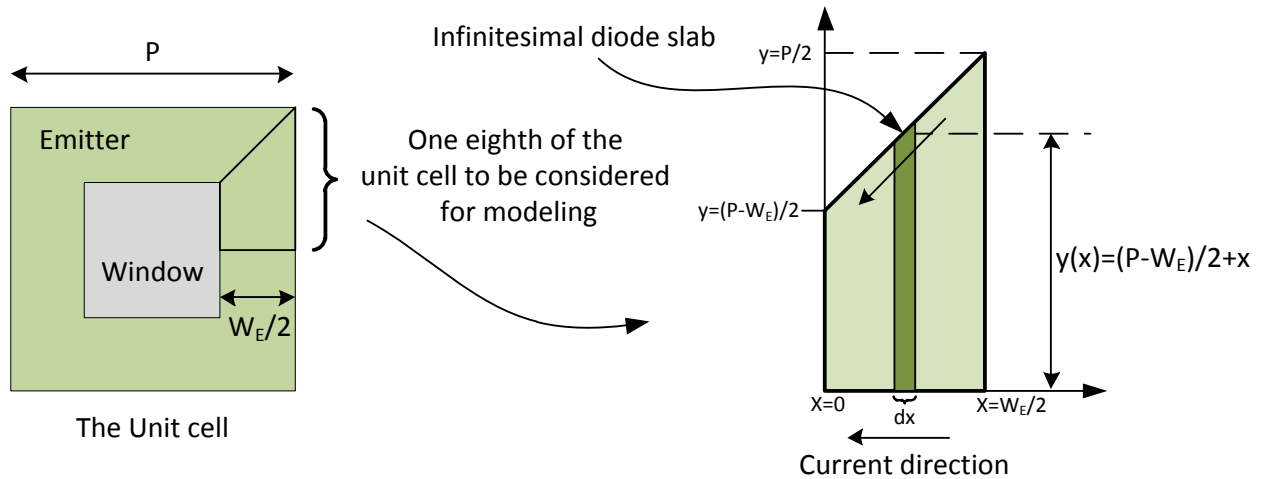


Figure 27 – left: the schematic of the square shaped unit cell representing the periodic structure of the windowed emitter. right: the trapezoid representing the one eighth of the unit cell. Because of the symmetry, the model will assume that this trapezoid is the most primitive building block of the structure being modeled.

Extending this logic to all the trapezoidal area, one can imagine that the whole trapezoidal area is composed of infinitesimal diodes connected in parallel using infinitesimal resistors. An equivalent circuit of this spread diode is shown in Figure 28. Since we are interested in the photovoltaic behavior of this device, one can add a current source in parallel to each infinitesimal diode to model the photo generated current from each diode as well. Adding the second diode in the model of each diode won't change the final results for us, and as a result is omitted for simplicity. Also omitted is the shunt resistance for each infinitesimal diode as shunt resistance is not necessarily a uniform function of area and can happen because of randomly spread defects. A lumped shunt resistance can be used to model the shunting of the whole area.

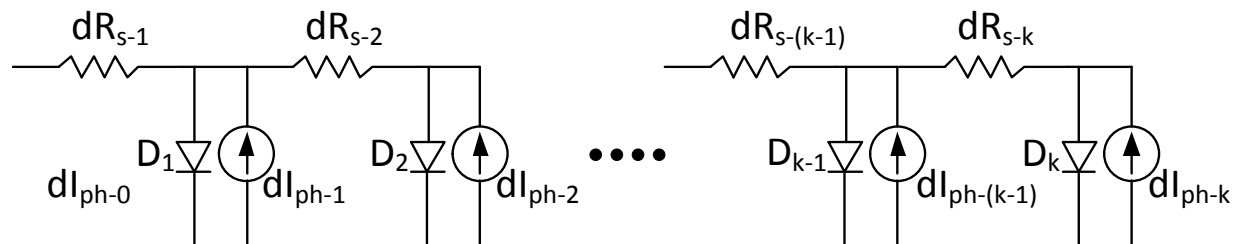


Figure 28 – the equivalent circuit of the spread diode of the top layer represented by infinitesimal diodes, series resistors and the current sources representing the photo-current.

To the best of author's knowledge, the equivalent circuit shown in Figure 28 cannot be reduced into a limited number of lumped elements since during any attempts to do so, one would come across to summations of exponential terms with different exponents (because of the different diodes with different bias voltages) which as a generally known practice, can't be lumped into a single expression. However, as we will see soon, using a reasonable simplifying assumption, one can make a lumped model

to represent the equivalent power loss in the series resistance of this device, which is what we are more interested anyways.

4.2- formulation of the model equations

Imagine that we want to have an equivalent circuit of the form shown in Figure 29 to represent the top diode.

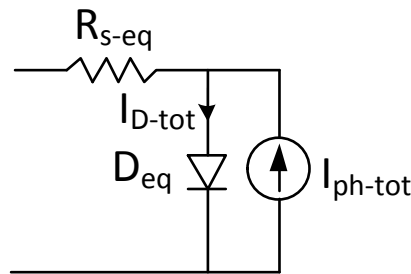


Figure 29 – the target equivalent circuit to be considered for the top diode. The values of the parameters of this equivalent circuit should be calculated using the values of the equivalent circuit shown in Figure 28 to make them equivalent.

The power dissipation in the equivalent series resistance is:

$$P_{loss-eq} = R_{s-eq} (I_{ph-tot} - I_{D-tot})^2 \quad Eq. 1$$

Where, I_{ph-tot} is the overall photo-current extracted from the whole trapezoid and, likewise, I_{D-tot} is the total diode current passing through the junction excluding the photo generated current.

But, let's see what we can get for the resistive power loss for the circuit shown in Figure 28. In this spread diode representation, the current passing through the infinitesimal resistor of dR_{s-i} corresponding to an infinitesimal diode slab at point x can be expressed as:

$$I_{@dR_{s-i}} = \int_x^{\frac{W_E}{2}} (dI_{ph}(x) - dI_D(x)) \quad Eq. 2$$

Which is the sum of the infinitesimal photo currents generated between points x and $\frac{W_E}{2}$ minus the sum of the infinitesimal diode currents in between the same two points. Using this current, the power loss in the infinitesimal resistor dR_{s-i} will be:

$$P_{loss-@dR_{s-i}} = dR_{s-i} \left(\int_x^{\frac{W_E}{2}} (dI_{ph}(x) - dI_D(x)) \right)^2 \quad Eq. 3$$

Thus, the total power loss in all the infinitesimal resistors can be expressed as:

$$P_{loss-tot} = \int_0^{\frac{W_E}{2}} dR_{s-i} \left(\int_x^{\frac{W_E}{2}} (dI_{ph}(x) - dI_D(x)) \right)^2 \quad Eq. 4$$

Which is simply the sum of all the infinitesimal losses in between points $x=0$ and $\frac{W_E}{2}$.

To proceed with this integral let's replace all the known terms. dR_{s-i} at point x is a slab like resistor with a length of dx and the cross sectional area of $T \cdot y(x)$, where T is the thickness of the top layer and $y(x)$ is the width of the slab at point x as shown in Figure 27, therefore we get:

$$dR_{s-i} = \frac{\rho dx}{T y(x)} = \frac{\rho dx}{T \left(\frac{P - W_E}{2} + x \right)} \quad Eq. 5$$

Where, ρ is the resistivity of the top layer.

The photo-current due to collection from a uniformly thick top layer and some part of the emitter can be expressed in terms of an absorption-dependent function times the area of the diode under consideration, so, we can write:

$$dI_{ph}(x) = f_{abs}(T, \tau) \cdot y(x) \cdot dx \quad Eq. 6$$

Where $f_{abs}(T, \tau)$ is a function representing the amount of photo-current generation in a semiconductor of thickness T and a minority carrier lifetime of τ under a certain illumination (e.g. AM1.5). What matters here is that this function is independent of x . for crystalline silicon; one can calculate this function using the absorption coefficient of crystalline silicon and the spectrum of the AM1.5 solar irradiation, as has been shown in Figure 15 of chapter-2.

For the diode current $dI_D(x)$, we will have to make a simplifying but reasonable assumption. We know that the infinitesimal diodes at different x locations will have a different bias voltage because of the

resistive voltage drop on the top layer because of lateral current conduction. But how considerable will this voltage drop be? To have an estimate, let's consider a worst case scenario with parameters in the practical range. Assume we have a top layer of $1\mu\text{m}$ thick crystalline silicon and $1\Omega\text{cm}$ resistivity to assure a good film quality. Let's assume the emitter strip width $W_E = 30\mu\text{m}$ and a unit cell Pitch of $P=50\mu\text{m}$. using Figure 15 of chapter-2 An upper bound for the current generated in a $1\mu\text{m}$ silicon slab can be estimated to be around 15mA cm^{-2} . The area of the trapezoid is $\frac{W_E}{4} (p - \frac{W_E}{2})$ which will lead to a total photo-current of 39.3nA from the area being considered. Let's assume pessimistically that all this current will pass through the total resistance of the one eighth of the unit cell shown in Figure 27, which can be calculated to be as:

$$R_{all} = \int_0^{\frac{W_E}{2}} \frac{\rho dx}{T \cdot (\frac{P - W_E}{2} + x)} = \frac{\rho}{T} \ln \left(x + \frac{P - W_E}{2} \right) \Bigg|_0^{\frac{W_E}{2}} = \frac{\rho}{T} \ln \left(\frac{p}{p - W_E} \right) \quad \text{Eq. 7}$$

This resistor will have a value of $9.16\text{k}\Omega$ for the parameters assumed above. The voltage drop on the two ends of the slab will be only 0.36mV . This small voltage difference between the infinitesimal diodes of our analysis, justifies the critical simplification of assuming that for the current ranges of interest for photovoltaic action, the bias voltages of these infinitesimal diodes are the same and as a result x dependence of $dI_D(x)$ is only due to the change of the area of the infinitesimal diode as a function of x. so we can write:

$$dI_D(x) = y(x) \cdot dx \cdot J_0 \left(e^{\frac{V}{n_t V_T}} - 1 \right) \quad \text{Eq. 8}$$

Where J_0 is the saturation current density of the diode of the structure under consideration and n_t is the ideality factor of the top diode and V is the voltage at the edge of the window area.

Now we can replace $dI_{ph}(x)$ and $dI_D(x)$ from Eq.6 and Eq.8 respectively into Eq.2 to solve for the current in the infinitesimal resistor at point x. we get:

$$\begin{aligned} I_{@dR_{s-i}} &= \int_x^{\frac{W_E}{2}} \left(f_{abs}(T, \tau) \cdot y(x) \cdot dx - y(x) \cdot dx \cdot J_0 \left(e^{\frac{V}{n_t V_T}} - 1 \right) \right) \\ &= \left(f_{abs}(T, \tau) - J_0 \left(e^{\frac{V}{n_t V_T}} - 1 \right) \right) \cdot \int_x^{\frac{W_E}{2}} y(x) \cdot dx \\ &= \text{Cte.} \left[\frac{W_E}{4} \left(P - \frac{W_E}{2} \right) - \frac{p - W_E}{2} x - \frac{x^2}{2} \right] \end{aligned} \quad \text{Eq. 9}$$

Where,

$$\text{Cte.} = f_{abs}(T, \tau) - J_0 \left(e^{\frac{V}{n_t V_T}} - 1 \right) \quad \text{Eq. 10}$$

has been used to represent the parts of the expression which are independent of x for simplicity. Replacing current from Eq.9 into Eq.4 will give the total power loss in the top layer due to lateral current conduction as:

$$P_{loss-tot} = Cte.^2 \int_0^{\frac{W_E}{2}} \left(\frac{W_E}{4} \left(P - \frac{W_E}{2} \right) - \frac{P - W_E}{2} x - \frac{x^2}{2} \right)^2 \frac{\rho dx}{T. \left(\frac{P - W_E}{2} + x \right)} \quad Eq. 11$$

After some tedious but straight forward work, Eq.11 results in:

$$P_{loss-tot} = \frac{\rho(Cte.)^2}{128T} \left(-W_E^4 + 2PW_E^3 - P^2W_E^2 - 2P^3W_E + 2P^4 \ln\left(\frac{P}{P - W_E}\right) \right) \quad Eq. 12$$

Now to find the equivalent series resistor as shown in Figure 29, we can equate Eq.12 to Eq.1. But before that we need to find the expression for the I_{ph-tot} and I_{D-tot} in the equivalent circuit of Figure 29. The photo-generated current (I_{ph-tot}) can be expressed as the area of the trapezoid times the same $f_{abs}(T, \tau)$ function used for previous analysis. Similarly, the diode current (I_{D-tot}) can be expressed as the area of the trapezoid times the current density of the diode assuming that the whole diode is operating under an identical bias voltage. Therefore we have:

$$I_{ph-tot} = Area. f_{abs}(T, \tau) = \frac{W_E}{4} \left(P - \frac{W_E}{2} \right) f_{abs}(T, \tau) \quad Eq. 13$$

$$I_{D-tot} = Area. J_0 \left(e^{\frac{V}{n_t V_T}} - 1 \right) = \frac{W_E}{4} \left(P - \frac{W_E}{2} \right) \cdot J_0 \left(e^{\frac{V}{n_t V_T}} - 1 \right) \quad Eq. 14$$

Now we can rewrite Eq.1 using the values from Eq.13 and Eq.14:

$$\begin{aligned} P_{loss-eq} &= R_{s-eq} (I_{ph-tot} - I_{D-tot})^2 = R_{s-eq} \left(\frac{W_E}{4} \left(P - \frac{W_E}{2} \right) \right)^2 \left(f_{abs}(T, \tau) + J_0 \left(e^{\frac{V}{n_t V_T}} - 1 \right) \right)^2 = \\ &= R_{s-eq} \cdot (Cte.)^2 \cdot \left(\frac{W_E}{4} \left(P - \frac{W_E}{2} \right) \right)^2 \end{aligned} \quad Eq. 15$$

Now by equating $P_{loss-eq}$ from Eq.15 to $P_{loss-tot}$ from Eq.12 we can solve for the equivalent series resistance R_{s-eq} as:

$$P_{loss-tot} = P_{loss-eq}$$

$$\begin{aligned}
 &\equiv \frac{\rho(Cte.)^2}{128T} \left(-W_E^4 + 2PW_E^3 - P^2W_E^2 - 2P^3W_E + 2P^4 \ln\left(\frac{P}{P-W_E}\right) \right) \\
 &= R_{s-eq} \cdot (Cte.)^2 \cdot \left(\frac{W_E}{4} \left(P - \frac{W_E}{2} \right) \right)^2 \\
 \rightarrow R_{s-eq} &= \frac{\frac{\rho}{128T} \left(-W_E^4 + 2PW_E^3 - P^2W_E^2 - 2P^3W_E + 2P^4 \ln\left(\frac{P}{P-W_E}\right) \right)}{\left(\frac{W_E}{4} \left(P - \frac{W_E}{2} \right) \right)^2}
 \end{aligned}$$

Which simplifies to:

$$R_{s-eq} = \frac{\rho}{2T} \frac{\left(-W_E^4 + 2PW_E^3 - P^2W_E^2 - 2P^3W_E + 2P^4 \ln\left(\frac{P}{P-W_E}\right) \right)}{W_E^4 + 4P^2W_E^2 - 4PW_E^3} \quad Eq. 16$$

From one eighth to a full unit cell: we calculated the equivalent series resistor, photo-current and diode current of one eighth of a unit cell, but since the 8 trapezoidal diodes making the unit cell (one of which was analyzed) are operating equivalent to parallel to each other (not because of real physical parallel connection but because of symmetry), the photo-current and diode current of the unit cell equivalent circuit will be those of one trapezoid (Eq.13 and Eq.14) multiplied by 8 and the equivalent series resistor of one unit cell will be that of one trapezoidal diode (Eq.16) divided by 8.

From one unit cell to the whole BWE cell: assume that a BWE solar cell of total Area A_{tot} is tiled by the unit cells of our former analysis all over except where the top metal contacts lie. These unit cells are not physically in parallel, but because of the identical structure and conditions they will be operating at (assuming uniform illumination), they can be considered equivalent to being in parallel and hence their photo and diode currents will add up and the equivalent series resistor representing all the unit cells will be that of one unit cell divided by the number of the unit cells tiling the whole area.

Note that so far we have been trying to find an equivalent circuit model for only the top diode. The bottom diode can be modeled using the standard one dimensional diode model with modified junction area and modified carrier collection behavior. If we assume we can model the bottom diode using the standard method, the whole BWE cell can be modeled using the equivalent circuit shown in Figure 30 where top and bottom diodes are connected in parallel to each other using the equivalent top layer resistance.

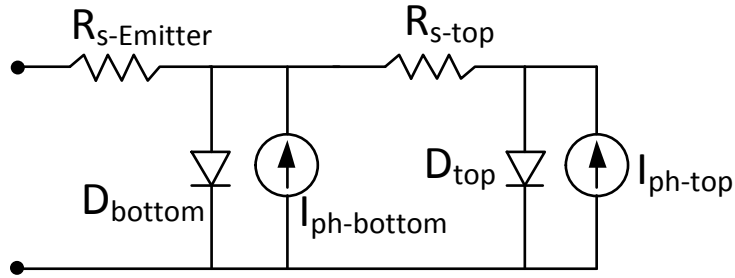


Figure 30 – the equivalent circuit of the whole BWE solar cell including the top and bottom diodes together with series resistances and photo-currents of each.

The parameters for the top diode part of the circuit are as follows:

$$I_{ph-top} = N_t W_E (2P - W_E) f_{abs}(T, \tau) \quad Eq. 17$$

$$I_{D-top} = N_t W_E (2P - W_E) \cdot J_{0t} \left(e^{\frac{V}{n_t V_T}} - 1 \right) \quad Eq. 18$$

$$R_{s-eq-top} = \frac{1}{N_t} \frac{\rho}{16T} \frac{\left(-W_E^4 + 2PW_E^3 - P^2W_E^2 - 2P^3W_E + 2P^4 \ln\left(\frac{P}{P - W_E}\right) \right)}{W_E^4 + 4P^2W_E^2 - 4PW_E^3} \quad Eq. 19$$

$$N_t = \frac{Area_{cell} - Area_{contact}}{Area_{unit-cell}} = \frac{A_{cell} - A_{contact}}{P^2} \quad Eq. 20$$

Where N_t is defined as the number of the unit cells covering the whole cell area.

So we were able to breakdown the complicated structure of the BWE solar cell into two diodes which are inherently connected through the structure of the cell. The method used to propose a lumped equivalent circuit for the top diode was by equating the total resistive loss in the top layer due to the distributed current flow to the loss in a lumped equivalent resistor carrying the same total current.

As a future work, this model can be further expanded to include semi-analytical expressions for the photo-currents of the top and bottom diodes by numerical solution of continuity equation in the BWE fitting a descriptive model to the results.

Chapter 5 - Technology development for low temperature Silicon epitaxy

In order to realize the proposed Buried-Windowed-Emitter solar cell, a technology for a high quality epitaxial silicon film deposition with controlled doping is required. Epitaxial silicon technology of silicon is clearly capable of producing epitaxial films of very high quality; however this technology is mostly reliant on the high temperature of the growing surface. Because of the structure of the BWE solar cell, high temperature processes after the formation of the windowed emitter is to be avoided as the dopant redistribution during any high temperature step can lower the control over the architecture of the cell especially the definition of the emitter. High temperature processes are indeed not very welcome in solar cell industries because of the possibility of the diffusion of the impurities into the substrate and resultantly a deteriorated minority carrier lifetime of the bulk material which is among the most important parameters determining the performance limits of a solar cell. Wherever a high temperature step is unavoidable for a solar cell, ultra clean environments are required which lead to an increased cost of the fabrication.

The epitaxial silicon process useful for the fabrication of the BWE solar cell must be of low to medium (maximum 750°C) temperature nature limited by the dopant redistribution constraint. In the last decade, there have been reports of epitaxial silicon deposition at low temperatures (less than 500°C) [30-36] using Plasma Enhanced Chemical Vapor Deposition (PECVD) or CVD which usually state possibility of growing a thin epitaxial silicon on silicon substrates. This technique, even though still immature and in need of further improvement, was the most attractive option for us because of the following reasons:

- (i) It is of low temperature nature and, as mentioned above, very appealing for a low thermal budget step in solar cell fabrication
- (ii) Relative freshness of the topic of low temperature epitaxy using PECVD and limited literature resources available for it and possibility of expanding its horizon during this research
- (iii) Availability of the required deposition tool in Center for Advanced Photovoltaic Devices and Systems (CAPDS)

This chapter presents the work done to achieve high quality epitaxial film with controlled doping profiles using Plasma Enhanced Chemical Vapor Deposition. Findings and novelties used in the deposition and characterization of the develop technology is discussed in detail. The following topics are discussed:

- Some theoretical concepts describing what leads to epitaxy at such low temperatures are presented.
- Description of the PECVD tool used for this purpose is given
- Chamber preparation prior to film deposition is described
- Process details and results of the experiment to produce n-type, intrinsic and p-type epitaxial films are presented
- Dependency of the epitaxy on the crystallographic orientation of the growing surface is discussed
- Assessment of quality of the crystalline films using reflection spectra is proposed and the results are presented.
- The study done on the effects of post deposition annealing on the electrical and structural quality of the deposited films is presented.
- Capability of the developed technology for super lattice formation is demonstrated.

5.1 Theoretical background leading to the new epitaxial silicon process

Research groups working on silicon film deposition on crystalline silicon substrates have long noticed the occurrence of some epitaxial film deposition close to the interface with the substrate [20,21] and [24,25]. Conditions, for which one can achieve epitaxial films, are surprisingly broad; however these films tend to lose their epitaxial nature after a certain thickness. The reason for this limit in epitaxial film thickness is believed to be the gradual development of defects and crystal faults which leads to termination of epitaxy when the underlying surface has reached to a critical level of deviation from perfect crystalline surface. [23]

There are two factors believed to be responsible for low temperature PECVD epitaxy:

- (i) Increased surface mobility of the precursors at the growing surface due to hydrogen passivation of the growing surface. This feature, although beneficial for the existence of the epitaxy, has a drawback by nature; it causes the incorporation of hydrogen atoms in the epitaxial film.
- (ii) Hydrogen plasma etching of the weakly bonded silicon atoms which have likely bonded in a crystallographically unfitting site. The result is a mechanism similar to the “survival of the fittest” or the “elimination of the weakest”.

Almost all reports of epitaxial film deposition using PECVD indicate a minimum Hydrogen dilution for the onset of epitaxy or else the resulting film will be amorphous, nano-crystalline or micro-crystalline.

5.1.1 Role of Hydrogen

Low temperature PECVD epitaxy owes its feasibility to the hydrogen diluted plasma. Existence of Hydrogen in the deposition environment of the PECVD has the following effects:

- (i) The major role of hydrogen in epitaxy using PECVD is the etchings of the weakly bounded silicon atoms which haven't had the chance to bond in a more crystallographically favorable site due to low surface mobility of the adatoms at low temperatures. This might also explain why epitaxial film growth on <111> crystallographic surfaces has not been reported yet. Hydrogen plasma has a lower etch rate of silicon on <111> orientation compared to <100> [26] which leads to retardation of hydrogen's major role in PECVD epitaxy.
- (ii) Hydrogen's second role is to partially increase the surface mobility of the adatoms on the growing surface by passivating the dangling bonds of the surface. This role, however, could adversely affect the quality of the epitaxy if the amount of hydrogen exceeds certain value. Too much hydrogen in the plasma will passivate the surface to an extent that will separate the underlying surface from the new coming adatoms. This will stop the effect of the crystal atoms in positioning of the new coming atoms. The result will be the transition of the deposition phase to amorphous. Another adverse consequence of excessive hydrogen passivation of the growth surface is that there will be more hydrogen atoms trapped in the crystal matrix which will increase the hydrogen content of the growing film. Excess hydrogen content will deviate the film structure from pure silicon crystal and eventually will lead to loss of epitaxy.

We have noticed that there is an inverse correlation between how much hydrogen is trapped in the deposited film (even if fully crystalline) and how high quality the epitaxial film is.

5.1.2 Role of temperature

Substrate temperature contributes in epitaxial film deposition in three ways:

- (i) Increasing temperature leads to higher surface mobility of the adatoms on the growth surface. Although this is favorable for epitaxial film growth, the increased surface mobility solely because of increased temperature is not enough for a successful epitaxy unless the substrate temperature exceeds the medium temperature range (more than 650°C).
- (ii) Hydrogen plasma etching of silicon is stronger at lower temperatures [27]. In the low temperature range that we have focused on, even though increasing the temperature enhances the surface mobility, for a successful epitaxy, temperature dependent behavior of the other phenomena involved in epitaxy should also be considered. As mentioned above, the main mechanism which makes epitaxy possible at low temperature is the hydrogen plasma etching of the weakly bounded atoms. This phenomenon is lessened at higher temperatures.

- (iii) Another effect temperature has on PECVD film deposition is that films prepared with a certain process conditions, tend to have less hydrogen content if deposited at higher temperatures. The reason for this is likely the easier break-down of the superficial Si-H bonds because of the increased lattice vibrations at higher temperatures. This is favorable for epitaxial growth as a good epitaxial layer will have nearly no hydrogen content.

Because of the above mentioned competing phenomena, in the low temperature regime, there should be an optimum temperature for a certain process conditions. Epitaxy of doped and undoped films using PECVD has been reported for temperatures as low as 165°C [22] but usually electrical properties of films are better if deposition is carried on at slightly higher temperatures (250-350°C) or else a post deposition anneal step would be necessary to improve the film properties. Because of these reasons, temperatures around 300°C has been chosen for this research as the favorable deposition temperature and most of the depositions are held at such temperature.

5.2 Description of the PECVD system used

A standard parallel plate capacitively coupled PECVD system developed by Trion Technology (Orion III) available in CAPDS was used for this study. The system is a cluster tool comprised of a load lock and two PECVD chambers, one is an Inductively Coupled Plasma (ICP) PECVD and the other consists of a capacitively coupled parallel plate PECVD. Because of potentially lower ion damage on the film from the Plasma with ICP head PECVDs, these also offer the possibility of high quality film deposition. However, only the parallel plate PECVD chamber was tested in this research.

Figure 31 shows a correctly-proportioned schematic of the PECVD system used. The electrode separation is 37mm. The steel made bottom electrode on which the sample sits, has a diameter of 196mm and can be heated up to around 500°C using embedded heaters. The remainder of the chamber is constructed with Aluminum. This system uses two power sources; a 600Watt, 13.56MHz power supply connected to the top electrode and a 600Watt, 300KHz power supply connected to the bottom electrode. Such a configuration is called "Triode" by the manufacture. In the development of the epitaxial film during this research, we have avoided using the low frequency power supply of the bottom electrode because of the increased ion damage it will create and depended only on the top electrode's RF power supply.

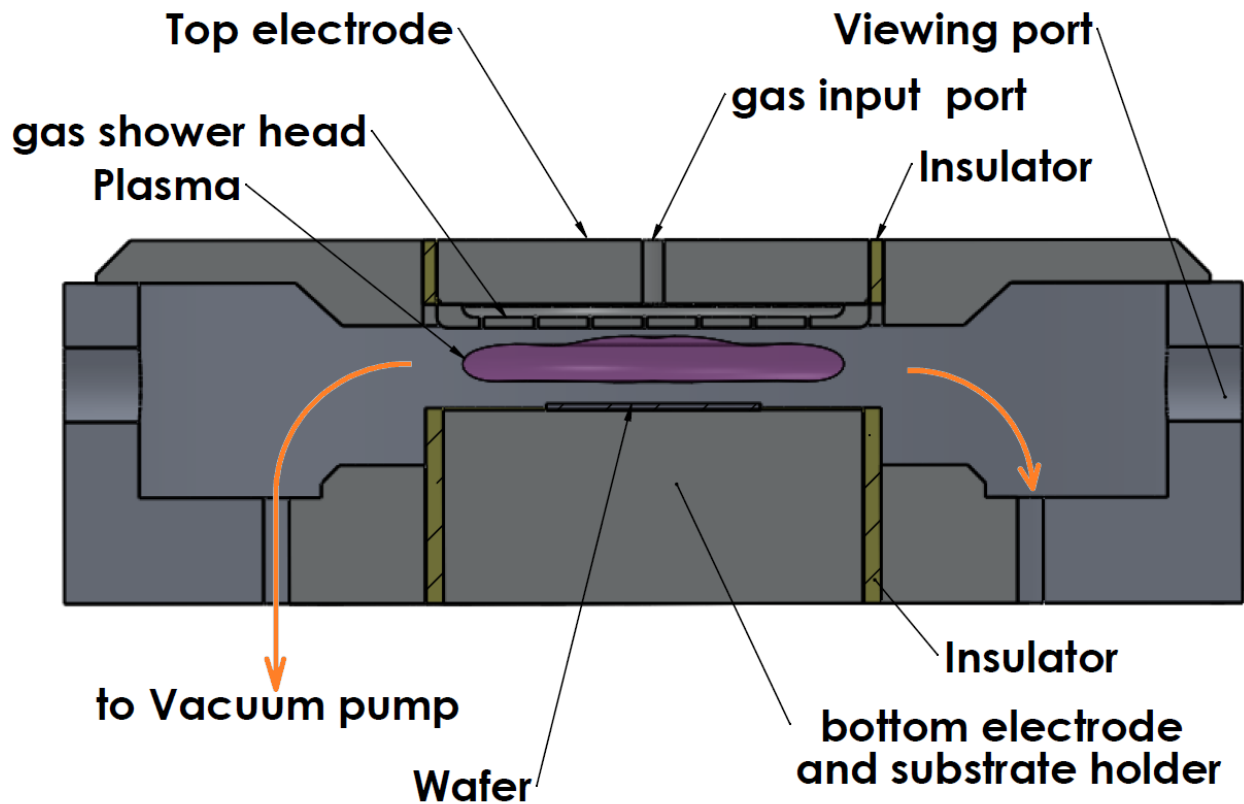


Figure 31, schematic of the PECVD tool used for epitaxial silicon film deposition. The system is configured in a Triode mode with a 13.56MHz power supply connected to the top electrode and a 350KHz source to the lower electrode. Only the top electrode's high frequency power supply was used for this research.

A sample carrier was made to make loading of samples of arbitrary shapes through load lock possible which otherwise would only be loadable by directly opening the PECVD chamber. This carrier, which is made of 6000 series Aluminum, covers the whole bottom electrode and helps reducing the physical cleaning steps needed to perform directly on the bottom electrode. Figure 32 shows a sketch of this carrier.

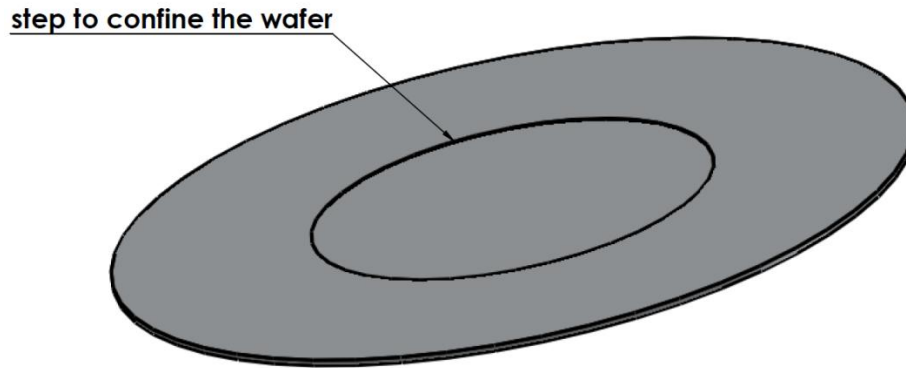


Figure 32, A carrier plate made from 3mm thick 6000 series Aluminum to make loading of arbitrary shaped samples using load lock possible. It also reduces the number of physical cleaning steps needed to be done directly on the bottom electrode.

The chamber is pumped down using a turbo molecular vacuum pump backed up by a mechanical pump and can reach to the base vacuum of the range 10^{-7} Torr in around 10 minutes. The gases connected to the PECVD chambers are: SiH_4 , H_2 , PH_3 , B_2H_6 , N_2 , NH_3 , and GeH_4 for deposition and CF_4/O_2 mix for cleaning purpose.

5.3 Chamber preparation prior to film deposition

Before each film deposition, the chamber was reset to a known and controlled condition. After deposition of silicon films of accumulative thickness more than 800nm, a chemical cleaning process was run using 20% O_2 in CF_4 plasma to etch the deposited film from the chamber walls and electrodes. It's well known that the cleaning process should be stopped immediately after the deposited films are etched. over etching will cause powder (yellowish color) generation because of the interaction of the CF_4 plasma with the metal surfaces and will cause the conditions of the inside of the chamber to vary uncontrollably. When this happens, a physical cleaning of the surfaces will be necessary. The recipe used for cleaning of $1\mu\text{m}$ of deposited film is shown in Table 3. For different thicknesses of the films to be cleaned, the duration of the two steps would need to be adjusted accordingly.

Pressure	Top electrode power	CF_4/O_2 flow	Temperature	duration
300mTorr	200W	50 sccm	300°C (or deposition temperature)	30 min
50mTorr	200W	50 sccm	300°C (or deposition temperature)	5 min

Table 3 - The cleaning recipe used for cleaning the PECVD chamber after a deposition.

The high pressure (300mTorr) step cleans mainly the electrodes while the lower pressure (50mTorr) step cleans areas of the chamber far from the electrode. This is because lower pressure plasma spreads more in the chamber whereas higher pressure plasma is mainly confined in between the top and bottom electrodes.

After a successful chemical cleaning of the chamber, multiple steps of high flow hydrogen flush followed by vacuuming down steps were used to remove the particles created during the cleaning step (because of the interaction of oxygen and residual silane gas). This was followed by a hydrogen rich silicon deposition to passivate the chamber walls and the electrode surfaces. The recipe for this pre-deposition is shown in Table 4.

Pressure	Top electrode power	H2 flow	SiH4 flow	Temperature	duration	Film thickness
400mTorr	15W	250 sccm	10 sccm	300°C	30 min	130nm

Table 4, recipe used for chamber conditioning before film deposition. The high hydrogen dilution helps the passivations of the damaged chamber surfaces during the cleaning step while a thin silicon film is being deposited on the chamber walls and electrodes.

High hydrogen dilution during the pre-deposition step is required to passivate the damaged surface of the recently cleaned interior surfaces of the chamber.

5.4 Results and discussion on the developed process for low temperature silicon epitaxy

This section will present the details of the various process conditions used for deposition of n-type, intrinsic and p-type epitaxial silicon films, the methods used to find the maximum possible epitaxial film using a recipe, results of the studies on the effects of the post deposition annealing and the findings and observations encountered during these experiments.

5.4.1 Variation of the film quality as a function of the distance from the interface

Figure 33 shows a cross sectional Transmission Electron Microscope image of an epitaxial film deposited on a (100) silicon substrate. Shown in this figure is the gradual increasing of the defects (darker areas) and the eventual termination of the epitaxy and start of the amorphous phase deposition. This behavior happened for all the recipes we have tried as well as the ones reported in literature. The condition for the deposition of this film is shown in Table 5.

Pressure	Top electrode power	H ₂ flow	SiH ₄ flow	PH ₃ flow	Temperature	Deposition rate
400mTorr	15W	250 sccm	12 sccm	8 sccm	300°C	2.75 nm/min

Table 5 - the recipe used to deposit the film shown in Figure 33

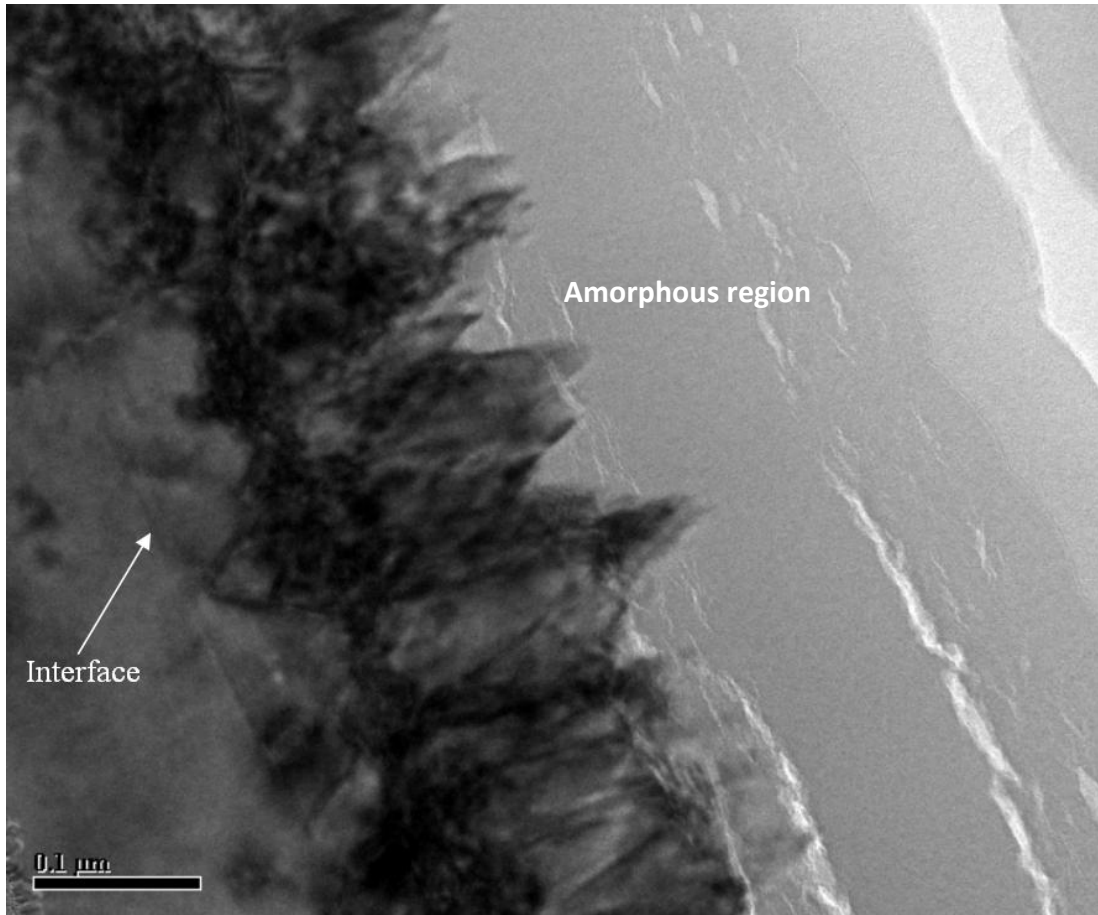


Figure 33 - TEM image of the cross section of an epitaxial film deposited using PECVD at 300°C with the deposition conditions listed in Table 5. the arrow points at the faint line of the interface between the film and substrate. This image shows that the parts of the film very close to the interface (grey areas) have higher quality and as the thickness increases, more defects are generated in the film (darker areas) and eventually the deposition turns into amorphous phase after around 250nm.

In the case shown in Figure 33 the epitaxy is lost after around 250nm of deposition. The maximum thickness of epitaxy achievable using a certain deposition condition is dependent the recipe, substrate cleanliness and chamber conditions. One of our goals was to be able to find a recipe which can produce epitaxial films with thicknesses in the several micrometer range. This by itself should mean a better crystal quality since it reflects that the density of the defects in the film is low enough to sustain the epitaxy to a higher thickness.

Figure 34 shows a closer look at the interface and the epitaxial film. It shows the cross sectional TEM image of an epitaxial film deposited using a low temperature PECVD process. Darker areas are considered to be under stress while the brighter areas are close to perfect crystalline. It clearly shows that the film is close to perfect in the vicinity of the interface with the mono-crystalline substrate but defective farther away from it. It also shows an example of how the film starts to become more defective as the thickness increases by origination of defects in the lower thicknesses.

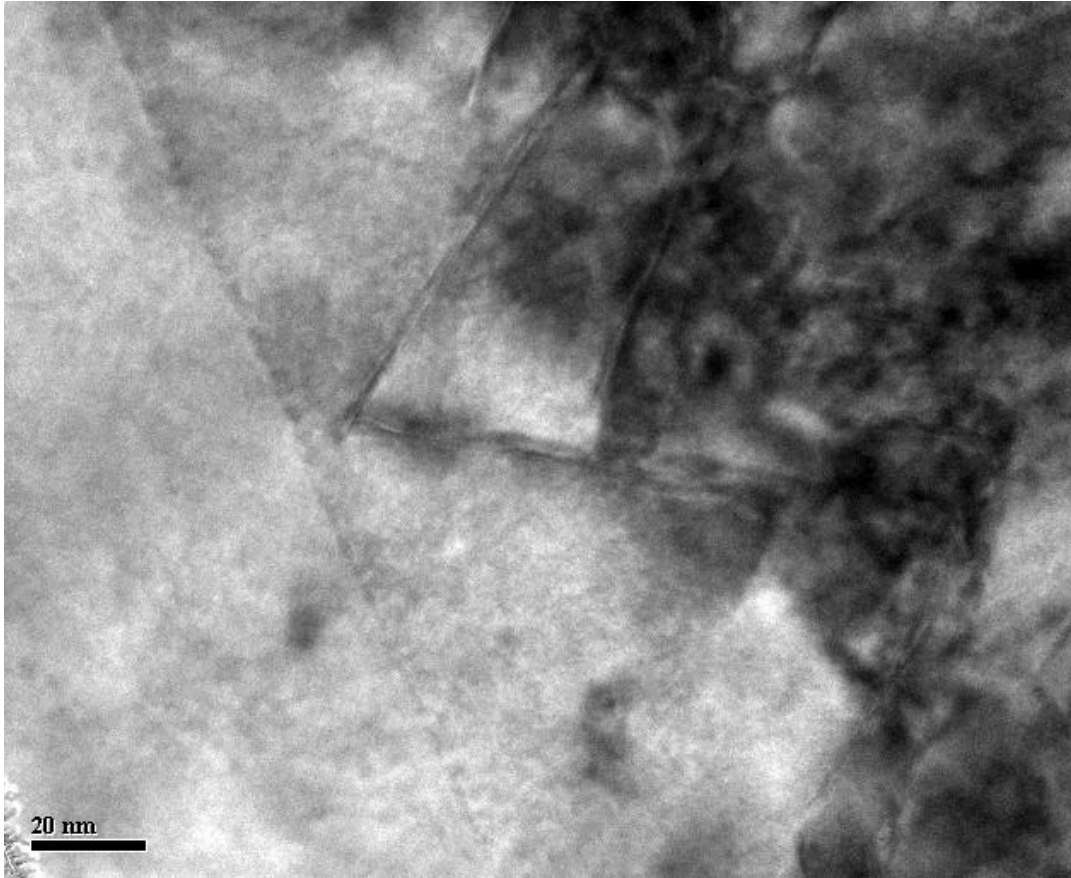


Figure 34, Cross sectional TEM image of an epitaxial film deposited using a low temperature PECVD process. Darker areas are considered to be under stress while the brighter areas are close to perfect crystalline. It clearly shows that the film is close to perfect in the vicinity of the interface with the substrate but defective farther away from it. Also visible is an example of how the film start to become more defective by origination of defects in the lower thicknesses.

Figure 35 shows a higher resolution TEM image of the cross section of the same sample used in Figure 33. It shows almost perfect epitaxy in the regions close to the interface with the mono-crystalline substrate.

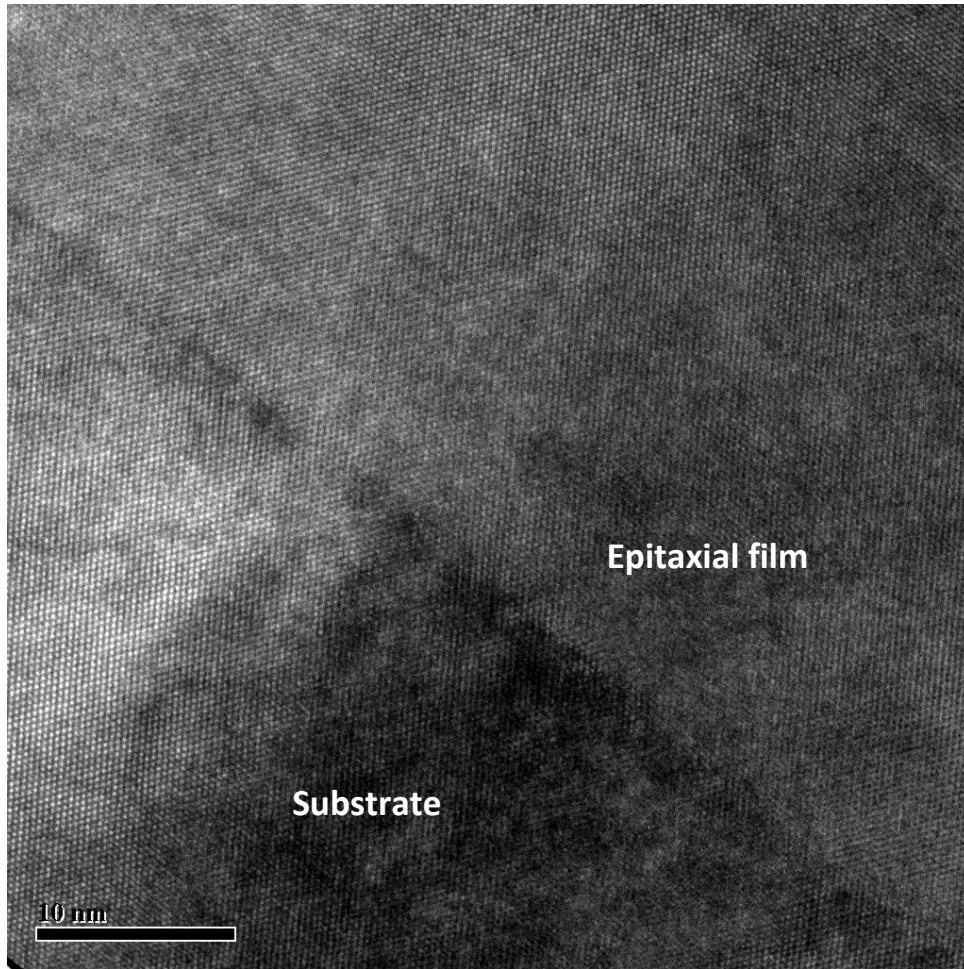


Figure 35, High resolution TEM image of the cross section of an epitaxial film deposited using PECVD using the recipe shown in Table 5. The darker diagonal line shows the interface between the substrate and the film. This image clearly shows the high quality of the epitaxial film in the regions close to the interface.

What these TEM images and similar observations show is that the low temperature epitaxial deposition using PECVD is not self-corrective; meaning that some defects of particular nature when generated at a thickness will always become an origin for more defective growth as the film continues to grow. Most likely increased substrate temperature will improve this short coming but that case has not been studied in this report and the strategy for increasing the quality and resultantly the thickness of epitaxial film was to find the conditions which produce less defects of non-correctable nature.

5.4.2 N-type silicon epitaxy

Investigation of epitaxial films began with the n-type films achieved by phosphorous doping. 1% Phosphine (PH_3) diluted in hydrogen was used as the dopant source gas. Traditionally it's thought to be

easier to achieve n-type doping than p-type. The method we used to find an optimum condition for epitaxial silicon film deposition is algorithmically illustrated in the flowchart in Figure 36.

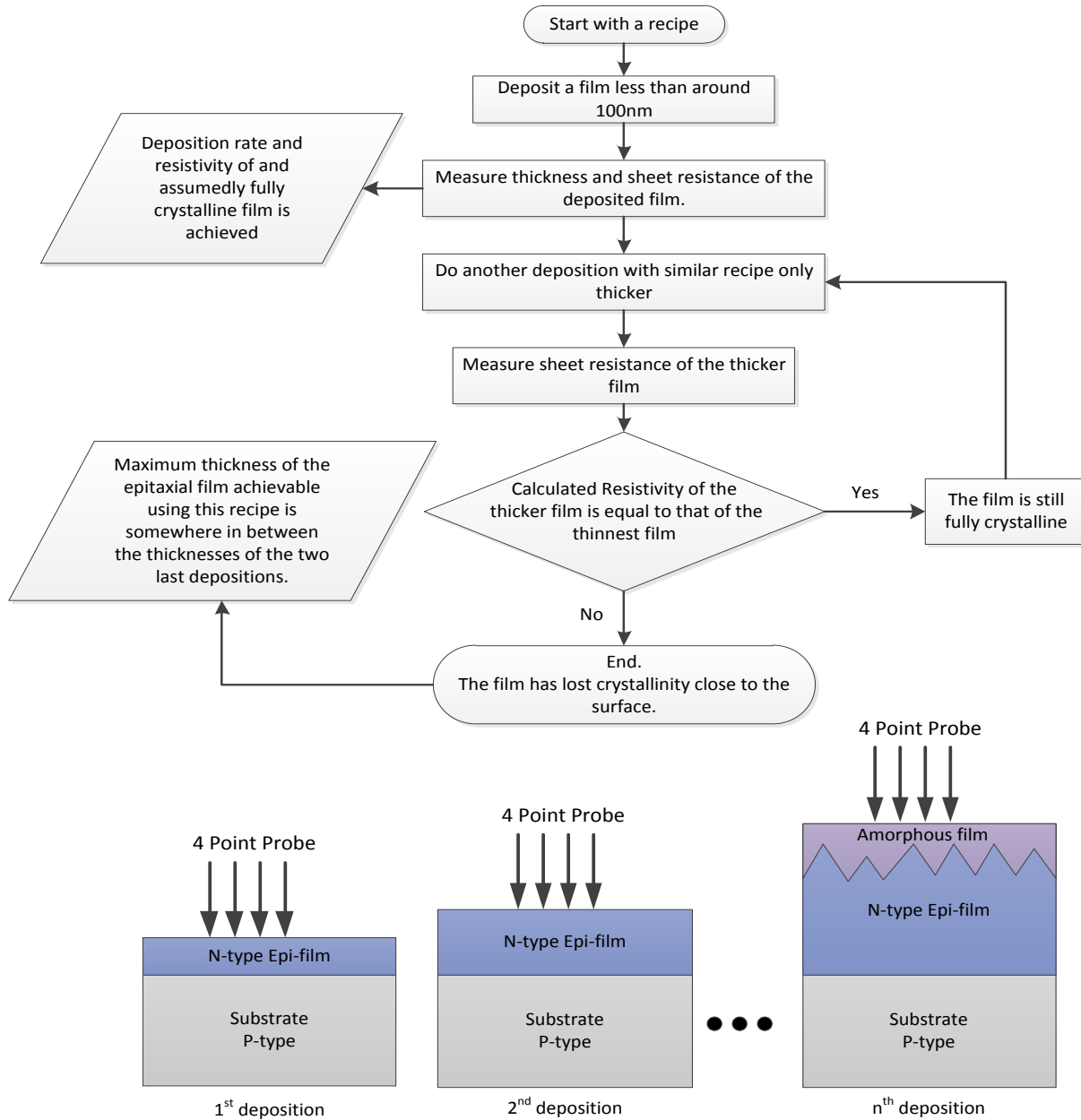


Figure 36, top: the flowchart showing the scheme we used to find an approximate value for the maximum thickness of epitaxy using a certain deposition conditions. Bottom: schematic representation of the method. Four point probe was used to measure the sheet resistance of the deposited film.

This method relies on the assumption that the conductivity of the film will stay the same as long as the film stays mono-crystalline. The first step would be to start with a hopeful recipe and deposit a thin layer (less than 100nm) of film. Next, the thickness and sheet resistance of the film was measured and from

these deposition rate (thickness over deposition time) and resistivity (sheet resistance times the film thickness) of the film was calculated. From experience, it was expected that such recipe should produce epitaxial films at least less than 100nm thick and if that was not the case we would find out during the next steps. Next, another deposition with higher thickness was run using the same recipe. if the sheet resistances of the two different thicknesses of the film were inversely related to the difference in thickness between them, then we would conclude the film in the thicker deposition is fully crystalline and will proceed with a thicker deposition and repeat these steps until the sheet resistivity of the film is no longer equal to the originally calculated resistivity of the thinner films over its thickness. In this case we would conclude that some portion of the film (top part of it) is not crystalline anymore. This way we were able to find a maximum thickness for the epitaxy for the recipes we tried. Transmission Electron Microscopy of the cross section of the deposited films can also be used for this purpose alternatively but it is easier, faster and less costly to use the abovementioned method.

The best recipe found, during this research, for highly doped N-type silicon film is shown in Table 6. Using this recipe we were able to achieve sheet resistance of lower than $7\Omega/\text{sq}$ for film thicknesses of around 800nm, this is much better than $150\Omega/\text{sq}$ reported in [20]. This film is degenerately doped with a dopant concentration in the range of 10^{21} cm^{-3} and carrier mobility around $22\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$.

Pressure	Top electrode power	H ₂ flow	SiH ₄ flow	PH ₃ flow	Temperature	Deposition rate	Maximum Crystalline thickness achieved
200mTorr	15W	250 sccm	10 sccm	8 sccm	300°C	2.2 nm/min	800nm

Table 6, PECVD recipe to deposit highly phosphorous doped epitaxial films up to around 800nm thick.

Figure 37 shows the Spreading Resistance Profiling (SRP) profile of an epitaxial film deposited using the recipe shown in Table 6. The film thickness is around $1.1\mu\text{m}$ and it took around 8 hours for its deposition as the deposition rate is very low. The SRP was done at Solecon Technology. According to our estimations based on the comparison of a thinner film deposited using similar recipe, only up to 800nm of this film should be fully crystalline while the SRP shows full crystallinity all over the film thickness up to a thickness of $1.1\mu\text{m}$. the author thinks that there could be some error in the calculations of doping during analysis of the SRP data when there is a layer with much lower conductivity (the amorphous layer on the very top of the film) on top of a layer (the epitaxial layer beneath) with much higher conductivity because of the way SRP is measured. Similar artifacts in the SRP results have been observed before. Anyways, even with the most pessimistic estimation, this film is crystalline up to a thickness of around 800nm.

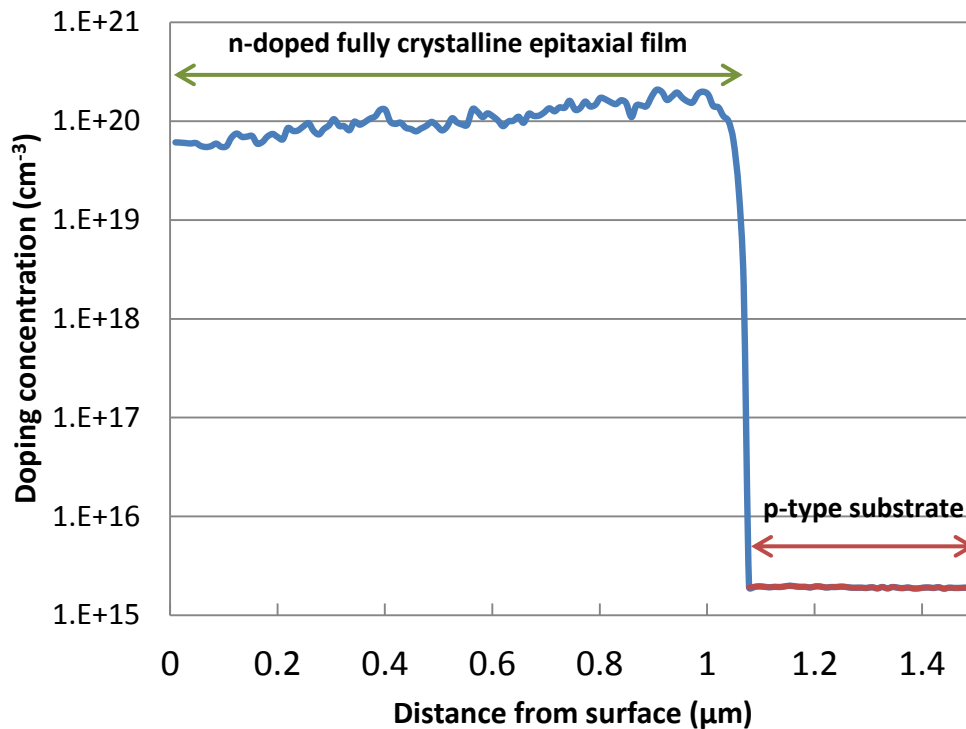


Figure 37, Spreading Resistance Profiling (SRP) profile a highly phosphorous doped epitaxial film deposited on a mono-crystalline (100) p-type silicon wafer using the recipe shown in Table 6. High activated doping all over the film thickness also indicates complete crystallinity of the film.

5.4.3 Findings on the role of Phosphine in enhancing epitaxy

To our surprise and opposite to what is reported in the literature [20] we were able to achieve better (thicker and with less hydrogen content) highly phosphorous doped epitaxial films than the intrinsic (unintentionally doped) ones. Reports of low and medium temperature epitaxy using PECVD or CVD point out that the epitaxy of undoped films can be achieved easier because of the adverse effect of the addition of the dopant gases on the chemistry of the deposition environment. [20,22,24] Romain Cariou et. al were able to achieve up to 3μm of intrinsic films but only a maximum of 50nm of phosphorous doped film with a sheet resistance of 150 Ω/sq.

The same recipe which will result in an epitaxial film of around 800nm thickness would only produce around 450nm of intrinsic film if the phosphine gas was turned off with all the other parameters unchanged. In addition, the lower thickness intrinsic film, when annealed, would develop pin holes indicating high hydrogen content in the film while the thicker phosphorous doped film would remain topologically unchanged after similar annealing step.

Rosenblad [23] has reported that the addition of Germane gas for their silicon epitaxy using CVD had improved the epitaxy. Their explanation was that having too much hydrogen in the deposition

environment at lower temperatures leads to excessive hydrogen adsorption in the growing surface to a degree that ends up in incorporation of excessive hydrogen in the film which in turn results in generation of defects and eventual termination of epitaxy. However, by introduction of Germane to the deposition chemistry, germanium compounds retard hydrogen incorporation in the film by partially replacing the hydrogen atoms passivating the surface. The author thinks that similar explanation might apply to the case we have been dealing with using PECVD. In our case, introduction of Phosphine gas might lower the hydrogen incorporation in the film by reducing the hydrogen content on the surface leading to better epitaxy.

5.4.4 Intrinsic silicon epitaxy

In searching for a better recipe to deposit epitaxial intrinsic silicon, most of the important parameters of deposition such as hydrogen dilution, total gas flow, pressure and power were varied to test the effect they have on silicon epitaxy. Since electrical characterization of the intrinsic silicon is practically too difficult, we used a thin phosphorous doped film with known conductivity deposited on top of the intrinsic layer to assess its crystallinity. The intrinsic film was deposited using a recipe of interest to a certain thickness and then immediately followed it up with a deposition of a thin N-doped silicon layer which would result in a known sheet resistivity if deposited on bare bulk silicon. If the sheet resistivity of the stack of the N-doped layer on top of the intrinsic layer was similar to that of the n-doped layer on bare silicon we would conclude that the intrinsic layer is fully crystalline and would repeat the process until this doesn't hold to be the case anymore. Similar to the case for the determining of the maximum epitaxial thickness of the n-doped films, this way we would also be able to find out the maximum epitaxial film deposition possible with the recipe under study. The algorithm for this method is shown in Figure 38.

The best recipe in terms of highest achievable thickness of epitaxy is shown in Table 7. Even though this recipe produces almost complete epitaxy in terms of crystallinity, unfortunately it results in an excessive incorporation of hydrogen in the film to an extent that a higher temperature post deposition annealing step creates lots of pinholes and bubbles in the film.

Pressure	Top electrode power	H ₂ flow	SiH ₄ flow	Temperature	Deposition rate	Maximum Crystalline thickness achieved
800mT	22 Watts	5 sccm	100 sccm	300°C	9 nm/min	450nm

Table 7 – best recipe found for deposition of intrinsic epitaxial silicon films

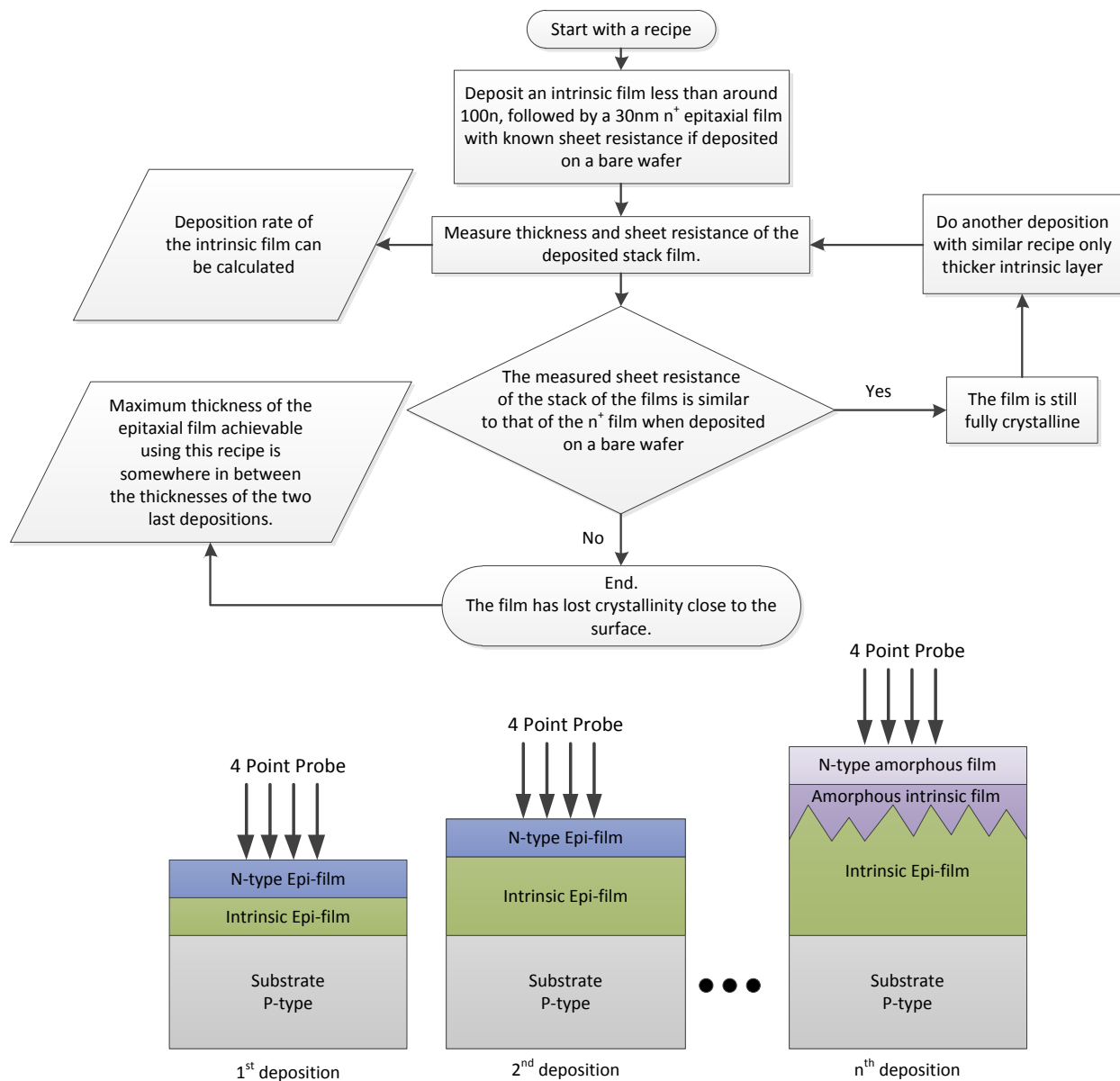


Figure 38, top: Flowchart showing the scheme we used to find an approximate value for the maximum thickness of epitaxy using a certain deposition conditions for intrinsic silicon. **Bottom:** schematic representation of the method.

In general we noticed that intrinsic silicon can be deposited with a higher rate of deposition (as also reported by [22]) but one thing most of these films suffer from is the high hydrogen content trapped in the film.

It is not possible to claim that the developed recipes are the best for intrinsic film deposition. Most likely recipes with lower deposition rate will lead to better quality of the epitaxy.

5.4.5 P-type silicon epitaxy

Our main focus was to develop n-type silicon epitaxial films to be used in the fabrication of the BWE solar cell but several recipes for p-type epitaxial film deposition were also tested. P-type epitaxy is usually considered to be more difficult than n-type silicon epitaxy mostly because of the higher dissociation energy Diborane needs compared to Phosphine. Diborane also causes higher adverse changes in the chemistry of the deposition environment (e.g. powder generation). However M. Labrune, et. Al [20] has conversely reported an easier job when depositing Boron doped silicon than that of phosphorous doped films.

The best result achieved among the few trials we had is shown in Table 8. The film is not fully crystalline as a post deposition annealing step improves the conductivity to a large extent.

Pressure	Top electrode power	H ₂ flow	SiH ₄ flow	B ₂ H ₆ flow	Temperature	Deposition rate	Maximum Crystalline thickness achieved
200mT	15W	250 sccm	10 sccm	8 sccm	300°C	2.8 nm/min	Less than 80nm

Table 8, a deposition condition which produces a boron doped p-type epitaxial silicon film with thicknesses less than 80nm.

5.4.6 Epitaxy on different substrate orientations

Low temperature epitaxial technology using PECVD seems to be very sensitive to the crystallographic orientation of the underlying substrate. There is no report of low temperature epitaxy on (111) silicon surfaces using PECVD as it appears that the mechanisms responsible for low temperature epitaxy by PECVD which lead to successful results on (100) surface fail to govern epitaxy on (111) silicon surfaces. As mentioned earlier in this chapter the reason for this failure might be the retardation of the hydrogen plasma etching of the weakly bounded silicon adatoms on the growing surface since hydrogen plasma etching of silicon is much slower on (111) surfaces.

Feasibility of epitaxy on (111) surfaces are especially important in solar cells because the common pyramid texturing technique used for light trapping results in a (111) surface finish on the surface of the silicon. After several failures in achieving epitaxy on (111) surfaces using methods similar to those previously explained, we did two kinds of experiments to see the difference between the films on (100) and (111) surfaces. In one experiment a shallow step was created by anisotropic wet etching on a (100) wafer which led to a (100) surface immediately beside a (111) tilted surface. This way both surfaces are exposed to the very same plasma and deposition condition (except the angle with electrodes) so that a reliable comparison can be made. Figure 39 shows the cross sectional TEM image of this structure with the film deposited on both surfaces. As clear, the film on (100) surface is crystalline to an expected height but the film on (111) surface is almost completely amorphous.

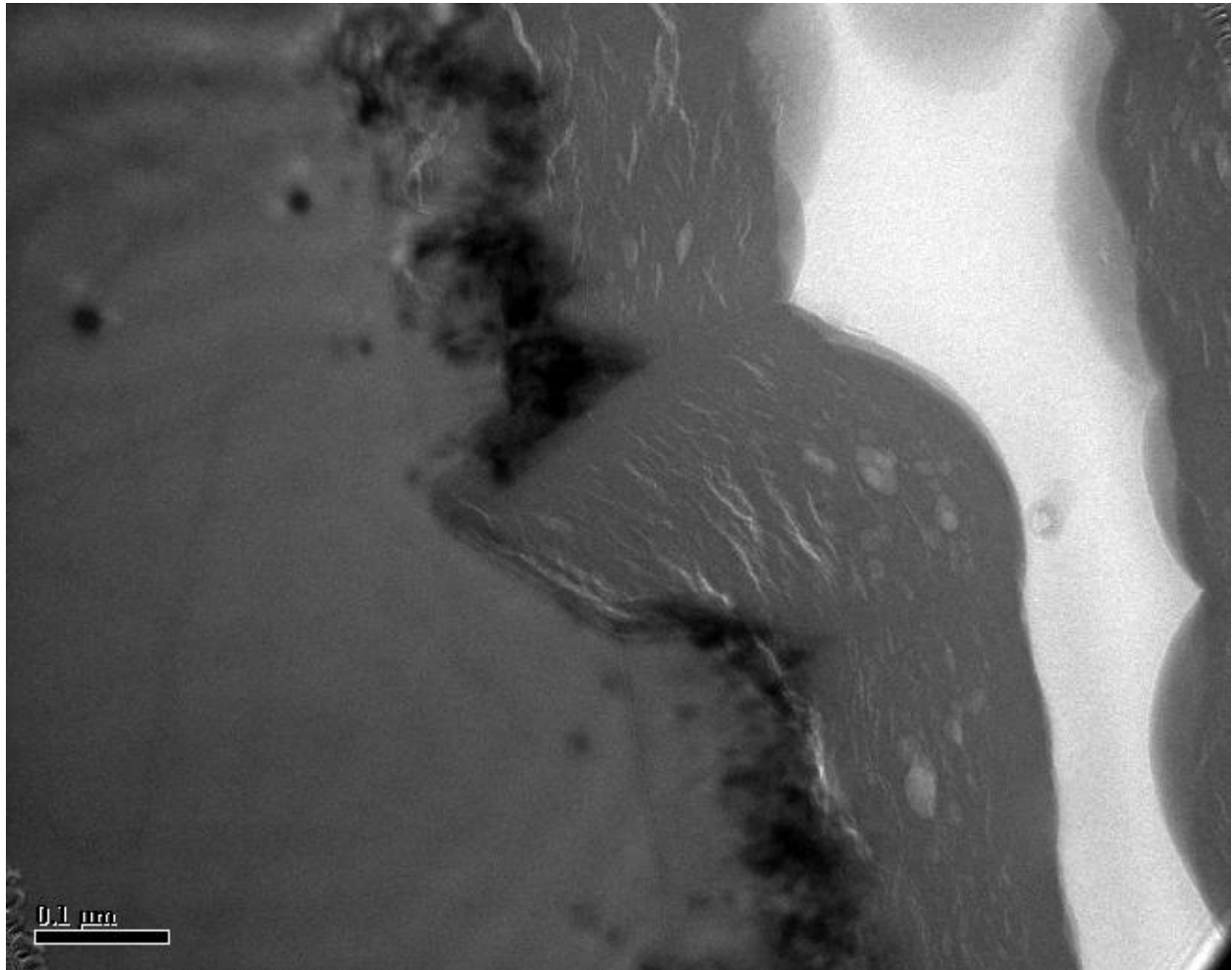


Figure 39, cross sectional TEM image of a film deposited on a stepped structure on (100) silicon wafer. The created step exposes the (111) surface so that the resulting film can be compared on both surfaces. The parts of the film on top of the (100) surfaces are epitaxial to an expected thickness while the parts on the (111) surfaces are almost completely amorphous.

To eliminate the effect of angle difference the (111) and (100) surfaces make with the electrodes of the PECVD machine and to avoid the possible defects introduced during chemical etching, another deposition was done on a (111) wafer directly. Figure 40 shows the high resolution TEM image of the resultant film. It shows that only around 3-5nm of the film has crystallinity and the rest is completely amorphous.

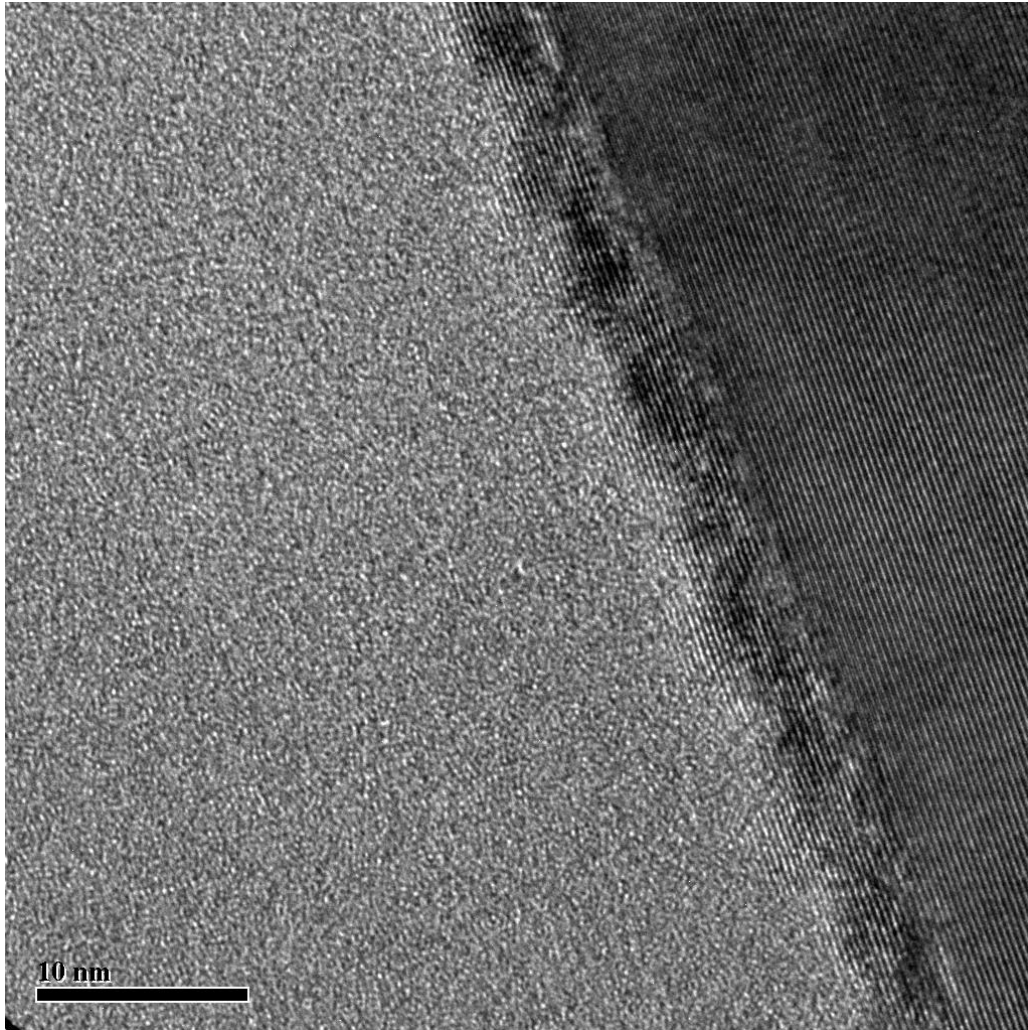


Figure 40, HRTEM image of the cross section of a silicon film deposited on (111) silicon surface. This recipe results in epitaxial deposition on (100) surfaces but as this image shows it only produces few nanometers of epitaxy on (111) surface.

Whether it is possible to achieve higher thicknesses of lower temperature epitaxy by PECVD on (111) silicon surfaces, is not known to the author but if it is, then the proper conditions for it need extra work to be found and might be in the extremely high hydrogen dilution and/or low deposition rate regimes where the increased amount of hydrogen in the plasma might compensate for the slower etch rate on (111) surfaces.

5.4.7 Control over dopant incorporation

Control over dopant density in the deposited epitaxial film is very important for what these epitaxial films are needed for in the fabrication of BWE solar cells. This can be achieved by controlling the amount

of the dopant gas entering the deposition chamber. A 1% Phosphine gas diluted in hydrogen has been used as the dopant source gas. With the accuracy the related mass flow controller has, we were able to vary the doping level in between 10^{19} and 10^{21} cm^{-3} ranges. The lowest flow successfully settable for the Phosphine MFC in the PECVD tool was around 0.8 sccm. This minimum value would result in still a very high doping level of 10^{19} cm^{-3} in the epitaxial films tried. When the dopant gas was turned off for intrinsic film deposition, a very low n-type doping level of around 10^{14} cm^{-3} was measured in the film which probably have a similar origin to the n-type nature of intrinsic amorphous silicon deposited by PECVD. Figure 41 shows the spreading resistance profiling (SRP) profile of a stack of intrinsic- n^+ epitaxial films deposited to demonstrate the control over doping level and ability to create sharp junctions between high and low doped regions.

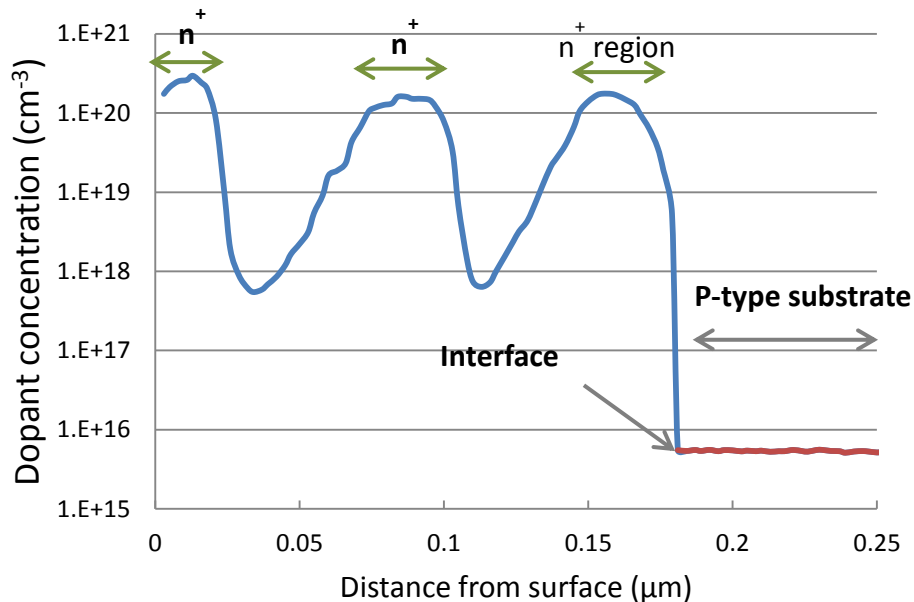


Figure 41, SRP profile of a multiple stack of intrinsic- n^+ epitaxial silicon layers. The doping level in the intrinsic parts is over estimated due to an artifact in the SRP measurement.

The lower doped regions shown in between the highly doped n-type regions must have much lower doping but because of the same artifact in SRP measurement mentioned earlier in this chapter, there is a higher value estimated for the doping of these regions. To prove this fact, another sample was made with a single n^+ layer on top of a thicker intrinsic layer. The SRP for this sample is shown in Figure 42. This SRP clearly shows that the region intended to be intrinsic (closer to the interface) has a much lower n-type doping density (of the range 10^{14} cm^{-3}) than what is shown in Figure 41.

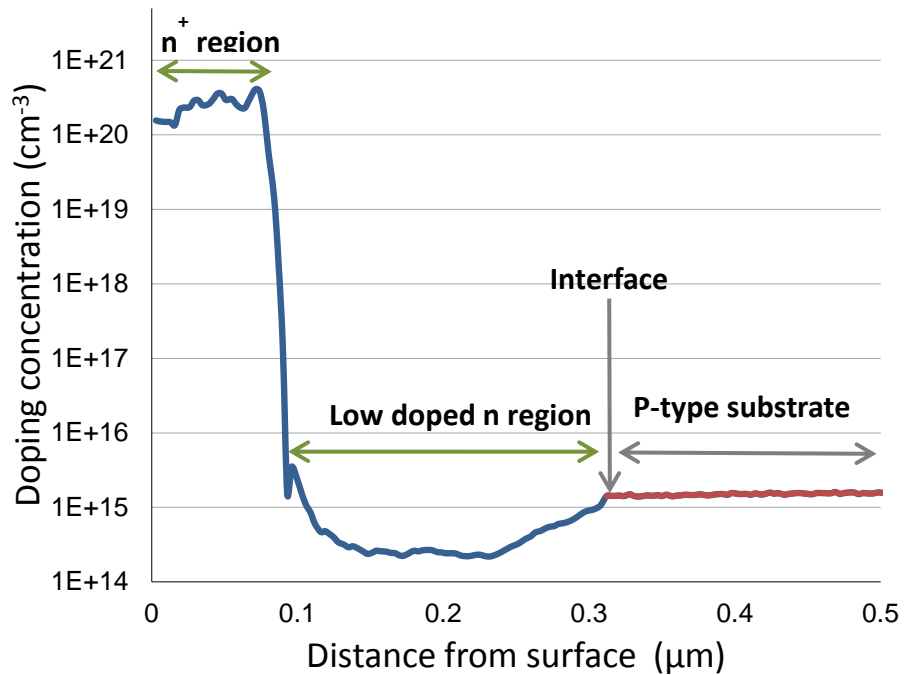


Figure 42 SRP profile a single stack of n⁺ epitaxial silicon on top of a thicker intrinsic layer. Some n-type unintentional doping of around 10¹⁴ cm⁻³ is measured for the region intended to be intrinsic.

To achieve medium (10¹⁵-10¹⁸ cm⁻³) dopant densities, a lower dilution of the phosphine gas in hydrogen will be necessary for the setup used.

5.4.8 Quality assessment of the epitaxial films using reflection spectra

Different methods can be used for assessment of the crystallinity of the deposited epitaxial silicon films. Some authors [20, 22, 24] have used the spectroscopic ellipsometry for this purpose. They have used the sharp peaks of the ellipsometry spectra of the bulk crystalline silicon as the comparison criterion. The films with ellipsometry spectra which resembled the spectrum of a mono-crystalline bulk silicon were considered to be of closer structural nature to that of the bulk silicon and hence better crystalline.

The peaks in the ellipsometric spectra of mono-crystalline silicon happen to be around 3.4eV and 4.2eV. The light source of the ellipsometry equipment available in the CAPDS doesn't give the option to achieve photons of energy higher than 3eV, this made us look for alternative methods and noticing that the equivalent sharp peaks can be seen in the reflectance spectra of the mono-crystalline silicon as well.

The UV-VIS measurement tool available in CAPDS (PerkinElmer, Lambda 1050 UV/VIS/NIR spectrometer) is capable of producing a wider range of photon energies. The reflection behavior of high energy photons is strongly affected by the structure of the immediate subsurface of the sample and as a result provides a sensitive method to study the structures of our interest. Figure 43 shows a plot of the measured reflectance spectra of the bulk mono-crystalline silicon together with a mixed epitaxial/amorphous film deposited on mono-crystalline silicon .in the short wavelength region, there

are two sharp peaks in the mono-crystalline sample's spectrum that are absent in that of the amorphous film. This proposes that this method can be used for the assessment of the crystallinity of the deposited film when compared to spectrum of a perfect crystalline sample.

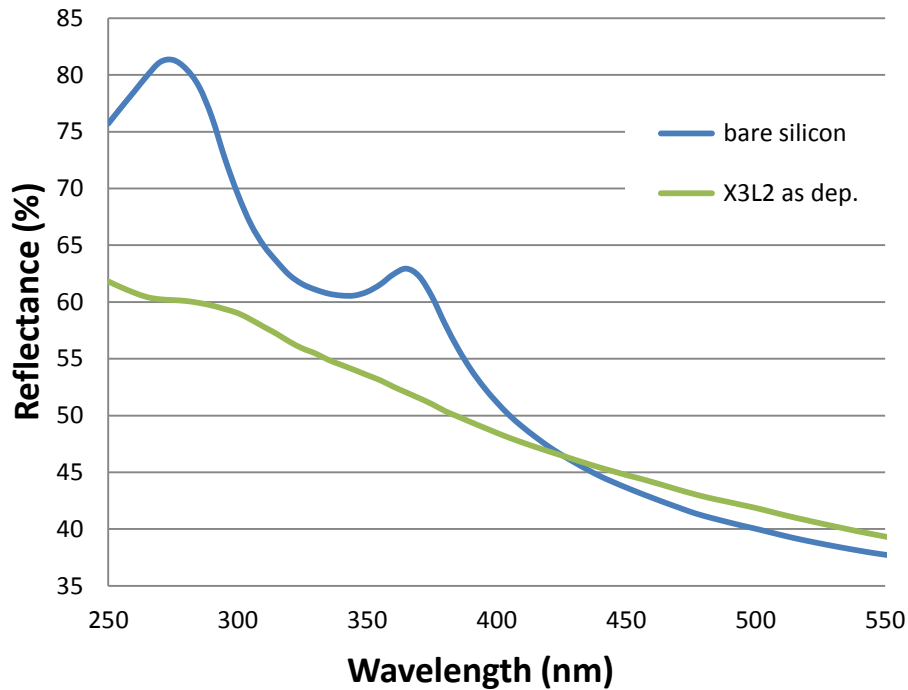


Figure 43 - Reflectance Spectra of mono-crystalline bulk silicon and a mixed epitaxial/amorphous film deposited on mono-crystalline silicon substrate. The sharp peaks at around 280nm and 365nm can be used as a comparison basis to assess the crystallinity of the deposited films.

This method is fast and non-destructive and even be incorporated in deposition tools for in situ monitoring of the film conditions. It should be mentioned that the electrical measurements are not sensitive enough to show much difference among the films shown in this figure.

Using this method, it was possible to compare the crystalline quality of films deposited using different recipes. This helped in finding better recipes which would result in better quality films. Figure 44 shows a comparison of the measured reflection spectra of several epitaxial films deposited using various recipes. Assuming that a reflection spectra with sharper peaks similar to that of the mono-crystalline reference curve indicates a higher quality of the related film, it is possible to find better recipes which produce better quality films using this method.

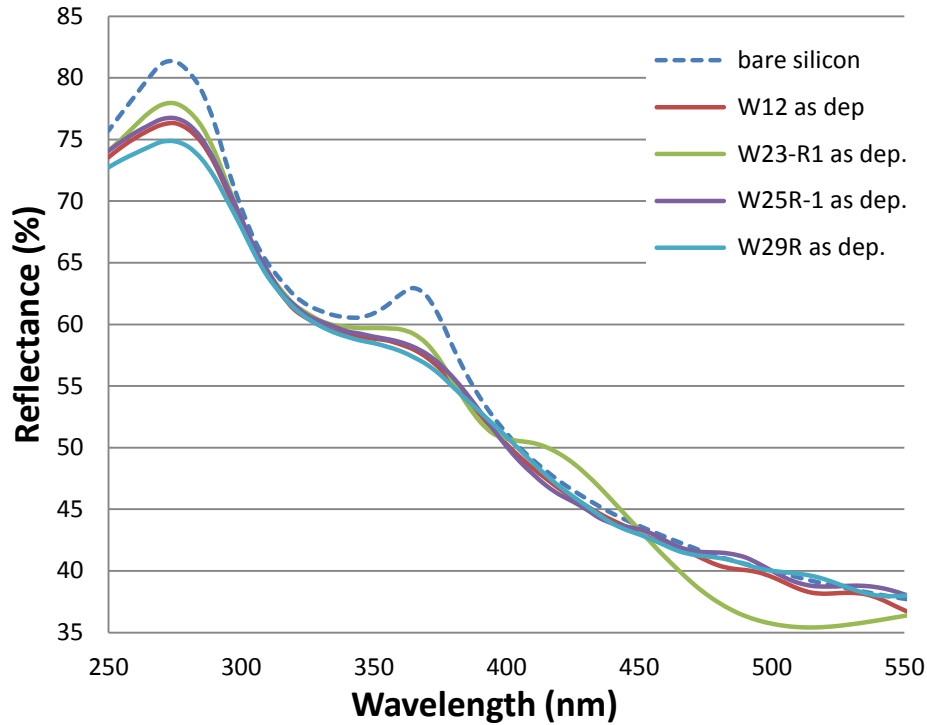


Figure 44 – reflection spectra of several epitaxial films deposited at 300°C in PECVD using different deposition conditions. This graph shows the effect of the recipe on the crystalline quality of the epitaxial film. reflection spectra of mono-crystalline silicon is also shown for comparison.

A conclusion from observing the curves shown in Figure 44 is that the epitaxial films deposited, even though confirmed that are fully crystalline, have a different nature when compared to bulk crystalline silicon. The reason for this difference could be the high density of defects, high doping density, impurities from the deposition environment embedded in the film as well as some hydrogen trapped in the film.

As we will see in the future chapters, when used as the top layer in a BWE solar cell or even as the emitter in a standard solar cell, the quality of such epitaxial films seems to be insufficient in fulfilling the requirements. The problem is perhaps the very low minority carrier lifetime of the films which is a consequence of the high density of the defects as well as the high hydrogen content trapped in the film.

5.4.9- studying the effects of post deposition annealing

Measurements of carrier mobility in the doped epitaxial film deposited using PECVD reveals that the crystal quality improves after a post deposition anneal at a temperature above 550C. Several combinations of peak temperature, duration and ramp slope for different samples were tested. According to our observations, the amount of hydrogen content of the film plays an important role on the after effects of annealing. High hydrogen content in the film mandates a slow ramp or else the film will develop pin holes, bubbles and cracks and in extreme cases, may even peel off [37-41]. This is because of the destructive effect of hydrogen gas while outgassing from the film at temperatures higher than the deposition temperature. The outgassing behavior of hydrogen from PECVD deposited silicon film has not been reported in literature to date but Cerofolini et.al [29] reports a temperature dependent behavior for the outgassing of hydrogen from amorphous silicon films deposited by CVD. According to their measurements, during a ramped heating of a specimen, hydrogen outgassing from the deposited film increases as the temperature increases above the deposition temperature, peaks at around 550°C and then start to decrease to almost negligible values after temperatures above 650C. Decreasing amount of hydrogen outgassed from the film at higher temperatures is because of the depletion of the film from hydrogen at the lower temperatures.

Assuming a similar hydrogen dependent behavior for the annealed films deposited by PECVD, It can be concluded from this report that a quick ramp to temperatures above 550°C in annealing of PECVD silicon films will cause excessive outgassing rate of hydrogen which will potentially create plenty of defects in the film because of destructive interaction with the silicon lattice. The quickest safe ramp an epitaxial film can be annealed with without creation of defects in the film is limited, at least, by the amount of the hydrogen content in the film. As a matter of fact, we used this as another method to find out about the crystal quality of the film as a good epitaxial film would have low hydrogen content and resultantly can be annealed using a quick ramp to the peak annealing temperature without evolution of pinholes or cracks in it.

Figure 45 show the annealing profiles used for rather quick temperature treatment of the samples. Figure 46, on the other hand, shows the annealing profiles with slower temperature changes used to study the effects of slow annealing on the morphology of the deposited films. The furnace used for this purpose was a 2 meters long quartz tube with an inside diameter of around 6" heated by resistive elements. Large size and good insulation around the furnace had made the furnace's response times long especially when cooling off. This has caused some deviation from the heating profiles shown in these figures during the cooling period, but since the deviations were considerable only at lower temperatures we didn't consider them in our reports. All the cases of annealing were performed under 3 lit/min flow of nitrogen.

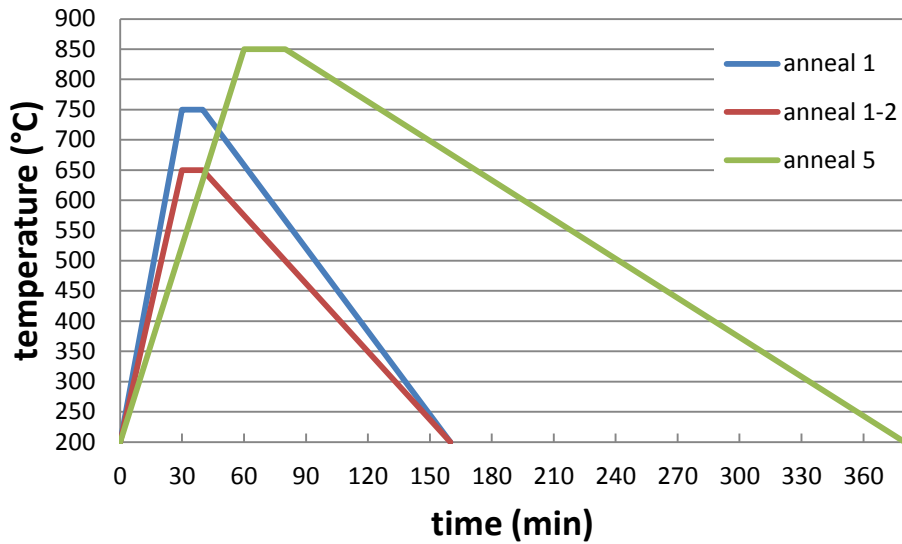


Figure 45 - several annealing profiled used for rapid annealing of the samples. The slow cool down of the profiles are forced by the natural built of the used furnace.

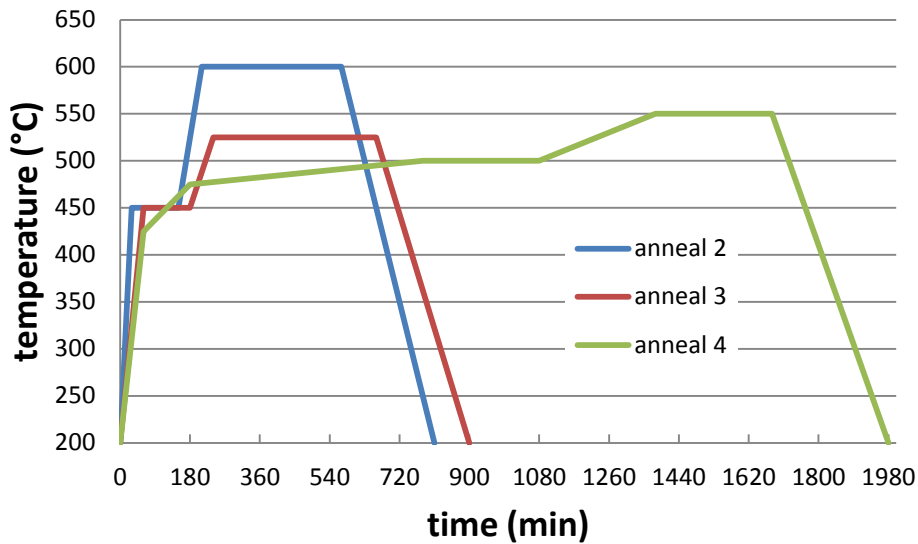


Figure 46 – several annealing profiles used for slow annealing of the samples. Slower increases in the annealing temperature gives the outgassing hydrogen more time to escape the film without violently effecting it.

Table 9 lists the measured majority carrier mobility and the active dopant concentration in several epitaxial films before and after annealing. it also shows the recipe used for each film. An Ecopia HMS-3000 Hall Effect measurement system, available in CAPDS was used to measure the carrier concentration and carrier mobility in the deposited films. To eliminate the effect of the substrate on the measurements films were deposited on substrates with opposite type of dopant in order to form a p-n

junction and electrically separate the substrate from the epitaxial layer. Square samples of 15x15mm size were cleaved or cut for Hall Effect measurement.

Pressure	Power	SiH4	H2	PH3	Temp.	Mobility As deposited ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)	Carrier concentration As deposited (cm^{-3})	Mobility after annealing ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)	carrier concentration after annealing (cm^{-3})
400	25	5	125	4	300	23.9	-1.43E+20	71	-1.16E+20
400	15	5	85	8	300	6.8	-5.04E+20	50	-1.18E+20
800	15	10	250	8	300	20.1	-8.20E+20	65.3	-2.37E+20
800	15	10	250	0.8	300	58.8	-3.29E+19	73.2	-8.93E+19
200	15	10	250	8	300	22.82	-2.40E+21	62.9	-7.00E+20

Table 9 – measured majority carrier mobility and active dopant concentration for the deposited film with the recipes shown before and after annealing at 750°C. in all cases, mobility is improved after the annealing step.

The results show that after annealing, there is always an increase in the value of the carrier mobility. This is most likely linked to an improvement in the crystal structure quality, namely reduction of the defects and hydrogen content. This conclusion is further verified by comparing the measured reflection spectra of the deposited samples before and after annealing. Reflection spectra of several epitaxial films deposited on mono-crystalline silicon substrate before and after annealing are shown in Figure 47, Figure 48 and Figure 49.

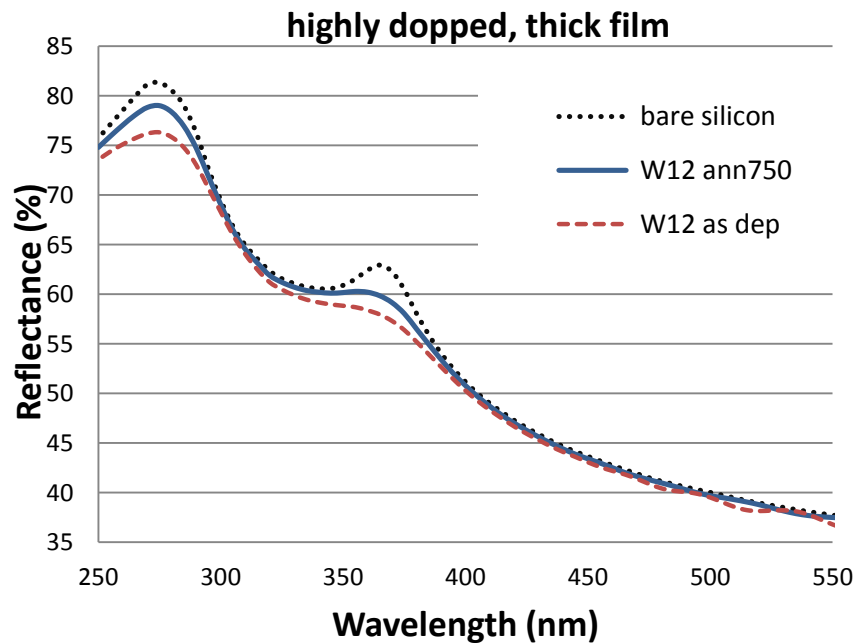


Figure 47 – reflection spectra for a highly phosphorous doped epitaxial film as deposited and after annealing at 750°C. Mono-crystalline silicon reflection spectra is also shown for comparison.

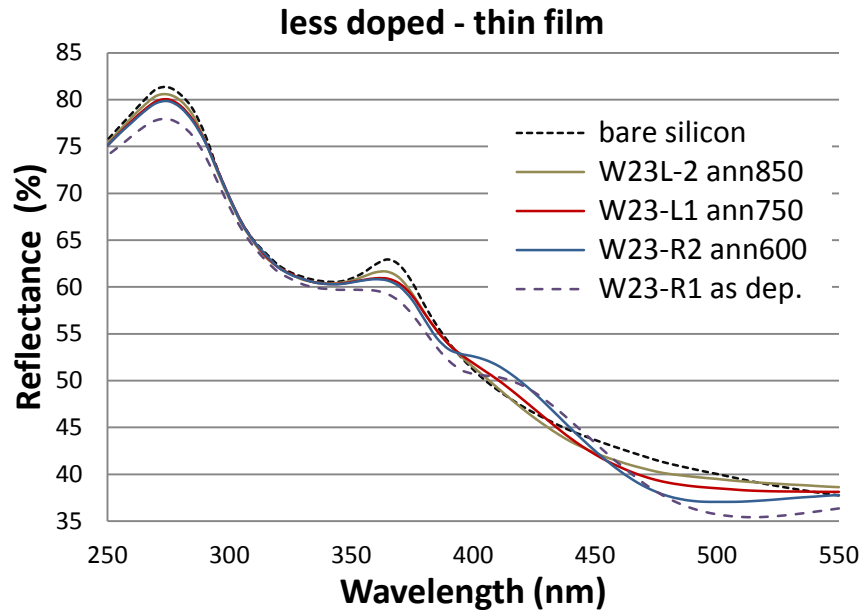


Figure 48 - reflection spectra for a phosphorous doped epitaxial film as deposited and after different annealing processes. Mono-crystalline silicon reflection spectra is also shown for comparison.

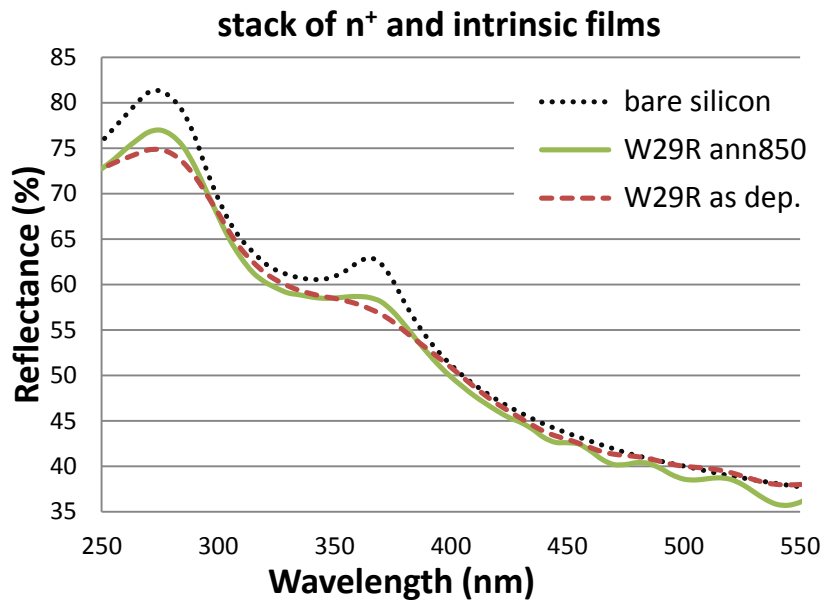


Figure 49 - reflection spectra for a stack of highly phosphorous doped epitaxial film on top of an intrinsic epitaxial film as deposited and after annealing at 850°C. Mono-crystalline silicon reflection spectra is also shown for comparison.

These results collectively show the positive effect of the annealing on the crystallinity of the films. Studying the effects of annealing helped us gain more information about the as-deposited epitaxial films and consider the possibility of adding an annealing step in case the as-deposited film does not have sufficient quality. Finding the optimum annealing conditions for a certain deposition condition will need further work and is not what we have intended to achieve as a part of this research.

Evolution of pin-holes as a result of annealing step:

It was mentioned before that after the annealing step, a common occurrence would be the development of pin holes and bubble in the film indicating that the film had considerable amount of hydrogen trapped in it. It was observed that the form of the pin-holes or bubbles would depend on the nature of the silicon film and the annealing profile. In general, quicker temperature ramps would lead to more violent deformations in the film, but it was interesting to note that both annealing profile and the film deposition conditions play important roles in how the film will change after annealing. Figure 50 shows this fact more evidently. In this figure, the three optical microscope images on the left side are from the same deposition condition but each with a different annealing profile. The size of the pin-holes are obviously different in each of these images. On the right side, the three images show three films with three different deposition condition which have been treated with an identical annealing step. Here as well, it is clear that size of the pin holes vary greatly depending on the deposition condition.

Although these pin-holes indicate that there is too much hydrogen in the crystal matrix in some of the deposited films, but it also proposes a possibility for a mask less pattern generation scheme. By controlling the deposition and the subsequent annealing conditions, it should be possible to create a film with controlled size and density of pin-holes which can act as the windows similar to what is needed in the structure of the proposed BWE solar cell. This can offer cheaper alternative fabrication methods for this device.

In summary, two conclusions can be made from these experiments:

- 1- The slower the ramp up in annealing process the smoother the resulting film
- 2- The shape of the pin-holes changes depending on the deposition and annealing conditions.

The first result in theory should lead to higher quality epitaxy and potentially solid phase epitaxy (SPE) of the PECVD deposited silicon films.

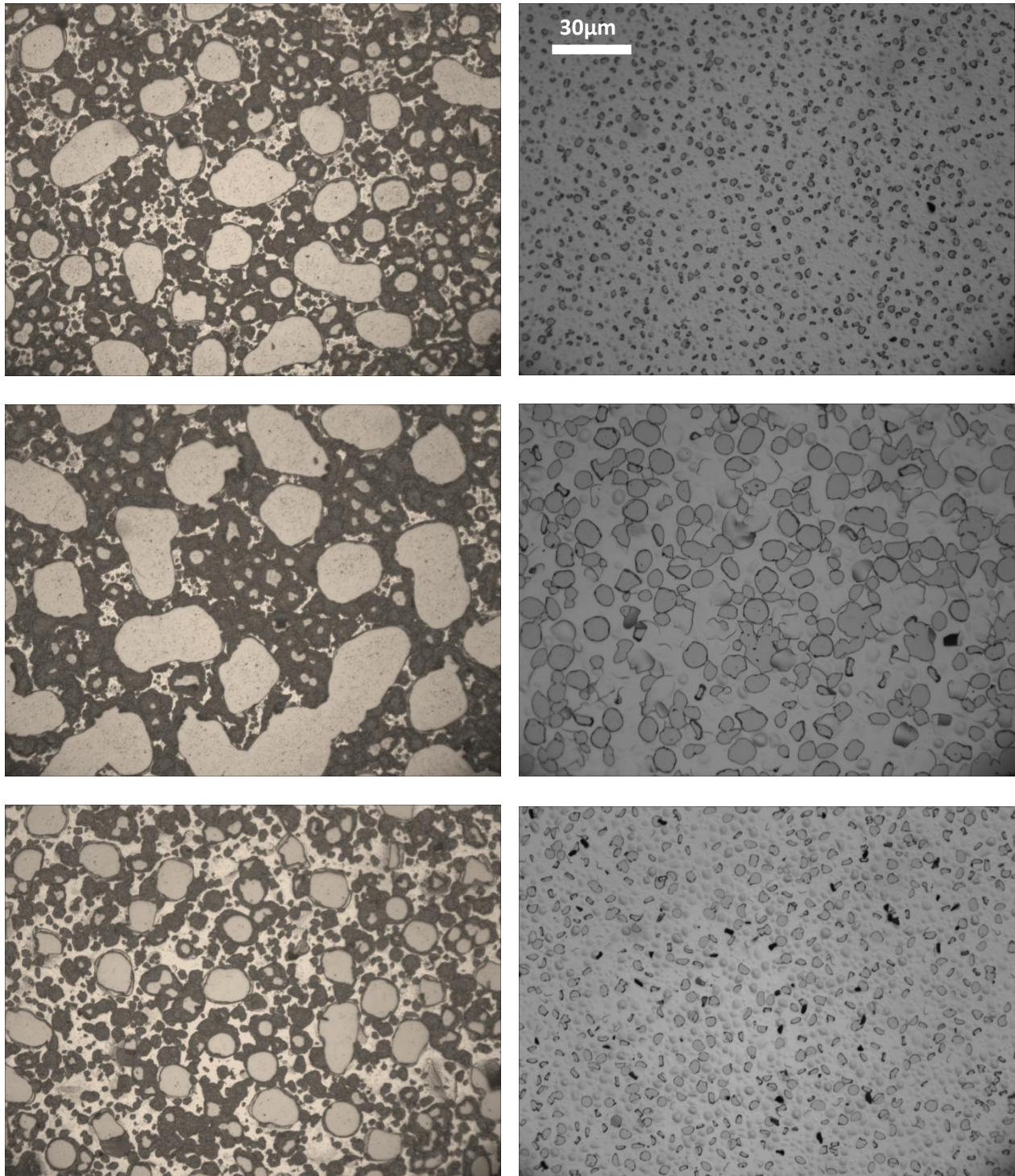


Figure 50 – optical microscop images from the morphology of the films after annealing process. (left) the three images on the left side are from the same deposition condition but each with a different annealing profile (anneal1, 2 and4 from top to bottom). The size of the pin-holes is obviously different. (right) On the right side, the three images show three films with three different deposition conditions which have been treated with an identical annealing step. it is clear that size of the pin holes vary greatly depending on the deposition condition. The scale bar is identical for all the images.

5.4.10- Potential of the developed deposition techniques for super-lattice formation

The ability to control the thickness of the deposited layers of silicon and silicon-nitride made us run some experiments targeting the idea of embedding controlled size nano dots of silicon in a medium of Silicon nitride or other high bandgap material. Figure 51 shows a cross sectional TEM image of a multiple stack of silicon and silicon-nitride deposited on a silicon substrate. Figure 52 shows a higher resolution TEM image of the same sample, thinner layers are silicon and they are clearly amorphous.

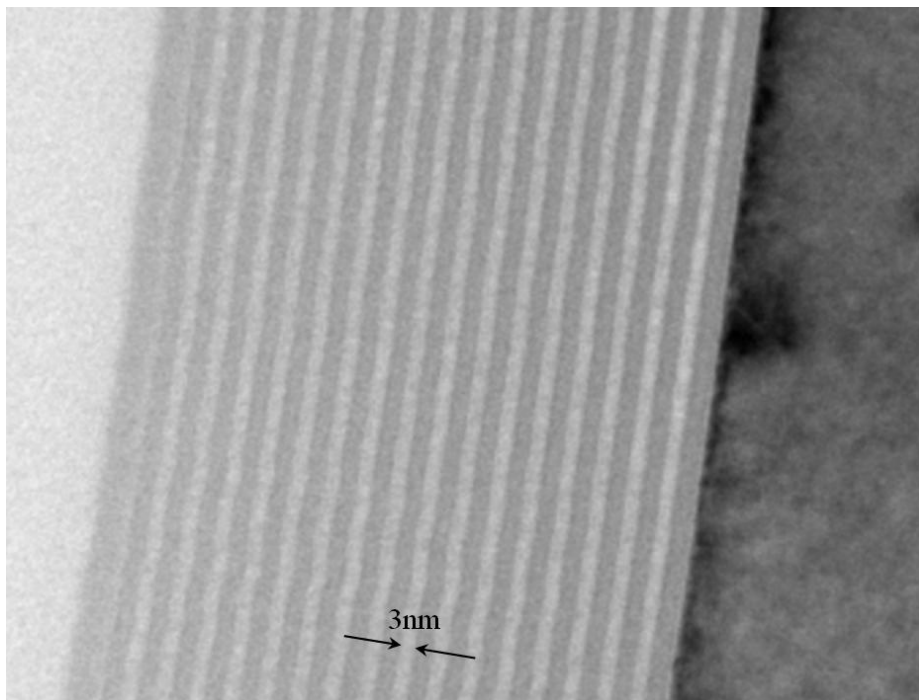


Figure 51 TEM image of multiple layers of silicon and silicon-nitride on a silicon substrate. This stack is intended for the study of the possibility of incorporating silicon nano dots in an insulator.

The next step in making nano-dots embedded in a high bandgap material is to etch nano-pillars in the layered deposited layer leaving islands of silicon separated by silicon-nitride in the vertical direction and by etched space in horizontal direction. The etched spaces can be filled by another deposition layer with silicon nitride or even some kind of TCO to have an active layer of quantum dots. This layer can be used in solar cells since one can control the overall band gap by adjusting the spacing between dots in the layer. A low cost method to achieve the nano sized rod etching of this layer could be the use of nano powders to form a colloidal crystal structure to be used as an etch mask in RIE.

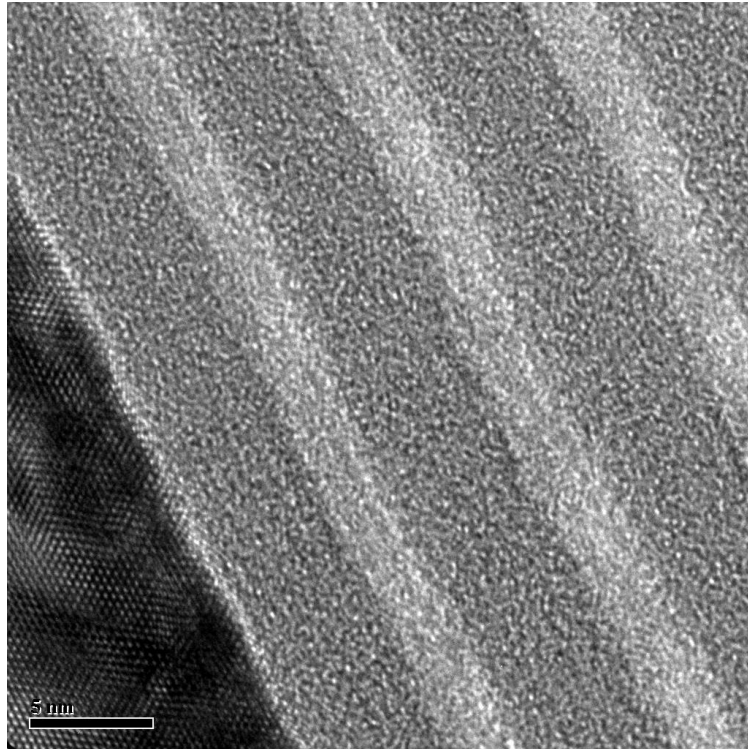


Figure 52 HRTEM image of the sample shown in figure 32. The thinner brighter looking layers are silicon and the thicker ones are silicon-nitride. Substrate is at left.

An alternative method of transformation of the deposited super-lattice to a matrix of quantum dots spread in a controlled arrangement is to use the self-masked silicon or silicon nitride RIE etching techniques.

What was presented in this chapter was most of the work done in search for a low temperature technique capable of producing high quality epitaxial silicon films with controlled doping concentration. The results of this study will be used in the fabrication of a demo BWE solar cell, where for the top layer; an epitaxial film deposited by PECVD will be used.

Chapter 6 – Technology development for the proposed BWE solar cell fabrication

In order to be able to fabricate the novel proposed Buried-Windowed-Emitter solar cell, because of the complicated structure of it a full technology development is required. This chapter presents the work done to fabricate a prototype for the proposed structure. It starts with first choosing a method of fabrication, based on the suitability of the methods for a solar cell fabrication and also the availability of the equipment. Then it explains the considerations for the design of the photo-masks required for the chosen fabrication method. It proceeds with explaining all the steps taken in the fabrication of the proposed solar cell with the details of each step. Occasional anomalous observations and findings are also mentioned where applicable. And at the end, some alternative fabrication methods are discussed briefly.

6.1 Choice of the technology path

There are two critical and nonstandard steps in fabrication of the Buried-Windowed-Emitter solar cell;

- (i) Realizing the windowed emitter
- (ii) Deposition of a high quality top layer on top of highly processed surface.

Windows: Two methods can be used to open windows in the emitter:

- (i) To etch away the emitter on the window areas after a uniform emitter formation
- (ii) Form the emitter in a selective way by using a mask material.

We chose masked dopant diffusion at high temperature as the primary method to fabricate the windowed emitter because of the following reasons:

- 1- equipment required for this method is available in CAPDS
- 2- the dopant diffusion is a mature and standard method
- 3- More importantly, it will leave a smoother surface for the seed layer of the top layer epitaxy. As will be mentioned later, low temperature PECVD epitaxy that we will use for top layer formation is not favorable when the substrate surface orientation deviates from $\langle 100 \rangle$; and creation of any kind of steps because of etching will make epitaxy more difficult if not impossible by low temperature PECVD.

Top layer: to form a high quality top layer any means of homo epitaxy capable of producing high quality single crystalline layers on both high and low doped substrates will work, however this method shall not

be of a high temperature nature as it will redistribute the already formed selective emitter layer. An important requirement for the epitaxial deposition method (for high efficiency cell fabrication) is to have tolerance on the orientation and morphology of the underlying substrate. As we will see later on, the method we will use for top layer epitaxy (low temperature PECVD) will lack this feature because of its low temperature nature (at least to the limit the author has explored and literature suggests) and this will put a limit on the performance one can expect from the final cell.

Fabrication steps for the Buried-Windowed-Emitter cell are shown in Figure 53 in a general way. More detailed fabrication steps with the difficulties one would encounter will be presented later on in this chapter while some of the steps will have minor differences with what is shown in this figure to make each step more reliably accomplishable.

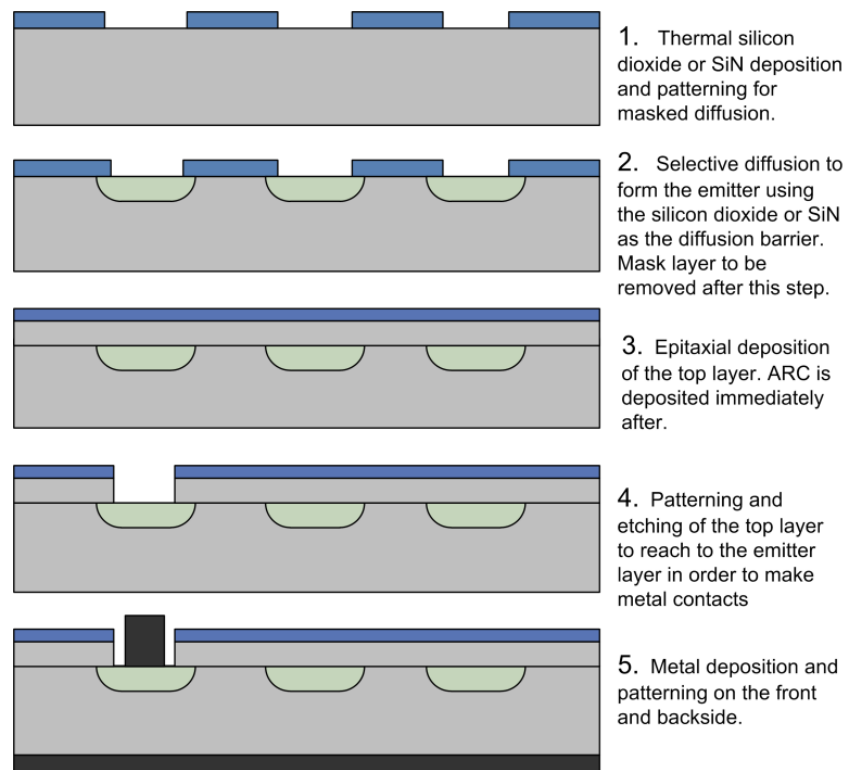


Figure 53, simplified fabrication steps used for fabrication of the proposed BWE solar cell.

This fabrication method involves a masked diffusion step as the means for windowed-emitter formation and a low temperature epitaxial silicon deposition for top layer creation.

6.2 Design considerations for photo-masks and cell architectures

After deciding the method of choice for fabrication it was necessary to design and fabricate the required photo-masks for the BWE cell. There are three important design parameters in the architecture of the windowed emitter:

- (1) the shape of the emitter,
- (2) the emitter coverage percentage
- (3) Width of the emitter strip.

Square shaped windows, as shown in Figure 54, were chosen because of the following reasons:

- 1- In case there is a discontinuity in an emitter strip, there are redundant connections to the neighboring emitter strips. This design is less vulnerable to photolithography defects. An instance of such defect is shown in Figure 59.
- 2- Square windows are compatible if silicon anisotropic etching is to be used for light trapping purposes in future runs. It offers the possibility of making inverted pyramids.
- 3- It's a simple and symmetric structure and the same shape we developed our model in chapter-4 for.

Cris-crossed emitter pattern

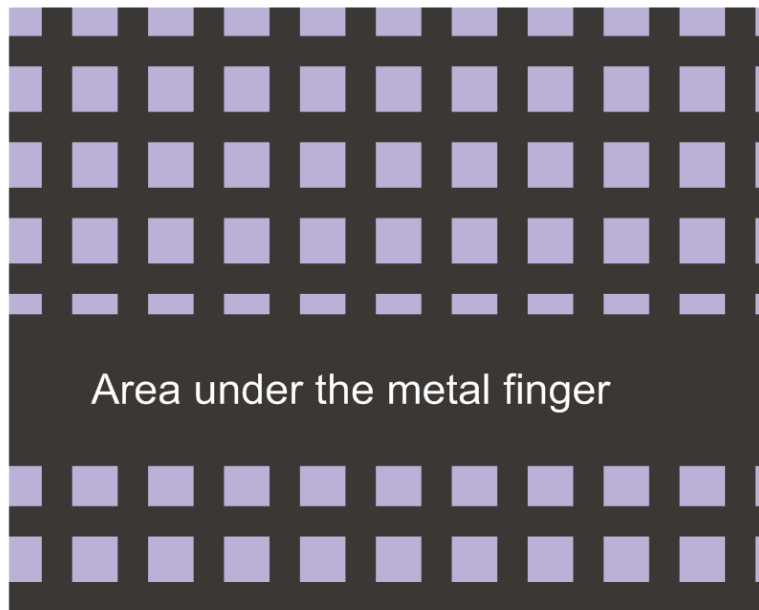


Figure 54 – the emitter pattern chosen to be used as the main scheme for photo-mask design. The emitter strips are arranged in a criss-crossed way. And where ever the metal fingers and bus bars lye, emitter pattern covers the whole area.

In order to experiment with different emitter coverage percentage and emitter strip width 10 different combinations of various emitter widths and emitter coverage percentages were included in the mask. These combinations are listed in Table 10. It should be mentioned that the lateral diffusion of the dopants during the high temperature diffusion step will make the emitter strips slightly wider than what is designed but this effect is ignored in the coverage calculations.

Emitter architecture number	Emitter width (μm)	Unit cell pitch (μm)	Emitter coverage
0	-	-	100%
1	3	13	40%
2	3	23	25%
3	5	10	75%
4	5	15	55%
5	5	55	17%
6	10	15	88%
7	10	30	55%
8	10	60	30%
9	25	45	80%

Table 10 – list of the 10 different emitter architectures included in the photo-mask design. Architecture number 0 is basically a standard solar cell with an emitter covering everywhere.

The cells were design to be 1x1cm and as a result, on one 4” wafer, 4 of each architecture were accommodated and randomly spread to even out the localized or random non uniformities over the wafer. Architecture number “0” is basically a standard cell without top layer and is made to have a reference for comparison of the performance. Also included on the mask are some test device structures to facilitate the study of the diodic behavior of the junctions and measurements of contact and sheet resistances of the various layers.

In general, three masks are needed for BWE cell fabrication. Figure 56 shows snap shots of the masks designed with a short description of each.

6.2.1 Top Metal contact Design

Using the formulation presented in [2] top layer contact was designed for an emitter layer of 40 Ω /sq sheet resistivity and a metal layer of around 15 m Ω /sq sheet resistivity which is equivalent to a 2 μm thick Aluminum layer. Figure 55 shows the schematic of the top contact together with the intended dimensions. Assuming the maximum power point of the cell would have a current density of

$J_{mp}=40\text{mAcm}^{-2}$ and $V_{mp}=0.60\text{ V}$, this contact design will account for 5.6% loss due to shadowing and resistive losses in the metal fingers and bus bar.

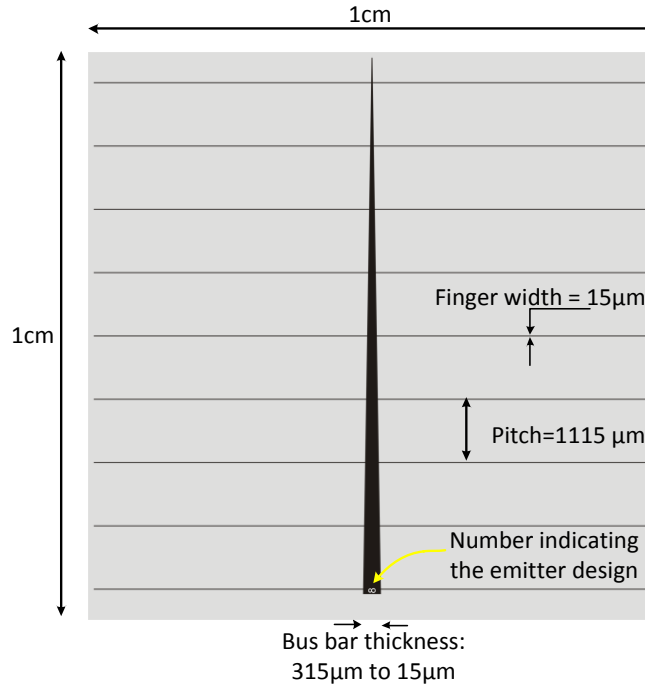
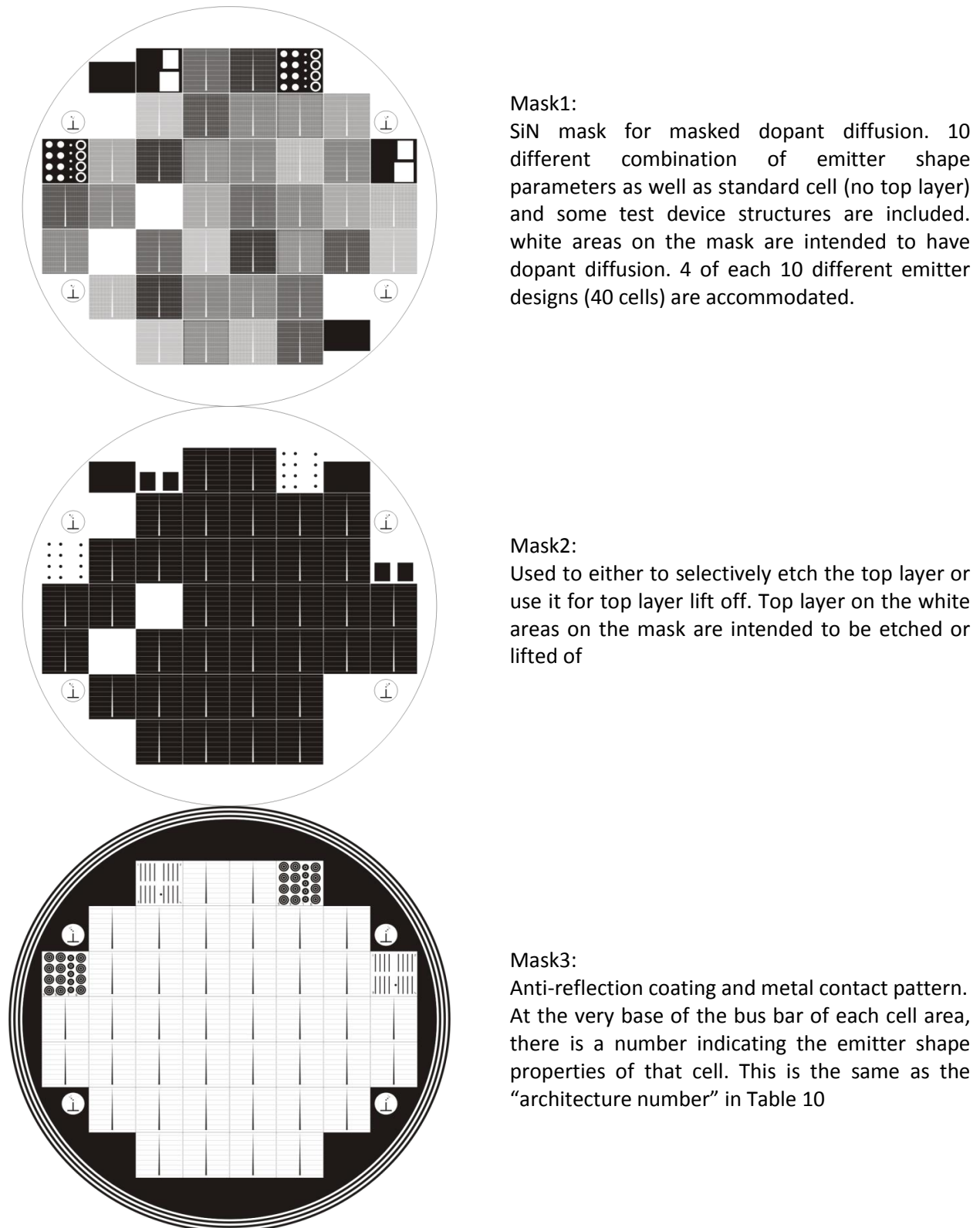


Figure 55 – schematic of the designed metal contact. The spacing and thicknesses of the fingers and the bus bar is designed for an emitter with 40 Ω/sq and a metal layer of 15 mΩ/sq sheet resistivity.

The mask for selective epitaxy or selective etch back of the top layer is designed in a way to give 7.5µm of error margin between the edge of the top layer and that of the emitter metal contact. This means that around the metal fingers, the opening in the top layer is 30µm wide for a metal finger of 15µm width. This will lower the chances of shunting in case the metal fingers make contact with the top layer because of misalignment in photolithography.



Mask1:
SiN mask for masked dopant diffusion. 10 different combination of emitter shape parameters as well as standard cell (no top layer) and some test device structures are included. white areas on the mask are intended to have dopant diffusion. 4 of each 10 different emitter designs (40 cells) are accommodated.

Mask2:
Used to either to selectively etch the top layer or use it for top layer lift off. Top layer on the white areas on the mask are intended to be etched or lifted of

Mask3:
Anti-reflection coating and metal contact pattern. At the very base of the bus bar of each cell area, there is a number indicating the emitter shape properties of that cell. This is the same as the “architecture number” in Table 10

Figure 56 - snap shots of the three photo-masks designed for the fabrication of the novel BWE solar cell.



Figure 57 – a color coded map of how different architectures of the designed emitters are spread on the mask. There are 4 instances of each architecture spread uniformly on the wafer to compensate for the random or localized defects over the wafer during processing. the numbers on each square represents the architecture number for the emitter on that area. Table 10 can be used as a reference for each architecture.

After fabrication of the masks, to verify that the method of masked diffusion will be implemented correctly a test phosphorous diffusion was performed through a silicon nitride mask patterned using the designed photo-masks. The result is a wafer with non-uniform back-surface field. The selective diffusion happened wherever there was an opening (transparent on mask) on photo-mask 1. Using the μ PCD photoconductivity decay measurement method of the bulk lifetime it was possible to see the effect of the masked diffusion the way it was expected. Figure 58 shows the bulk minority carrier lifetime map of the resultant wafer. It clearly shows the effect of the back-surface-field on each area. Higher lifetime measurement is expected where the emitter coverage percentage is higher. Comparing the lifetime map

shown in Figure 58 with the designed mask pattern shown in Figure 56 and the allocated spots for each architecture traceable from Figure 57 clearly verifies the validity of the masked diffusion process.

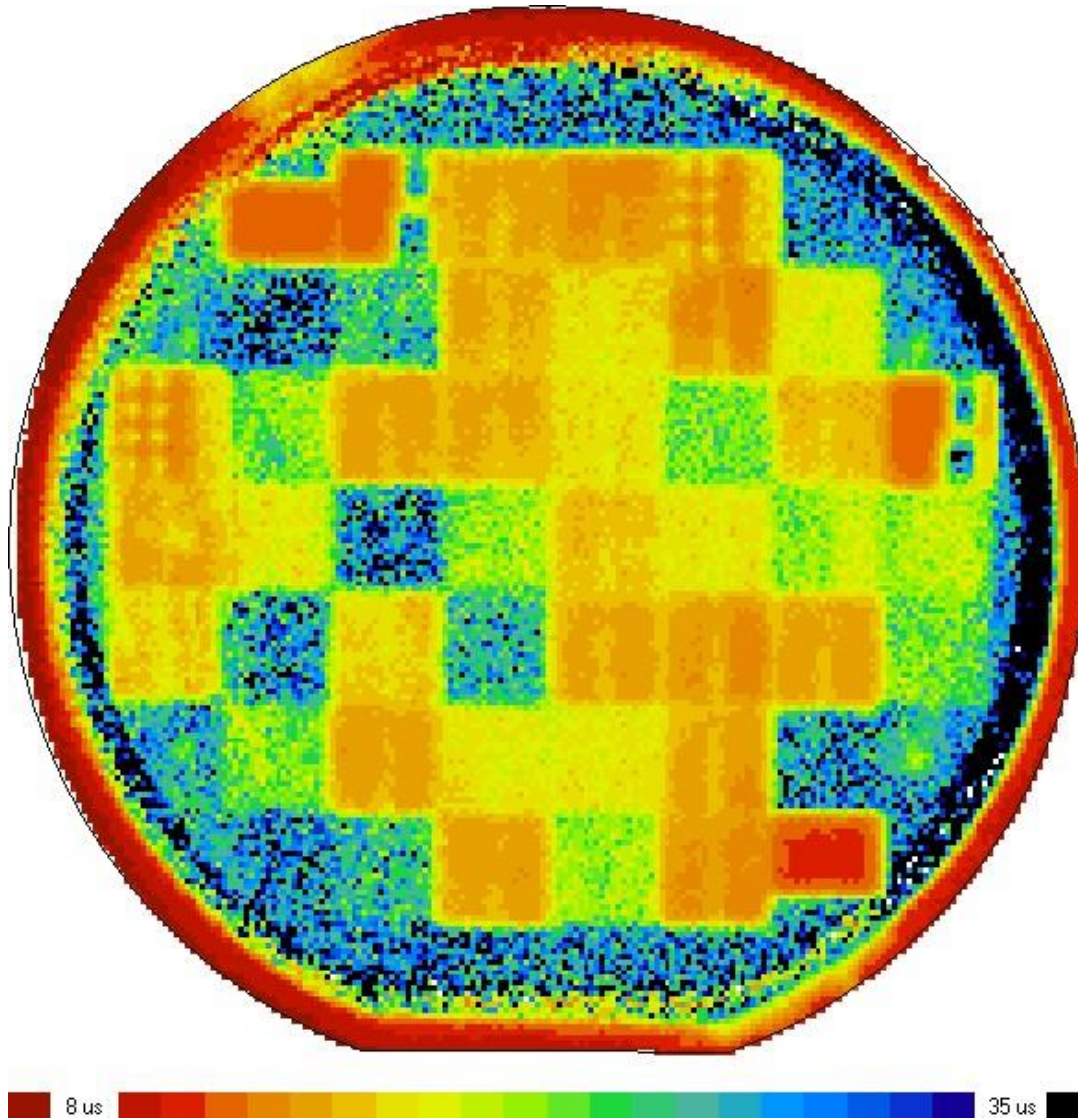


Figure 58 – bulk minority carrier lifetime map of a silicon wafer with BSF formed by masked diffusion of phosphorous through a SiN mask patterned by the fabricated photo-masks 1 measured using the μ PCD lifetime measurement tool in CAPDS. Comparison of this map with the pattern of the designed photo-mask clearly verifies the efficacy of the masked diffusion process.

Also as mentioned earlier in this chapter, some defects were observed in the fabricated masks leading to some discontinuities in the emitter patterns especially where the emitter strips were narrower. Figure 59 shows an image of an example of such defects. As stated before, the criss-crossed emitter pattern lessens the adverse effect of these defects by providing alternative connections through neighboring strips.

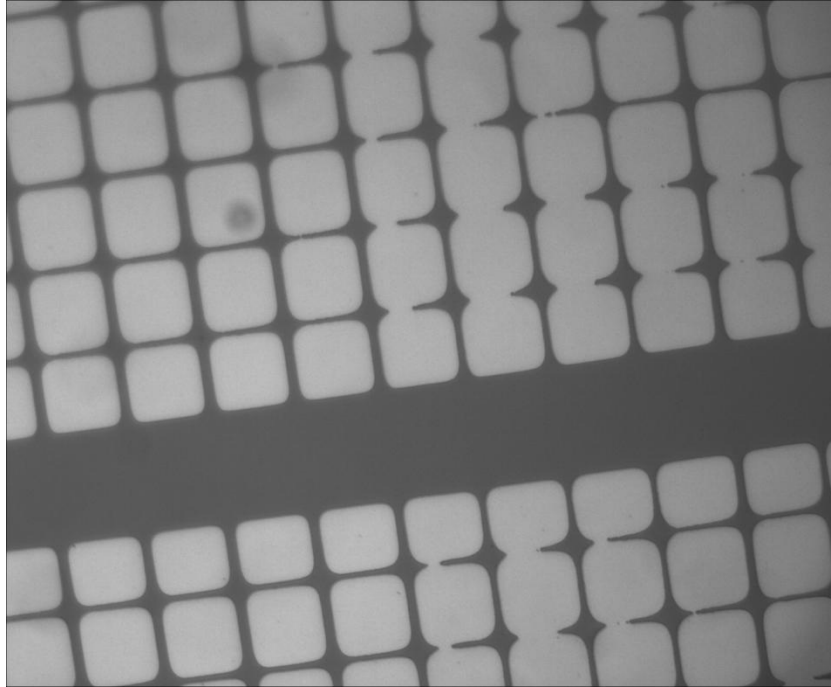


Figure 59, optical microscope image of the defective area on the mask for windowed emitter formation. Some disconnections are evident in the emitter strips but because of the redundant connections, the overall connectivity is preserved thanks to the crisscrossed pattern shown in Figure 54.

6.3 Detailed fabrication steps and discussion

Previously the general method we were going to use for the fabrication of BWE cell was outlined. In this section we will look at the fabrication in more details and will mention the difficulties encountered in each step and the way they were surpassed.

Table 11 lists all the steps taken to fabricate the whole cell. In what comes after, each step listed in this table will be explained in detail.

Step #	description
Step0	Examination of the wafers
Step1	Chemical cleaning
Step2	BSF formation using depant diffusion
Step3	Deglazing and removal of the parasitic diffusion on the front surface by acid etch back
Step4	PECVD SiN deposition on the front
Step5	PECVD SiN deposition on the back
Step6	Patterning of the front SiN layer using Mask1 for masked diffusion
Step7	Deep etching of the silicon only on the alignment mark areas using RIE
Step8	O ₂ aching to remove residual photoresist
Step9	Chemical cleaning
Step10	Masked emitter diffusion on the front
Step11	Deglazing and removal of the SiN mask
Step12	Emitter etch back on the front side to remove the dead layer or the borosilicate layer
Step13	PECVD SiN deposition to be used as top layer lift off layer
Step14	Patterning of the SiN using Mask2 and negative photoresist
Step15	O ₂ aching to remove residual photoresist
Step16	Chemical cleaning
Step17	PECVD epitaxy of the top layer
Step18	Patterning of positive photoresist using Mask2 to etch away the deposited silicon
Step19	RIE of the top layer.
Step20	Removal of the sacrificial SiN layer
Step21	O ₂ aching
Step22	Chemical cleaning
Step23	PECVD SiN deposition as front surface passivation and Anti-Reflection Coating
Step24	Patterning of the ARC SiN using Mask3 and negative photoresist also to be used for metal layer liftoff
Step25	Metal deposition on the front side
Step26	Metal deposition on the back side of the wafer
Step27	Liftoff of the metal on the front side using acetone
Step28	Forming gas anneal to improve the contact resistance
Step29	Dicing of the individual cells

Table 11 - all the steps taken to fabricate the proposed novel BWE solar cell.

Step0 Examination of the wafers

Before starting the processing, the wafers were examined using 4 point probe for the uniformity of the conductivity. Minority carrier lifetime was also measured on some select wafers to have an estimate of the original wafer's lifetime for cell fabrication.

Step1 Chemical cleaning

Wafers were given a sample number which was then engraved on an edge of the wafers using a diamond scribe. Then standard RCA1 clean (around 13 minutes in 5:1:1 combination of DI water: Ammonium hydroxide: hydrogen peroxide at 75-85° C) was performed and after washing the wafers, immediately RCA2 clean (around 13 minutes in 10:2:1 combination of DI water: hydrogen peroxide : Hydrochloric acid at 75-85° C) was done. After washing the wafers thoroughly with DI water, a 30 seconds dip in 2% Hydrofluoric acid was performed to remove the native oxide. After this step, the wafers will be aqua phobic. A subsequent wash in DI water followed by nitrogen gun dry were performed to finish the cleaning process. After this point, wafers were handled by only nonmetallic tweezers. We used PFA tweezers or quartz vacuum pens.

Step2 BSF formation using dopant diffusion

High temperature quartz furnaces with solid dopant sources were used for dopant diffusion. The solid dopant sources are thin circular disks of Boron Nitride for P-type diffusion and a phosphorus dopant material on an inert silicon carbide substrate for N-type diffusion. P-type sources were BN-975 from Saint-Gobain ceramic materials and the N-type sources were PH-950 from the same company. Boron diffusion sources need to be activated in oxygen ambient to form a B_2O_3 layer on the solid sources which will act as the dopant source. In order to make a diffusion of a certain dopant, one needs to place the wafers in the vicinity of these solid sources (around 1mm apart) and increase the temperature to the desired temperature for the required duration of time. The outcome of this process is very uniform and repeatable doping profiles. We used the following conditions for the two types of diffusion:

P-type: boron was diffused at 950°C for 60 minutes at 3 lit/sec N_2 flow. This process produces a p-type layer or around 40 Ω /sq sheet resistivity and a junction depth of around 0.6 μ m.

N-type: Phosphorous was diffused at 900°C for 45 minutes at 3 lit/sec N_2 flow. The outcome of this process is an n-type film of around 18 Ω /sq sheet resistivity and a junction depth of around 1.1 μ m.

The solid sources, when idle, are kept at 400°C under 2 lit/sec of N_2 flow to avoid hydration of the sources. In order to load the wafers, the boats which are carrying the sources are pulled out slowly from the furnace and kept in the cleanroom area for around 5mins to cool down. At this point, the wafers are loaded on the quartz boats using quartz vacuum pens. For BSF formation, the backside of the wafers was placed in the vicinity of the solid sources. Then the quartz carrier boats are loaded in the furnace and pushed slowly into the middle section of the quartz tubes and temperature is ramped up to the

diffusion temperature in around 30 minutes, and kept at that temperature for the required time, and then ramped down back to standby temperature (400° C). The ramp down time is much longer due to the design of the furnaces and it takes around 4 hours to finish.

Step3 Deglazing and removal of the parasitic diffusion on the front surface by acid etch back

After the dopant diffusion, there is a layer of glass 50-200nm thick which is deposited on the wafer surface during diffusion process. Etching for 2 minutes in 10% Hydrofluoric acid will remove this layer. In the case of Boron diffusion, there is a thin (around 20nm) layer of silicon-boron alloy which is the result of reaction of the dopant glass and silicon. This layer is not soluble in HF and has a brownish color and is aqua-fillic . The manufacturer of the dopant sources recommends a low temperature oxidation step after the dopant diffusion step to oxidize this layer and thin layer of silicon underneath. A subsequent dip in Hydrofluoric acid will etch away the oxide and expose the silicon surface. Instead of oxidation, to remove this layer we used the combination of 1% Hydrofluoric acid plus 99% nitric acid (silicon acid etch). Usually a 10 second dip in this solution will etch away the Si-Br layer and expose the silicon surface which is hydrophobic.

During the dopant diffusion, there is some diffusion on the opposite side of the wafer as well. This is because of deposition of the dopant source material on the back side of the wafer even though the opposite side of the wafer is not directly facing the solid dopant source. This needs to be removed. One could use PECVD SiN on the opposite side to mask the diffusion. We used acid etching of silicon (5%HF and 95% HNO₃) for around 2 minutes to remove a layer of around 2 μm thickness from the opposite side of the wafer to make sure that the opposite side (in this case the front side of the wafer) is purely the bulk type silicon. During this etching, one needs to protect the back (BSF) side of the wafer. For this, a PTFE holder designed by the author was used which seals the back side of the wafer using Viton O-rings and exposes only the front surface to the solution.

Step4 PECVD SiN deposition on the front

Up to this point we have a silicon wafer with Back-Surface-Field formed and the front surface is clean enough (provided that we have used clean acid solutions) for next step which is hydrogenated Silicon Nitride deposition in PECVD. According to author's experience, a SiN layer of 100nm thickness will serve well to mask the dopant diffusion, but to be on the safe side we deposited 200nm of SiN. Table 12 shows the PECVD conditions used for this deposition.

Recipe name	Pressure	TOP Electrode Power	SiH4 flow	N2 flow	NH3 flow	Temp.	Deposition rate	duration	Film thickness
SiNRec1	600mT	15W	5 sccm	0 sccm	100 sccm	350°C	5 Å/sec	6 mins	180nm
SiNRec2	200mT	40W	5 sccm	105 sccm	20 sccm	350°C	3 Å/sec	1 mins	18nm

Table 12 – PECVD recipe for the deposition of Silicon Nitride to be used as the diffusion mask.

The reason for using a two layer SiN film is that the film deposited using recipe SiNRec1 has bad photoresist adhesion properties, while the film from recipe SiNRec2 doesn't have this problem. On the other hand the film from SiNRec2, after going through the high temperature treatment in nitrogen ambient during the diffusion process, becomes annealed and closer to the stoichiometric silicon nitride and as a result it takes too long (sometimes more than 10 mins) for it to etch away in 10% HF solution after the diffusion is done. Long exposures of the silicon surface to HF can cause roughening of the surface which can be detrimental to the low temperature epitaxy we will do later on. To solve these issues, we use SiN from SiNRec1 (which etches away in around 3mins after annealing) as the main mask material but use a thin layer of the SiN from SiNRec2 on top of it to solve the photoresist adhesion problem.

Step5 PECVD SiN deposition on the back

After the front side SiN deposition, sample is flipped immediately and 200nm of SiN is deposited on the back side using similar recipe to protect the BSF when doing the emitter diffusion. We made sure that wafer doesn't take contaminations especially under the SiN layer, as one won't be able to clean the contaminants which are trapped under the SiN layer and these could be very detrimental to bulk lifetime and emitter-base diode quality during the high temperature emitter diffusion.

Step6 Patterning of the front SiN layer using Mask1 for masked diffusion

SiN on the front side was then patterned using Mask1 and positive photoresist to create openings in the SiN mask wherever emitter needs to be formed. AZ-3312 photoresist was used using the following conditions:

- 1- Spin coating, 4500 RPM, 45 seconds
- 2- 1 min soft bake at 90°C
- 3- UV exposure, 60 seconds, at 60mWcm⁻²
- 4- Developing in AZ-MIF Developer for around 60 seconds
- 5- 3 minutes hard back at 110°C (since it will be used in an HF solution)

After patterning the photo resist, Buffered Hydrofluoric acid solution was used to etch the SiN. It would take around 90 seconds to reach to an aqua phobic silicon surface. In order to have a uniform etch especially on the small openings, wetting of the wafer in DI water would help prevent bubble formation on the small openings. The bubble trapped around smaller geometries reduce the etch rate on these areas causing a non-uniform etch over the wafer. Note again that, the SiN on the back side needs to be protected during this etching step and the PTFE one side etching holder was used again for this purpose.

Step7 Etching of the silicon only on the alignment mark areas using RIE

After a successful etch and before removing the photoresist, we made some deep etching on the alignment parts only. The reason for this is to be able to align the second and third masks with the first

one. It had been assumed that a masked diffusion would leave a clean surface without visible traces of the mask pattern, hence decided to etch the alignment mark areas. Although it turned out that actually masked dopant diffusion (especially Boron diffusion) leaved a clear step between the masked and non-masked areas which became a source of doubt whether the epitaxy will work perfectly on such a stepped surface. We will talk about this issue later on.

To be able to etch the alignment mark areas, an aluminum plate of thickness around 3mm with 4 holes on the same locations of the alignment marks, as shown in Figure 60, was used to cover the whole wafer and protect it during the Reactive Ion Etching. The RIE condition used is shown in Table 13.

Recipe name	Pressure	RIE voltage	SF6 flow	O2 flow	Duration	Etch depth
Si-RIE1	50mTorr	-40 VDC	22 sccm	3 sccm	60 seconds	1.3 – 1.6 μ m

Table 13- the RIE recipe for alignment mark etching on silicon. This recipe was learnt from the previous users of the lab.

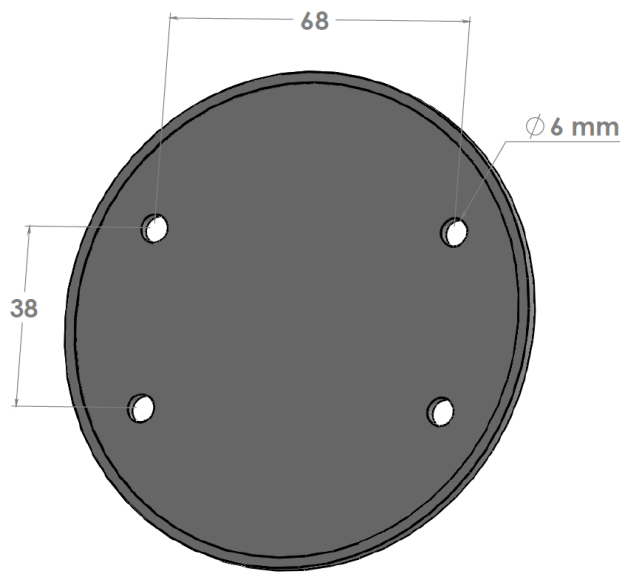


Figure 60 - the Aluminum mask used to etch only the alignment mark areas of the SiN mask pattern. The alignment marks were aligned to be under the 4 holes shown. The rest of the wafer is unaffected by the RIE etching.

Step8 O2 ashing to remove residual photoresist

After the etching of Sin and engraving of the alignment marks, the photo resist is washed away using HPLC grade acetone followed immediately (without letting acetone to dry and leave residues on the wafer) by an HPLC grade Isopropanol Alcohol rinse and then washed by DI water. This will remove most of the photoresist but there is a high chance of some residual photoresist remaining on the wafer. To lower the content of this residual photoresist, Oxygen plasma ashing was used to clean the surface further. The RIE condition for this ashing is shown in Table 14.

Recipe name	Pressure	RIE voltage	ICP power	O2 flow	Duration
Ph-ashing1	50mTorr	-50 VDC	50 W	25 sccm	3 minutes

Table 14 - photoresist ashing condition in RIE.

Step9 Chemical cleaning

After the completion of the SiN mask making process and before loading it into diffusion furnace, we did another set of RCA1 and RCA2 cleaning. A quick (10 sec) dip in 2% HF followed by DI water rinse was also performed right before loading the wafer onto the diffusion furnace. Once again after this point, the wafers were not handled by metal tweezers to avoid metallic contamination before the high temperature step of the diffusion.

Step10 Masked emitter diffusion on the front

After the chemical cleaning, the wafers were loaded in the diffusion furnaces in a way that the front side of the wafer was facing the solid diffusion source. Since the back side is protected by a SiN layer, then there won't be any interference in the BSF layer. The BSF layer will diffuse a bit deeper though because of the excess heat the wafer gets exposed to. Emitter formation was done in the same conditions as the BSF formation mentioned in step2.

Step11 Deglazing and removal of the SiN mask

After completion of the diffusion process, wafers were dipped in 10% Hydrofluoric acid to remove the dopant glass as well as the SiN mask. Since the SiN has effectively been annealed in nitrogen ambient, it takes a bit longer for it to etch away (around 3mins).

Step12 Emitter etch back on the front side to remove the dead layer and/or the borosilicate layer

As mentioned before, after dopant diffusion, the layers of silicon very close to the surface are very highly doped and defective and in the case of Boron diffusion there actually is a layer of Si-Br which needs to be removed. We use silicon acid etch to remove some layer from the diffused layer to both remove the defective layer and also adjust the sheet resistance to what the masks are designed for (40Ω/sq in our case). Where n-type substrates were used, the emitters was made by Boron diffusion and 10 second etch in 1%HF and 99% HNO3 would remove the Si-Br layer and expose the silicon underneath it. After this etch the sheet resistance increase to around 43-45 Ω/sq.

In case of p-type substrates which would need phosphorous doping for the emitter formation, longer times of etch in the acid mix would be needed to adjust the sheet resistance because the phosphorous diffusion would produce a layer of around 18Ω/sq sheet resistivity while Boron diffusion gives a layer of around 40 Ω/sq.

One thing we noticed at this stage was that masked diffusion creates steps between the mask and non-masked areas. Figure 61 shows a height profile of the surface of the silicon after diffusion. Dektak was used for this profilometry. These steps might cause problems later on for the low temperature epitaxy we will need but this issue will need more work to be completely resolved.

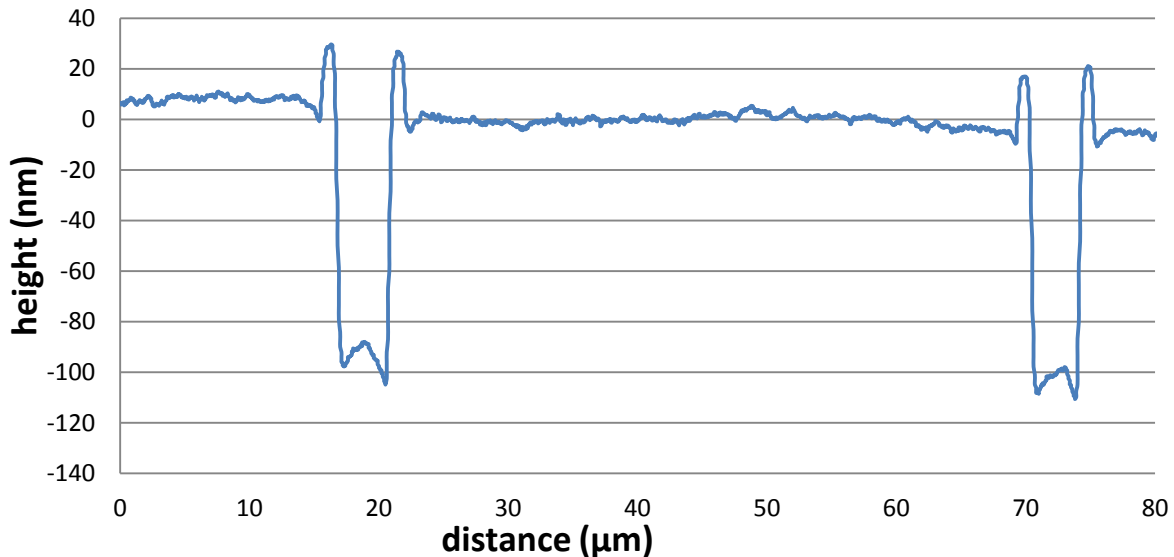


Figure 61 – Dektak profiling of the surface morphology of silicon wafer after masked dopant diffusion. It shows that after dopant diffusion, there are height differences between the masked and non-masked areas.

Step13 PECVD SiN deposition to be used as top layer lift off layer

After emitter etch back, the wafer was loaded to PECVD for a SiN film deposition to be used as the sacrificial layer for the top layer epitaxy. The reason to use this sacrificial layer is that it might be difficult to control the etching of the top layer and make sure the etching stops immediately on it underlying emitter surface. To facilitate this, a SiN layer is deposited and patterned using Mask 2 and negative photoresist. To form this layer, the recipe SiNRec2 mentioned in step4 was used to deposit a layer of around 400nm thickness. The reason for the large thickness of this layer is the necessity of an HF dip step before epitaxy. The SiN sacrificial layer is made thick enough to survive this HF dip step.

Step14 Patterning of the SiN using Mask2 and negative photoresist

The SiN layer was then patterned using Mask2 and negative photoresist. We used AZ nLOF2035 as the negative resist with the following conditions:

- 1- Spin coating, 4500 RPM, 45 seconds
- 2- Soft bake, 1 min at 110°C
- 3- Exposure, 120 seconds, 60mWcm⁻²

- 4- Post exposure bake, 1 min at 110°C
- 5- Developing in AZ-MIF Developer for round 60 seconds
- 6- Hard bake, 2 mins at 110°C (because of exposure to HF)

Then the SiN layer was etched in Buffered HF solution. It would take around 4mins to reach to an aqua phobic silicon surface. Note that one should avoid extra exposure of the sample at this stage to BHF because of two reasons:

- 1- The SiN pattern would over etch and will cover smaller area than what they are supposed to
- 2- An interesting phenomena, of unknown nature to author, would happen to the exposed isolated emitter islands. A dark blue layer would start forming on only the islanded emitter areas. This layer will etch away in a subsequent RCA1 clean though but is an interesting issue to find the nature of.

After the completion of the etch, the photoresist was removed by acetone and immediate wash of IPA and water

Step15 O₂ ashing to remove residual photoresist

Similar to a previous case, in order to remove small residues of the photoresist, a 3 min photoresist ashing in RIE was performed with conditions mentioned in Step8.

Step16 Chemical cleaning

Since the epitaxy is very sensitive to the interface of the underlying substrate, cleaning is of crucial importance for a successful epitaxy. Because of this, another set of RCA1 and RCA2 cleans was performed on the wafers..

Step17 PECVD epitaxy of the top layer

The epitaxy of the top layer is the most critical part of the BWE solar cell and the improvement of performance is mainly dependent on the quality of this layer. If the film quality is not high enough, not only the performance will not improve but will experience severe degradation. We will see in the results and discussion section that an epitaxial film good enough for BWE cell might be very difficult to achieve using low temperature epitaxy. However, This issue needs more investigation.

As mentioned in chapter-5, we noticed that films of different doping have different optimum conditions for deposition. The top layer for the BWE cell has two critical requirements:

- 1- It is an absorbing layer, so it must have high minority carrier lifetime and hence a highly doped layer will most likely not be the right candidate
- 2- It should have a minimum conductivity as otherwise there will be considerable resistive losses.

Since we were only able to deposit either highly doped or intrinsic layers then the natural choice was to go with a stack of intrinsic absorbing layer with a thin highly conductive layer on top.

The best recipes we had found for each layer were used to deposit an intrinsic layer of around 370nm thickness to serve as the main absorbing layer and then an n+ layer of 30nm thickness on top to serve as the conductive layer. We believed that the intrinsic layer should have high minority carrier diffusion length.

Right before loading the wafers into the PECVD chamber for epitaxy, a 20 seconds dip in 2% HF solution was performed to make sure the native oxide is etched away. This step needs to be done with care as the sacrificial SiN layer is also being etched during the HF exposure.

The PECVD deposition conditions of the top layer are shown in Table 15.

Type of film	Pressure	Top electrode power	SiH4 flow (sccm)	H2 flow (sccm)	PH3 flow (sccm)	Temp.	Duration	Film thickness
Intrinsic	800mT	22W	5	100	0	300°C	41mins	370nm
n ⁺	200mT	15W	10	250	8	300°C	14mins	30nm

Table 15 – deposition recipes for the top epitaxial layer.

This film, in total, has a sheet resistance of around 180Ω/sq which is solely the conductivity of the thin n⁺ layer. This high conductivity is also an indicator of full crystallinity of the top layer up to the n⁺ layer.

Step18 Patterning of positive photoresist using Mask2 to etch away the deposited silicon

After unloading from PECVD, in some cases, the amorphous silicon film deposited on the SiN sacrificial parts will start to peel off automatically because of the stress in it. If this mechanism works throughout the wafer, then one doesn't need another patterning to remove the a-Si, but this automatic peeling off is stronger on larger patches of the SiN sacrificial layer and stops on the narrow strips. Using ultrasonic bath to speed up the process helps to remove the a-si on some smaller SiN areas as well but it doesn't give a perfect finish. Figure 62 shows an optical microscope image of the sample after 10minutes in ultrasonic bath in DI water followed by 4 minutes etch in 10% HF solution to remove the underlying SiN layer. One can see some residues of the top layer on the edges of the SiN strips. An ultrasonic step after HF etch helps remove more of the residues but still there will be some parts which are not perfectly lifted off. So if this method is being used for the lift off method, it needs some fine tuning to achieve perfect and reliable results. We also tried some rapid heating of the film hoping the hydrogen content of the amorphous layer will make small pin-holes while outgassing from the film and will open some access points for the HF to penetrate under the a-Si layer, but the results didn't show much improvement. And actually there were some pin holes created in the top layer itself as can be seen in Figure 62.

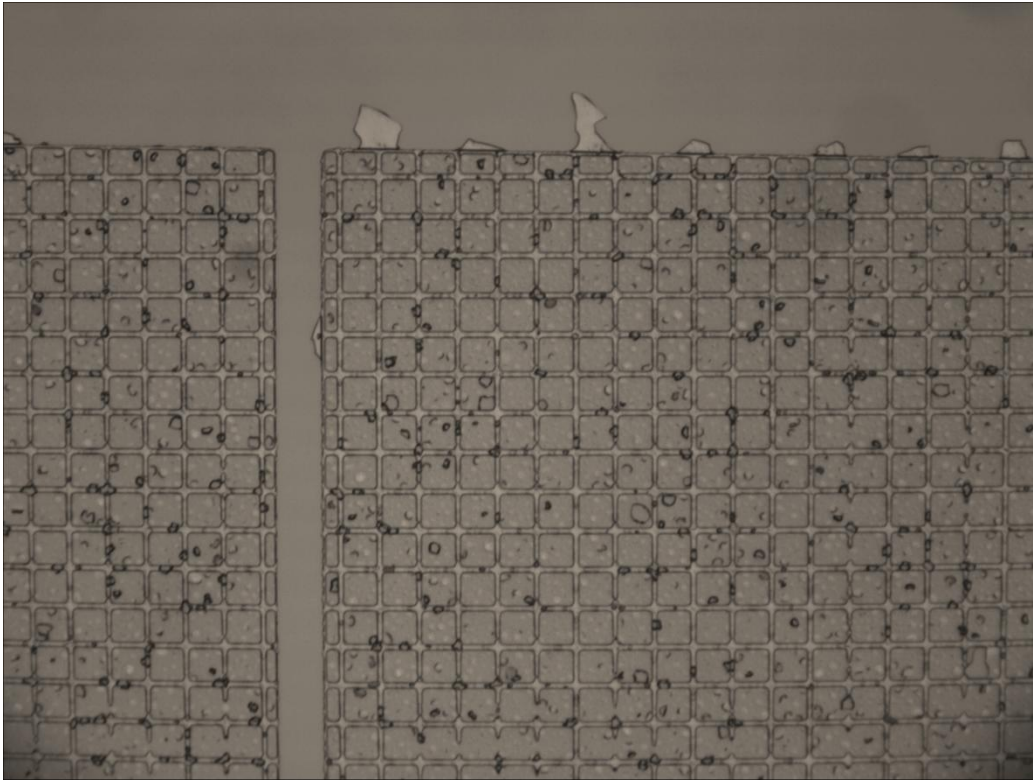


Figure 62 - optical microscope image showing the residues of the lifted off a-Si layer after Ultra-sonication and Hydrofluoric etch of the sacrificial SiN layer. Also visible are the pin holes generated on the top layer because of a rapid heat treatment.

What was said above won't apply for all the samples, as sometimes the film won't peel off by itself. In these cases which were the usual case, a photolithography step using Mask 2 and negative photoresist would be needed to etch the top layer where needed. For etching a time-controlled RIE process was used to etch away the a-Si on the SiN part.

Step19 RIE of the top layer.

Having SiN under the parts to be etched, gives some error margin in the etch depth control as well as a visual indication of when the etching is complete. This will be the case only if there was not much of over etching of the SiN layer when patterning it. If the SiN layer is narrower than the mask because of over etching of it during buffered HF etch used for patterning it in step14, then while etching using RIE, a thin strip of the area to be etched does not have sacrificial layer underneath and if the etching process goes on for too long, there could be some over etching of the underlying emitter layer. It is possible, however, to avoid this fairly easily by careful etching control.

Multiple steps of RIE etching with the same recipe mentioned earlier in Step7 (Si-RIE1) was used to do the etching. We noticed that the etch rate by mentioned RIE recipe is not a linear function of time. The etch rate is low at the start of the etch process but then suddenly increases to a very high value. To have good control, the etching was performed in 2 or 3 shorter steps. In one case, after 22+33 seconds of

etch using recipe Si-RIE1 the top layer was fully removed together with less than 100nm of over etching of the underlying emitter. In another case, etch times of 11+11+11+22+22 seconds produced an almost perfect finish on the emitter surface.

Step20 Removal of the sacrificial SiN layer

After the RIE etching of the top layer, the exposed sacrificial SiN was etched in 10% HF solution for around 60 seconds.

Step21 O₂ aching

After the SiN sacrificial layer removal, the photoresist was removed by Acetone and IPA. Another photoresist ashing step similar to what was mentioned in Step8 (recipe Ph-ashing1) was performed to remove the remaining residues of the photo resist before the chemical cleaning step

Step22 Chemical cleaning

After successful patterning of the top layer, next step is to deposit the anti-reflection coating on. For the ARC to have good surface passivation features, a clean interface between the ARC and the underlying silicon is required. Because of this a RCA1 clean step was done again before SiN ARC deposition

Step23 PECVD SiN deposition as front surface passivation and Anti-Reflection Coating

Next was to deposit the anti-reflection coating. We used PECVD SiN using recipe SiNRec1 (mentioned in Step4). 253 seconds of such deposition will make a 78nm thick ARC layer which is close to the optimum value for a single layer SiN for AM1.5 spectrum. The reflection spectra of such a film on bulk silicon is shown in Figure 63, but as we will see later on, the reflection spectra of such a SiN layer deposited on BWE cell's top layer has a different shape. This is because of the different refractive index the epitaxial film has which is somehow a disappointing news in terms of how perfectly crystalline with close to bulk characteristic the epitaxial film is. The SiN from this recipe, should also give decent surface passivation [28].

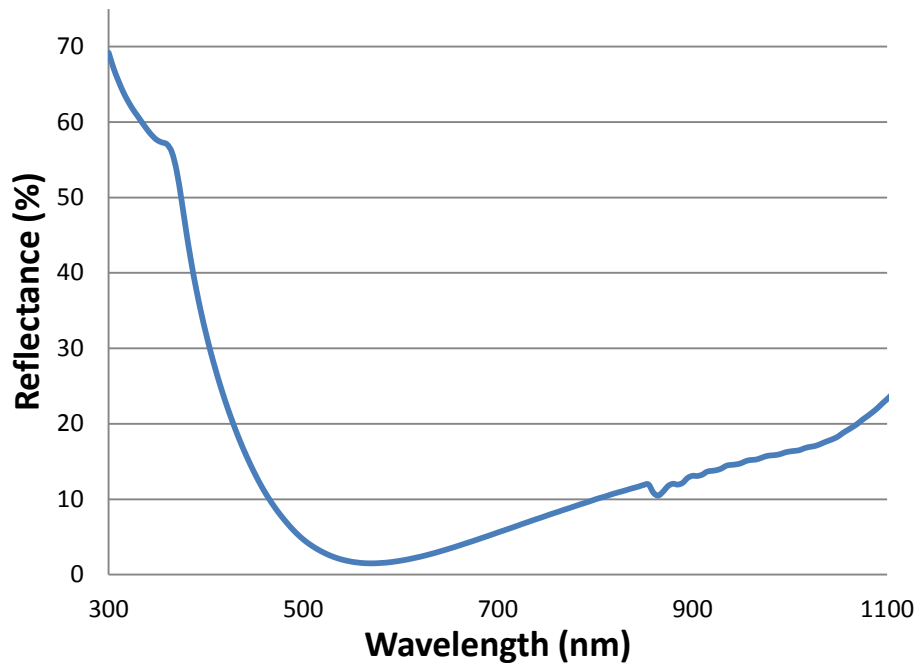


Figure 63 – measured reflection spectra of 78nm of SiN deposited using PECVD on crystalline silicon substrate

Step24 Patterning of the ARC SiN using Mask3 and negative photoresist, also to be used for metal layer liftoff

The deposited SiN alyer was then patterned using Mask3 and negative photoresist (AZ nLOF 2035). This time the photoresist spinning was set to 2500RPM for 90 seconds to produce a photoresist layer of around 4µm thickness. High thickness is necessary as this layer will be used as the sacrificial layer for the metal layer which will at least be 1µm thick (if silver is used)

After patterning the photoresist and a 2 minutes hard bake at 110°C, SiN was etched in BHF solution. Again wetting the wafer surface with DI water before dipping it into the BHF solution leads to a better uniformity of the etch on small openings. The etching of this layer took around 40 seconds to reach to an aqua phobic silicon surface.

Step25 Metal deposition on the front side

Immediately after SiN etch in BHF, the wafers were loaded (with the photoresist on) into the electron beam evaporation chamber for metal deposition. After reaching to base pressure in the 10⁻⁷ Torr range, metal deposition was started by first a 30nm thick layer of Titanium followed by a 1µm thick Aluminum layer. Titanium layer is deposited to act as a barrier for Aluminum to prevent its diffuse into the silicon during the forming gas anneal performed later on.

As mentioned before, the metal contact masks were designed for a metal layer of $15\text{m}\Omega/\text{sq}$ which is equivalent to $2\mu\text{m}$ Aluminum. But we deposited only $1\mu\text{m}$ to have easier job lifting it off as thicker layers of metal would have some difficulty being lifted off by the $4\mu\text{m}$ thick sacrificial photoresist. One can alternatively use $1\mu\text{m}$ of silver instead or used metal layer etching alternatively. Metal etching will have its own difficulties as Titanium makes a very thin layer of alloy with silicon which needs Hydrofluoric acid based solutions to be removed and exposure to HF causes severe over etching of the Aluminum layer on top of it. In short, it's possible to do metal etching, but the process needs to be optimized. A metal layer thinner than the optimized one will cause a little loss due to series resistance but for the device analysis we are looking for (mainly spectral response), this will not cause any problems.

Step26 Metal deposition on the back side of the wafer

After the front side metal deposition, the sample was flipped immediately (to avoid oxidation of the back surface because of air exposure) and similarly 30nm Titanium and $1\mu\text{m}$ Aluminum was deposited on the back side as well.

Step27 Liftoff of the metal on the front side using acetone

Next was to lift off the metal on the front side and this was done by submerging the wafer into HPLC grade acetone for around 20 minutes. Occasional stirring of the acetone will help speed up the lift off process. Ultrasonic bath can also be used for this purpose.

Step28 Forming gas anneal to improve the contact resistance

In order to improve the electrical contact quality between the metal layer and the emitter as well as the metal layer and the BSF layer, a forming gas anneal step was done at the end. Wafers were annealed at 350°C for 10 minutes at a forming gas (10% H_2 , 90% N_2) flow of 3 lit/sec. note that the control of the time is critical here and if the samples are left at this temperature for too long, the barrier Titanium layer will be consumed and Aluminum will start spiking into the bulk causing the sever shorting of the emitter to bulk silicon.

Step29 Dicing of the individual cells

And as the last step, the individual cells and test device structures were diced. 4 of each 10 different types of emitter design plus the test device structures were separated and ready for analysis. Figure 64 shows a photo of the completed BWE solar cell before dicing. It also shows some individual cells and two instances of the test device areas after dicing.

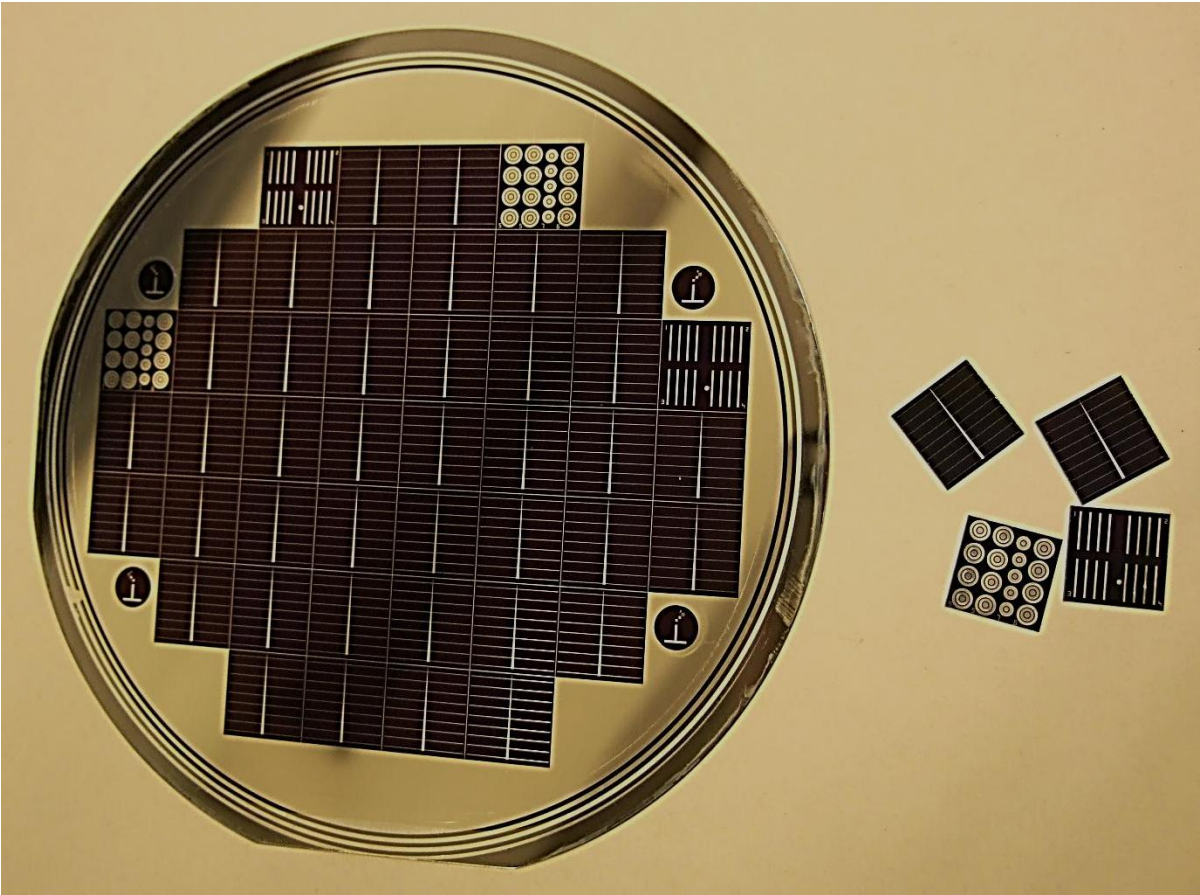


Figure 64 - photo of the completed BWE solar cell before dicing. On the right, shown are two individual cells and two instances of the test device areas after dicing.

Chapter 7 - Results and characterization of the fabricated novel BWE solar cells

This chapter presents the characterization results of the various cells fabricated using the method explained in chapter-6. The Proposed Buried-Windowed-Emitter solar cell is a novel device architecture with a rather complicated structure. To understand the benefits and drawbacks of its added complexity it is easier to study it in steps. In order to be able to study each novel part of BWE solar cell architecture, three series of solar cells were fabricated using the masks designed each focusing on one part of the whole structure. These three series of cells are as follows:

- (1) A BWE solar cell without the top layer; One of the major differences of this device is the windowed structure of its emitter which by itself has a considerable effect on the carrier collection performance of the solar cell. To study this feature separately, a set of solar cells were fabricated using the designed masks by only omitting the top epitaxial film deposition. The result is a conventional solar cell architecture but with windowed emitter instead. Spectral response measurements of these cells reveal interesting information about the effects of the various emitter architectures used on the carrier collection properties of the cells and proves that a fully fabricated BWE solar cell with a high quality top layer will have high conversion efficiency justifying the added complexity.
- (2) A solar cell with a conventional architecture which uses the developed epitaxial silicon film as its emitter: another major novelty in the architecture of the BWE solar cell is the introduction of an epitaxial silicon film on top of the windowed emitter. This layer must have high minority carrier lifetime in order to achieve the expected performance. To study the quality of the developed epitaxial technology discussed in chapter-5 a solar cell was made which used the deposited epitaxial layer as its emitter. Spectral response of this structure will give very valuable information about the quality of the epitaxial film.
- (3) And finally a full Buried-Windowed-Emitter was fabricated in order to prove its expected functionality as well as its fabricate-ability using the developed technology presented in chapter-6.

In what comes next, first the characterization methods used such as Dark and Illuminated IV, bulk minority carrier lifetime, External Quantum Efficiency and reflectance measurements are explained briefly and then the results of the characterization of the solar cells made are presented and the findings are discussed.

7.1 Characterization methods used:

7.1.1 Minority carrier lifetime measurements

Microwave photoconductivity decay method was used to measure the bulk minority carrier lifetimes of the bare wafers before the start of the cell fabrication. In this method, as shown schematically in Figure 65, a short laser pulse with wavelength of 904nm is shone on a spot on the wafer which results in a localized temporary rise in the concentration of the minority carriers. The increased non-equilibrium population of the minority carriers will decay exponentially and hence the measured conductivity of the excited area. An exponential form is fitted to the measured conductivity from which the lifetime is extracted. A Semilab WT-2000X μ -PCD tool available I the CAPDS was used for this purpose.

By moving the measurement head with respect to the wafer, it is possible to generate a map of minority carrier lifetime in a wafer as a function of location.

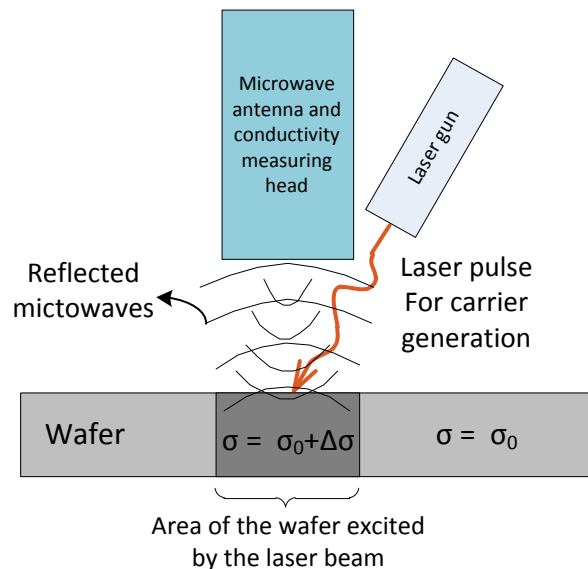


Figure 65 – schematic of the principles of minority carrier lifetime measurement using the μ -PCD method.

7.1.2 Measurement of reflection spectra

In order to be able to calculate the Internal Quantum Efficiency of the solar cells, it is necessary to know how much of the input light is actually entering the interior of the device and how much is being reflected. Figure 66 shows the schematic of a measurement setup to extract the reflection spectra of a sample. It uses a monochromator to create rays of light with known wavelengths. The input intensity of these rays is monitored using a semi-transparent mirror and a reference photo-detector. The reflected beams of light reflected from the surface of the specimen is collected using an integrating sphere and directed to the sensing photo-detector located inside the integrating sphere. The ratio of the signal at this detector to the signal at the input light monitoring detector represents how much of input light is reflected from the surface. A PerlinElmer Lambda 1050 UV/VIS/NIR spectrometer available in CAPDS was used for these measurements.

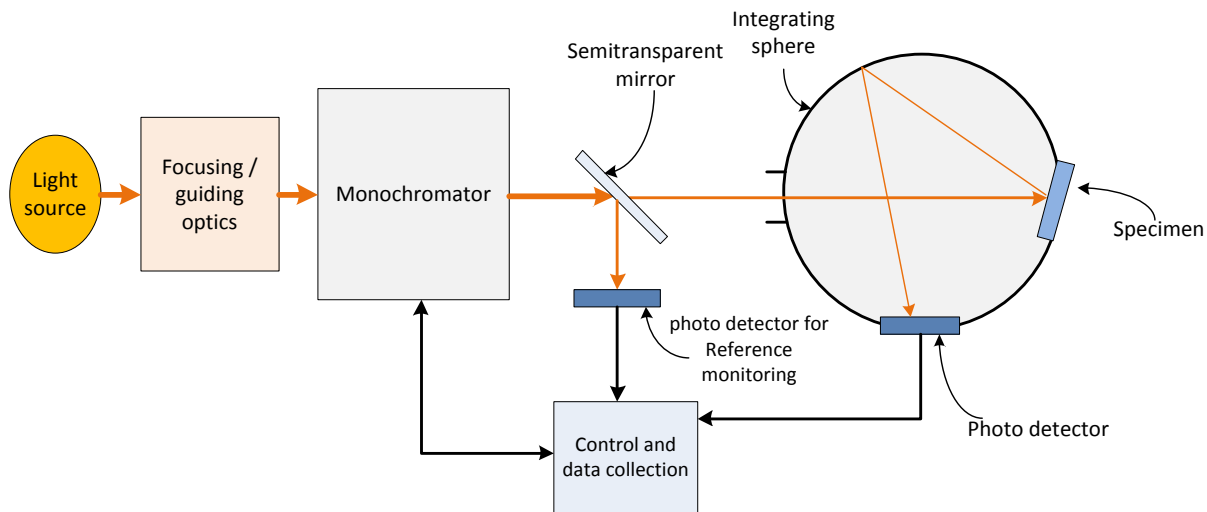


Figure 66 – schematic of a setup for measurement of the reflectance spectra of a specimen.

7.1.3 External Quantum Efficiency

The most reliable method of studying the performance of the fabricated cells is the Internal Quantum Efficiency, but this quantity cannot be measured directly. However, it can be calculated using the results of the measurement of the reflection spectra and the External Quantum Efficiency. EQE measurement setup is schematically presented in Figure 67. It has a great similarity to the reflectance measurement setup except that here, instead of an integrating sphere, the solar cell under the illumination by the ray of light with known intensity and wavelength is directly probed to measure its short circuit current. The

spectral measurement system made by PV measurements, Inc. available at the CAPDS was used for this purpose.

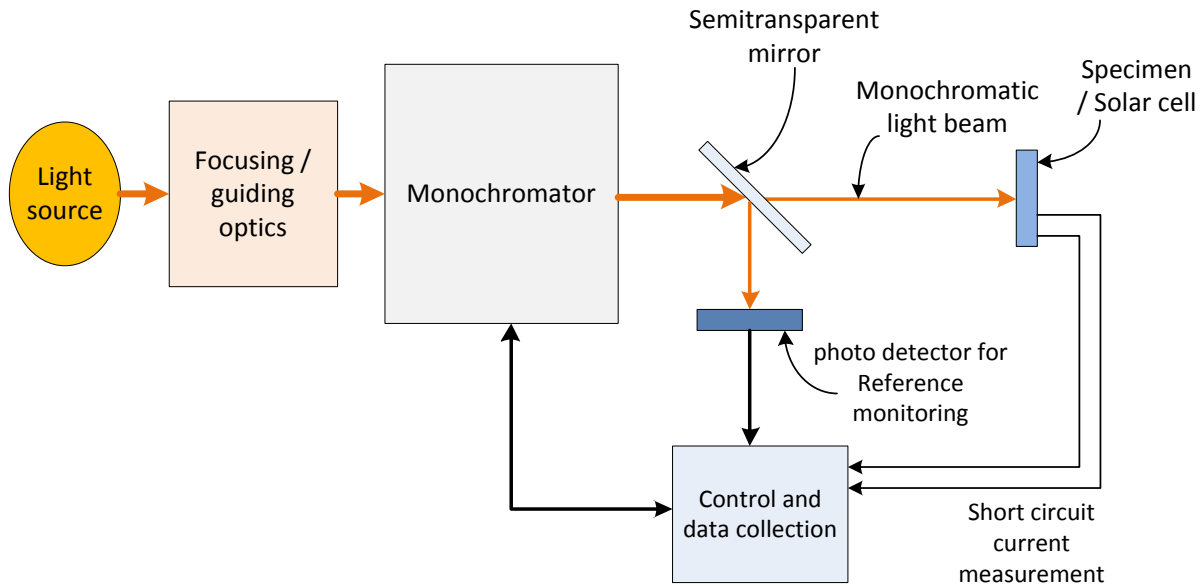


Figure 67 – schematic of a setup to measure the External Quantum Efficiency of a solar cell.

7.1.4 Dark and Illuminated current-voltage measurements

Electrical measurements give important information about the junction quality and performance under a standard illumination. Dark IV is used to extract the junction parameters and it is performed under absolute darkness to eliminate the effects of carrier generation because of ambient light. these measurements were performed in a light-tight housing in which the sample and the probing station is placed. The schematic of such measurement setup is shown in Figure 68. An Agilent HP4155C semiconductor parametric analyzer available in CAPDS was used to measure the dark IVs of the cells and test structures..

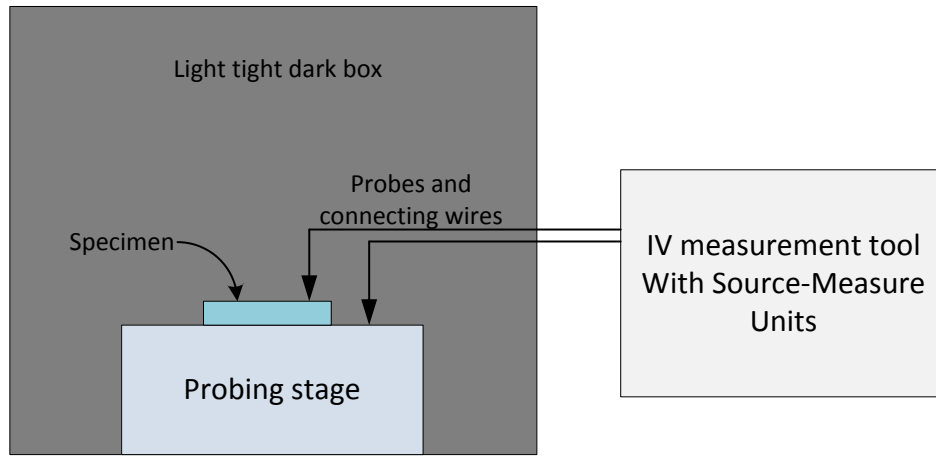


Figure 68 – schematic of a dark IV measurement setup.

To study the performance of the solar cells under the standard AM1.5 illumination, illuminated IV curves were measured using a setup similar to what is shown in Figure 69. It consists of a light source construction which estimated the spectrum of the AM1.5 light and can produce uniform lighting for industrial sized solar cells. The tool used for this purpose in CAPDS was made by PV measurements, Inc.

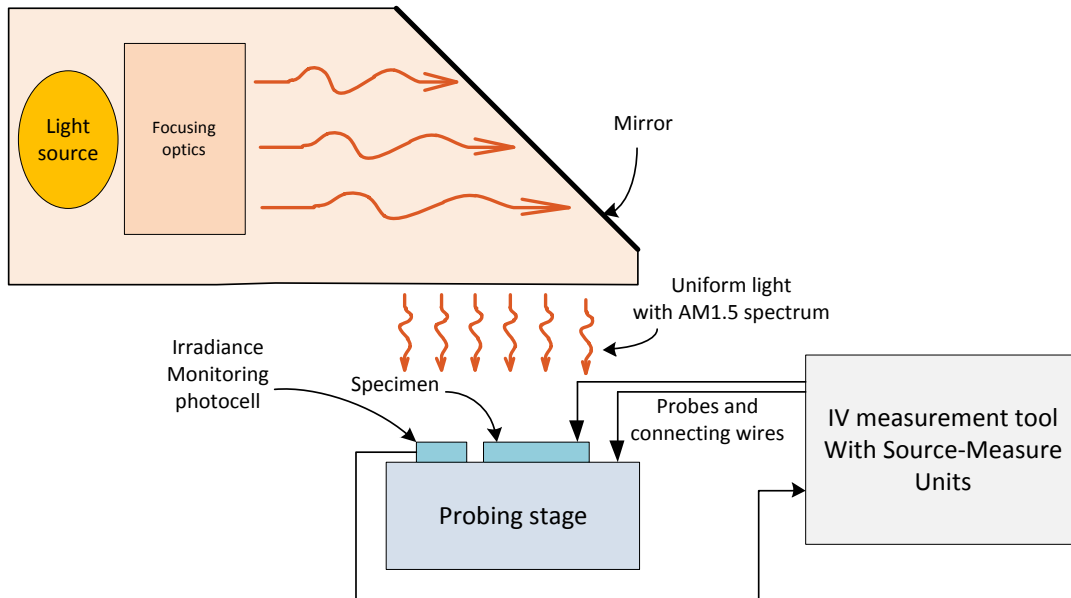


Figure 69 – setup used for the measurements of illuminated IV of the solar cells

7.2 Characterization and discussions of the cells with windowed emitter and without the top layer

In order to separately study the effects of windowed emitter on the device performance, a series of solar cells were made using the masks designed for BWE solar cells which had windowed emitter architecture but without the top layer. The schematic of this solar cell is shown in Figure 70.

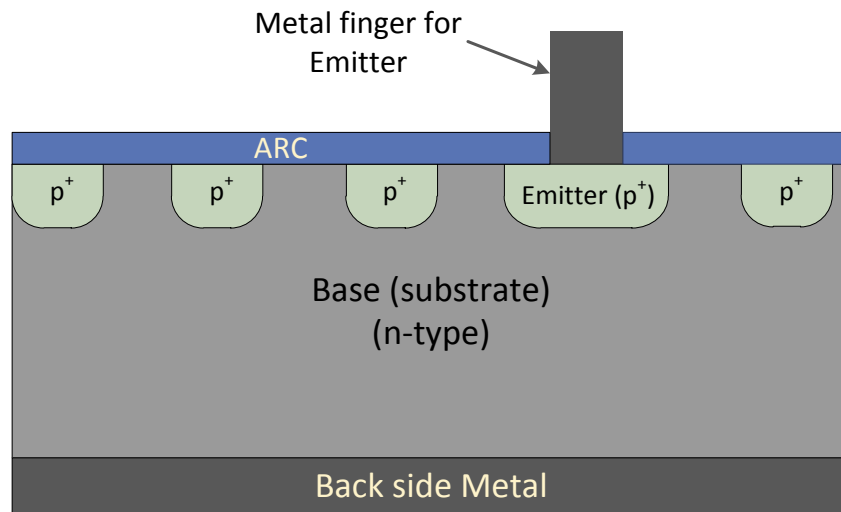


Figure 70 – schematic of the cell fabricated without the top layer to study the effects of partial coverage of emitter

This structure also meant to be used to study the addition of the top layer in BWE cell when compared with the cells without a top layer..

A brief description of the important information about the fabricated cell is as follows:

Substrate: 4 inch diameter, <100> n-type silicon wafer, 1-2 Ωcm bulk resistivity, 350 μm thick, 44 Ω/sq sheet resistance. Lifetime map of the wafer before fabrication is shown in Figure 71 showing an average minority carrier bulk lifetime of around 24 μs .

Back Surface Field (BEF): 18 Ω/sq , formed by phosphorous diffusion at 900°C for 45 minutes.

Emitter formation: 40 Ω/sq etched back to have 45 Ω/sq . formed by masked diffusion of Boron at 950°C for 60 minutes.

Anti-reflection-Coating: 78nm Silicon nitride deposited using PECVD.

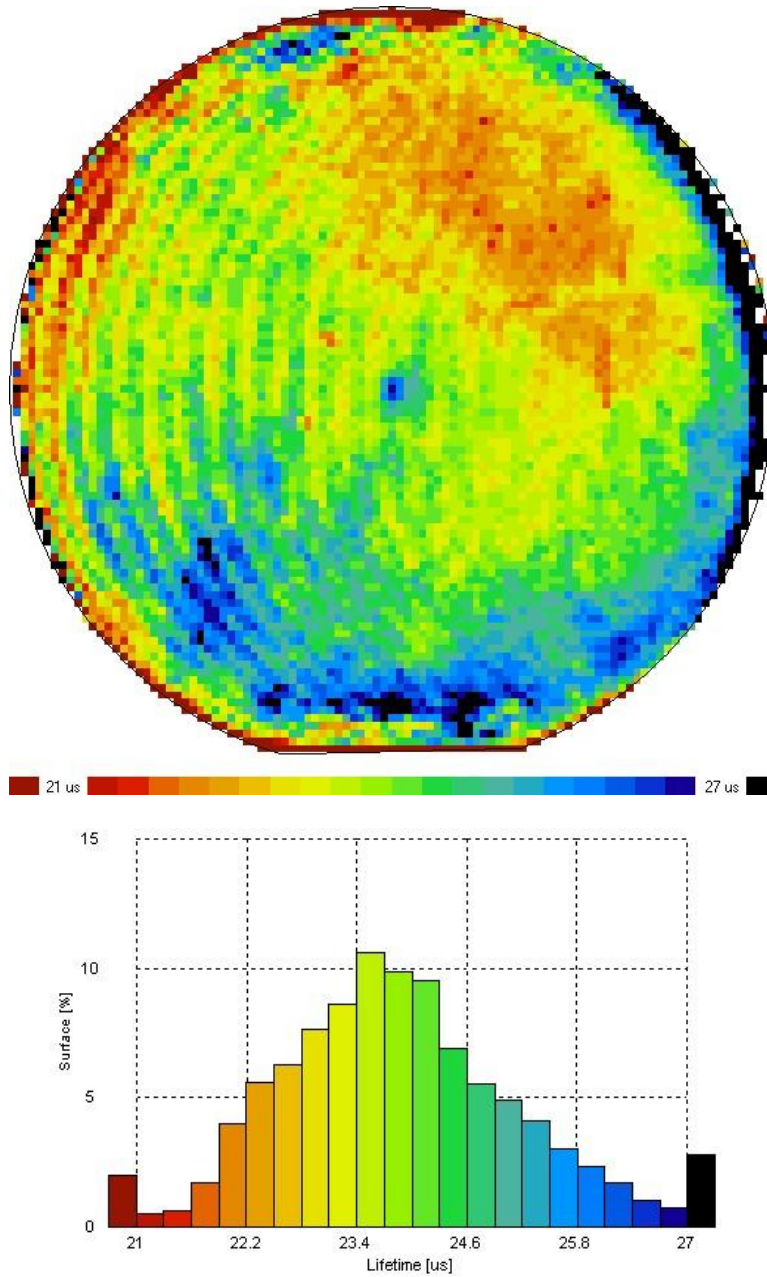


Figure 71 – top: minority carrier lifetime map of the wafer used for the fabrication of the cells with windowed emitter and without the top layer. Bottom: the distribution of the measured lifetime over the wafer.

After the completion of the cell fabrication, individual cells were diced into 1.01x1.01 cm dimensions using the dicing saw available in the CAPDS. At the end, there were 4 instances of each emitter pattern mentioned in the previous chapter and shown in Table 16 again for quicker reference.

emitter architecture number	Emitter width (μm)	Unit cell pitch (μm)	Emitter coverage
0	-	-	100%
1	3	13	40%
2	3	23	25%
3	5	10	75%
4	5	15	55%
5	5	55	17%
6	10	15	88%
7	10	30	55%
8	10	60	30%
9	25	45	80%

Table 16 - list of the 10 different emitter architectures included in the photo-mask design.

7.2.1 Cells with windowed emitter and without the top layer - External Quantum Efficiency

For each sample, External Quantum Efficiency (EQE) was measured under 1mA of current generated by a bias light source embedded in the measurement equipment. Figure 72 is a plot of the EQE for some of the cell architectures measured.

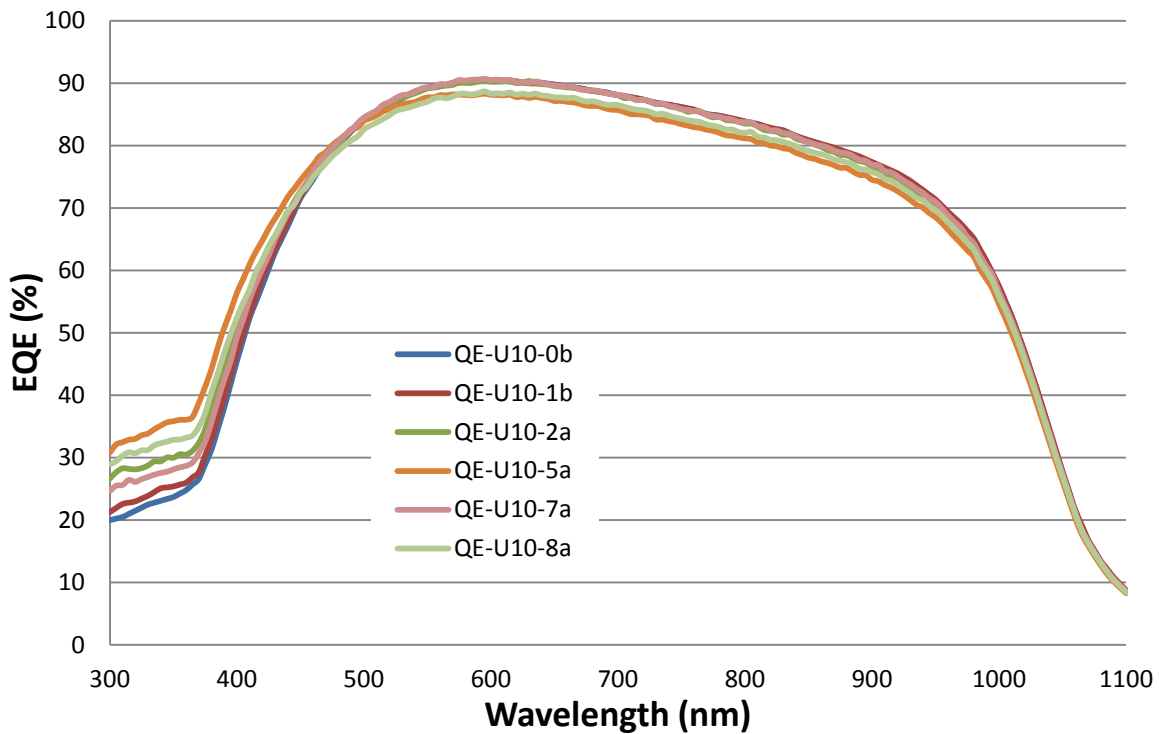


Figure 72 – measured External Quantum Efficiency for some of the cell architectures. There is clear impact of the cell architecture in the short and long wavelength spectral response of the cells.

It can obviously be seen from the EQE plots that the cell architecture has an impact on the spectral response of the solar cell. However it's more reliable to study the impact using the Internal Quantum Efficiency for calculation of which reflection spectra needs to be measured as well.

7.2.2 Cells with windowed emitter and without the top layer – Reflection Spectra

To measure the reflection spectra from the surface of a cell with a certain emitter pattern, the four instances of the cells with the same emitter architecture were placed tightly together on a vacuum holder to form a larger surface for the measurement. The reason for the necessity to use such an arrangement was that the light spot size of the UV-VIS spectrometer and accordingly the optical opening at the end of the integrating sphere were larger than the size of an individual cell. To address this issue, a holder, shown in Figure 73, was made to make the measurements on each emitter architecture possible. It was made from PTFE in order to have high reflectivity (similar to inside of the integrating sphere) for the secondary reflections.

It is worth mentioning that the measurement of reflection on a whole wafer (before dicing the wafer into individual cells) would've given doubtful results because of an interesting phenomenon observed

about the Anti-Reflection-Coating layer thickness. It was noticed that there was slight color variation in the Silicon nitride layer over the wafer; Dektak measurements showed that depending on the pattern of the emitter in a location on the wafer, the thickness of the deposited Silicon Nitride varied slightly. The reason for this variation could be the formation of some kind of an electric field at the surface of the sample where the masked diffusion of the emitter had formed lateral PN junctions which in turn become biased under the illumination from the plasma glow. Further study of this phenomenon might lead to interesting results for selective deposition of silicon nitride using PECVD.

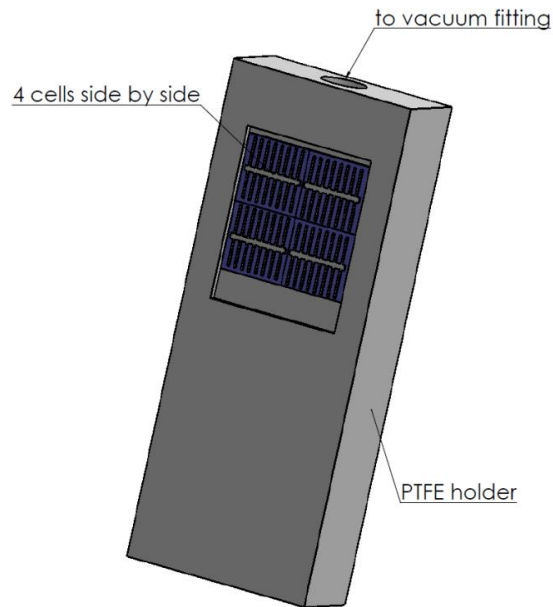


Figure 73 – a holder was made from PTFE to keep the four instances of each emitter architecture tightly together using vacuum to make a large enough reflective surface for reflection measurements.

This meant that the different cell design will have different anti-reflection-coating thickness which will affect the reflectance. And since the cells were randomly spread on the wafer (because of the mask design mentioned in previous chapter), the adjacent cells on the wafer had different emitter patterns and hence a different ARC thickness. This made it impossible to reliably measure the reflectance of each cell architecture while on the wafer (before dicing). Although the thickness difference and the resultant difference in reflection spectra among the cells were not too much but since we wanted to compare the performance of the cells as precise as possible, reflectance of each emitter architecture was measured using the PTFE holder explained.

The results of reflection spectra measurements for some of the cells are plotted in Figure 74 showing some small difference among the different architectures.

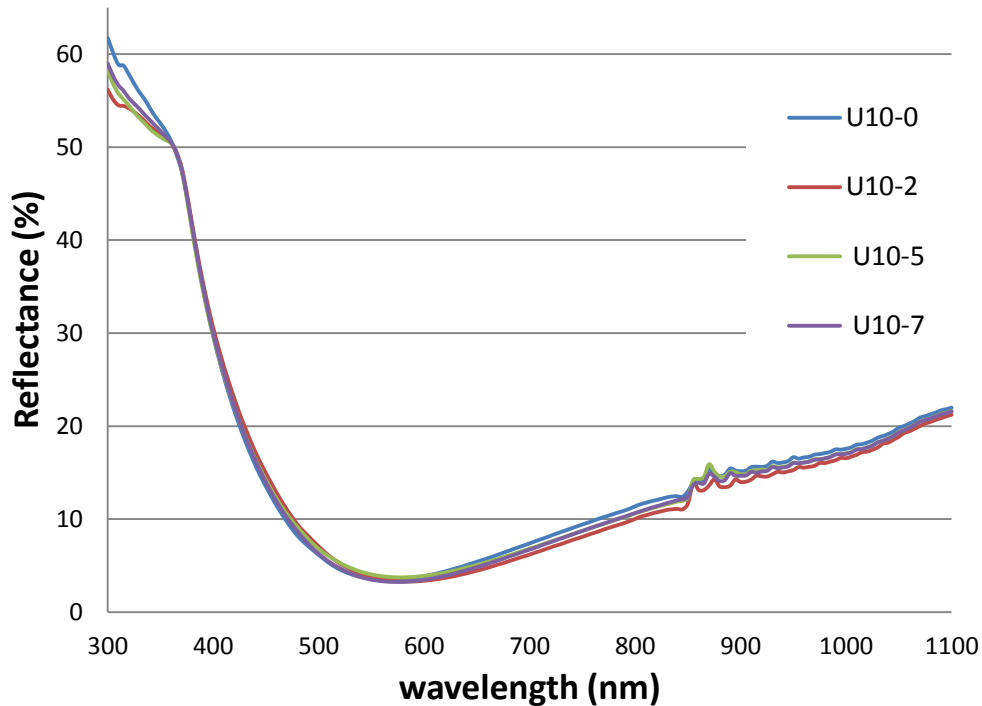


Figure 74 – reflection spectra of some cell architectures measured separatel. There is a slight difference among the cell with different emitter rchitecture because of the difference in the ARC layer on each.

7.2.3 Cells with windowed emitter and without the top layer – Internal Quantum Efficiency

Internal Quantum Efficiency (IQE) of the fabricated solar cells were then calculated using the relation

$$IQE = \frac{EQE}{1 - Reflectance}$$

IQE of the cells with different emitter architecture will give us more useful information about what is happening inside the cell. In what comes next, we will compare the IQE plots of different emitter architectures from which some interesting conclusion can be made.

Figure 75 shows the IQE curves for the standard cell (architecture number 0) and cell architecture number 5 (refer to Table 16 for the description of the architecture numbers) which has an emitter pattern with 55µm pitch and emitter strips of 5µm width (17% emitter coverage). As expected, because of the low coverage percentage of the emitter, the short wavelength spectral response is enhance significantly compared to the standard cell in which the emitter covers everywhere (100% coverage). Longer wavelength response, on the other hand, has deteriorated in comparison. The reason for the lower quantum efficiency at longer wavelengths is that by lowering the area of the emitter because of

the introduction of the windows, for a carrier generated somewhere in the bulk of the substrate, equivalent distance to a collection point (junction) has increased. The legends for the curves have the name of the wafer (U10 in this case) and then the architecture number. The letters “a” or “b” at the end denotes which of the four instances of that architecture was used.

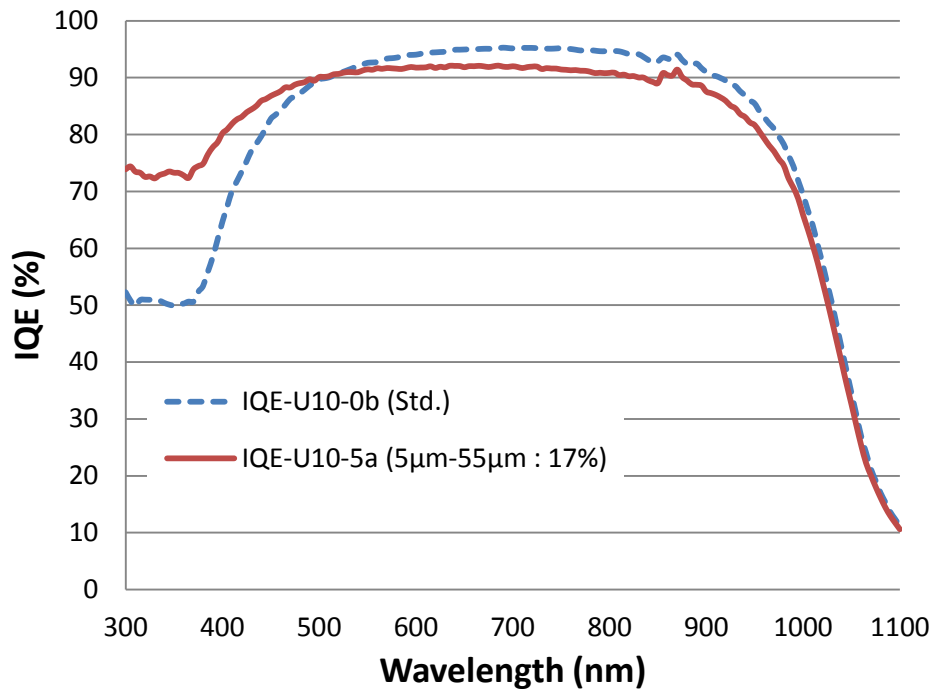


Figure 75 – IQE for the standard cell with 100% emitter (dotted line) and architecture number 5 with 17% emitter coverage. U10 is the wafer label and the letters “a” or “b” in the name of the curves referred to the specific cell among the 4 instances of each architecture and can be ignored.

Basically these comparative plots all reveal that there is some kind of gain in quantum efficiency at lower wavelengths and some loss at higher wavelengths. The amount of the gain and loss depends not only on the emitter coverage percentage but strongly on the design of the emitter pattern as well. Figure 76 shows another curve comparing the quantum efficiency of the standard cell to a cell of architecture number 6 with an emitter pattern of 15µm pitch and emitter strips of 10µm width (88% emitter coverage). Unlike cell number 5 which had a significant gain in the short wavelength region, this cell has just a small amount of increase in the quantum efficiency in the UV range but on the other hand has a similar performance to a standard cell in the high wavelength part (not deteriorated like the case of architecture number 5)

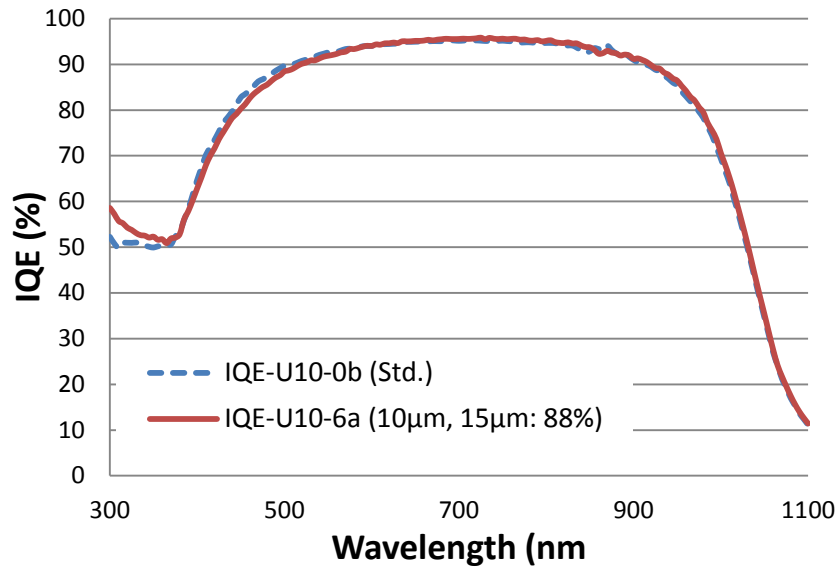


Figure 76 – comparison of the IQE of the standard cell and the cell with architecture number 6 (88% coverage)

To show that other than the emitter coverage percentage, the pitch of the unit cell also plays a role, IQE curves of the cells architectures 4 and 7 are compared to each other and to the standard cell in Figure 77. Both cells have an emitter coverage percentage of around 55% while cell architecture number 4 has a smaller pitch (15µm) while architecture number 7 has the higher pitch of 30µm. the comparison shows that a higher pitch for the emitter pattern causes an enhanced short wavelength and a worse high wavelength response.

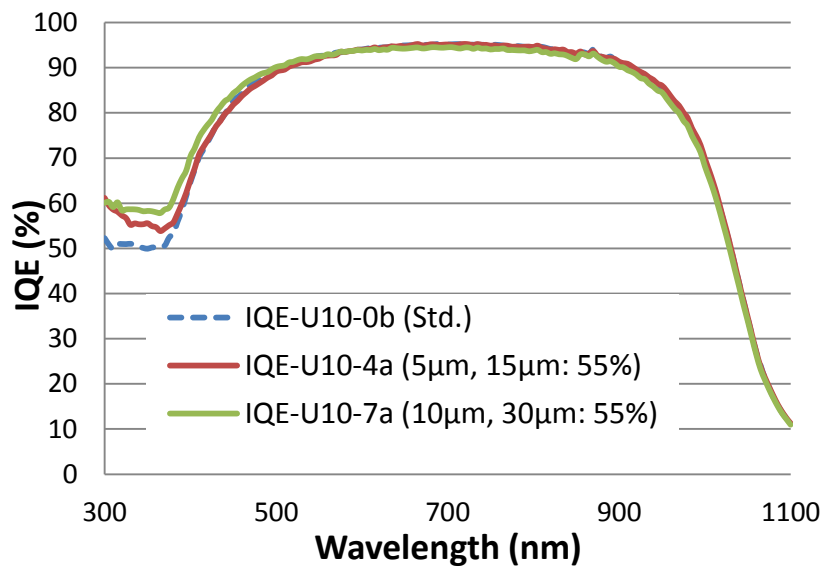


Figure 77 - comparison of the IQE of the standard cell to the cell with architecture number 4 (55% coverage, pitch: 15µm) and architecture number 7 (55% coverage, pitch: 30µm)

This conclusion is further backed up by another comparison shown in Figure 78 where the IQE of the cells architecture number 1, 2, 8 and the standard cell are compared. These three cells have similar emitter coverage percentages with cell architecture number 1 with 40% coverage and 13 μm emitter pattern pitch, cell number 2 with 25% coverage and 23 μm pitch and cell number 8 with 30% emitter coverage and 60 μm pitch. The result of comparison is similar to the previous case; that is for similar emitter coverage percentage, a higher pitch for the emitter pattern causes an enhanced low wavelength response and a worse high wavelength response compare to a standard cell.

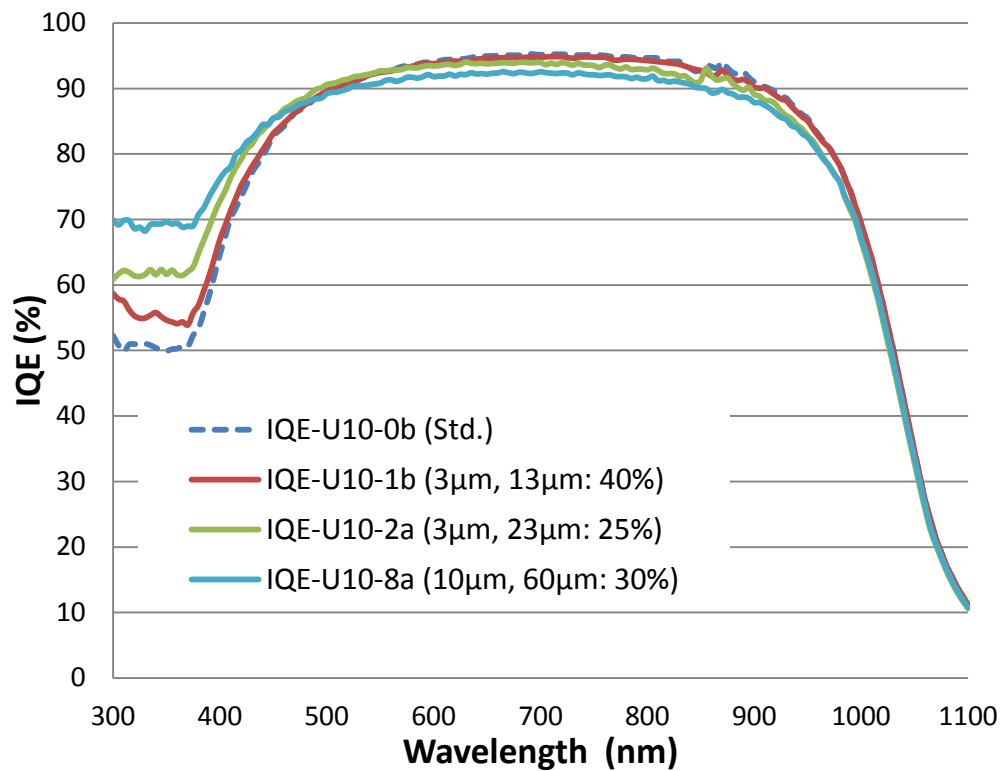


Figure 78 - comparison of the IQE of the standard cell to the cell with architecture number 1 (40% coverage , 13 μm emitter pattern pitch), architecture number 2 (25% coverage, 23 μm pitch) and architecture number 8 (30% emitter coverage and 60 μm pitch)

Another observation from the comparison of the curves of Figure 78 is that even though architecture 2 has a slightly smaller emitter coverage compared to architecture 8 (25% versus 30% respectively) which suggests that it should have a better UV response but measurement shows that architecture 8 has a better UV response. This observation proposes that emitter coverage percentage and the emitter pattern pitch can have independent but aligned effects on the spectral response of the solar cell.

The last two comparisons were for the cases of low to medium emitter coverage percentage. Next one is for the two cases with higher emitter coverage and yet the outcome is similar to the previous ones.

Figure 79 shows the IQE for cell number 3 with 75% emitter coverage and a pitch of 10 μ m and cell number 9 with 80% emitter coverage and a pitch of 45 μ m. although the difference in the performance is not as evident as the previous cases, it still reflects the same observation that for a certain emitter coverage percentage higher pitch for emitter pattern results in better UV and worse long wavelength response.

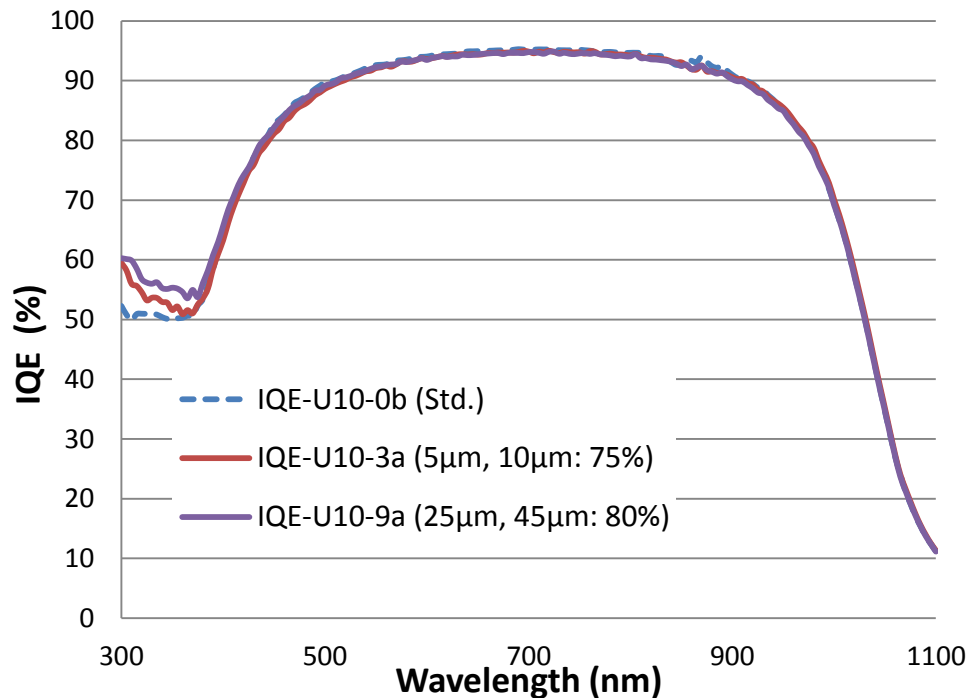


Figure 79 - comparison of the IQE of the standard cell to the cell with architecture number 3 (75% coverage, 10 μ m emitter pattern pitch) and architecture number 9 (80% coverage, 45 μ m pitch)

Whether the changes of the spectral response of a solar cell because of a specific emitter pattern are beneficial or detrimental to solar cell performance depends on the spectrum of the input light. If a cell is being lit by a spectrum which is richer in short wavelength photons (e.g. spectrum with lower air mass), replacing the conventional emitter with a windowed emitter might actually improve the cell efficiency by itself.

Even though the 10 different emitter architectures tested might not be able to give a complete picture of the resultant effects in a cell, but consistent observations in all the fabricated and tested cases lead to certain clear and interesting conclusions as follows:

- (i) Lower emitter coverage results in better short wavelength and worse long wavelength spectral response
- (ii) For a similar value of emitter coverage percentage, a higher value for the pitch of the emitter pattern leads to enhanced short wavelength and weakened long wavelength spectral response
- (iii) Depending on the spectrum of the input light, it should be possible to design an emitter pattern which increases the short circuit current of the solar cell compared to a standard cell. Of course this will be possible only for an input light spectrum with higher short wavelength light intensity.
- (iv) In case of the fabrication of the full Buried-Windowed-Emitter cell; higher emitter coverage (without the loss in the long wavelength spectral response) should be the preferable case.

These results have several important consequences:

- 1- They give insight about the carrier collection performance of the fabricated cells for the different emitter patterns
- 2- The predictable impact on the spectral response as a function of the emitter pattern verifies that the processes used for cell fabrication were expectedly under control.
- 3- The results set the path for the optimum design patterns for future cell fabrications.

7.2.4 Cells with windowed emitter and without the top layer – Dark and Illuminated IV

Even though, as the first step, the main focus was on the measurements of the spectral response of the cells, dark and illuminated IVs of some of the cells were also measured for verification of the electrical performance. Figure 80 shows the dark IV curves for the standard cell and cell architecture number 1 after being diced into individual cells of 1.02 cm^2 area. The measured dark IVs demonstrate similarity among all the cells. There is a rather large second diode visible in the IV curve which could be because of the possible defects from the recycled wafers. because all the cells (including the standard cell) have similarly large value for this second diode, it can be concluded that it is most likely due to the combination of high temperature dopant diffusion and possible defects existing in the subsurface of recycled wafers.

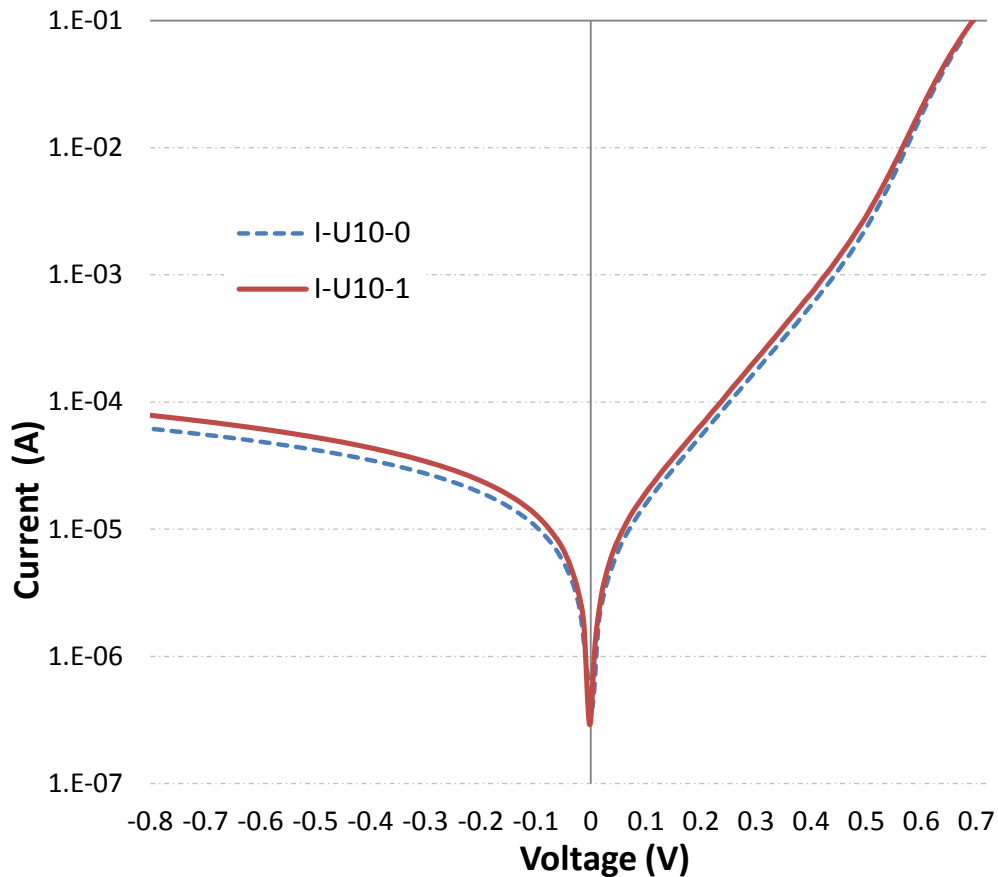


Figure 80 – dark IV curves for a standard cell and the cell with architecture number 1.

Illuminated IV of some of the cells was also measured under AM1.5 light illumination Figure 81 and Figure 82 show the illuminated IV curves for the standard cell and cell architecture number 7 respectively. Summary of the important photovoltaic parameters of the cells is shown beside each curve. Both cases have rather low fill factor which is most likely because of the high shunt resistance introduced mostly because of the defects in photolithography of the emitter mask layer. Large second diode observed in the dark IV curves can also help to lower the fill factor. Both of these reasons can be eliminated with proper control over the fabrication process such as using higher quality substrates and cleaner environment for photolithography.

It should be noted that these illuminated IV curves are not to be used to judge the maximum performance of the fabricated cells as the main focus was to study the spectral response of the cells. For example, there is no light trapping scheme incorporated in these cells and as a result the photo-current of the cells (including the standard cell) are obviously lower than the state of the art.

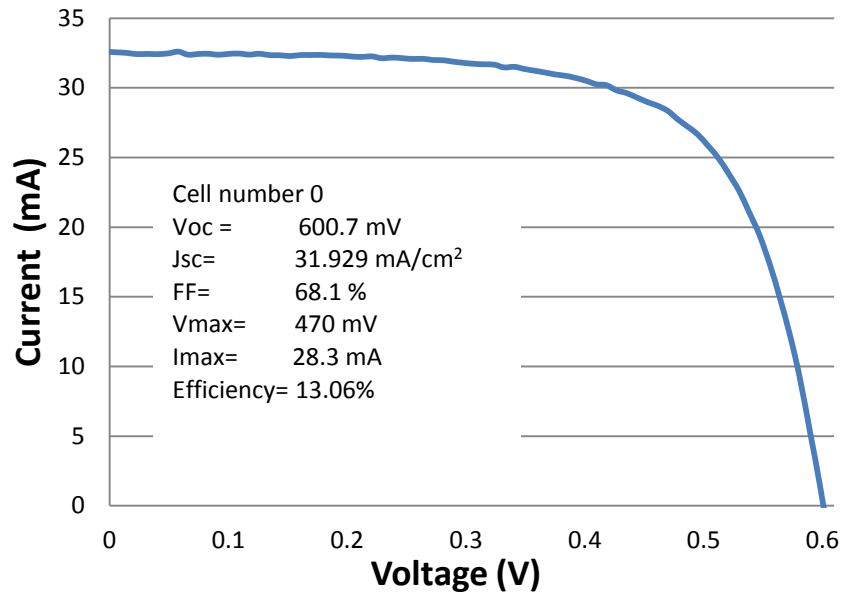


Figure 81 – illuminated IV curve for the standard cell fabricated on the same wafer as the other cell architectures.

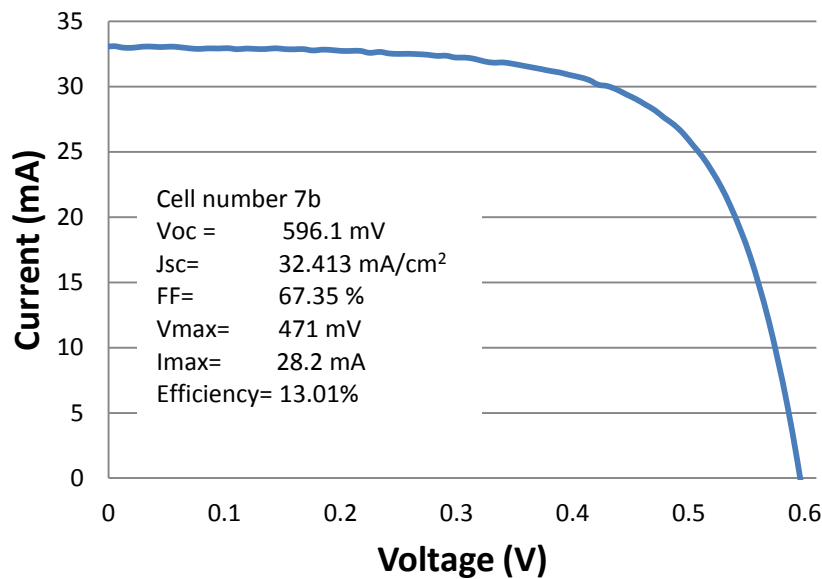


Figure 82 – illuminated IV curve for the cell architecture number 7. Slight increase in the short circuit current can be seen compared to the standard cell.

The important observation here is that both standard cell and cells with partial emitter coverage have similar energy conversion performance which means by adding a top layer to this device the performance of the overall cell will definitely increase, however this will only be the case if the top layer has the required high quality for this purpose.

7.3 Characterization and discussions of the Control experiment cells: standard cell with epitaxial film as emitter

Using electrical measurements and Transmission Electron Microscopy, we have already determined the full crystalline nature of the epitaxial films deposited using the developed low temperature epitaxial technology; however, whether these films are up to the standards of solar cells especially to serve as the top layer in the BWE solar cell structure, needs a direct evaluation method. To study the optical performance of these epitaxial films, they were used as the emitter layer of solar cells with standard structure in a control experiment. This method gives a very direct approach in the assessment of the efficacy of these epitaxial films for solar cell applications. The schematic of the control cell structures is shown in Figure 83.

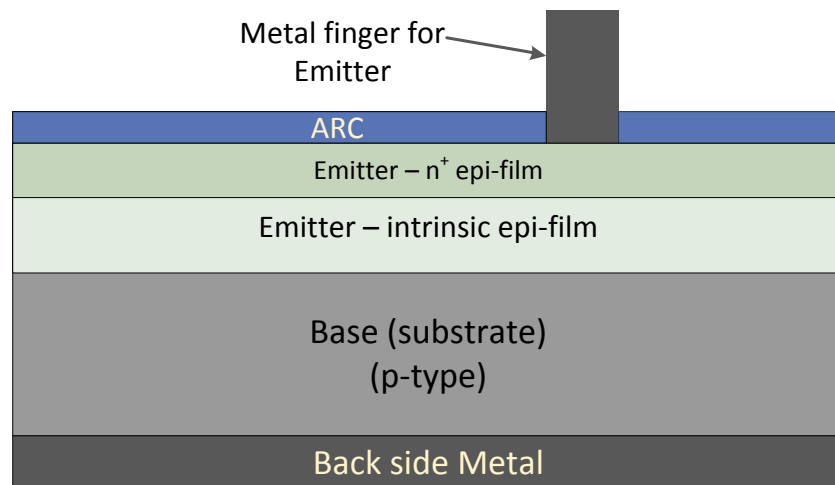


Figure 83 – schematic of the control solar cell structure fabricated to study the optical performance of the develop epitaxial films.

These cells were made on a p-type silicon substrate with the following specifications:

Substrate: 4 inch diameter, <100> p-type silicon wafer, 0.5-1 Ωcm bulk resistivity, 550 μm thick, 17 Ω/sq sheet resistance. Average minority carrier lifetime in the bulk around 12.5 μs . Lifetime map of the wafer before fabrication is shown in Figure 84

Back Surface Field (BEF): 40 Ω/sq , formed by Boron diffusion at 950 $^{\circ}\text{C}$ for 60 minutes.

Emitter formation: 100nm n^+ epitaxial film on top of 370nm of intrinsic epitaxial film deposited using PECVD with the recipes shown in . The resultant film had a sheet resistivity of 52 Ω/sq .

Anti-reflection-Coating: 78nm Silicon nitride deposited using PECVD.

Type of film	Pressure	Top electrode power	SiH4 flow (sccm)	H2 flow (sccm)	PH3 flow (sccm)	Temp.	Duration	Film thickness
Intrinsic	800mT	22W	5	100	0	300°C	41mins	370nm
n ⁺	200mT	15W	10	250	8	300°C	47mins	100nm

Table 17 – PECVD deposition conditions for the epitaxial layer to serve as the emitter in the fabricated control cells.

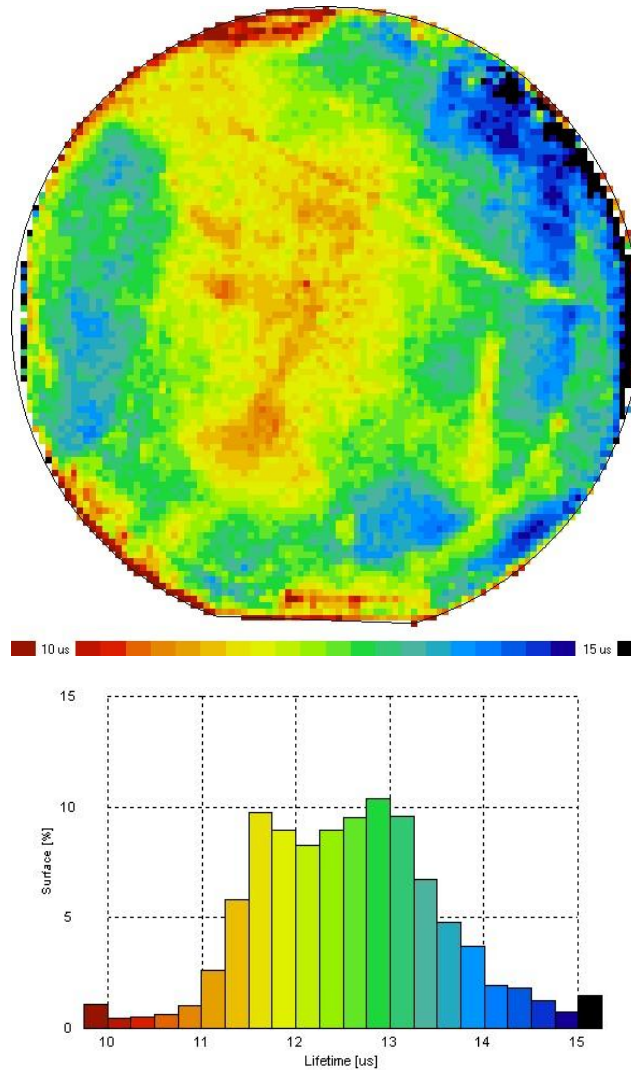


Figure 84 – top: bulk minority carrier lifetime map of the wafer on which the control cells were fabricated. Bottom: the distribution of the lifetime value over the wafer.

Measurements of the spectral response for these cells showed that even though these layers are fully epitaxial, they lack the high quality required for the top layer in the BWE solar cell. Figure 85 shows the

measured External Quantum Efficiency, Reflection spectrum for a case without anti reflection coating and the calculated Internal quantum efficiency.

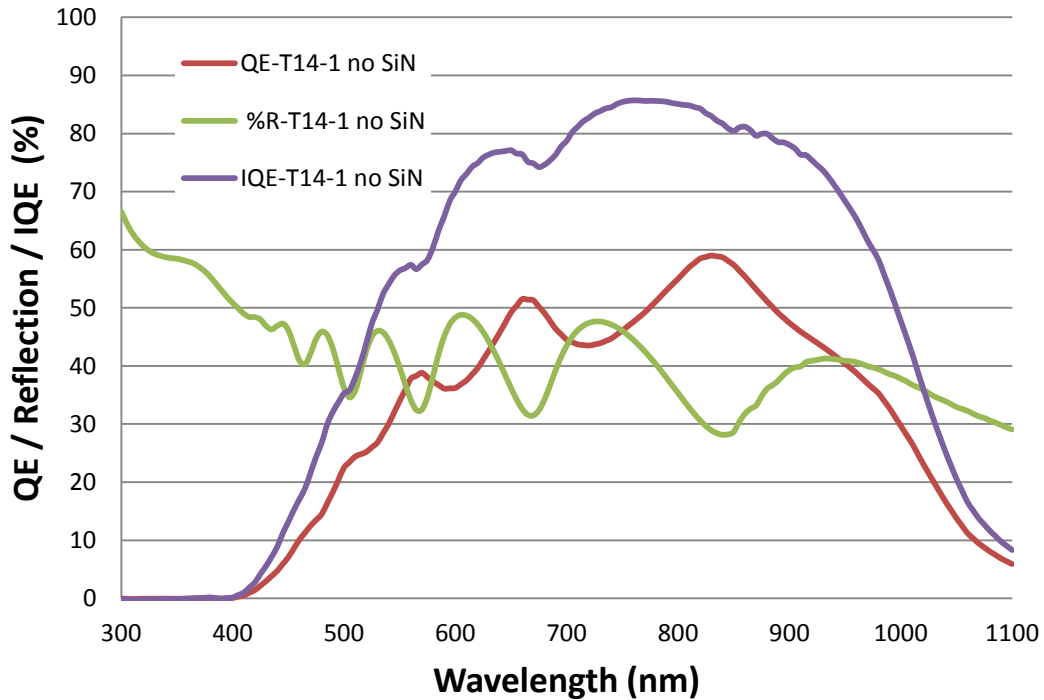


Figure 85 – EQE, Reflection Spectra and the IQE of the control cells fabricated using a low temperature epitaxial film as the emitter. This measurement is for a sample without anti-reflection coating and as a result there is a strong reflection from the surface.

There are some humps visible in the IQE curve extracted from the measured QE and reflection curves which seems to be due to slight variation of the reflection over the wafer.

The IQE shown in this figure reveals a poor short wavelength response. This means that the emitter layer used (the epitaxial film) has a very low minority carrier diffusion length. The oscillation of the reflectance curve also proves that the refractive index for the epitaxial emitter is different than the bulk silicon which is another indication that the epitaxial film is not a perfect silicon crystal. Although these results doesn't seem promising, we went on further and fabricated a complete BWE solar cell using the developed epitaxial films as the top layer.

7.4 Characterization and discussions of the complete BWE solar cells

Of course, having observed the poor optical performance of the epitaxial films in the fabricated control cells, we were not expecting that the fabricated BWE cells will have high performance if the same epitaxial films were used as the top layer but to demonstrate that the proposed novel BWE structure can be fabricated using the developed technology, a series of complete BWE solar cells were fabricated.

The complete BWE cells were made on similar substrates to the cells with windowed emitter and without the top layer. The schematic of the fabricated complete BWE solar cells is shown in Figure 86. A summary of the important information about the structure and some parameters of the fabricated BWE cells are as bellow:

Substrate: 4 inch diameter, <100> n-type silicon wafer, 1-2 Ω cm bulk resistivity, 350 μ m thick, 51 Ω /sq sheet resistance. Average minority carrier lifetime in the bulk around 27 μ s (similar to the case of the cells without the top layer)

Back Surface Field (BEF): 18 Ω /sq, formed by phosphorous diffusion at 900 $^{\circ}$ C for 45 minutes.

Emitter formation: 40 Ω /sq etched back to have 52 Ω /sq. formed by masked diffusion of Boron at 950 $^{\circ}$ C for 60 minutes.

Top layer: 30nm n+ epitaxial film on top of 370nm of intrinsic epitaxial film deposited using PECVD with the recipes shown in Table 18. The resultant film had a sheet resistivity of 122 Ω /sq.

Type of film	Pressure	Top electrode power	SiH4 flow (sccm)	H2 flow (sccm)	PH3 flow (sccm)	Temp.	Duration	Film thickness
Intrinsic	800mT	22W	5	100	0	300 $^{\circ}$ C	41mins	370nm
n ⁺	200mT	15W	10	250	8	300 $^{\circ}$ C	14mins	30nm

Table 18 – the PECVD conditions for the deposition of the epitaxial top layer for the fabricated BWE solar cells

Anti-reflection-Coating: 78nm Silicon nitride deposited using PECVD.

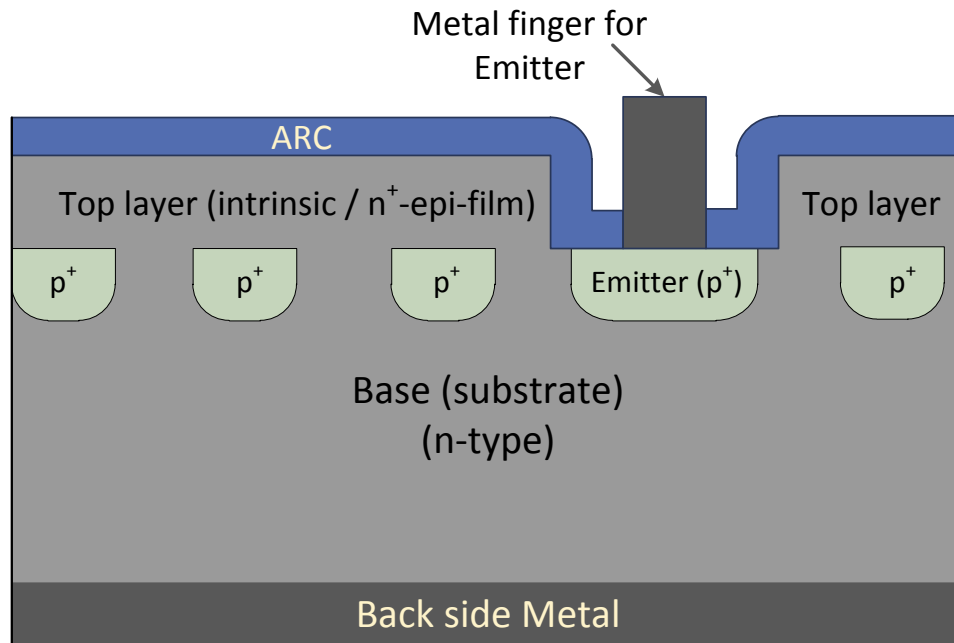


Figure 86 – schematic of the fabricated complete BWE solar cells. The top layer is a stack of a thin n^+ epitaxial film on top of a thicker intrinsic epitaxial layer.

7.4.1 Characterization and discussions of the complete BWE solar cells - Quantum Efficiency

Similar to the previous case of cell analysis, the main focus was on the spectral response as it would give important information about the internal structure of the BWE cell. As was expected from the experience of the control cell, all the cells with a top layer on them had gone through similar degradation in the spectral response while the standard cell which was fabricated on the same wafer, had a normal spectral response. Figure 87 shows the plots of the External Quantum Efficiency of some of the cells together with the standard cell. Two important conclusions can be made from comparing the spectral response curves shown in this figure.

- 1- All the cells which had top layer on them have lost significant amount of spectral response in all the wavelengths.
- 2- Even though the thickness of the top layer and the Anti-Reflection-Coating is the same on all the cells, the value and shape of External Quantum Efficiency curves among them varies by a great value.

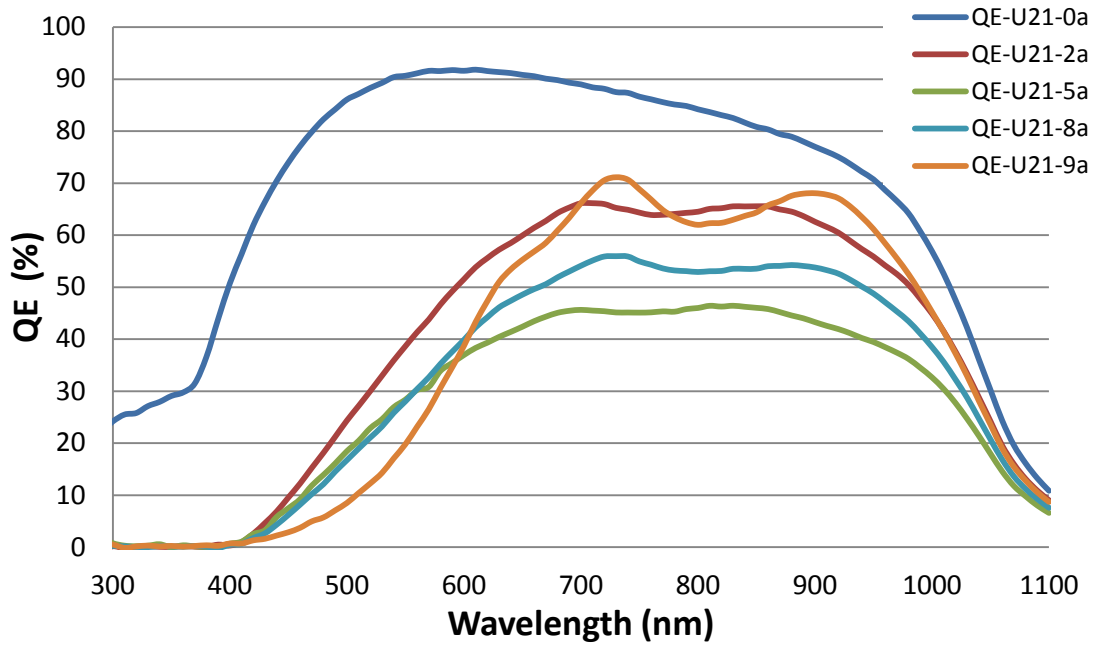


Figure 87 – external quantum efficiency of several BWE cells and the standard cell. The drop in the spectral response for the BWE cells is due to the low quality of the used top layer.

Part of the variation among spectral responses of the different BWE cells is due to the different reflection spectra. Figure 88 shows several reflection spectra curves measured on different spots on the wafer before dicing it into individual cells.

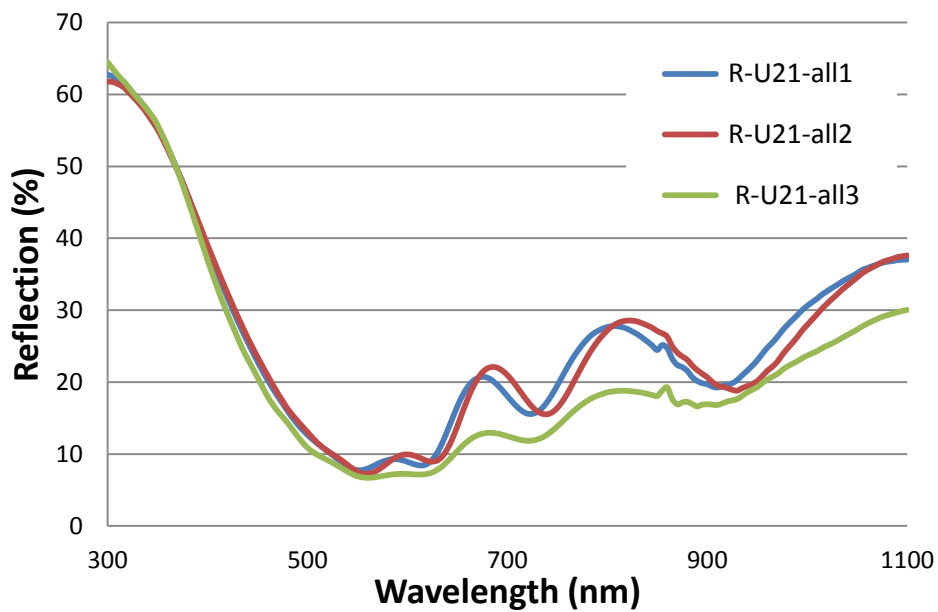


Figure 88 – reflection spectra for the fabricated BWE solar cells measured on several spots on the wafer. The variation is due to the difference in the morphology of the top layer over the wafer

The reason for such variation can be explained using the rather surprising observation of the various bubbling forms developed in the top layer shown in Figure 89. As the last step after metal deposition there was a metal contact sintering step (350°C in forming gas) after which it was noticed that there are many bubbles formed in the top layer which had a very smooth and uniform appearance before the sintering step. Even though the sintering temperature was only 50°C higher than the deposition temperature of the top layer but top layer (which was covered by the silicon nitride layer) still developed many pin holes and bubbles.

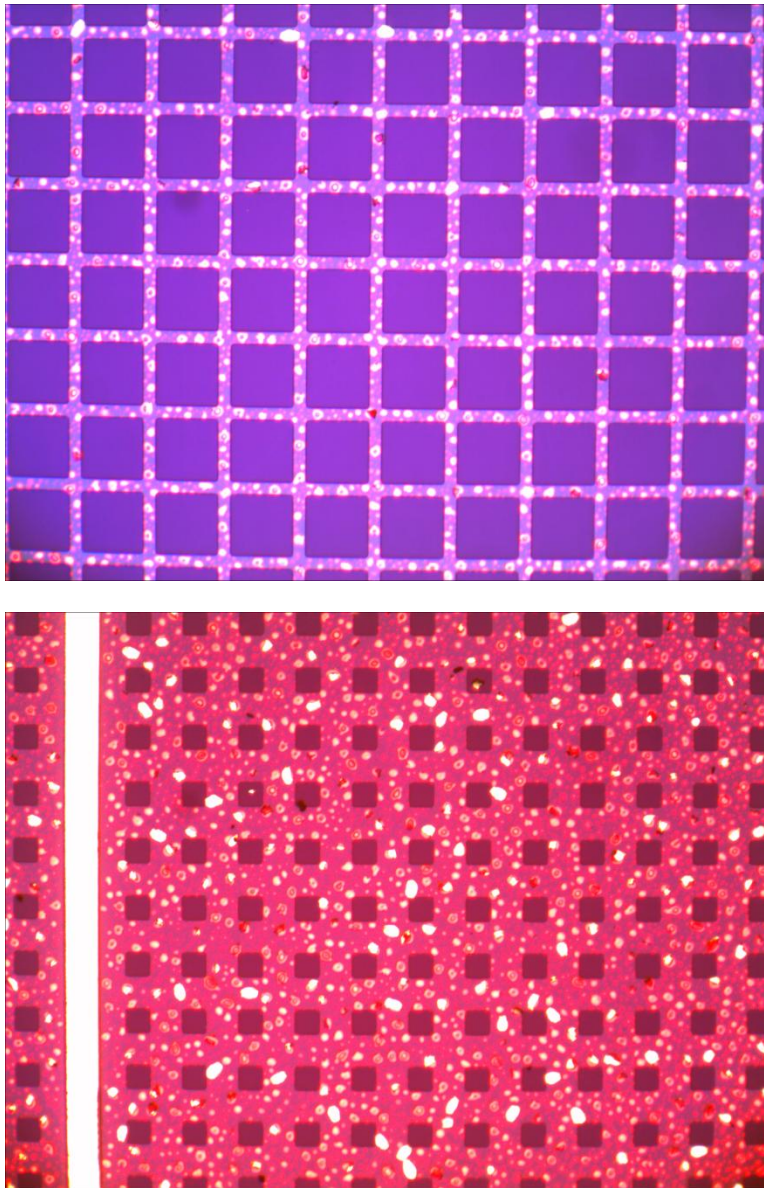


Figure 89 – optical microscope images of two different cell architectures on the fabricated BWE cells. Top image shows less pin-hole generation in comparison due to the lower emitter coverage. Bottom image on the other hand is for an architecture

with higher emitter coverage and hence with more pin-holes density. Pin-holes are unwantedly generated during the contact sintering step.

Another surprising observation is that the bubbling has happened almost exclusively on the areas where the top layer is deposited on the emitter strips. Figure 89 shows two different emitter designs with different emitter strip widths. It clearly shows that the amount of bubbling per unit area is higher for the case with thicker emitter strip (higher emitter coverage). This might explain the different optical behavior including the reflection among cells as each will have a different portion of the top layer bubbled up.

Electrical measurements also reveal a large shunting due to the leaky interface between the top layer and the emitter. Figure 90 compares the dark IV of the standard cell (architecture number 0) and a BWE cell (architecture number 2). The origin of this low shunt resistance seen in this curve is indeed the leaky interface between the top layer and the emitter. This is verified by independent measurements of the IV of the junction between the emitter and top the layer using the test device structures placed on various places on the wafer during mask design. Figure 91 shows this IV curve and reveals a large shunt current in this junction which should be the reason for the large shunt current seen in the dark IVs of these BWE cells.

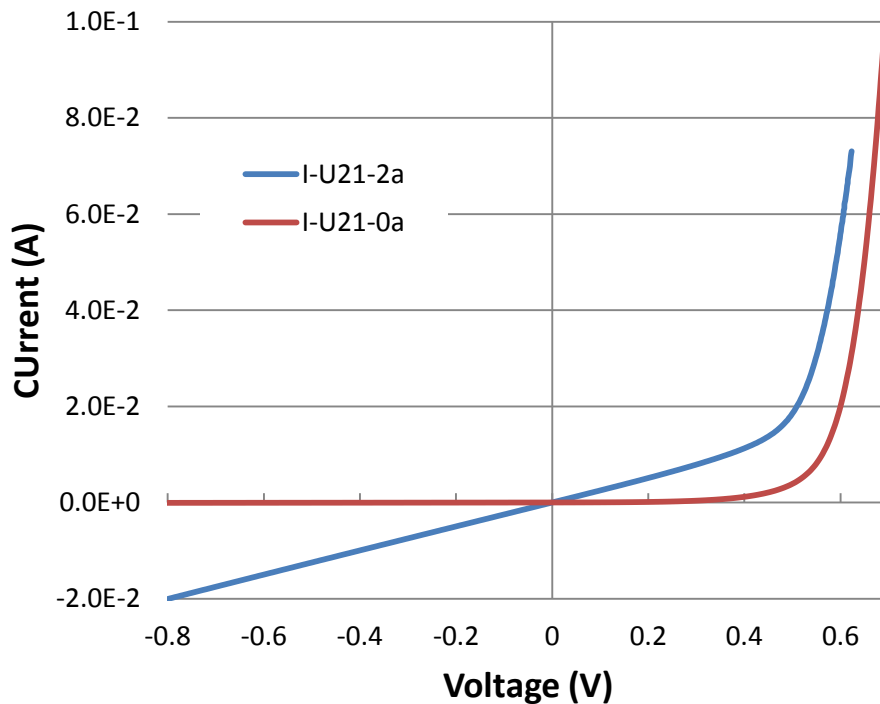


Figure 90 – comparison of the dark IVs for the standard cell and a BWE cell with architecture number 2. Severe shunting is observed in the BWE cell's IV due to the leaky interface of the top layer and the emitter.

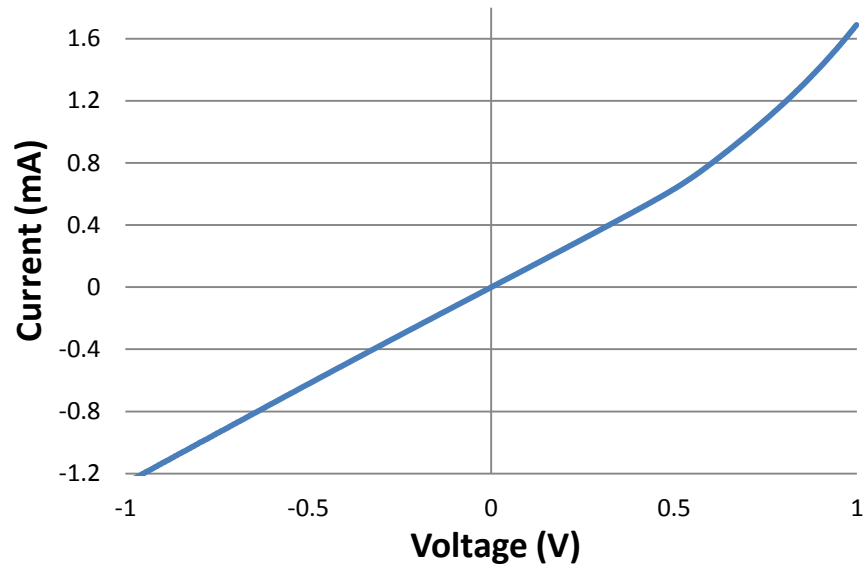


Figure 91 – dark IV curve measured between the top layer and the emitter using the test device structures incorporated in the mask. Large shunt current is observed which reveal a leaky interface between these two layers

Comparing the IQEs of control cell and that of the fabricated BWE cells reveals the similarity of the loss of performance in the short wavelength range of the light spectrum. This observation proves that the reason for such loss is the low minority carrier lifetime in the deposited epitaxial film. Two conclusions can be made from this result:

- 1- Quality of the top layer plays a very important role in the performance of the BWE cell structure. While a good quality film can increase the performance, a lower quality film can actually deteriorate it despite the extra steps involved in the fabrication of the cell.
- 2- The quality of the deposited epitaxial film is lower than expected. Even though full crystallinity of this layer is proven by various experiments, there are a lot of defects in the crystal structure which act as recombination centers and lower the minority carrier lifetime by a great extent.

This instance of the fabricated BWE cells doesn't show an improved performance due to the low quality of the top epitaxial layer deposited at low temperature. However, measurement results collectively prove the efficacy of the proposed structure in achieving what is claimed and expected. Because of the time limitations in the accomplishment of this PhD thesis because of the diversity of its nature, it was not possible to try alternative methods of fabrication of the novel BWE solar cell, however with the experience and knowledge gained through the process of the fabrication presented in this thesis, realizing a complete BWE solar cell with improved performance seems well within reach. The first issue to be addressed for this goal to come true is the deposition of a higher quality epitaxial layer. Perhaps, the medium temperature regime of epitaxial silicon deposition will be able to provide the required film quality for the novel Buried-Windowed-Emitter solar cell. Alternative fabrication methods can also be used for the realization of the solar cell structure proposed which could be proposed as the future work.

Chapter 8 – Conclusions

Introduction of a novel solar cell structure - To address the commonly poor short wavelength response of the conventional solar cell structure which consists of a highly doped thin emitter layer on top of a thicker and less doped base, the novel concept of the Buried-Windowed-Emitter is introduced. This new solar cell structure makes use of a high quality semiconductor layer on top of the traditionally made highly doped emitter and greatly enhances the spectral response of the solar cell by giving the superficially generated carriers a higher chance of collection at the junction. In the proposed BWE structure the emitter is windowed in order to electrically connect the top layer to the base for current collection.

Proof of concept – the efficacy of the proposed novel device is proven by computer aided device simulations using the available device simulation tools such as MEDICI. The results of simulation show that the proposed novel Buried-Windowed-Emitter solar cell will not only improve the short wavelength spectral response of the overall cell as expected, but also will boost the spectral efficiency for all the wavelengths. Another exciting conclusion from the results of the computer simulation of the BWE solar cell is that the minority carrier lifetime in the top layer does not need to be very high for a superb performance and values as low as $1\mu\text{s}$ can still boost the short circuit current of the cell to values close to the theoretical limit of the photo-current collectable by a silicon solar cell. This is indeed a good news for manufacturability of this device as it should be practically feasible to achieve epitaxial films with minority carrier lifetime in this range.

Development of an analytical model for the new solar cell – in order to increase the understanding about the rather complex structure of the proposed Buried-Windowed-Emitter solar cell, an analytical circuit level model, similar to the case of the standard solar cell, is developed for the proposed device. The developed analytical model helps to understand the importance of the main design parameters such as the dimensions of the pattern of the windowed emitter. It also sets the path for further development of similar analytical models for various emitter shapes usable as the pattern for the windowed emitter.

Development of low temperature epitaxial silicon technology - on the path to fabricate the proposed BWE solar cell, great deal of work is done on the development of a low temperature ($<300^\circ\text{C}$) epitaxial silicon technology using the benefits of Plasma Enhanced Chemical Vapor Deposition (PECVD). Highly doped epitaxial silicon layers of up to around $1\mu\text{m}$ thickness are achieved with sheet resistivity as low as $7\Omega/\text{sq}$ which is much lower than what is reported in the literature in similar deposition conditions. Intrinsic, phosphorous doped n-type and boron doped p-type epitaxial films have been developed on

(100) silicon substrates. Because of the importance of the epitaxy on (111) silicon surfaces for solar cell applications which has never been reported for such low temperatures, experiments have been performed to increase our understanding of the major mechanisms governing the low temperature epitaxy to expand the possibility of epitaxy on various substrate orientations.

Measurement of reflection spectra of the deposited epitaxial films is proposed as a fast, non-destructive and process-integrate-able method to assess the crystalline quality of the epitaxial films. Effects of higher temperature post deposition annealing have been studied on the develop epitaxial films

Development of a technology to fabricate the proposed novel BWE solar cell - Masked dopant diffusion and the developed low temperature epitaxial silicon technology are used to build a technology for the fabrication of the proposed Buried-Windowed-Emitter solar cell. Photo-masks are designed to create 10 different architectures for the design of the windowed emitter in the BWE cell. All the steps taken in the successful fabrication of the novel BWE cells are presented in detail and the relevant findings are discussed and proposed as future research topics.

Characterization of the fabricated novel solar cells - Using the developed technology, three kinds of cells are fabricated to separately study:

- (i) The effects of partial coverage of the windowed emitter
- (ii) The optical performance of the developed epitaxial silicon films
- (iii) The performance and manufacturability of the novel BWE solar cell

The results show that the concept of windowed-emitter by itself (even without the top layer) is capable of enhancing the performance of the solar cell when compared to a standard design. It also promises high conversion efficiency for the BWE solar cell in case a high quality top layer can be deposited on top of the windowed emitter. The results further reveal the lower than expected quality of the low temperature epitaxial films despite the proof of their full crystallinity using other methods. Use of the epitaxial films as the emitter of the solar cell is proposed as a direct and effective method of studying the photovoltaic performance of the low temperature epitaxial films. The fabricated complete BWE solar cells, even though lacking the promised performance due to the low quality of the used top layer, show that proposed novel device can be fabricated using the available technology despite the inherent complexity of its structure. Further development of the epitaxial technology will lead to feasibility of a BWE solar cell with very high photovoltaic performance.

References

- [1] The Physics of Solar Cells, Jenny Nelson, Imperial College Press, Reprinted 2007
- [2] Solar Cells, operating principals, technology and system applications. Martin A. Green. Prentice-Hall Series in solid state. 1982.
- [3] A. S. Bouazzi, M. Abaab, B. Rezig, “ A new model of very high efficiency buried emitter silicon solar cell” , Solae Energy Material and Solar Cells 46, 1997, p.29-41
- [4] M. Emziane, R. J. Nicholas, “Double-junction three-terminal photovoltaic devices: A modeling approach” JOURNAL OF APPLIED PHYSICS 102, 074508 , 2007
- [5] Handbook of optical constants of solids III, Volume 4, edited by Edward D.. Palik, 1998
- [6] Plasma Techniques for Film Deposition, Mitsuharu Konuma, Alpha Science, 2005
- [7] Third Generation Photovoltaics, Martin A. Green, Springer, 2006
- [8] M. Farrokh-Baroughi, R. S. Tarighat, S. Sivoththaman, “MEASUREMENT OF EXCESS CARRIER LIFETIME IN EPITAXIAL SILICON THIN FILMS”, PVSEC 17, 2007, Tokyo, Japan
- [9] Siva Sivoththaman, “Photovoltaic Devices” lecture slides, university of waterloo, 2008
- [10] M. Wolf, “Historical Development of Solar Cells” Solar Cells, New York Press, 1976
- [11] W. J. Varhue, J. L. Rogers, and P. S. Andry, “Epitaxial film thickness in the low-temperature growth of Si(100) by plasma enhanced chemical vapor deposition”, Appl. Phys. Lett. 68 (3), 15 January 1996
- [12] M. Ben Rabha, M.F. Boujmil, N. Meddeb, M. Saadoun, B. Bessai, “Front buried metallic contacts and thin porous silicon combination for efficient polycrystalline silicon solar cells”, Thin Solid Films 511– 512 (2006) 108 – 111
- [13] G. Ekanayake, T. Quinn, H.S. Reehal, B. Rau, S. Gall, “Large-grained polycrystalline silicon films on glass by argon-assisted ECRCVD epitaxial thickening of seed layers”, Journal of Crystal Growth 299 (2007) 309–315
- [14] Cheng-Hsien Chen, Tri-Rung Yew, “Silicon epitaxial growth by plasma enhanced chemical vapor deposition from SiH₄/H₂ at 165-350°C” Journal of Crystal Growth 147 (1995) 305-312

References

- [15] A. Bouzidia, A.S. Bouazzi, and B. Rezig, "Photocurrent simulation in an n-p-n-p silicon multilayer solar cell" *Eur. Phys. J. Appl. Phys.* 31, 11–16 (2005)
- [16] B. O'Regan, M. Gratzel, "A low cost, high-efficiency solar cell based on dye-sensitized colloidal TiO₂ films" *Nature*, Vol.353, 24 October 1991
- [17] D. E. Aspnes and A. A. Studna, "Dielectric Functions And Optical-Parameters Of Si, Ge, Gap, Gaas, Gasb, Inp, Inas, And Insb From 1.5 To 6.0 Ev," *Phys. Rev. B* 27, pp. 985-1009, 1983.
- [18] K. Rajkanan, R. Singh and J. Shewchun, "Absorption-Coefficient Of Silicon For Solar-Cell Calculations," *solid-state electronics*, vol. 22, no. 9, pp. 793-795, 1979.
- [19] M. Lammert and R. Schwartz, "Interdigitated Back Contact Solar-Cell - Silicon Solar-Cell For Use In Concentrated Sunlight," *IEEE Transactions on Electron Devices*, vol. 24, no. 4, pp. 337-342, 1977.
- [20] M. Labrune, M. Moreno and P. R. i. Cabarrocas, "Ultra-shallow junctions formed by quasi-epitaxial growth of boron and phosphorous-doped silicon films at 175°C by rf-PECVD," *Thin solid films*, pp. 2528-2530, 2010.
- [21] H. Fujiwara and M. Kondo, "Impact of epitaxial growth at the heterointerface of a-Si : H/c-Si solar cells," *Applied Physics Letters*, 2007.
- [22] a. Romain Cariou, a. MartinLabrune and p. Rocai cabarrocas, "Thin crystalline silicon solar cells based on epitaxial films grown at 165C by RF-PECVD," *SOLAR ENERGY MATERIALS AND SOLAR CELLS* , pp. 2260-2263, 2011.
- [23] H. R. D. A. D. T. M. P. S. e. a. C. Rosenblad, "Silicon epitaxy by low-energy plasma enhanced chemical vapor deposition," *J. Vac. Sci. Technol. A* , p. 2785, 1998.
- [24] J. Damon-Lacoste and P. Roca i Cabarrocas, "toward a better physucal understanding of a-Si:H/c-Si heterojunction solar cells," *J. Appl. Phys*, 2009.
- [25] X. Tan and G. W. Yang, "Physical mechanisms of hydrogen-enhanced onset of epitaxial growth of silicon by Plasma-enhanced chemical vapor deposition," *Appl. Phys. Lett.*, 2008.
- [26] Y. WEI, L. LI and I. TSONG, "ETCHING OF SI(111)-(7X7) AND SI(100)-(2X1) SURFACES BY ATOMIC-HYDROGEN," *Applied Phys. Lett.*, pp. 1818-1820, 1995.
- [27] K. Sasaki and T. Takada, "Etching effect of hydrogen plasma on electron cyclotron resonance-chemical vapor deposition and its application to low temperature Si selective epitaxial growth," *JAPANESE JOURNAL OF APPLIED PHYSICS PART 1-REGULAR PAPERS SHORT NOTES & REVIEW* , pp. 402-407, 1998.

References

- [28] J. Schmidt and M. Kerr, "Highest-quality surface passivation of low-resistivity p-type silicon using stoichiometric PECVD silicon nitride," *SOLAR ENERGY MATERIALS AND SOLAR CELLS*, pp. 585-591, 2001.
- [29] G. Cerofolini, F. Corni, S. Frabboni, C. Nobili, G. Ottaviani and R. Tonini, "Hydrogen and helium bubbles in silicon," *Materials science and engineering*, pp. 1-52, 2000.
- [30] Mahdi Farrokh-Baroughi and Siva Sivoththaman, "A Novel Silicon Photovoltaic Cell Using a Low-Temperature Quasi-Epitaxial Silicon Emitter" *IEEE ELECTRON DEVICE LETTERS*, VOL. 28, NO. 7, pp. 575-577 2007
- [31] M. Kambara, H. Yagi, M. Sawayanagi, and T. Yoshida, "High rate epitaxy of silicon thick films by medium pressure plasma chemical vapor deposition", *J. Appl. Phys.* 99, 074901 (2006); doi: 10.1063/1.2181279
- [32] Y. Mori, K. Yoshii, K. Yasutake, H. Kakiuchi, H. Ohmi, K. Wada "High-rate growth of epitaxial silicon at low temperatures (530–690 K) by atmospheric pressure plasma chemical vapor deposition" *Thin Solid Films* 444 (2003) 138–145
- [33] Scott J. DeBoer, Vikram L. Dalal, George Chumanov, and Randy Bartels. "Low temperature epitaxial silicon film growth using high vacuum electron cyclotron resonance plasma deposition" *Appl. Phys. Lett.* 66, 2528 (1995); doi: 10.1063/1.113156
- [34] Kiyoshi YASUTAKE, Naotaka TAWARA, Hiromasa OHMI, Yoshikazu TERAJ, Hiroaki KAKIUCHI, Heiji WATANABE, and Yasufumi FUJIWARA "Photoluminescence Study of Defect-Free Epitaxial Silicon Films Grown at Low Temperatures by Atmospheric Pressure Plasma Chemical Vapor Deposition" *Japanese Journal of Applied Physics* Vol. 46, No. 4B, 2007, pp. 2510–2515
- [35] J. Damon-Lacoste and P. Roca i Cabarrocas, "Toward a better physical understanding of a-Si:H/c-Si heterojunction solar Cells" *J. Appl. Phys.* 105, 063712 (2009); doi: 10.1063/1.3091283
- [36] Masao Sakuraba, Daisuke Muto, Masaki Mori, Katsutoshi Sugawara, Junichi Murota, "Very low-temperature epitaxial growth of silicon and germanium using plasma-assisted CVD" *Thin Solid Films* 517 (2008) 10–13
- [37] W. BEYER, H. WAGNER, J. CHEVALLIER AND K. REICHEL, "COMPARATIVE STUDY OF HYDROGEN EVOLUTION FROM AMORPHOUS HYDROGENATED SILICON FILMS" *Thin Solid Films*, 90(1982) 145-152
- [38] W. Beyer, "Diffusion and evolution of hydrogen in hydrogenated amorphous and microcrystalline silicon" *Solar Energy Materials & Solar Cells* 78 (2003) 235–267

References

- [39] Li Cai, and Ajeet Rohatgi, "Effect of Post-PECVD Photo-Assisted Anneal on Multicrystalline Silicon Solar Cells" IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 44, NO. 1, JANUARY 1997
- [40] M. A. El Khakani, M. Chaker, A. Jean, S. Boily, H. Pépin et al., "Effect of rapid thermal annealing on both the stress and the bonding states of aSiC:H films" J. Appl. Phys. 74, 2834 (1993); doi: 10.1063/1.354635
- [41] K. J. Matysik, C. J. Mogab, and B. G. Bagley, "Hydrogen evolution from plasmadeposited amorphous silicon films" J. Vac. Sci. Technol. 15, 302 (1978); doi: 10.1116/1.569575

Appendix A – Medici Code for BWE solar cell simulation

TITLE Buried WIndowed Emitter structure-

COMMENT thicknesses of Antireflection coatin, epi layer, emitter, base and back-surface field

COMMENT looping the thickness of epi layer

LOOP STEPS=3

ASSIGN NAME=L1 N.VAL=(1,2,3)

ASSIGN NAME=Tepi N.VAL=(0.2,0.5,1)

COMMENT looping the coverage of emitter

LOOP STEPS=3

ASSIGN NAME=L2 N.VAL=(1,2,3)

ASSIGN NAME=Xemit N.VAL=(5,7,8.5)

COMMENT looping the lifetime in epi layer

LOOP STEPS=3

ASSIGN NAME=L3 N.VAL=(1,2,3)

ASSIGN NAME=Taw N.VAL=(1e-4,1e-5,1e-6)

ASSIGN NAME=Tarc N.VAL=0.07

ASSIGN NAME=Temit N.VAL=0.6

ASSIGN NAME=Tbase N.VAL=200

ASSIGN NAME=Tbsf N.VAL=1

ASSIGN NAME=Yepi N.VAL=@Tepi

ASSIGN NAME=Yemit N.VAL=@Tepi+@Temit

ASSIGN NAME=Ybase N.VAL=@Tepi+@Temit+@Tbase

ASSIGN NAME=Ybsf N.VAL=@Tepi+@Temit+@Tbase+@Tbsf

COMMENT Mesh Generation

MESH OUT.FILE="BPE_mesh"@L1""@L2""@L3""

X.MESH WIDTH=10.0 H1=0.40

Y.MESH Y.MIN=-@Tarc Y.MAX=0 H1=@Tarc/2

Y.MESH Y.MIN=0 Y.MAX=@Yepi H1=@Tepi/10

Y.MESH Y.MIN=@Yepi Y.MAX=@Yemit H1=@Temit/20

Y.MESH Y.MIN=@Yemit Y.MAX=@Ybase/2 H1=@Temit/10 H2=15

Appendix A – Medici Code for BWE solar cell simulation

Y.MESH Y.MIN=@Ybase/2 Y.MAX=@Ybase H1=15 H2=@Tbsf/10

Y.MESH Y.MIN=@Ybase Y.MAX=@Ybsf H1=@Tbsf/10

REGION NAME=arc Y.MAX=0 NITRIDE

REGION NAME=epi Y.MIN=0 Y.MAX=@Yepi SILICON

REGION NAME=emitter X.MAX=@Xemit Y.MIN=@Yepi Y.MAX=@Yemit SILICON

REGION NAME=base2 X.MIN=@Xemit Y.MIN=@Yepi Y.MAX=@Yemit SILICON

REGION NAME=base1 Y.MIN=@Yemit Y.MAX=@Ybase SILICON

REGION NAME=bsf Y.MIN=@Ybase Y.MAX=@Ybsf SILICON

COMMENT Electrodes, 1:emitter and 2:base

ELECTR NUM=1 X.MAX=1 Y.MIN=@Yepi+(@Temit/2) Y.MAX=@Yepi+(@Temit/2)

ELECTR NUM=2 BOTTOM

COMMENT Specify Doping

PROFILE P-TYPE Y.MIN=0 Y.MAX=@Ybsf UNIFORM N.PEAK=5e15

OUT.FILE="BPE_doping"@L1""@L2""@L3""

PROFILE N-TYPE X.MAX=@Xemit Y.MIN=@Yepi Y.MAX=@Yemit UNIFORM N.PEAK=1e19

PROFILE P-TYPE Y.MIN=@Ybase Y.MAX=@Ybsf UNIFORM N.PEAK=1e18

COMMENT surface recombination at the top surface

INTERFACE MATERIAL=(SILICON,NITRIDE) S.N=1e2 S.P=1e2

COMMENT Grid refinement based on doping.

REGRID DOPING LOG RATIO=1 SMOOTH=1 IN.FILE="BPE_doping"@L1""@L2""@L3""

COMMENT Specify Electrode Characteristics

CONTACT NUM=1 PRINT TRANSELE

CONTACT NUM=2 REFLECT=1

COMMENT Specify Optical Parameters

+ The cell is assumed to be coated with indium tin oxide

+ MATERIAL REGION=TCO PR.TAB WAVE.RE=(0.2,1.0) INDEX.RE=(2.10,2.10)

+ FIRST LAST

MATERIAL REGION=epi TAUN0=@Taw TAUP0=@Taw

MATERIAL REGION=emitter TAUN0=1E-7 TAUP0=1E-7

MATERIAL REGION=base1 TAUN0=1E-4 TAUP0=1E-4

MATERIAL REGION=base2 TAUN0=1E-4 TAUP0=1E-4

MATERIAL REGION=bsf TAUN0=1E-6 TAUP0=1E-6

Appendix A – Medici Code for BWE solar cell simulation

COMMENT Display the grid at the top and bottom on the same plot.

PLOT.2D TITLE="Buried partial emitter cell "@L1""@L2""@L3""

+ ^MARKS ^LABELS X.LEN=15

PLOT.2D GRID SCALE FILL Y.MAX=10 TITLE=""

+ X.LEN=6 X.OFF=2 ^CLEAR

PLOT.2D GRID SCALE FILL Y.MIN=@Ybsf-10 TITLE=""

+ X.LEN=6 X.OFF=11 ^CLEAR

MODELS CONMOB CONSRH AUGER

ASSIGN NAME=wavenum N.VAL=90

PHOTOGEN

+ RAYTRACE SP.FILE=AM15.DAT

+ WAVE.ST=0.295 WAVE.EN=1.255 WAVE.NUM=@wavenum INT.SCAL=1

+ X.ORG=5 Y.ORG=-1 ANGLE=90

+ RAY.WIDT=10 RAY.NUM=1 INT.RATI=1E-3 N.INTEG=10 TRANSPAR PRINT.AB

SYMBOLIC NEWTON CARRIERS=2

COMMENT Solve for each wavelength of the spectral response

LOG OUT.FILE="BPE_spec"@L1""@L2""@L3""

COMMENT solve for short circuit current for each wavelength

SOLVE SPECTR

PLOT.1D X.AXIS=WA Y.AXIS=CE(2) POINTS COLOR=2 SYMB=2 ABS CLEAR PRINT

LABEL LABEL="BPE "@L1""@L2""@L3"" COLOR=2 SYMB=2

+ X=0.6 Y=30 C.SIZE=0.2

PLOT.1D X.AXIS=WA Y.AXIS=IT POINTS COLOR=2 SYMB=2 ABS CLEAR PRINT

LABEL LABEL="AM1.5" COLOR=2 SYMB=2

+ X=0.6 Y=30 C.SIZE=0.2

COMMENT solve for DC IV values for the whole spectrum

LOG OUT.FILE="BPE_IV"@L1""@L2""@L3""

SOLVE V(2)=0.00 ELEC=2 VSTEP=.05 NSTEP=10

Appendix A – Medici Code for BWE solar cell simulation

```
SOLVE V(2)=0.52 ELEC=2 VSTEP=.02 NSTEP=3
```

```
SOLVE V(2)=0.59 ELEC=2 VSTEP=.01 NSTEP=6
```

```
PLOT.1D X.AXIS=V(2) Y.AXIS=I(2) POINTS COLOR=2 SYMB=2 CLEAR PRINT
```

```
LABEL LABEL="BPE "@L1""@L2""@L3" IV-AM1.5" COLOR=2 SYMB=2
```

```
COMMENT + X=0.2 Y=30 C.SIZE=0.2
```

```
COMMENT Calculate the power generated and load impedance.
```

```
+EXTRACT NAME=Power EXP="-1e7*@I(2)*@V(2)" PRINT
```

```
+ UNITS=Watts/cm^2
```

```
COMMENT Plot the power-vs-load resistance curve.
```

```
+PLOT.1D X.AXIS=V(2) Y.AXIS=Power POINTS COLOR=2 PRINT
```

```
+ TITLE="BPE "@Tepi" Power vs. voltage - AM1.5"
```

```
L.END
```

```
L.END
```

```
L.END
```