A Doherty Power Amplifier with Extended Bandwidth and Reconfigurable Back-off Level

by

Yu-Ting David Wu

A thesis
presented to the University of Waterloo
in fulfilment of the
thesis requirement for the degree of
Doctor of Philosophy
in
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2013

Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Yu-Ting David Wu

Abstract

Emerging wireless standards are designed to be spectrally efficient to address the high cost of licensing wireless spectra. Unfortunately, the resulting signals have a high peak-to-average ratio that reduces the base station power amplifier efficiency at the back-off power level. The wasted energy is converted to heat that degrades the device reliability and increases the base-station's carbon footprint and cooling requirements. In addition, these new standards place stringent requirements on the amplifier output power, linearity, efficiency, and bandwidth.

To improve the back-off efficiency, a Doherty amplifier, which uses two device in parallel for back-off efficiency enhancement, is deployed in a typical base station. Unfortunately, the conventional Doherty amplifier is narrowband and thus cannot satisfy the bandwidth requirement of the modern base station that needs to support multiple standards and backward compatibility.

In this thesis, we begin by studying the class F/F^{-1} high efficiency mode of operation. To this end, we designed a narrowband, harmonically-tuned 3.3 GHz, 10 W GaN high efficiency amplifier. Next, we investigate how to simultaneously achieve high efficiency and broad bandwidth by harnessing the simplified real frequency technique for the broadband matching network design. A 2 to 3 GHz, 45 W GaN amplifier and a 650 to 1050 MHz, 45 W LDMOS amplifier were designed. Finally, we analyze the conventional Doherty amplifier to determine the cause of its narrow bandwidth. We find that the narrow bandwidth can be attributed to the band-limited quarter-wave transformer as well as the widely adopted traditional design technique.

As an original contribution to knowledge, we propose a novel Doherty amplifier configuration with intrinsically broadband characteristics by analyzing the load modulation concept and the conventional Doherty amplifier. The proposed amplifier uses asymmetrical drain voltage biases and symmetrical devices and it does not require a complex mixed-signal setup. To demonstrate the proposed concept in practice, we designed a 700 to 1000 MHz, 90 W GaN broadband Doherty amplifier. Moreover, to show that the proposed concept is applicable to high power designs, we designed a 200 W GaN broadband Doherty amplifier in the same band. In addition, to show that the technique is independent of the device technology, we designed a 700 to 900 MHz, 60 W LDMOS broadband Doherty amplifier. Using digital pre-distortion, the three prototypes were shown to be highly linearizable when driven with wideband 20 MHz LTE and WCDMA modulated signals and achieved excellent back-off efficiency.

Lastly, using the insights from the previous analyses, we propose a novel mixed-technology Doherty amplifier with an extended and reconfigurable back-off level as well as an improved power utilization factor. The reconfigurability of the proposed amplifier makes it possible to customize the back-off level to achieve the highest average efficiency for a given modulated signal without redesigning the matching networks. A 790 to 960 MHz, 180 W LDMOS/GaN Doherty amplifier demonstrated the extended bandwidth and reconfigurability of the back-off level. The proposed amplifier addresses the shortcomings of the conventional Doherty amplifier and satisfies the many requirements of a modern base station power amplifier.

Acknowledgements

Dedication

To my loving family

Contents

List of Tables

List of Figures

xv

Nomenclature

3G	Third generation
4G	Fourth generation
AC	Alternating current
ACPR	Adjacent channel power ratio
AM–AM	Amplitude to amplitude modulation
CDMA	Code division multiple access
CW	Continuous wave
DC	Direct current
DE	Drain efficiency
DPD	Digital pre-distortion
EVM	Error vector magnitude
FET	Field effect transistor
GaAs	Gallium arsenide
GaN	Gallium nitride
GSM	Global System for Mobile communication
HEMT	High electron mobility transistor
HVHBT	High voltage heterojunction bipolar transistor
LDMOS	Laterally diffused metal oxide semiconductor

LTE	Long Term Evolution
MMIC	Monolithic microwave integrated circuit
OFDM	Orthogonal frequency division multiplexing
PA	Power amplifier
PAE	Power-added efficiency
PAPR	Peak-to-average power ratio
PCB	Printed circuit board
PDF	Probability density function
QAM	Quadrature amplitude modulation
RF	Radio frequency
SRFT	Simplified real frequency technique
TD-SCDMA	Time Division Synchronous Code Division Multiple Access
UMTS	Universal Mobile Telecommunications System
VCCS	Voltage-controlled current source
VCVS	Voltage-controlled voltage source
WCMDA	Wideband Code Division Multiple Access
WiMAX	Worldwide Interoperability for Microwave Access

Chapter 1

Introduction

1.1 Motivation

The enormous cost to license wireless spectra has driven next generation wireless standards such as Long Term Evolution (LTE) and Worldwide Interoperability for Microwave Access (WiMAX) to adopt spectrally efficient modulation schemes that maximize the data throughput and network capacity. Unfortunately, techniques that improve the spectral efficiency produce signals with a high peak-to-average power ratio (PAPR). For radio frequency (RF) power amplifiers (PA) in wireless base stations, the high PAPR is a major problem because it significantly reduces the amplifier efficiency at the average (i.e. back-off) power level.

The problem can be illustrated using Figure 1.1a which contains an orthogonal frequency division multiplexing (OFDM) spectrum with four sub-carriers. Although the overlapping carriers improve the spectral efficiency, the associated time domain waveform illustrated in Figure 1.1b exhibits a high PAPR because of the summation of correlated sub-carriers. For a typical power amplifier with an efficiency versus output power profile shown in Figure 1.2, the high PAPR signal yields a very low average efficiency. The wasted energy is converted to heat that not only degrades the device reliability but also increases the carbon footprint and cooling requirements of the base station.

The emerging wireless standards also require the base station power amplifier to be more linear and output higher power. As Figures 1.3a and 1.3b illustrate, moving from 16 quadrature amplitude modulation (QAM) to 64 QAM requires higher output power to maintain the signal to noise ratio and bit error rate at the receiver [3]. Moreover, because the signal is modulated in amplitude and phase, there are stringent linearity requirements for in-band and adjacent channels.

The base station power amplifier design is further complicated by a proliferation of new standards in an increasingly diverse wireless environment in which emerging and legacy standards

(a) Four-carrier OFDM spectrum

(b) OFDM waveform illustrating high PAPR
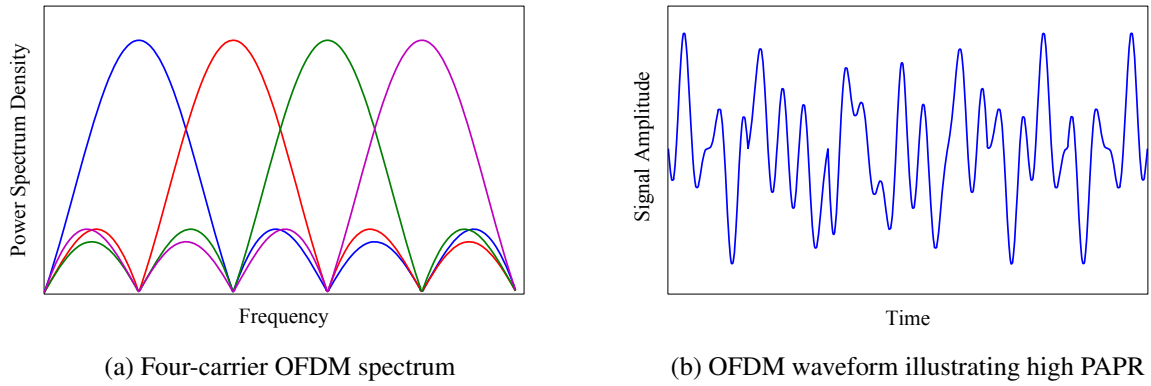
Figure 1.1: An OFDM modulation with four sub-carriers.

PA Eff. at Peak Power = 78.5%

2G Signal PAPR = 0-4 dB
Avg. Eff. = 49.7%

3G Signal PAPR = 8-9 dB
Avg. Eff. = 28.0%

4G Signal PAPR = 10-12 dB
Avg. Eff. = 19.8 %

Output Power (2 dB/div)
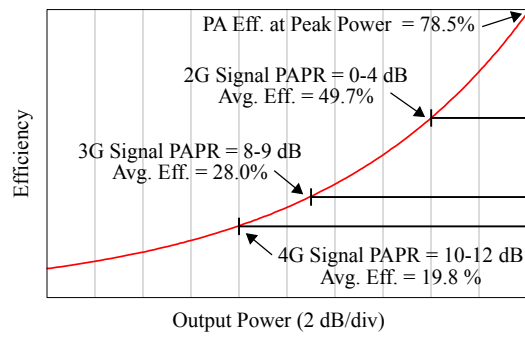
Figure 1.2: The reduced amplifier average efficiency when driven with high PAPR signals.

(a) 16 QAM constellation.

(b) 64 QAM constellation.
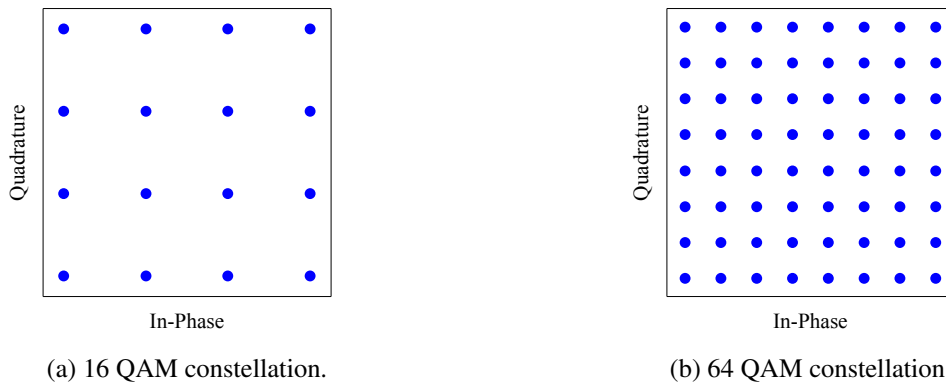
Figure 1.3: An increase in modulation bits per symbol in emerging wireless standards.
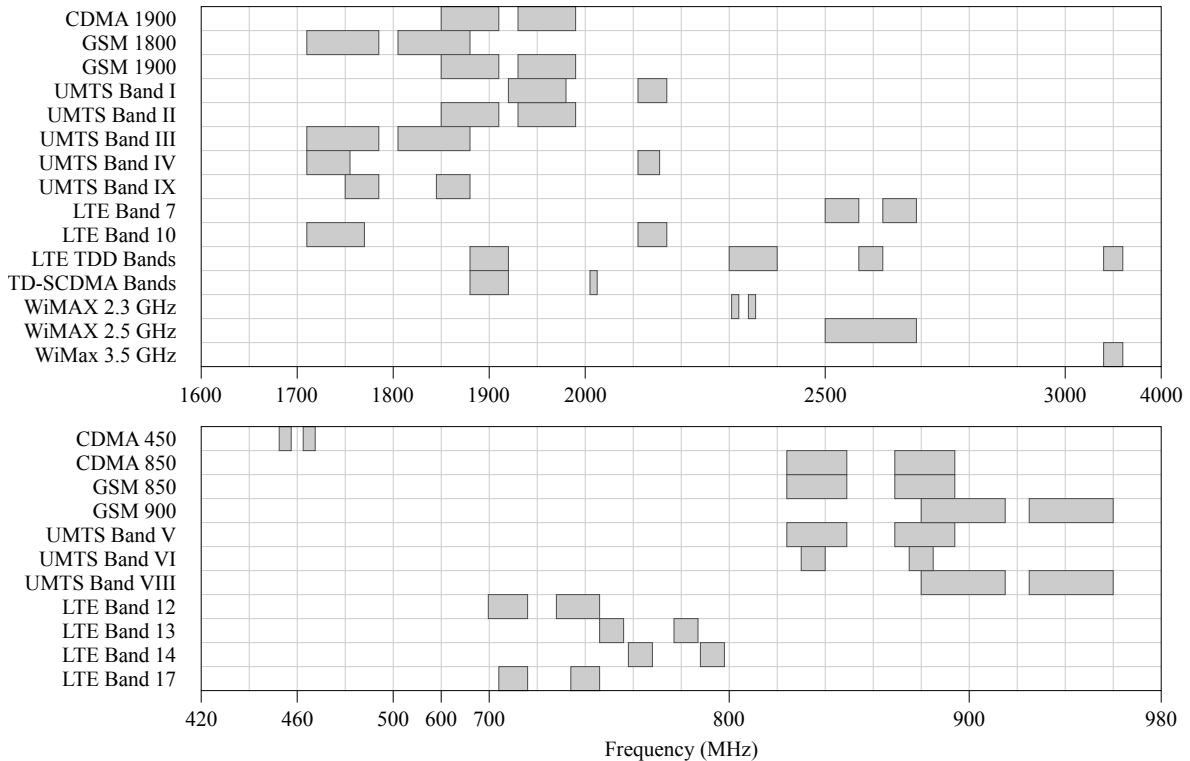
Figure 1.4: The wireless communication spectrum allocation.

must coexist. Figure 1.4 illustrates the frequency bands containing the legacy GSM and CDMA standards, the 3G UMTS standard, as well as the emerging 4G LTE, WiMAX, and TD-SCDMA standards. Conventionally, multiple narrowband radios are deployed to support each standard, resulting in an approach that is power inefficient and redundant in hardware.

1.2   Problem Statement

From the discussion in Section 1.1, the modern base station power amplifier needs to satisfy multiple criteria for efficiency, linearity, output power, and bandwidth. In particular, the amplifier needs to be highly efficient when driven with a high PAPR signal. To achieved high efficiency at the back-off power level, advanced circuit techniques such as the Doherty power amplifier [4] and the envelope tracking amplifier technique [5] were proposed in the literature. Of the two, the Doherty amplifier has been widely adopted in the industry due to its ease of implementation.

Unfortunately, the conventional Doherty amplifier exhibits a narrowband characteristics of less than 10% fractional bandwidth. Therefore, despite being able to satisfy the modern base

station requirements for efficiency, linearity and output power, the conventional Doherty amplifier is unable to meet the bandwidth requirement of a modern base station amplifier. The limited bandwidth means that currently, multiple Doherty amplifiers are deployed in a single base station, one for each standard that a wireless carrier serves. This approach is power inefficient and redundant in hardware.

In this thesis, we propose a novel approach that extends the bandwidth of the conventional Doherty amplifier. The proposed amplifier is simple to implement and meets the multitude of requirements of a modern base station amplifier. The proposed technique is an important milestone towards building a single power amplifier that can simultaneously support multiple wireless standards while reducing the complexity and cost of the base station transmitter.

1.3   Thesis Organization

The thesis is organized as follows. Chapter 2 provides the background on the theory and design of single-ended RF power amplifiers. Traditional and high efficiency classes of operation are introduced based on voltage and current waveform analyses. LDMOS and GaN device technologies used in base station power amplifiers are briefly discussed. Practical input and output matching network requirements are outlined along with the widely adopted load-pull design technique. The design of a 3.3 GHz GaN high efficiency amplifier is presented.

Chapter 3 outlines the design of highly efficient and broadband single-ended amplifiers using broadband load-pull results and the simplified real frequency technique to synthesize the broadband matching network. Theoretical analyses using the class B/J design space explains the efficiency insensitivity to the second harmonic terminations. The design of a 2 to 3 GHz GaN amplifier and a 650 to 1050 MHz LDMOS amplifier are discussed in detail.

Chapter 4 introduces the conventional Doherty amplifier which uses two devices in parallel to achieve efficiency enhancement at the back-off power level. The inadequate load modulation and limited bandwidth are found to be key shortcomings of the conventional Doherty amplifier. The widely adopted traditional technique is outlined and a literature review shows the limited bandwidth of the conventional Doherty amplifier in existing literature.

Chapter 5 proposes a novel approach to extend the bandwidth of the conventional Doherty amplifier. Derivations based on the load modulation concept and the conventional Doherty amplifier show that asymmetrical drain voltage biasing with symmetrical devices can achieve an extended bandwidth without the use of a complex mixed-signal setup. Two 700 to 1000 MHz GaN Doherty amplifiers and a 700 to 900 MHz LDMOS Doherty amplifier achieve excellent continuous-wave and linearization results, thus demonstrating the feasibility of the proposed concept in practice.

Chapter 6 builds upon the concept in Chapter 5 to obtain efficiency enhancement at extended back-off levels greater than 6 dB. By adjusting the drain and the gate voltage bias of the main and auxiliary devices respectively, the back-off level is shown to be reconfigurable on the fly. Moreover, to improve the power utilization factor of the amplifier, a 790 to 960 MHz mixed-technology Doherty amplifier is proposed with a LDMOS device as the main device and a GaN device as the auxiliary device. The measurements show excellent continuous wave results and linearizability.

Lastly, Chapter 7 concludes the thesis by summarizing the contributions in the each chapter. Future work to improve the feasibility of the proposed concept at higher frequency and to improve the proposed amplifier performance through device optimization are discussed.

Chapter 2

High Efficiency Power Amplifier Overview

2.1 Introduction

In this chapter, we outline the background theory and design of single-ended RF power amplifiers in base station transmitters. The analyses lay the groundwork for understanding advance circuit techniques presented in subsequent chapters such as the Doherty power amplifier which uses two devices in parallel. Using an ideal FET, various classes of operations and their respective linearity, efficiency, and gain characteristics are derived. Next, we briefly discuss the characteristics of high power LDMOS and GaN device technologies used in base station amplifiers. Practical design considerations such as the effects of the device parasitic and package on the load impedances are presented. In addition, we briefly discuss the requirement for stability, biasing, and minimal matching network insertion loss. The popular load-pull design technique and a multi-harmonic matching network design method are introduced. Lastly, we apply these techniques to design a 10 W 3.3 GHz GaN high efficiency amplifier.

2.2 Ideal FET

Currently, device technologies in base station power amplifiers are primarily field effect transistors (FET). As such, the analyses in this chapter are based on an ideal FET as shown in Figure 2.1. This device has no parasitic element and has infinite AC input and output impedances. Consequently, the device behaviour at the intrinsic drain is frequency independent. The gate voltage V_{gs} is converted to drain current I_{ds} through the transconductance g_m within the linear region of the transfer characteristics as indicated in Figure 2.2a. This device is unilateral with no feedback mechanism from the drain to the gate.

Figure 2.1: The ideal FET.

(a) The V_{gs} to I_{ds} transfer characteristic.

(b) The I_{ds} vs. V_{ds} for varying V_{gs}.
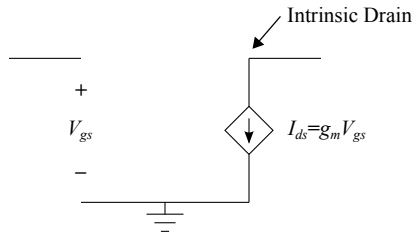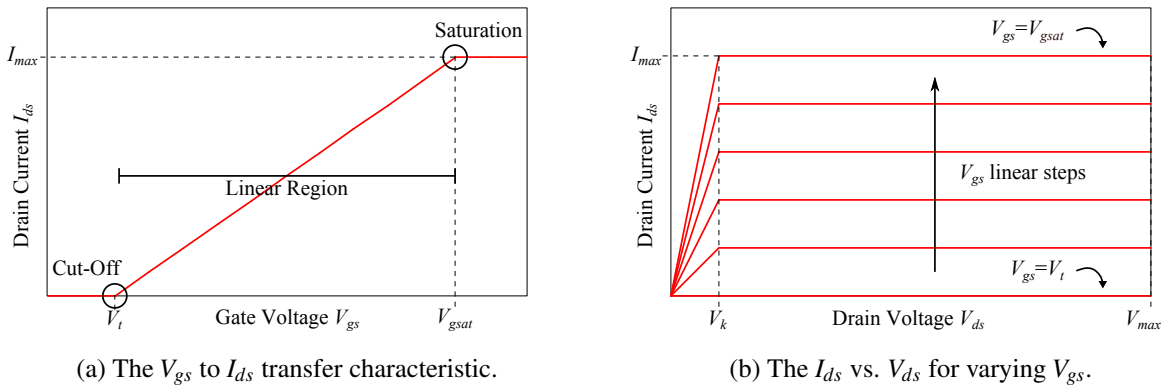
Figure 2.2: The DC characteristics of the ideal FET.

Unlike a small signal amplifier, a power amplifier is designed to fully utilize a given device. Therefore, device parameters such as the saturation current I_{max}, knee voltage V_k, and breakdown voltage V_{br} (also known as V_{max}) are specified in the ideal FET. The full device parameters are defined in Table 2.1. Figure 2.2b contains the DC-IV characteristics of the ideal FET with V_{max}, I_{max}, and V_k indicated.

Despite its simplicity, the ideal FET can capture the device behaviours that are key to the design of a high efficiency power amplifier. In particular, the harmonic current generated through the cut-off and saturation regions circled in Figure 2.2a and the nonlinearity caused by an intrusion into the device knee region can be predicted by the ideal FET in a harmonic balance simulator.

In the subsequent sections, we will analyze the intrinsic drain waveforms of different classes of operation using a test bench containing the ideal FET as illustrated by Figure 2.3. For the DC bias, the device gate and drain are biased to V_{gg} and V_{dd} respectively via two separate voltage

Table 2.1: Ideal FET parameters.

Parameter	Definition
I_{max}	Maximum drain current, also known as the saturation current I_{sat}
V_{max}	Maximum allowable drain voltage, also known as the breakdown voltage V_{br}
V_t	Threshold voltage, defined at the gate, also known as the cut-off voltage
V_k	Knee voltage, defined at the drain
V_{gsat}	Lowest gate voltage that yields the current I_{max} at the drain
g_m	Device transconductance, measuring drain current per unit gate voltage
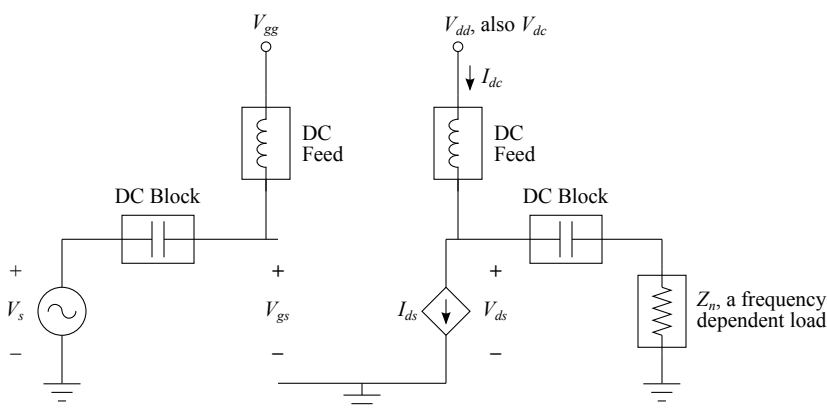
Figure 2.3: Waveform analysis using the ideal FET in a test bench.

supplies fed via ideal DC feeds. The DC feeds reject AC and ensure that no RF power leaks to the DC supply. For a given bias condition, a quiescent DC drain current I_{dc} is drawn. No gate current is drawn. In terms of RF, the gate is driven with a single-tone voltage source V_s fed via an ideal DC block. The time domain gate voltage V_{gs} contains both DC and RF components. The drain is terminated with a load impedance Z_n that varies depending on the frequency. The subscript n denotes the harmonic number. For example, Z_1, Z_2, and Z_3 refer to the impedance value at the fundamental, second, and third harmonic frequencies respectively. The DC blocks adjacent to V_s and Z_n prevent DC power dissipation in the RF source and the load termination.

We will focus our analyses on the time domain drain current and voltage waveforms I_{ds} and V_{ds} respectively that directly determine the amplifier efficiency and output power. We also define the parameters I_n and V_n to denote the Fourier components of I_{ds} and V_{ds} respectively. The subscript n again refers to the harmonic number. For example, I_1, I_2, and I_3 refer to the fundamental, second, and third harmonic current components. The DC component V_{dc} of V_{ds} is simply equal to the drain bias V_{dd}.

Table 2.2: Ideal FET test bench parameters.

Parameter	Definition
V_{gg}	Gate DC bias voltage
V_{dd}	Drain DC bias voltage
V_s	RF input voltage
V_{gs}	Time domain voltage waveform at the intrinsic gate
I_{ds}	Time domain current waveform at the intrinsic drain
$I_n, n \geq 1$	Fourier component of I_{ds} where n denotes the harmonic number
I_{dc}	DC component of I_{ds}
V_{ds}	Time domain voltage waveform at the intrinsic drain
$V_n, n \geq 1$	Fourier component of V_{ds} where n denotes the harmonic number
V_{dc}	DC component of V_{ds} which is equal to V_{dd}
Z_n	A frequency dependent load where n denotes the harmonic number

2.3 Power Amplifier Efficiency

The efficiency of an amplifier is defined as the RF output power divided by the DC power drawn from the supply. For wireless applications, we are interested in the output power P_1 at the fundamental frequency. As such, the DC-to-RF conversion efficiency is defined as

$$\eta = \frac{P_1}{P_{dc}} \tag{2.1}$$

The parameter η, also known as the drain efficiency (DE), is completely determined by the time domain voltage and current waveforms at the device intrinsic drain. Conversely, designing for a given efficiency is achieved by engineering the voltage and current waveforms at the intrinsic drain.

To illustrate how the waveforms and efficiency are related, the maximum efficiencies of an ideal class A and class F amplifier are derived from their respective drain waveforms as depicted in Figure 2.4a and 2.4b. For the class A amplifier, the drain current waveform I_{ds} and drain voltage waveform V_{ds} are sinusoidal with fundamental phasor I_1 and V_1 and DC components I_{dc} and V_{dc} respectively. Using (2.1), the maximum class A efficiency is given by

$$\eta_{\text{classA}} = \frac{P_1}{P_{dc}} = \frac{\Re(\frac{1}{2}V_1 I_1^*)}{V_{dc}I_{dc}} = \frac{1}{2}\frac{(V_{max}I_{max})/4}{(V_{max}I_{max})/4} = 50\% \tag{2.2}$$

On the other hand, computing the maximum class F efficiency requires Fourier analyses of the drain waveforms because the DC and fundamental components are not apparent from the time

(a) The ideal class A waveforms.

(b) The ideal class F waveforms.
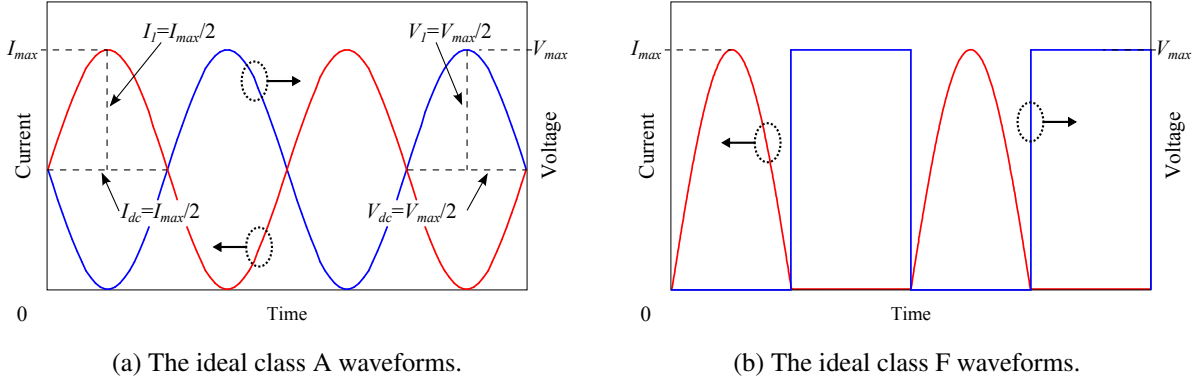
Figure 2.4: The ideal class A and class F current and voltage waveforms.

domain waveforms. For the half-wave rectified sine wave current in Figure 2.4b, the Fourier series is given as

$$I(t) = I_{max}\left[\frac{1}{\pi} + \frac{1}{2}\sin(\omega t) - \frac{2}{\pi}\left(\frac{\cos(2\omega t)}{1\cdot 3} + \frac{\cos(4\omega t)}{3\cdot 5} + \frac{\cos(6\omega t)}{5\cdot 7} + \cdots\right)\right] \qquad (2.3)$$

Similarly, the Fourier series of the square wave voltage is given as

$$V(t) = V_{max}\left[\frac{1}{2} + \frac{2}{\pi}\left(\frac{\sin(\omega t - \pi)}{1} + \frac{\sin[3(\omega t - \pi)]}{3} + \frac{\sin[5(\omega t - \pi)]}{5} + \cdots\right)\right] \qquad (2.4)$$

Taking only the DC and fundamental components from (2.3) and (2.4), the maximum class F efficiency is determined as

$$\eta_{\text{classF}} = \frac{P_1}{P_{dc}} = \frac{1}{2}\frac{(I_{max}/2)(2V_{max}/\pi)}{(I_{max}/\pi)(V_{max}/2)} = 100\% \qquad (2.5)$$

From the above analysis, class F is preferable to class A from an efficiency perspective since a perfect DC-to-RF conversion can be achieved by eliminating the overlap between the instantaneous voltage and current waveforms. As a result, the power dissipation within the device is minimized. However, the class F waveforms contain harmonic components that require advance technique to synthesize. For the current waveform, the required harmonics can be synthesized via the nonlinearity generated by the device gate cut-off. For the voltage waveforms, the harmonics follow Ohm's law and are the product of the current and impedance at each harmonic frequency.

10
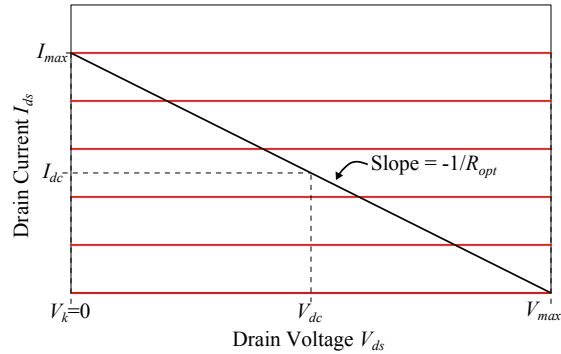
Figure 2.5: The class A load line.

The fact an efficient amplifier requires drain waveforms with harmonics content underlines the inherent trade-off between efficiency and design complexity. Moreover, practical efforts to increase the amplifier efficiency generally result in a nonlinear transfer characteristic. As such, linearization techniques such as digital pre-distortion (DPD) are required to correct the nonlinearity.

The subsequent sections will discuss techniques to leverage the device nonlinearity for waveform engineering as well as matching network design techniques that enable high efficiency power amplifier operation.

2.4 Power Amplifier Theory

2.4.1 Class A Amplifier

Despite its simplicity, the class A amplifier serves as an important efficiency and linearity benchmark for other advanced classes of operation. Moreover, the concept of load line analysis that is easily illustrated using a class A amplifier is also applicable to other classes of operation.

The class A gate bias is halfway between the saturation and cutoff limits circled in Figure 2.2a. Any RF gate voltage that does not breach these limits is converted linearly to the drain as current. Using the ideal FET with zero knee voltage (i.e. $V_k=0$), the dynamic load line corresponding to the maximum linear input can be plotted over the device DC-IV curves as shown in Figure 2.5. The dynamic load line is a plot of the instantaneous drain current versus drain voltage. The slope of the load line in class A is determined by the fundamental load impedance Z_1 presented to the device. The optimal impedance R_{opt} that maximizes the voltage swing and output power is determined as

Table 2.3: The definition of different classes of operation.

Class of operation	Conduction angle α
Class A	$\alpha = 2\pi$
Class AB	$\pi < \alpha < 2\pi$
Class B	$\alpha = \pi$
Class C	$\alpha < \pi$

$$R_{opt} = \frac{V_{dd}}{I_{max}/2} \tag{2.6}$$

Correspondingly, the maximum output power is given by

$$P_{out} = \frac{1}{8}V_{max}I_{max} \tag{2.7}$$

The main advantages of class A are the linear transfer characteristic and the ease of implementation. Unfortunately, because of its waveform characteristics, the maximum efficiency for a class A amplifier is only 50%. Moreover, DC power is consumed regardless whether an RF input is present. For wireless applications that can tolerate some degree of nonlinearity, the low efficiency of the class A amplifier is not acceptable. Nevertheless, it remains the chosen solution where a very linear amplifier is required.

2.4.2 Reduced Conduction Angle Modes: Class AB, B, C

To increase the drain efficiency as defined by (2.1), the ratio of the fundamental output power to the DC power consumed must increase. One method to improve the drain efficiency is by varying the DC gate bias V_{gg} of the device which changes the conduction angle α, defined as the portion of the gate voltage waveform above the threshold voltage V_t. Table 2.3 defines the different classes of operation based on the conduction angle α. The class A amplifier has a conduction angle of 2π because the input voltage is always above the cutoff. For reduced conduction angle modes, a portion of the input waveform dips below V_t into the non-conducting region as shown in Figure 2.6a. As a result, only a portion of the gate waveform, corresponding to α, is converted to the drain current as illustrated in Figure 2.6b.

Mathematically, the drain current waveforms of Figure 2.6b can be expressed as a piecewise function in terms of I_{max}, α, and θ as given by

(a) An illustration of the increased input drive requirement.

(b) The drain current waveforms for different conduction angles.
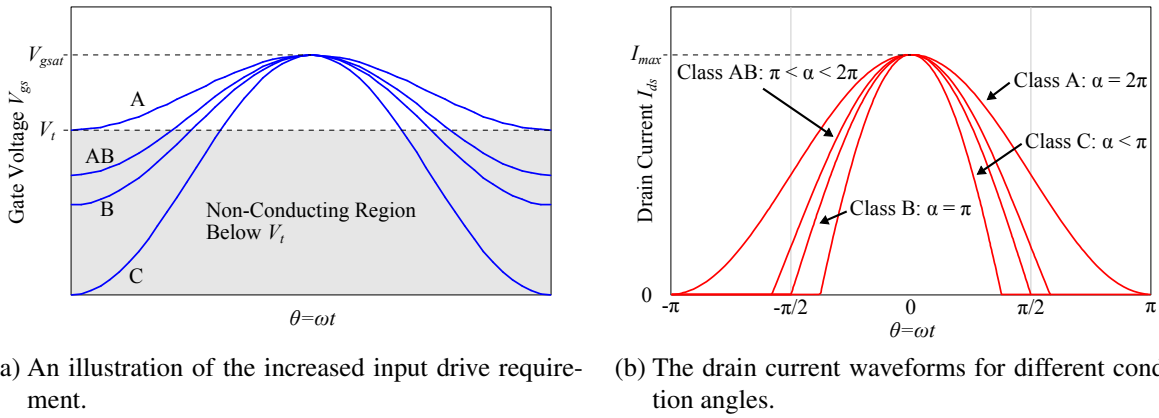
Figure 2.6: The gate and drain waveforms for different classes of operation.

$$
I(\theta) = \begin{cases} 0 & -\pi \leq \theta < -\alpha/2 \\ \dfrac{I_{max}}{1-\cos(\alpha/2)}[\cos(\theta)-\cos(\alpha/2)] & -\alpha/2 \leq \theta \leq \alpha/2 \\ 0 & \alpha/2 < \theta \leq \pi \end{cases} \tag{2.8}
$$

where $\theta = \omega t$.

To determine the DC, fundamental, and harmonic components of the current waveform as a function of the conduction angle α, Fourier analyses are carried out using (2.9) and (2.10).

$$
I_{dc} = \frac{1}{2\pi} \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1-\cos(\alpha/2)}[\cos(\theta)-\cos(\alpha/2)]d\theta \tag{2.9}
$$

$$
I_n = \frac{1}{\pi} \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1-\cos(\alpha/2)}(\cos(\theta)-\cos(\alpha/2))\cos(n\theta)d\theta, n \geq 1 \tag{2.10}
$$

The results up to the 5th harmonic, plotted in Figure 2.7, show that as the conduction angle decreases, the DC component current decreases monotonically while the fundamental component remains above the DC component for all α. Therefore, an improved drain efficiency is possible when the DC current component decreases more than the fundamental component. However, because the amplifier efficiency is based on power calculation, the drain voltage waveform also has to be considered.

The presence of higher harmonic content in the current in Figure 2.7 implies that unlike class A, the drain voltage of class AB, B, and C is not only a function of the fundamental impedance but also that of the harmonic impedances. As such, the amplifier efficiency can
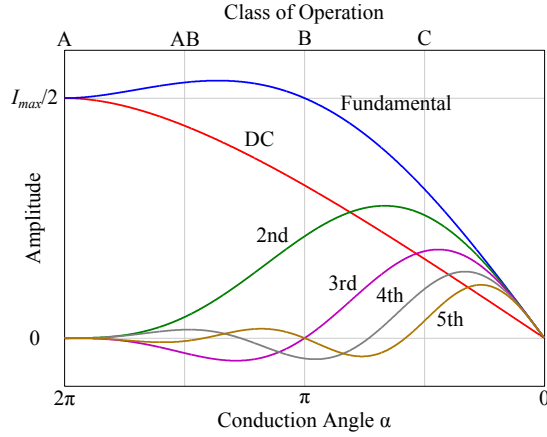
Figure 2.7: Fourier analyses of reduced conduction angle current waveforms [1].

Table 2.4: The efficiency of different classes of operation.

Class of operation	Peak drain efficiency η
Class A	$\eta = 50\%$
Class AB	$50\% < \eta < 78.5\%$
Class B	$\eta = 78.5\%$
Class C	$78.5\% < \eta < 100\%$

vary depending on the load impedance Z_n. In the classical "tuned load" analysis, the harmonic impedances are assumed to be zero (i.e. short circuited) as given by

$$Z_n = 0, \quad n \geq 2 \tag{2.11}$$

The "tuned load" condition results in a purely sinusoidal drain voltage. Table 2.4 lists the efficiency of the different classes of operation assuming the "tuned load" condition and a fundamental impedance Z_1 that yields the maximum drain voltage swing.

Aside from the improved peak efficiency, reduced conduction angle modes have several notable advantages to class A. First, the back-off efficiency characteristics, illustrated in Figure 2.8a, show that at the back-off power levels, the efficiency drop for the reduced conduction angle modes is less severe when compared to class A. In class A, the efficiency drops inversely versus the output power, whereas for class B, the efficiency drops as the square-root of the output power. The back-off efficiency improvement is very relevant for modern signals with a high PAPR. Second, the reduced conduction angle modes consume less DC power under zero stimulus. In fact, for an ideal class B amplifier, no DC power is consumed if the RF input is zero.

Despite the aforementioned advantages, reduced conduction angle modes are not without

14

(a) The efficiency versus output power.

(b) The input to output transfer characteristic.
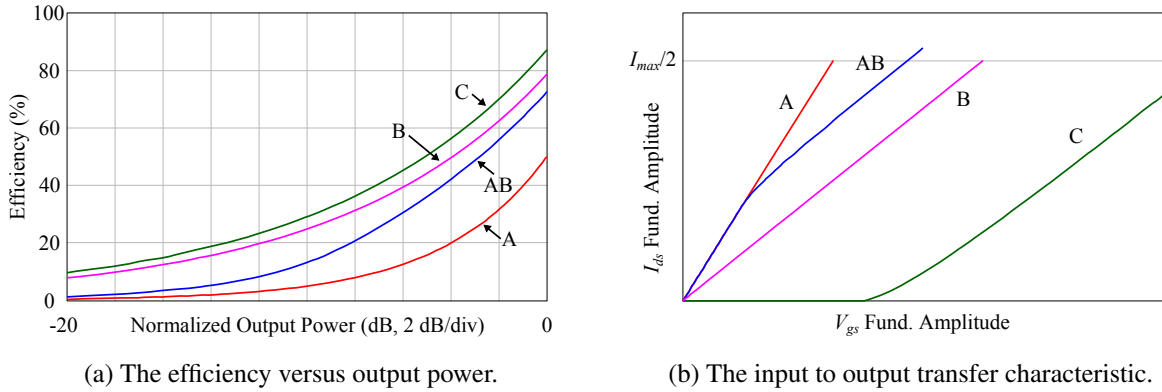
Figure 2.8: The characteristics of different classes of operation.
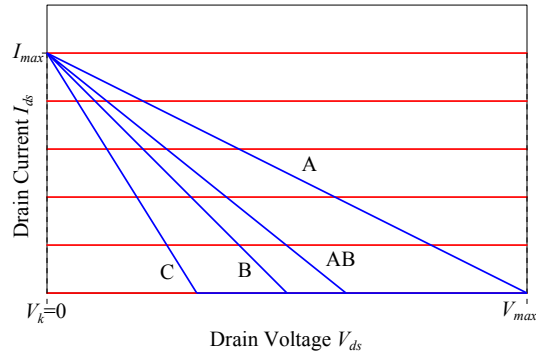
Figure 2.9: The dynamic load lines of different classes of operation.

drawbacks. As Figure 2.6a illustrates, the gate voltage swing for class AB, B, and C has to increase to reach I_{max} on the output. The increased drive requirements reduce the gain of the amplifier. At GHz frequencies, the reduced gain can outweigh the efficiency improvement. Moreover, the large negative swing below V_t can stress or cause breakdown in the device and lower the device reliability. In addition, as Figure 2.8b illustrates, except for class A and B, the transfer characteristics are nonlinear. Class B is linear because unlike class AB and C, the conduction angle is constant versus the gate voltage drive.

Finally, the dynamic load lines of the different classes of operation are plotted in Figure 2.9. As the efficiency increases, the load line tends to move toward the lower left corner. This general observation also applies to other high efficiency modes that are discussed in subsequent sections.

To summarize, reducing the conduction angle is an effective way of increasing the amplifier efficiency. However, thorough analyses and a systematic design method are required to tackle the increased design complexity.
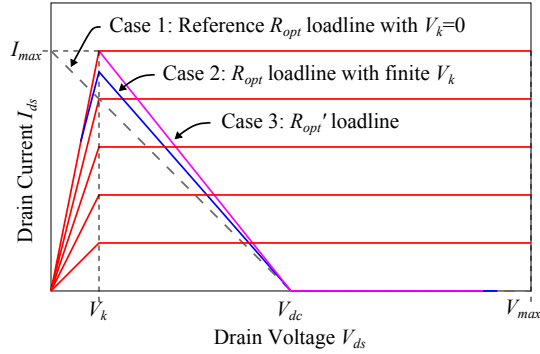
Figure 2.10: The class B load lines in the ideal FET with a finite knee region.

2.4.3 Effects of the Knee Voltage

The analyses so far have assumed zero knee voltage V_k. In practice, all device technologies exhibit a finite knee region (also known as the linear region) that negatively affects the amplifier performance. The severity of the performance degradation depends on the ratio of the knee voltage to the drain bias voltage V_{dd}. To illustrate the performance degradation, three different class B load lines are overlaid on the DC-IV curves of the ideal FET with a finite V_k as shown in Figure 2.10. Case one plots the reference class B load line under zero knee voltage condition with a fundamental load impedance R_{opt} calculated using (2.6) given that class A and B have the same R_{opt}. In case two, a device with $V_k = 0.2V_{dd}$ is terminated with the same R_{opt} as case one. This arrangement causes the load line to enter the knee region, distorting the drain current waveform when the voltage swings below V_k as illustrated in Figure 2.11. Because the drain voltage is a function of the current, the two waveforms are now recursively related. A Fourier analysis of the bifurcated current waveform shows reduced a fundamental component I_1 which manifests as compression in the amplifier's gain versus power characteristic.

To restore the class B current waveform and obtain a linear transfer characteristic, a lower load impedance R_{opt}' is presented the device as determined by

$$R_{opt}' = \frac{V_{dd} - V_k}{I_{max}/2} \tag{2.12}$$

which has a corresponding output power of

$$P_{out}' = \frac{(V_{dd} - V_k)I_{max}}{4} \tag{2.13}$$

The waveforms corresponding to (2.12) and (2.13) are plotted in Figure 2.11b and the load line is shown as case three in Figure 2.10. Because the voltage does not swing below V_k, the current

16

(a) The current distortion due to a finite knee region.

(b) The current restored by reducing the load impedance.
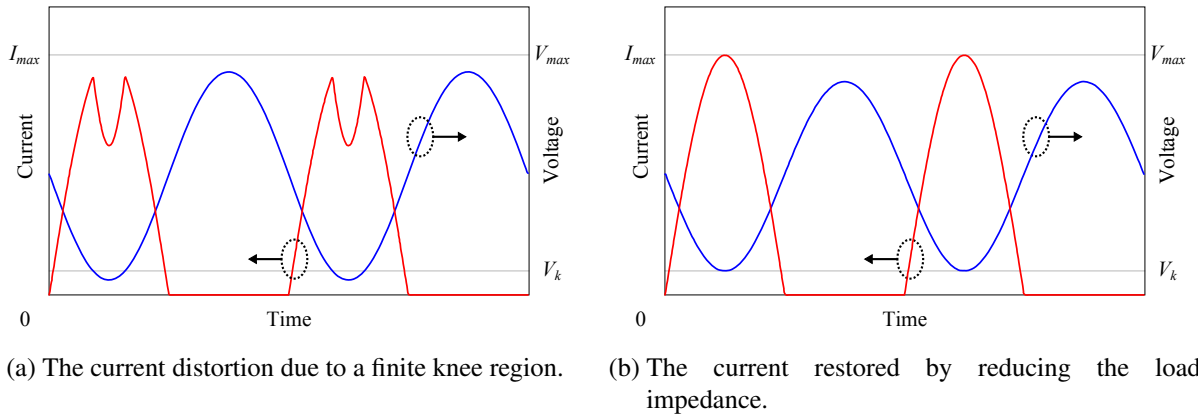
Figure 2.11: The impact of the knee region on class B waveforms.

Table 2.5: The impact of a finite knee voltage on the class B amplifier performance.

Case	V_k	R_{opt} calculation	Normalized P_{out}	Efficiency	Transfer characteristic
1	0	(2.6)	1.00	78.5%	linear
2	$0.2V_{dd}$	(2.6)	0.76	66.4%	compression
3	$0.2V_{dd}$	(2.12)	0.80	62.0%	linear

waveform is undistorted. The efficiency and normalized output power of the three case studies are summarized in Table 2.5.

A finite knee region degrades the output power and efficiency of an amplifier because there is less available voltage swing. Table 2.5 shows that the choice of R_{opt} yields a trade-off between efficiency and output power. With a finite knee region, the load delivering the maximum power no longer coincides with the load delivering the maximum efficiency. Table 2.5 also highlights a fundamental trade-off between the efficiency and linearity since case two has a higher efficiency but a nonlinear transfer characteristic and vice versa in case three.

2.4.4 Class F and F^{-1} Amplifier Theory

In the reduced conduction angle classes of operation, engineering the drain current waveform results in drastic efficiency improvements over class A. By applying the same technique to the drain voltage, class F and F^{-1} offer further efficiency enhancement without compromising the output power [1, 6–9].

Figure 2.12a illustrates the ideal class F waveforms. Biased in class B, class F benefits from the efficiency improvement of a half-wave rectified sine-wave current. To show how a square

(a) The ideal class F waveforms.

(b) Sinusoids with third harmonic components.
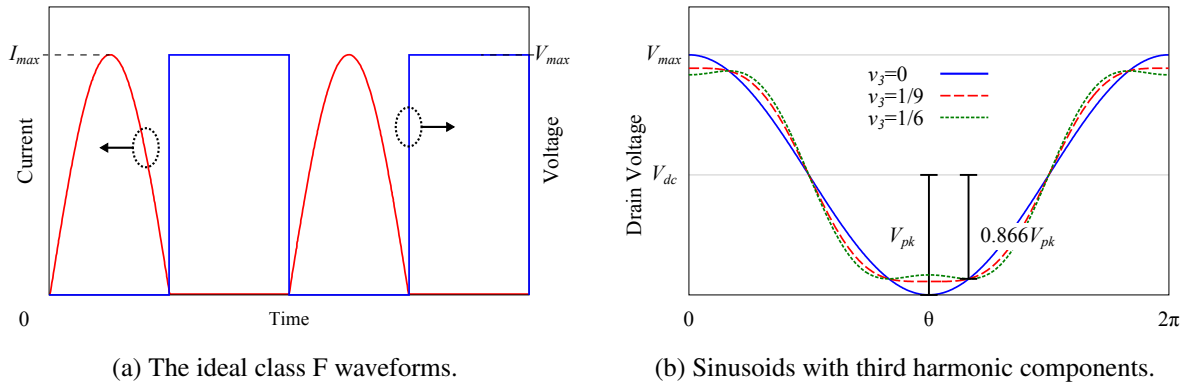
Figure 2.12: The class F waveform analysis.

wave voltage can further improve efficiency, Figure 2.12b illustrates the change in peak-to-peak amplitude of a sinusoidal voltage waveform as we add out-of-phase third harmonic component. The voltage waveforms are describe by

$$V(\theta) = V_1 \cos(\theta) - V_3 \cos(3\theta) \tag{2.14}$$

An increase in the normalized third harmonic component v_3 given by

$$v_3 = \frac{V_3}{V_1} \tag{2.15}$$

reduces the time domain peak-to-peak voltage without affecting the amplitude of the fundamental component. The maximally flat waveform occurs when $v_3 = 1/9$ while the waveform with the minimal peak-to-peak voltage occurs when $v_3 = 1/6$. If the latter waveform is scaled to swing from zero to V_{max}, the fundamental component will scale equally, in this case, by 1/0.866, or 1.155 times. Because the DC component remains constant, the higher fundamental component increases the drain efficiency to 90.7%, or 1.155 times the class B efficiency. Similarly, by injecting a fifth harmonic V_5 and seventh harmonic V_7, the efficiency and output power can be further improved. The optimal harmonic components that maximize the fundamental when considering finite harmonic terminations are given in Table 2.6 [1, 10]. The voltages are normalized to the class B voltage. With infinite odd harmonic terminations, ideal class F waveforms achieve 1.05 dB higher output power than class B and 100% efficiency.

In contrast, class F^{-1}, which is a dual of class F, has a half-wave rectified sine-wave voltage and a square wave current as shown in Figure 2.13a. The classical class F^{-1} is biased in class A [11]. The square wave current, obtain via a square wave input, has a fundamental component 1.273 times higher than a sinusoidal current with the same swing. As such, a square wave

18

Table 2.6: The optimal voltage components maximizing V_1 for m odd order terminations [1].

m	V_1	V_3	V_5	V_7	Normalized P_{out} (dB)	η (%)
1	1	-	-	-	0	78.5
2	1.155	0.1925	-	-	0.625	90.7
3	1.207	0.2807	0.073	-	0.82	94.8
4	1.231	0.3265	0.123	0.0359	0.90	96.7
∞	1.273	...	...	...	1.05	100

(a) The ideal class F^{-1} waveforms.

(b) Sinusoids with even harmonic components.
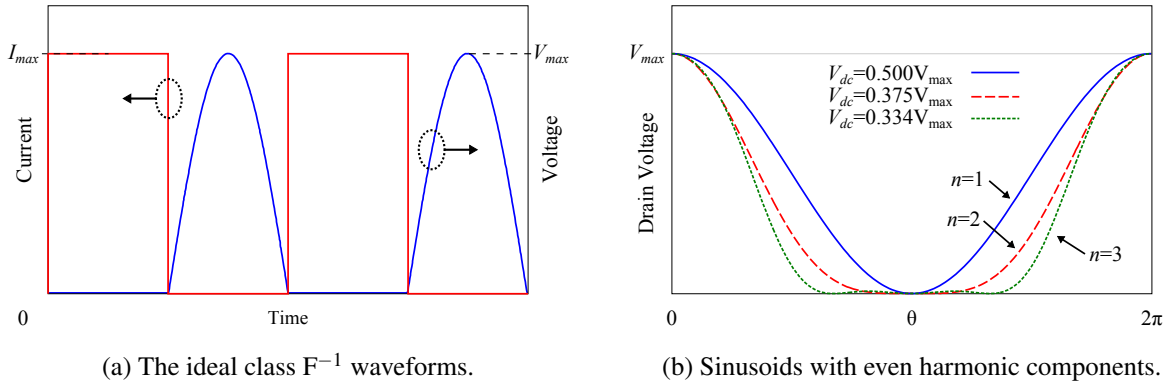
Figure 2.13: The class F^{-1} waveform analysis.

driven class A has 1.05 dB higher output power than conventional class A and an efficiency of 63.6%. The efficiency is increased further by shaping the drain voltage to contain even harmonics as given by (2.16).

$$V(\theta) = V_{dc} + V_1 \cos(\theta) + V_2 \cos(2\theta) - V_4 \cos(4\theta) \ldots \qquad (2.16)$$

Unlike class F, which improves efficiency by increasing the fundamental voltage component, class F^{-1} does so by reducing the DC voltage component as shown in Figure 2.13b. The optimal harmonic contents, normalized by V_{max}, that minimize the V_{dc} are outlined in Table 2.7 for various even order terminations considered. With infinite harmonics, perfect half-rectified sine wave is achieved. Because of the lower DC bias voltage, class F^{-1} is useful for applications with low drain bias and high device breakdown voltage.

2.4.5 Class F and F^{-1} Amplifier Realization using the Ideal FET

From the previous analyses, a square wave in conjunction with a half-wave rectified sine-wave result in a highly efficient amplifier operation. In this section, these waveforms are synthesized

Table 2.7: The optimal voltage components minimizing V_{dc} for k even order terminations.

k	V_{dc}	V_1	V_2	V_4	Normalized P_{out} (dB)	η (%)
1	0.5	0.5	-	-	1.05	63.6
2	0.375	0.5	0.125	-	1.05	84.8
3	0.334	0.5	0.193	0.026	1.05	95.4
∞	0.318	0.5	...	...	1.05	100

via the nonlinearity mechanism of the ideal FET. The analyses will show the knee region as the key mechanism that creates the needed harmonic current for shaping the voltage. Moreover, we show that despite the waveform similarities, the classical class F and F^{-1} modes have very different transfer characteristics. For simplicity, we only consider a limited number of harmonic terminations although the method can be generalized to include higher harmonics.

A starting point for synthesizing the class F waveforms is class B because they both have half-wave rectified sine-wave current. However, because the half-wave rectified sine-wave current does not contain odd harmonic components, the third harmonic voltage cannot be synthesized from the harmonic current and impedance product. One solution proposed in the literature is to bias the amplifier in class AB [12] which has the desired out-of-phase third harmonic current as illustrated in Figure 2.7. However, the theoretical class AB bias has a nonlinear transfer characteristic and the deviation from the half-wave rectified sine-wave current degrades the amplifier efficiency.

A better alternative, one that ultimately preserves the half-wave rectified sine-wave current, makes use of the odd harmonics in the distorted current waveform when the drain voltage dips below knee voltage V_k. This process of transforming the class B waveforms into class F using the knee region nonlinearity is illustrated in steps in Figure 2.14. To ensure the drain voltage enters the knee region, the class F amplifier has a higher fundamental impedance, given by

$$R_{opt}(\text{class F}) = \kappa R_{opt}{}' \tag{2.17}$$

where $R_{opt}{}'$ is given by (2.12) and κ corresponds to the V_1 column in Table 2.6 for the number of odd order terminations considered. In the present analysis, $m = 2$ and $\kappa = 1.115$ are assumed. By increasing the fundamental impedance Z_1 as given by (2.17), the class B voltage of the ideal FET with $V_k = 0.2V_{dd}$, shown in Figure 2.14a, enters the knee region and causes distortion in the current waveform as shown in Figure 2.14b. The distorted current contains the out-of-phase third harmonic current needed for the voltage shaping. Next, the third harmonic voltage is synthesized by increasing the third harmonic impedance Z_3. As the voltage waveform flattens, less of it dips below the knee voltage V_k and consequently, the current distortion eases as illustrated in Figure 2.14c. The relationship between the third harmonic voltage and current can be modelled as a negative feedback, whereby attempts to increase the third harmonic voltage by scaling Z_3 are

(a) The ideal linear class B waveforms with $V_k = 0.2V_{dd}$.

(b) The distorted current with $Z_1 = 1.155R_{opt}'$, $Z_3 = 0$.

(c) The current distortion eases with increasing Z_3.

(d) The fully restored current with $Z_3 = \infty$ and restored linearity.
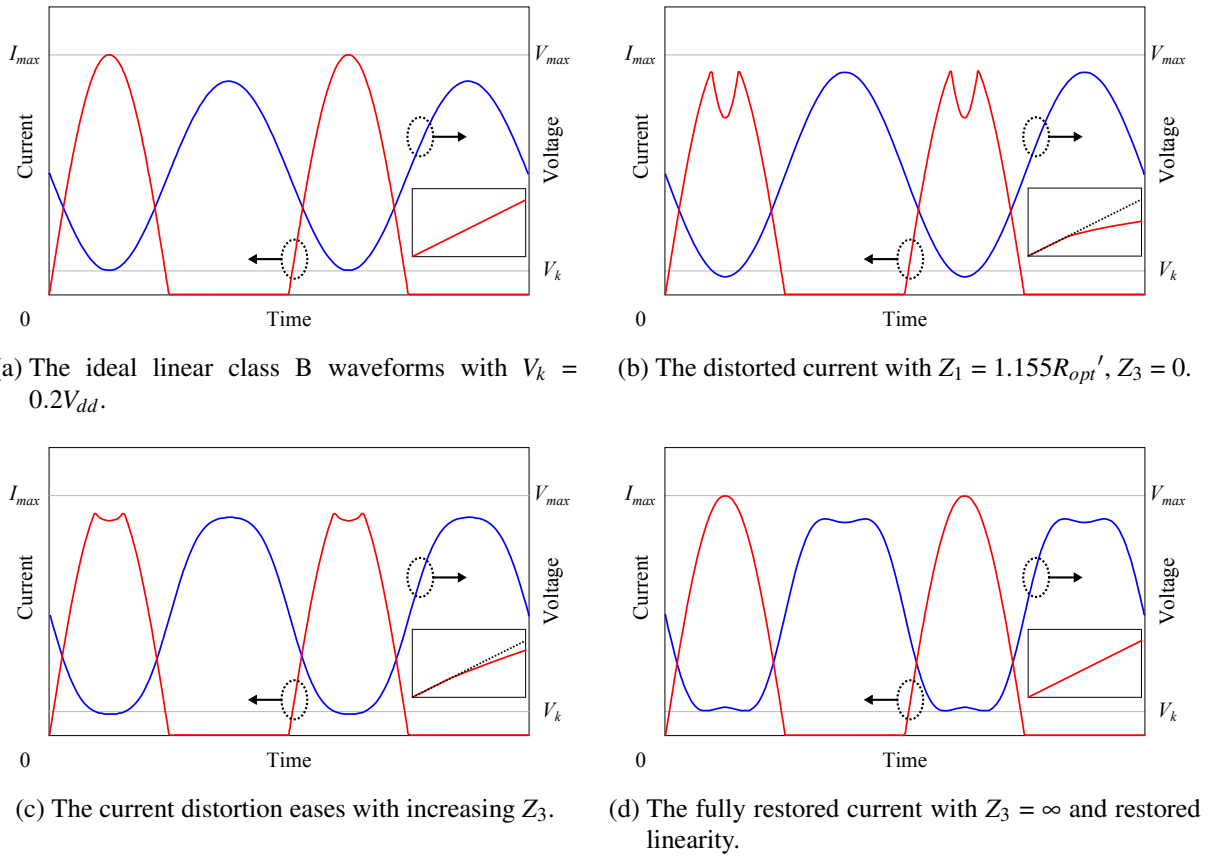
Figure 2.14: An illustration of the class B to class F transformation.

eventually limited by the reduced third harmonic current available because the current waveform becomes less distorted. In the limit where $Z_3 = \infty$, the current waveform is fully restored to a half-wave rectified sine-wave because the voltage no longer drops below the knee voltage V_k as shown in Figure 2.14d.

Despite having waveforms that are rich in harmonics, the class F amplifier has a linear transfer characteristic. This linearity exists because the current waveform is undistorted at all drive levels. As the lower right boxes of the sub-figures in Figure 2.14 illustrate, distortion in the current waveform results in compression in the transfer characteristic.

Table 2.8 compares the characteristics of class F in Figure 2.14d to the class B results derived earlier in Section 2.4.3. Given the same knee voltage, class F outperforms class B without compromising the linearity. From Table 2.8, the class F efficiency and output power approach that of class B with zero knee voltage.

To summarize, the class B to class F transformation is achieved by manipulating the impedance

Table 2.8: A comparison of class F and class B characteristics.

Class	V_k	R_{opt} calculation	Normalized P_{out}	Efficiency	Transfer characteristic
Class B	0	(2.6)	1.00	78.5%	linear
Class B	$0.2V_{dd}$	(2.12)	0.80	62.0%	linear
Class F	$0.2V_{dd}$	(2.17)	0.92	72.6%	linear

environment. For designs considering higher harmonics, the required odd and even harmonic terminations are given in (2.18) and (2.19).

$$Z_n(\text{class F}) = \infty, \quad n = 3, 5, 7 \dots \tag{2.18}$$

$$Z_n(\text{class F}) = 0, \quad n = 2, 4, 6 \dots \tag{2.19}$$

The synthesis of the classical class F^{-1} waveforms, on the other hand, can only be approximated. For an ideal square wave current and a knee voltage V_k, the optimal fundamental impedance is given by

$$R_{opt}(\text{class F}^{-1}) = \frac{\pi}{4} \frac{(V_{max} - V_k)}{I_{max}} \tag{2.20}$$

and the drain bias V_{dd} is given by

$$V_{dd} = \lambda(V_{max} - V_k) + V_k \tag{2.21}$$

where λ refers to the V_0 column in Table 2.7 for the order of even harmonic terminations considered. In the present analysis, $k = 2$ and $\lambda = 0.375$ are assumed.

Ideally, the square wave drain current is obtained with a square wave input voltage. However, for high power amplifiers, lack of broadband drivers limit the input to single tone sinusoids. To approximate the square wave current, we introduce the overdriven class A amplifier [13, 14]. Figure 2.15 shows an amplifier biased in class A that is driven with a large input voltage that partially enters the cutoff and saturation region as shown in Figure 2.15a. This arrangement creates a square-like drain current as shown in Figure 2.15b. The finite rise and fall time, controlled via the overdrive level, reduces the fundamental current component when compared to an ideal square wave and needs to be accounted for when employing (2.20) and (2.21).

The lack of even harmonics in the square wave current required for the drain voltage shaping can again be synthesized via the knee region nonlinearity. Although the $\pi/4$ term in (2.20) seems
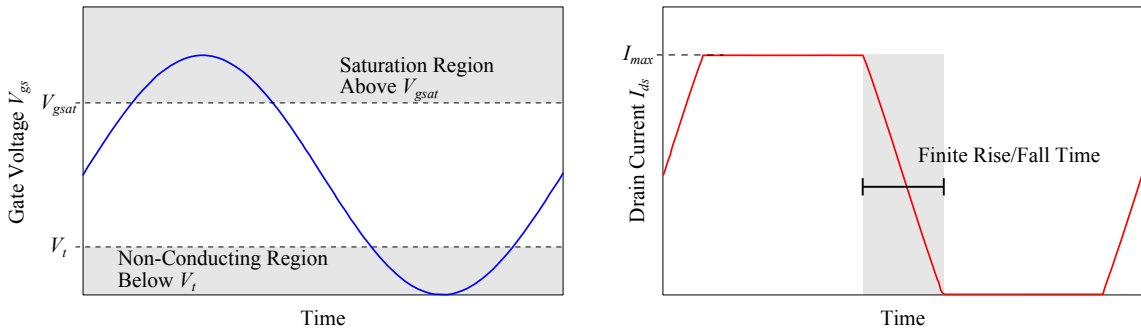
(a) The input voltage entering the cut-off and saturation regions.

(b) The drain current approximating a square wave.

Figure 2.15: The overdriven class A waveforms.

Table 2.9: class F and F^{-1} waveforms synthesized using the ideal FET with $V_k = 0$.

Class	Normalized P_{out} (dB)	Harmonic control	Efficiency	Transfer characteristic
B	0	all short	78.5%	linear
F	0.625	3rd open	90.7%	linear
F^{-1}	0.849	2nd open	81.1%	compression

to decrease the impedance, because V_{dc} is also reduced in (2.21), (2.20) is large compared to the associated load line impedance.

Similar to the class B to class F transformation, by applying a large second harmonic impedance, the current distortion caused by the knee region intrusion can be eliminated and the voltage is shaped to approximate a half-wave rectified sine-wave. The required harmonic terminations for class F^{-1} are given by

$$Z_n(\text{class F}^{-1}) = 0, \quad n = 3, 5, 7 \ldots \tag{2.22}$$

$$Z_n(\text{class F}^{-1}) = \infty, \quad n = 2, 4, 6 \ldots \tag{2.23}$$

Based on the techniques described in this section, the class F and F^{-1} waveforms are synthesized using the ideal FET with $V_k = 0$ and plotted in Figure 2.16. The performances are summarized in Table 2.9. For class F, the results are identical to those predicted by the theory for $m = 2$. However, for class F^{-1}, the pseudo square wave current degrades the efficiency when compared to the theory for $k = 2$. Moreover, because the approximation is only valid at high drive level, class F^{-1} is not linear. The load lines for class F and F^{-1} are plotted in Figure 2.17.

(a) The synthesized class F waveforms.

(b) The synthesized class F^{-1} waveforms.
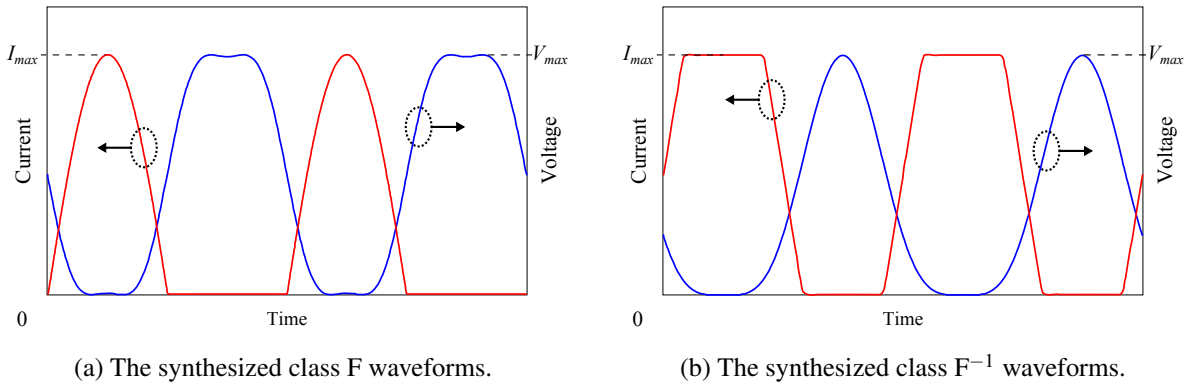
Figure 2.16: The class F and F^{-1} waveforms synthesized using the ideal FET.
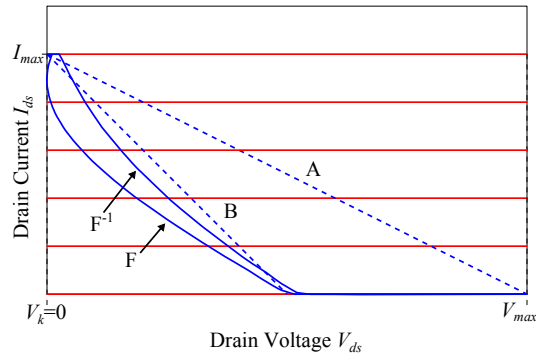
Figure 2.17: The class F and F^{-1} load lines.

The efficiency versus output power characteristics of class F and F^{-1}, normalized by the peak power, are plotted in Figure 2.18a. At reduced drive levels, class F degenerates into class B while class F^{-1} degenerates into class A. The transfer characteristics of class F and F^{-1} are shown in Figure 2.18b. The characteristic of class F is suitable for wireless signals with a high PAPR whereas the class F^{-1} amplifier is most suitable for constant amplitude signals because of the compression at high power and a poor back-off efficiency.

2.5   Power Amplifier Design

The power amplifier theory presented previously focused on the device bias and impedance environment that enable a highly efficient amplifier operation. In the subsequent sections, we discuss the challenges of applying these concepts in practical power amplifier design. Figure 2.19 illustrates the major components of a practical RF power amplifier. The ideal FET is replaced with

(a) The efficiency versus output power.

(b) The class F and F^{-1} transfer characteristics.
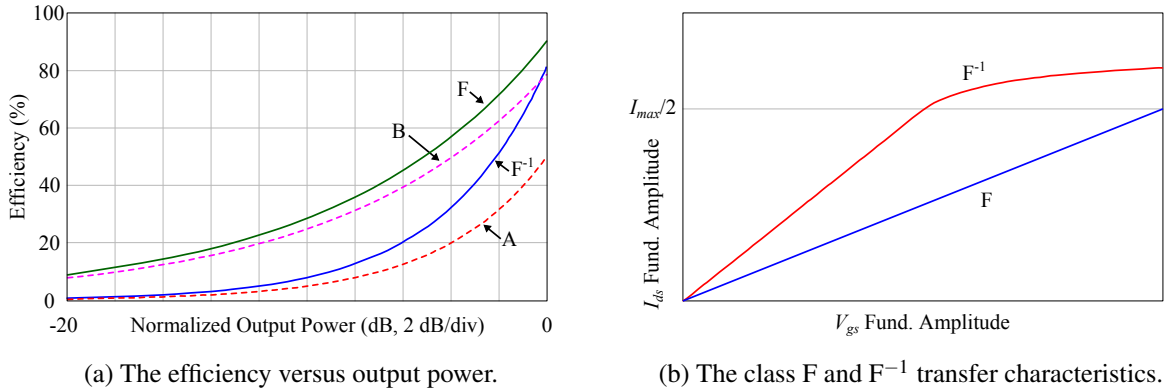
Figure 2.18: The class F and F^{-1} back-off and transfer characteristics.

a real device with parasitic and nonlinear transfer characteristics. In Section 2.5.1, we briefly discuss the market dominant laterally diffused metal oxide semiconductor (LDMOS) technology as well as the emerging gallium nitride (GaN) technology. In Section 2.5.2, we highlight the design complexity introduced by the presence of the device package and parasitic that shifts the reference plane from the intrinsic gate and drain to the package reference plane as shown in Figure 2.19.

Similar to other RF components, an RF power amplifier operates in a 50 Ω environment that requires an output matching network to transform the 50 Ω termination down to the optimal load impedance R_{opt} which is typically only a few ohms for high power devices. Similarly, the low input impedance requires matching to 50 Ω to maximize the amplifier gain. Therefore, the typical base station power amplifier is a hybrid circuit that consists of a packaged device and input and output matching networks fabricated on a high frequency substrate. The design of a multi-harmonic matching network is introduced in Section 2.5.5 which also discusses techniques to minimize the matching network insertion loss as well as a brief discussion on DC bias network design and stabilization techniques.

2.5.1 Device Technology: LDMOS vs. GaN

In this section, we analyze and compare two commercially available 45 W LDMOS and GaN devices using their respective large signal models. Unlike devices in integrated circuits, the base station device technologies are optimized for high output power, linearity, efficiency and ease of impedance matching.

Presently, LDMOS technology is the dominant technology in the base station amplifier market because of its low cost and high breakdown voltage. However, the emerging wide band-gap GaN high electron mobility transistor (HEMT) has even higher breakdown voltage that allows for
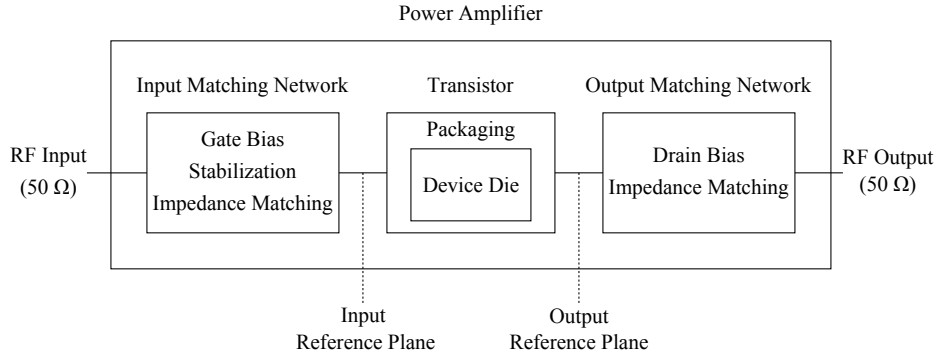
Figure 2.19: The key components of an RF power amplifier in practice.

Table 2.10: The device parameters of commercially available 45 W LDMOS and GaN devices.

Technology	f_t	I_{sat}	V_k	V_{br}	V_k/V_{br}	C_{iss}	C_{oss}
LDMOS	~10 GHz	14.5 A	4.5 V	~66 V	0.07	77 pF	27 pF
GaN	~20 GHz	11.4 A	6 V	~150 V	0.04	17.0 pF	3.5 pF

very high power density and small device parasitic. For a quick comparison, Table 2.10 outlines the device parameters of the 45 W MRF6S9045 LDMOS transistor from Freescale Semiconductor Inc. and the 45 W CGH60060D GaN transistor from Cree Inc.

The transition frequency f_t refers to the frequency at which the device current gain is equal to one. In base station amplifiers, the usable frequency is much less than f_t because the harmonics need to be taken into account in the typical reduced conduction angle bias such as class AB and class B. The device breakdown voltage V_{br} (also known as V_{max}) and the saturation current I_{sat} (also known as I_{max}) determine the maximum output power capability of the device. Moreover, because the optimal impedance R_{opt} is proportional to the ratio of the V_{br} and I_{sat}, the two parameters also dictate the ease of impedance matching to a 50 Ω termination.

For the two technologies, the saturation current I_{sat} can be increased by scaling the device, whereas the breakdown voltage V_{br} is a fixed technology parameter. In the 45 W GaN device, the breakdown voltage is more than two times that of the 45 W LDMOS device. Therefore, the GaN device achieves higher output power and matching impedance R_{opt} given the same saturation current. Moreover, because GaN has a lower V_k to V_{br} ratio, the efficiency degradation due to the knee region is less in GaN than in LDMOS. Finally, the high power density of GaN enables smaller device total input and output parasitic capacitances C_{iss} and C_{oss} respectively, thus enabling easier broadband impedance matching. However, GaN is currently several times more expensive than LDMOS and its performance can be limited by thermal dissipation because of its small footprint and high power density [2].
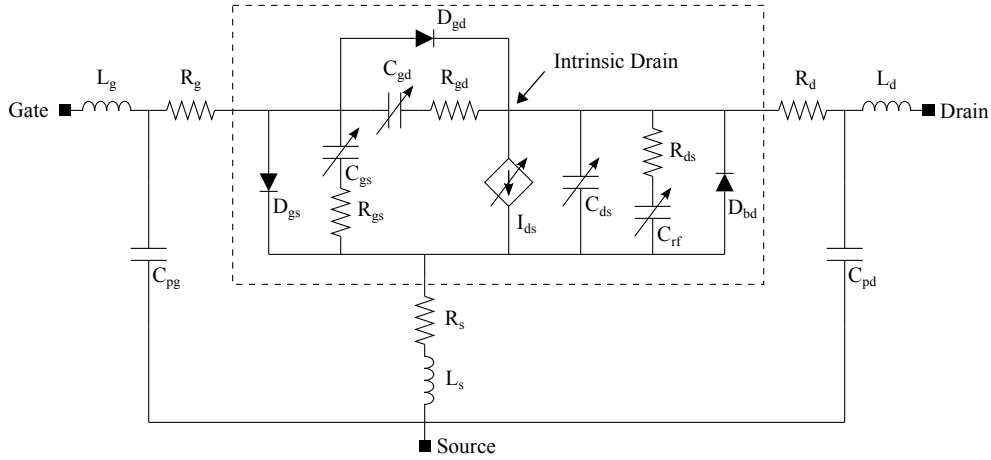
Figure 2.20: A generic large signal model [2].

To gain further insights without resorting to device physics, the devices are studied using their respective large signal models provided by the device foundries. Figure 2.20 illustrates a generic large signal FET model suitable for modelling the LDMOS and GaN device die. When compared to the ideal FET, the generic large signal model is significantly more complex with its intrinsic drain surrounded by many parasitic elements. The model parameters can be extracted using the cold-FET technique [15–20]. While the resistive parasitic incurs unavoidable performance degradation, the reactive parasitic can be removed by resonance, albeit only across a limited frequency range.

The parasitic can be categorized into intrinsic and extrinsic elements. The intrinsic elements, which are enclosed by dotted lines in Figure 2.20, are nonlinear functions of the device bias and terminal voltages, whereas the extrinsic elements are bias independent physical parasitic. The diodes model the forward gate conduction and device breakdown. For power amplifier designers, the parameters of interest are the nonlinear current source and the nonlinear input and output capacitances. The former affects the amplifier linearity, whereas the latter can generate unwanted harmonic currents that complicate the matching network design.

To illustrate the nonlinearity of current source in each technology, Figures 2.21a and 2.21b plot the simulated transfer characteristics of the 45 W LDMOS and GaN devices respectively. Both technologies deviate similarly from the ideal linear transfer characteristic indicated by the dotted lines. The current exhibits a slow turn on then expands quickly, followed by a gradual compression near I_{sat}, though the effect appears to be less severe in GaN. Empirical studies showed that the effect of the expansion can be mitigated by biasing the device in class AB which compresses, thus obtaining a linearity "sweep spot" [21]. Therefore, practical amplifiers are biased in deep class AB instead of class B. The isothermal DC-IV curves of Figures 2.22a and 2.22b show GaN to exhibit less I_{ds} dependence on V_{ds} above the knee region.

27
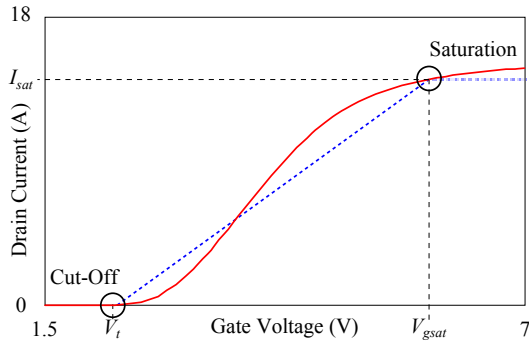
(a) The I_{ds} vs. V_{gs} transfer characteristic of LDMOS.
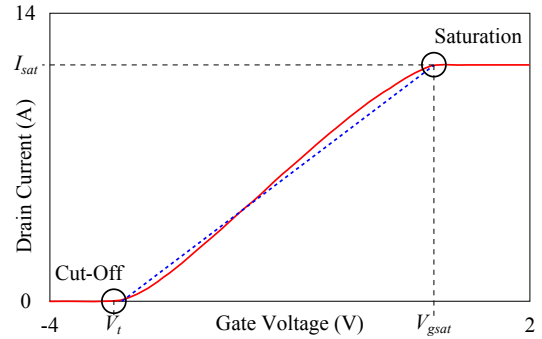
(b) The I_{ds} vs. V_{gs} transfer characteristic of GaN.

Figure 2.21: The transfer characteristics of the 45 W LDMOS and GaN devices.
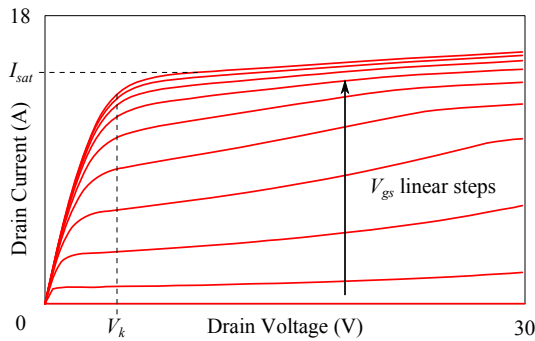
(a) The DC-IV characteristics of LDMOS.
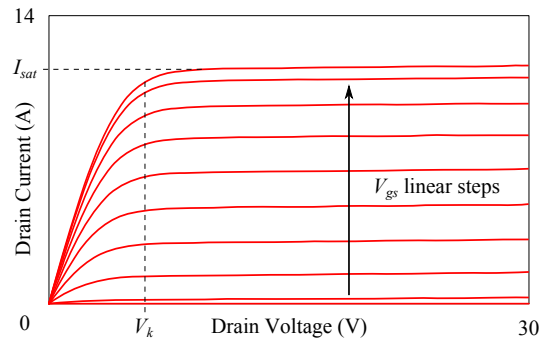
(b) The DC-IV characteristics of GaN.

Figure 2.22: The DC-IV characteristics of the 45 W LDMOS and GaN devices.

The nonlinear capacitances are of interest to designers because the generated harmonic current can distort the gate and drain waveforms. Moreover, they complicate the matching network design because a varying capacitance cannot be perfectly resonated out. To determine the input capacitance nonlinearity of the LDMOS and GaN devices, their respective small signal capacitances are extracted in simulation at multiple gate biases and plotted in Figures 2.23a and 2.23b. The gate voltage sweep corresponds to a class B drive up. In both technologies, the capacitance varies sharply around the threshold voltage V_t with a more abrupt change in GaN than in LDMOS. Despite having a smaller capacitance, the capacitance variation is larger in GaN, thus GaN devices generate more input harmonic content. If the input harmonic terminations are not explicitly controlled, the harmonic current can modify the gate voltage waveform and subsequently affect the drain current. A simple but suboptimal solution is to bias the device in class AB or

28
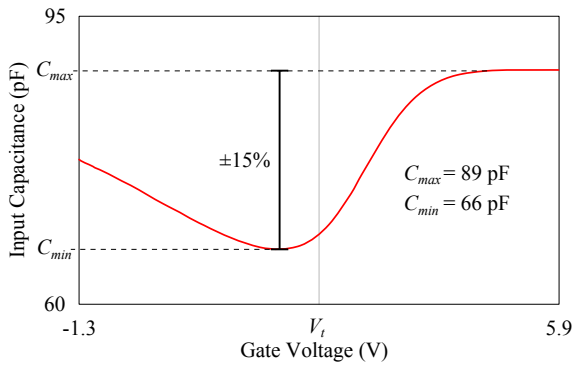
(a) The nonlinear input capacitance of LDMOS.
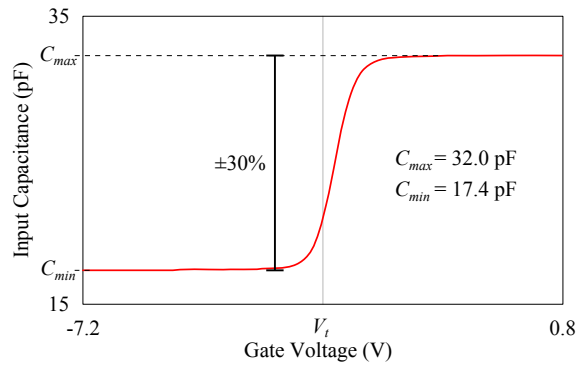
(b) The nonlinear input capacitance of GaN.

Figure 2.23: The input capacitance nonlinearity of the 45 W LDMOS and GaN devices.
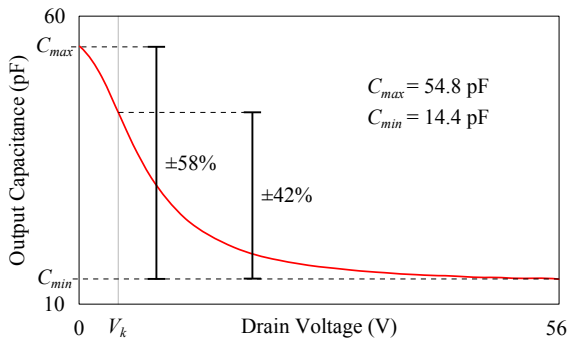
(a) The nonlinear output capacitance of LDMOS.
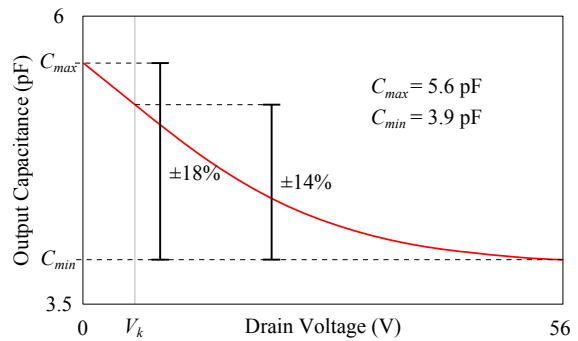
(b) The nonlinear output capacitance of GaN.

Figure 2.24: The output capacitance nonlinearity of the 45 W LDMOS and GaN devices.

class A and reduce the amount of capacitance variation. However, to fully eliminate the effect of the nonlinear input capacitance, the input matching network needs to present a short impedance at all the harmonic frequencies.

Similarly, the output capacitance nonlinearity of the LDMOS and GaN devices are extracted and plotted in Figures 2.24a and 2.24b respectively. In contrast to the input capacitance nonlinearity, LDMOS exhibits a much stronger output capacitance nonlinearity than GaN. The variation can be reduced by avoiding a voltage swing below the knee region which also helps achieve good linearity. Moreover, because the output harmonic terminations are already being controlled to improve the amplifier efficiency, the harmonic current generated by the nonlinear capacitor can be mitigated without additional circuitry.

To summarize, although LDMOS and GaN are both suitable technologies for base station power amplifier, they have different characteristics that can impact the amplifier design in differ-

29
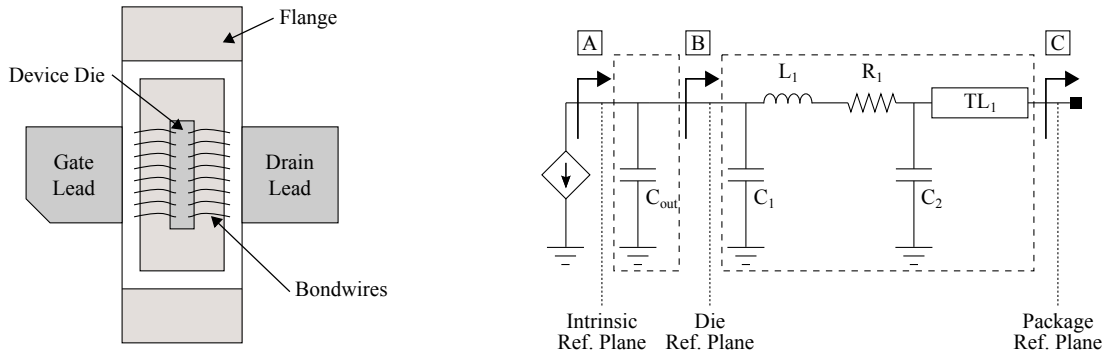
(a) A packaged, unmatched device with the top lid removed.

(b) The various output design reference planes.

Figure 2.25: A packaged device and the various design reference planes.

ent ways. LDMOS is superior in terms of cost and is a mature technology that has been widely deployed in the industry, while GaN is an emerging technology that offers a wider bandwidth, higher frequency of operation, and improved efficiency.

2.5.2 Device Package

Devices used in RF power amplifier are normally packaged to protect them from the environment and to aid thermal dissipation. Moreover, some designs pre-match the device within the package to ease the impedance matching over a narrow frequency range. However, to maximize the design flexibility, power amplifier research typically uses unmatched devices. Figure 2.25a shows a typical packaged, unmatched device with the top lid removed. The die is soldered onto a flange that has a very high thermal conductivity that also acts as an electrical ground for the source terminal. The gate and drain leads are connected to the device using bond-wires. The package can be modelled with lumped and distributive components as shown in Figure 2.26 with the device die modelled using Figure 2.20. The largest parasitic are L_1 and TL_1 that model the bond-wires and the package bond-pad respectively. Therefore, when compared to a bare die device, the packaged device has a narrower matching bandwidth and more frequency dispersive effects.

Because the impedance transformation caused by the device and package parasitic needs to be accounted for in the matching network design, the reference plane of interest shifts from the intrinsic drain to the package reference plane. The various reference planes at the device output are illustrated in Figure 2.25b. For the ease of analysis, the device output parasitic is reduced to the output capacitance C_{out} and the feedback capacitor C_3 is ignored. The reference planes A, B, and C, denote the intrinsic drain, die, and package reference plane respectively.

30
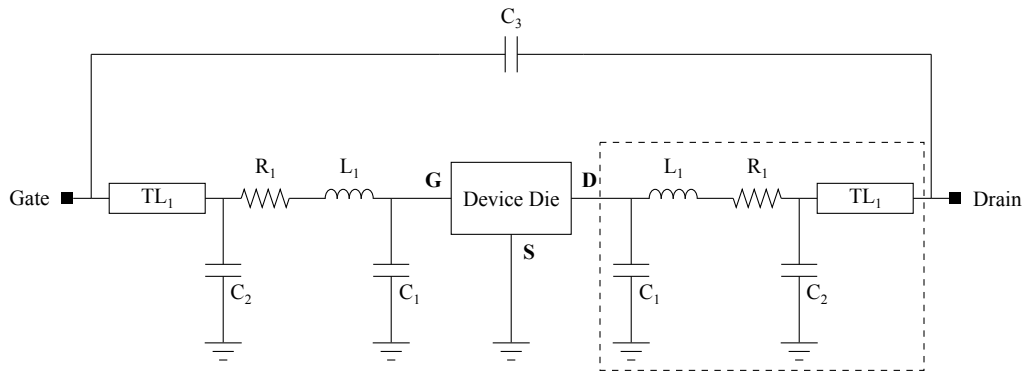
Figure 2.26: A typical device package model.
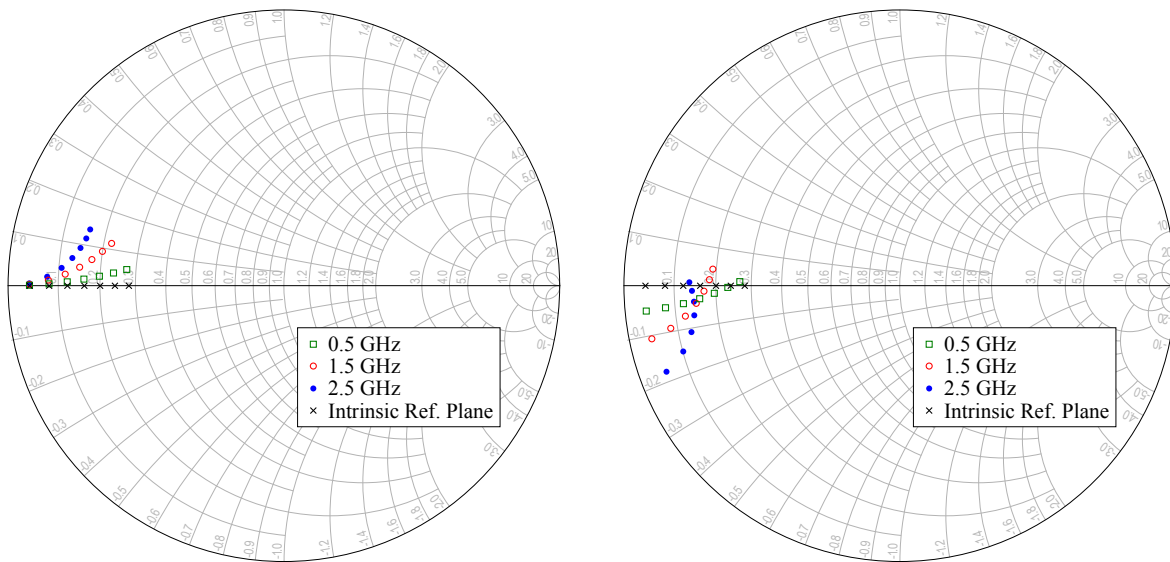
(a) The optimal load impedances at the die reference plane.

(b) The optimal load impedances at the package reference plane.

Figure 2.27: The optimal impedances at the intrinsic drain, die, and package reference planes.

For a given class of operation with a set of required fundamental and harmonic terminations at the intrinsic drain, we are interested in the matching requirements at the package reference plane. As an example, we illustrate the reference plane shift using the 45 W GaN device from Section 2.5.1 with $C_{out} = 4.0$ pF. The required impedances at the die reference plane B at 0.5, 1.5, and 2.5 GHz for intrinsic drain impedances of 2 to 14 Ω in 2 Ω steps are shown on the Smith chart in Figure 2.27a. From Figure 2.27a, the frequency independent impedances at the intrinsic drain become a function of frequency due to the capacitance C_{out}. At higher frequencies, the shifts are more severe, especially for higher intrinsic drain impedances. With the package information provided by the foundry, the required impedances at the package reference plane are calculated and illustrated in Figure 2.27b. With the package parasitic, the impedances rotate counter-clockwise versus increasing frequency. A similar analysis can also be applied at the harmonic frequencies to determine the harmonic impedances at the package reference plane.

2.5.3   Input Matching Requirements

So far, the optimal impedance analysis has been confined to the device output. In this section, we examine the input matching requirements. Although the input impedance presented to the device most notably affects the gain of the amplifier, it also affects other device characteristics such as the linearity and efficiency [22].

Input matching is needed because unlike the ideal FET, a real device has a frequency varying input impedance dictated by the device parasitic and package. At RF frequency, the magnitude of this complex impedance is very low. If the device is driven directly with an RF voltage V_s with a 50 Ω source resistance, the input voltage V_{in} at the device gate will only be a small fraction of V_s because of the voltage division between the 50 Ω source impedance and the device input impedance. In this configuration, very little drain current is produced which results in a poor amplifier gain. Although V_{in} can be increased by increasing the drive level V_s, the power dissipated across the 50 Ω source resistance is wasted. Therefore, this approach is rarely adopted in practice.

The solution is to maximize the device input voltage V_{in} for a given drive voltage V_s by placing a matching network between the RF source and the device input as shown in Figure 2.28. The device input is modelled with a resistance R_{in} in series with a capacitance C_{in}. R_{in} is primarily the gate resistance R_g, while C_{in} consists of the gate bond-pad capacitance C_{pg}, the device gate capacitance C_{gs}, and the Miller capacitance C_m given by

$$C_m = C_{gd}(1 + A_v) \tag{2.24}$$

where A_v is the amplifier voltage gain. At frequency f, the device input impedance is given by
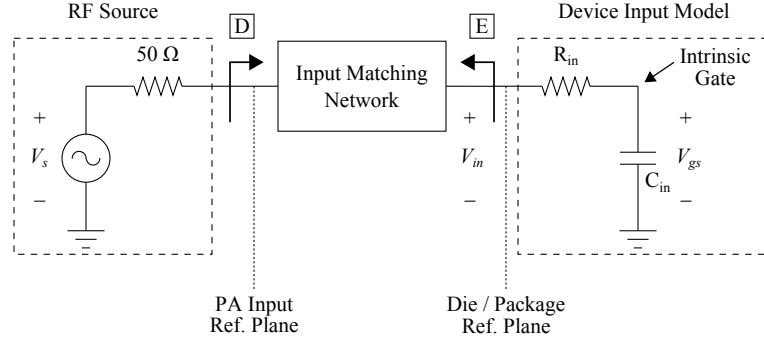
Figure 2.28: The input matching network between the RF source and the device.

$$Z_{in} = R_{in} + \frac{1}{j2\pi f C_{in}} = R_{in} - jX_{in} \tag{2.25}$$

The input voltage V_{in} is maximized when the device input is terminated with the conjugate of Z_{in} which can be obtained by transforming the 50 Ω source impedance to $R_{in} + jX_{in}$ at the reference plane E in Figure 2.28, or equivalently, by matching the Z_{in} to 50 Ω at the reference plane D. Assuming the matching network is lossless, the conjugate match maximizes the power transfer from the RF source to R_{in}. Under this condition, the power dissipated by R_{in} is equal to the power available from source P_{avs}, given by

$$P_{avs} = \frac{V_s^2}{8R_s} \tag{2.26}$$

where $R_s = 50 \Omega$. The minimum RF source power needed to obtain a given V_{in} is therefore equal to the power dissipated in R_{in} when the device gate is set to V_{in}. A low source power is desirable because it increases the amplifier power gain as given by

$$Gain = P_{out} - P_{avs} \tag{2.27}$$

Moreover, the power-added-efficiency (PAE) which accounts for the input drive level in the efficiency calculation is given as

$$PAE = \frac{P_{out} - P_{avs}}{P_{dc}} \tag{2.28}$$

As the frequency increases, $|Z_{in}|$ decreases as per (2.25), which results in a higher current through R_{in} for the same V_{in} at the reference plane E. Therefore, a higher source power P_{avs} is needed to achieve the same V_{in} at higher frequencies. As a result, high power gain and PAE are more difficult to obtain at higher frequencies.

33

Load-pull and source-pull at a given input drive, device bias, and frequency f_0
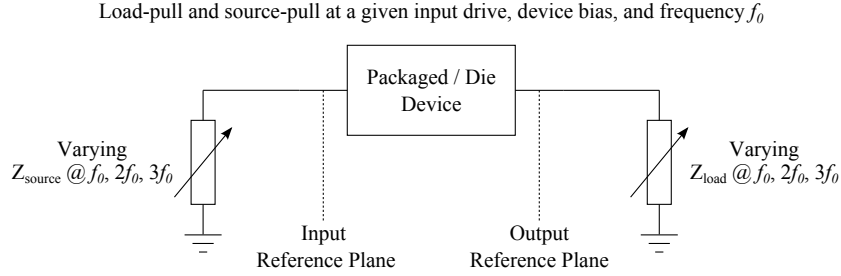
Figure 2.29: A simplified load and source pull setup.

Moreover, because the drain current is actually a function of the voltage V_{gs} across C_{in}, at higher frequencies, a larger V_{in} is needed to counter the voltage division between R_{in} and C_{in}. Devices with a smaller input capacitance such as GaN can therefore achieve higher gain and PAE at higher frequencies than LDMOS. However, because GaN devices have a nonlinear input capacitance, the input harmonic terminations should present a short to keep the input voltage waveform purely sinusoidal [23–28].

2.5.4   Load-pull and Source-pull

Although the power amplifier theory shows that the intrinsic gate and drain waveforms are critical to understanding the amplifier operation as well as the matching network design, in practice, designers rarely have access to the intrinsic waveforms because the device parasitic and package are considered proprietary properties of the foundry. Reverse engineering a packaged device is generally very difficult. In light of the lack of access, an empirical technique known as impedance pulling can be applied at the device output (i.e. load-pull) and the input (i.e. source-pull).

In a load-pull or source-pull, the fundamental and harmonic impedances at the die or package reference plane are arbitrarily swept until the amplifier exhibits the desired gain, efficiency, and output power under a given input drive level, frequency and bias condition. A simplified load pull setup is shown in Figure 2.29.

Load-pull and source-pull can be applied to large signal models in simulation or to real devices using impedance tuners. The results are shown as efficiency and output power contours on the Smith chart. As an example, Figure 2.30 illustrates the fundamental load-pull simulation of a 120 W GaN device at 700 MHz. The impedance that yields the peak efficiency is found at the center of the efficiency contours. Each contour represents a fixed percentage drop in efficiency. Similar concept applies to the output power contours. The non-overlap of the peak efficiency and peak power impedance can be explained by the device knee region. The contours are non-circular because of the voltage and current limits when the device is presented with a non-resistive termination [29].
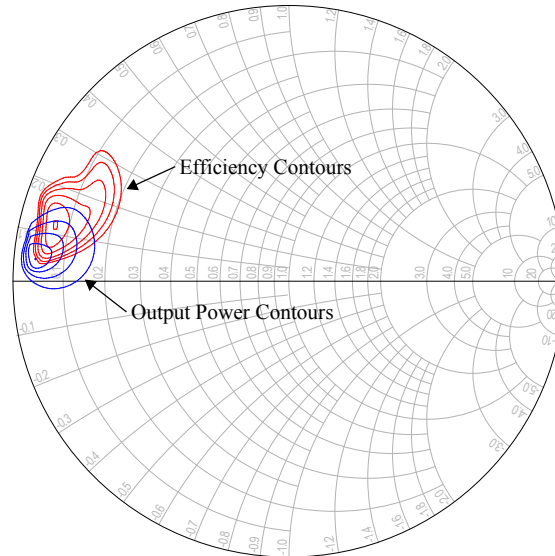
Figure 2.30: The simulated fundamental load-pull contours of a 120 W GaN device at 700 MHz.

Despite being widely adopted in the industry, load-pull and source-pull have several key disadvantages. First, without knowing the intrinsic waveforms, the class of operation cannot be determined. Therefore, the amplifier linearity cannot be known without additional measurements. Moreover, the optimal impedances from load-pull may be those that cause the drain voltage to exceed the breakdown voltage, thus compromising the device reliability. Second, a design based on load-pull cannot provide insights into how subsequent designs may be improved. Therefore, ideally, the load-pull design technique should only be adopted if the intrinsic gate and drain waveforms are not available.

2.5.5 Matching Network Design

Once the required impedances at the design reference plane are known, a matching network is designed to synthesize the impedances from the 50 Ω termination. The theory of single frequency impedance matching using lumped elements and transmission lines is well covered in recent text [30, 31]. In the design of matching networks, there are primarily two mechanisms that can degrade the amplifier output power and efficiency. The first is the loss due to low qualify-factor (Q) lumped components, substrate dielectric and conduction loss, and radiation loss. The second is the impedance mismatch that occurs when the matching network impedances differ from those required by the device. The former can be characterized using the network insertion loss (IL) as defined by

Table 2.11: The effects of the output network insertion loss on the amplifier efficiency and output power.

Insertion Loss (dB)	normalized P_{out} and η	Class B η (%)
0	1.00	78.5
0.2	0.95	74.6
0.5	0.89	69.9
1	0.79	62.0
3	0.50	39.3

$$IL = -10\log\frac{S_{21}{}^2}{1 - S_{11}^2} \tag{2.29}$$

where S_{21} and S_{11} are the two port S-parameter of the matching network at the frequency of interest. Table 2.11 outlines the effect of different insertion losses on the amplifier efficiency and output power. In base station amplifiers, the insertion loss is typically kept below 0.2 dB. To minimize the insertion loss, matching network are designed using transmission lines (TL) and high-Q capacitors on a low loss substrate. The radiation loss can be reduced by avoiding stubs close to short circuit [32]. Radiation loss can also be studied in an EM simulator using an ideal substrate.

On the other hand, the performance degradation due to an impedance mismatch is dependent on the amplifier sensitivity to the mismatch. The sensitivity can be determined via load-pull around the optimal impedance. If the amplifier performance varies greatly when the impedance deviates from the optimal value, then the matching network synthesis must be exact. Although EM simulations are highly accurate in theory, manufacturing tolerances and errors in the dielectric constant of the substrate can cause an unwanted impedance shift.

To illustrate how the impedance shift due to manufacturing tolerances may be minimized through design, we analyze the impedance sensitivity of an open circuited stub. The input admittance of an open circuited stub, which is typically used to synthesize the required matching network reactance, is given by

$$Y_{in} = jY_0\tan(\beta l) \tag{2.30}$$

where Y_0 is the characteristic admittance of the stub, βl is the electrical length of the stub, and l is the physical stub length. Taking the derivative of (2.30) with respect to βl yields (2.31). Isolating Y_0 in (2.30) and substituting it into (2.31) yields (2.32). From (2.32), the variation in Y_{in} is minimized when $\beta l = \pi/4$.
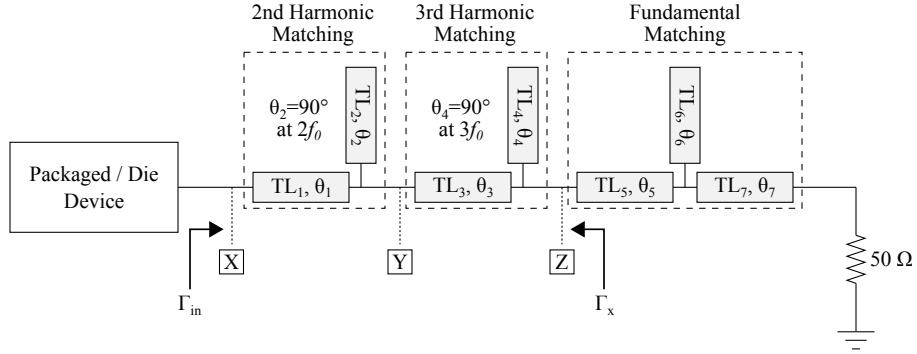
Figure 2.31: A multi-harmonic matching network with independent harmonic control.

$$\frac{dY_{in}}{d(\beta l)} = jY_0 \sec^2(\beta l) \tag{2.31}$$

$$\frac{dY_{in}}{d(\beta l)} = \frac{Y_{in}}{\sin(\beta l)\cos(\beta l)} \tag{2.32}$$

Therefore, using open circuited stubs with an electrical length of $\pi/4$ minimizes the impedance variation due to manufacturing errors in the stub length l. Equation (2.32) also shows that a large Y_{in} results in a high impedance variation when there are manufacturing errors. Therefore, a high power device with a very low R_{opt} requires a matching network that is inherently more difficult to fabricate accurately.

Multi-Harmonic Matching Network

To operate efficiently, an amplifier requires the harmonic impedances to be either a short or an open circuit at the intrinsic drain. Assuming the device and package parasitic are lossless, the short or open load at the intrinsic drain is transformed to a purely reactive impedance at the die or package reference plane. Figure 2.31 illustrates a matching topology that can independently control the fundamental, second harmonic and third harmonic impedances. Control beyond the third harmonic is rarely practiced because of an increased design complexity and diminished efficiency improvement.

In Figure 2.31, open circuited stubs are used instead of short circuited stub to avoid ground via holes that can be difficult to model. With a fundamental design frequency of f_0, the required impedances can be expressed using the reflection coefficient Γ_{in} as given by

$$\Gamma_{in}(f_0) = \Gamma_1 \angle \varphi_1 \tag{2.33a}$$

37

$$\Gamma_{in}(2f_0) = 1\angle\varphi_2 \qquad\qquad (2.33\text{b})$$

$$\Gamma_{in}(3f_0) = 1\angle\varphi_3 \qquad\qquad (2.33\text{c})$$

where Γ_1 is the magnitude of the fundamental reflection coefficient and φ_1, φ_2, and φ_3 are the phases of the reflection coefficient at the fundamental, second, and third harmonic respectively. Because the harmonic impedances are purely reactive, the harmonic reflection coefficients have a magnitude of one.

To synthesize the reflection coefficient given in (2.33), the transmission line impedance and length in Figure 2.31 are designed as follows. First, from the second harmonic matching between node X and Y, the open stub TL_2 with $\theta_2 = 90°$ at $2f_0$ creates a short circuit at node Y. This short circuit is in parallel with the rest of the circuit to the right of node Y, thus removing their effect at $2f_0$. The length θ_1 of TL_1 is increased until $\Gamma_{in}(2f_0) = 1\angle\varphi_2$. Next, the process is repeated for the third harmonic matching between node Y and Z. At $3f_0$, the second harmonic matching between node X and Y appears as a phase-shift that can be incorporated into the length θ_3 of TL_3 to yield $\Gamma_{in}(3f_0) = 1\angle\varphi_3$.

Finally, to match the fundamental impedance, the device is removed and node X is terminated with a load with a reflection coefficient $\Gamma_{in}{}^*(f_0) = \Gamma_1\angle\text{-}\varphi_1$. While in this configuration, the reflection coefficient Γ_x at node Z is determined. Using the single stub matching technique, a fundamental matching network is designed to match the 50 Ω termination to $\Gamma_x{}^*$. This last step completes the multi-harmonic matching network design. At node X, Γ_{in} now sees the required reflection coefficient at the fundamental and harmonic frequencies as given in (2.33).

For the multi-harmonic matching network, the impedance variation due to manufacturing tolerance is minimized as long as θ_6 is close to $45°$. The length θ_2 and θ_3 are $45°$ and $30°$ respectively at the fundamental frequency f_0. In addition, the network insertion loss is minimized because no open circuited stub is close to $90°$ at the fundamental frequency.

Bias Network

The device gate and drain are biased using DC voltage supplies fed through a DC bias network which consists of multiple decoupling capacitors that minimize the supply ripple. To prevent the RF signal from reaching the DC supply, an RF choke is placed between the bias network and the device. The RF choke can be a large inductor or a short circuited quarter-wave transmission line at the fundamental frequency. Both techniques present a high impedance to the matching network at the fundamental frequency, thus preventing it from loading the device. If the RF choke is implemented using a quarter-wave line, it can also function as a second harmonic stub because the impedance looking into the line is low at the second harmonic frequency. The bias network should also provide an adequate video bandwidth to improve the linearizability of the amplifier although a detailed discussion is beyond the scope of this thesis.

The RF input and output should be DC-decoupled to prevent the neighbouring stages from the seeing the bias voltage. Therefore, DC blocking capacitors are placed in series with the matching networks. The value of the blocking capacitors is chosen so that the capacitors behave as a short circuit at the fundamental frequency.

Stability

To prevent low frequency oscillations, the device stability is analyzed. Although in theory, the analysis should account for the large signal condition and the nonlinear device parameters, the conventional the K-Δ test and stability circles have been shown to be adequate in practical designs when large signal S-parameters are used. For the K-Δ test, the requirement for unconditional stability is given by

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{2.34}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2.35}$$

For an active device, the large signal S-parameter is a function of the frequency and drive level. Therefore, K and $|\Delta|$ are calculated from low frequencies up to the design frequency at different drive levels. To stabilize the amplifier, a resistance is added close to the device gate, typically at the bias line, to make the amplifier unconditionally stable at low frequencies. Stabilization resistor is only added at the device gate to minimize the impact on the RF performance. If the amplifier cannot be made unconditionally stable, stability circle analysis is applied to ensure the matching network impedances fall within the stable regions of the Smith chart.

2.6 Design and Validation: A 3.3 GHz 10 W GaN Amplifier

In this section, we outline the design of a 10 W high efficiency amplifier that won the first place award at the 2009 International Microwave Symposium student high efficiency power amplifier competition [33]. The design used a 10 W CGH40010F GaN device from Cree Inc. The device large signal model was used extensively to gather design insights that enabled a first pass design success.

The design objective was to achieve the highest efficiency at a design frequency f_0 of 3.3 GHz. The device was biased in deep class AB with a drain voltage of 28 V and a quiescent current of 200 mA. The RF source power P_{avs} was fixed at 25 dBm.
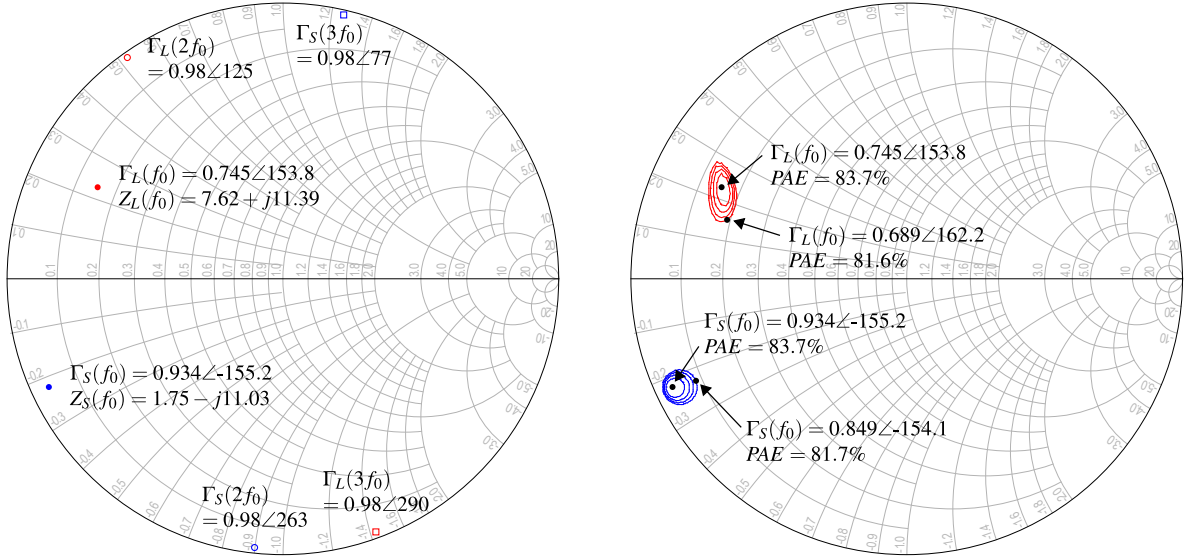
(a) The optimal Γ_S and Γ_L at f_0, $2f_0$, and $3f_0$.

(b) The efficiency sensitivity to $\Gamma_S(f_0)$ and $\Gamma_L(f_0)$ variation.

Figure 2.32: The optimal impedances and the PAE sensitivity to $\Gamma(f_0)$ variation.

Initially, we relied on load-pull and source-pull simulations to determine the optimal impedances because the device package and parasitic were not available. The optimal fundamental and harmonic source impedances expressed in terms of reflection coefficients $\Gamma_S(f_0)$, $\Gamma_S(2f_0)$, and $\Gamma_S(3f_0)$ and the corresponding optimal load impedances expressed using $\Gamma_L(f_0)$, $\Gamma_L(2f_0)$, and $\Gamma_L(3f_0)$ are plotted in Figure 2.32a.

As predicted by the theory, the optimal harmonic impedances are on the edge of the Smith chart. The load-pull and source-pull simulations in Figure 2.32b also show that the amplifier efficiency is not very sensitive to impedance variations at the fundamental frequency. The outer contours in Figure 2.32b represent a 2% efficiency drop from the peak efficiency. Using EM simulations, we ensured that the synthesized matching network impedances were within the top 2% efficiency regions.

On the other hand, efficiency sensitivity to harmonic impedance variations was studied in two stages. First, the phases of $\Gamma(2f_0)$ and $\Gamma(3f_0)$ were swept while their magnitudes were kept constant. Next, the phases were fixed at the optimal value while the magnitudes $|\Gamma(2f_0)|$ and $|\Gamma(3f_0)|$ were reduced. The efficiency sensitivity to the phase variation of $\Gamma(2f_0)$ and $\Gamma(3f_0)$ at the source and load is depicted in Figure 2.33a and Figure 2.33b respectively. Although the amplifier efficiency is not very sensitive to $\Gamma(3f_0)$ phase variation, the amplifier shows significant efficiency degradation caused by $\Gamma(2f_0)$ phase variation, especially at the device input.
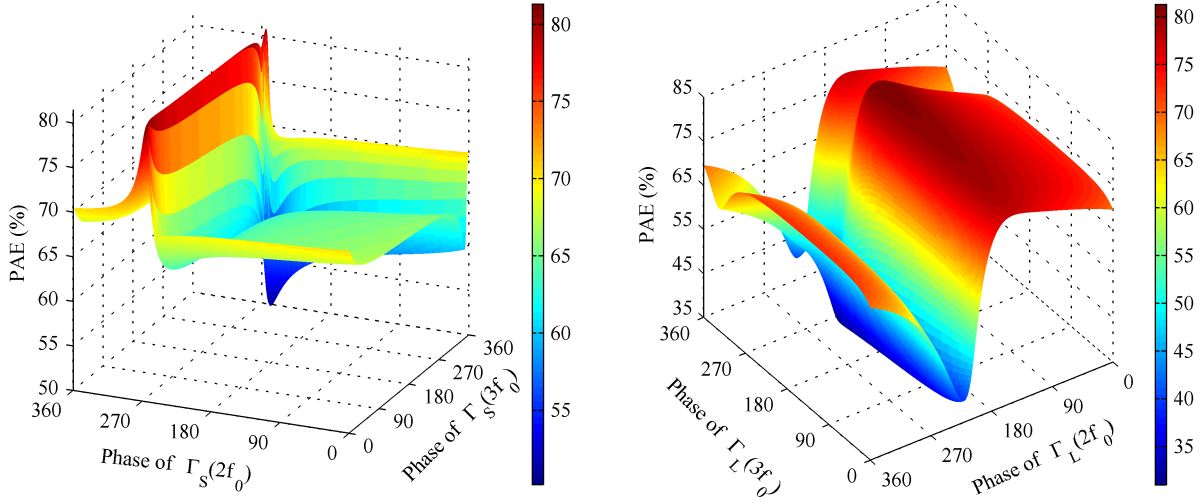
(a) The efficiency sensitivity to the phase variation of $\Gamma_S(2f_0)$ and $\Gamma_S(3f_0)$.

(b) The efficiency sensitivity to the phase variation of $\Gamma_L(2f_0)$ and $\Gamma_L(3f_0)$.

Figure 2.33: The efficiency sensitivity to the phase variation of $\Gamma(2f_0)$ and $\Gamma(3f_0)$.

Table 2.12: The efficiency sensitivity to the magnitude $|\Gamma(2f_0)|$ and $|\Gamma(3f_0)|$.

$|\Gamma|$	PAE, $\Gamma = \Gamma_S(2f_0)$	PAE, $\Gamma = \Gamma_S(3f_0)$	PAE, $\Gamma = \Gamma_L(2f_0)$	PAE, $\Gamma = \Gamma_L(3f_0)$
0.98	81.4 %	81.4 %	81.4 %	81.4 %
0.95	79.6 %	81.4 %	80.8 %	81.3 %
0.92	77.9 %	81.4 %	80.1 %	81.2 %
0.89	76.6 %	81.4 %	79.5 %	81.1 %

The efficiency sensitivity to the input second harmonic termination can be attributed to the nonlinear input capacitance of the GaN device that generates a large second harmonic current. To ensure the input voltage remains purely sinusoidal, the input second harmonic termination should present a short circuit. Unfortunately, from Figure 2.33a, the phase angle that yields the highest amplifier efficiency is only a few degrees away from the phase angle that yields the lowest efficiency. The phase error tolerance is very low because the impedance transformation by the gate capacitance and the device package makes the open and short circuit at intrinsic gate very close to each other at the package reference plane. To mitigate the sensitivity to the second harmonic phase, we design the input second harmonic termination phase not at its optimal value but slight offset towards the left side in Figure 2.33a so as to reduce the sensitivity while still achieving high efficiency.
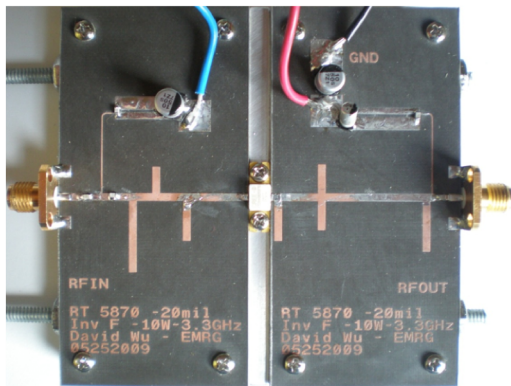
(a) A picture of the fabricated 10 W amplifier.
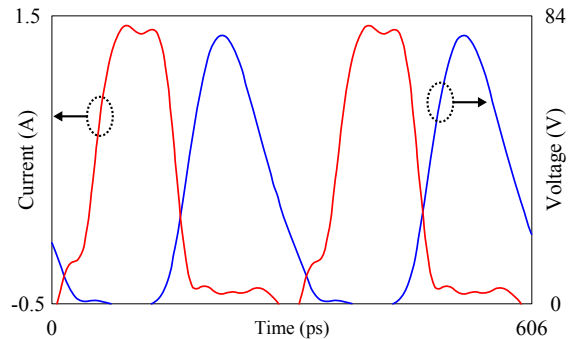
(b) The simulated intrinsic drain voltage and current waveforms.

Figure 2.34: A picture of the 10 W GaN high efficiency amplifier and the simulated intrinsic drain waveforms.

The efficiency sensitivity to a decrease in the magnitude $|\Gamma(2f_0)|$ and $|\Gamma(3f_0)|$ is outlined in Table 2.12, which shows that the efficiency is more sensitive to a reduction in $|\Gamma(2f_0)|$. To maximize $|\Gamma(2f_0)|$, the second harmonic is terminated before the third harmonic as shown in the multi-harmonic matching network in Figure 2.31. Following the design procedure presented in Section 2.5.5, multi-harmonic input and output matching networks were designed on a low loss Rogers 5870 substrate. A picture of the fabricated amplifier is shown in Figure 2.34a. Upon receiving the die and package information from Cree Inc., the intrinsic waveform were simulated and shown in Figure 2.34b. The waveforms resemble that of a class F^{-1} amplifier. A class F^{-1} amplifier biased in class B can be realizable based on the analyses in [34–36].

The simulated versus measured power added efficiency versus output power is shown in Figure 2.35a and the amplifier gain versus input power is shown in Figure 2.35b. The good agreement between the measurement and simulation highlights the accuracy of modern large signal models. With an output insertion loss of 0.2 dB, the peak power added efficiency measured 74% at a slightly shifted frequency of 3.27 GHz. The amplifier achieved 38.1 dBm of peak power and a peak power gain of 11 dB. From the gain versus input power characteristics, the amplifier is nonlinear and requires digital pre-distortion. Although the amplifier operates very efficiently at the peak power, it suffers from a very narrow bandwidth as shown in the power and efficiency versus frequency plots in Figures 2.36a and 2.36b. As such, the amplifier cannot satisfy the broadband requirement of a modern base station amplifier despite the high peak efficiency.

In summary, the analysis of the 10 W GaN device reveals that the nonlinear C_{gs} causes the amplifier efficiency to be very sensitive to the input second harmonic termination. A key contribution of this work is a matching network design that terminates the second harmonic first with a phase angle that reduces sensitivity. The result is a first-pass design success.

42
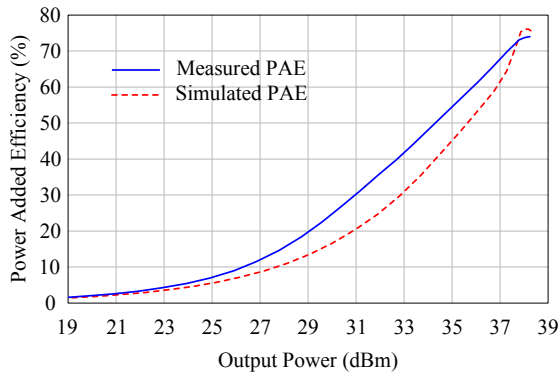
(a) The simulated versus measured power added efficiency versus the output power.
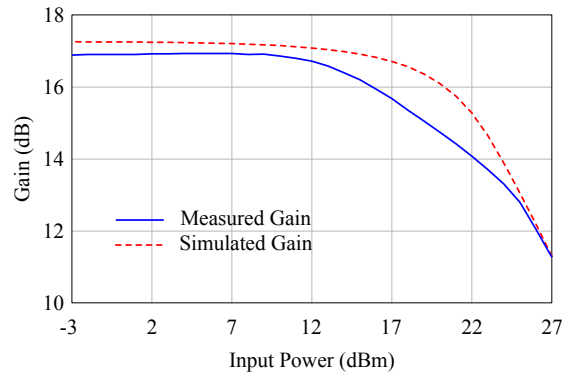
(b) The simulated versus measured gain versus the input power.

Figure 2.35: The simulated and measured power added efficiency and gain of the 10 W GaN high efficiency amplifier at 3.27 GHz.
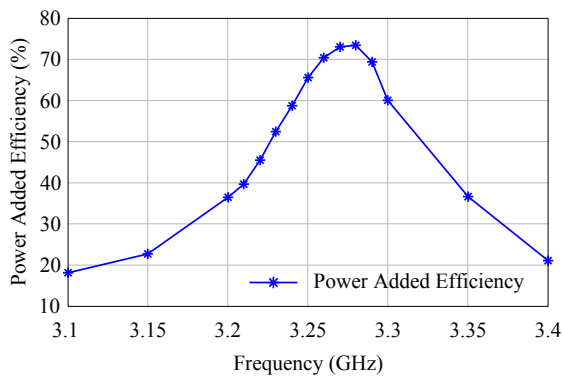
(a) The measured power added efficiency versus frequency.
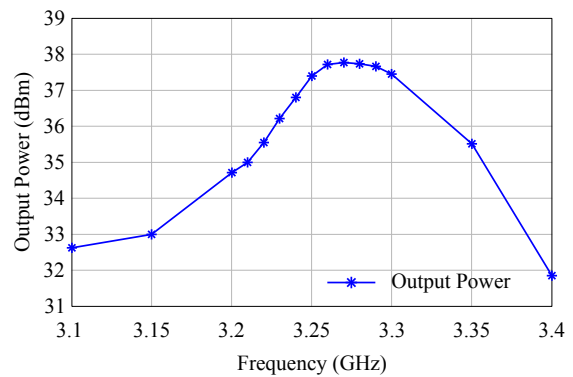
(b) The measured output power versus frequency.

Figure 2.36: The bandwidth characteristics of the 10 W GaN high efficiency amplifier with P_{avs} set to 25 dBm.

Chapter 3

Broadband and Highly Efficient Power Amplifier

3.1   Introduction

From the previous chapter, we found that the power amplifier efficiency can be very sensitive to harmonic terminations. In this chapter, we focus on the analysis and design of broadband and highly efficient power amplifiers that exploit properties of a broadband mode of operation to reduce the efficiency sensitivity to the output second harmonic termination.

There are mainly two complimentary aspects to broadband power amplifier research. The first investigates "broadband friendly" modes of operation such as the continuous class B/J design space that gives designers more impedance choices to match to over a wide frequency range [37]. The second aspect studies practical network synthesis techniques that can optimally match a given set of impedances to a resistive termination over a wide frequency range.

Analyzing the class B/J design space, we show that a practically realizable matching network cannot track the class B/J design space impedances without impedance mismatch. In light of this limitation, we analyze the efficiency degradation due to the mismatch and subsequently discover that at the package reference plane, some impedances in the class B/J design space can reduce the amplifier efficiency sensitivity to the second harmonic terminations. Specifically, we find that the class J* fundamental impedances yield the minimal sensitivity to the second harmonic terminations at the package reference plane.

For the broadband matching network synthesis, we harness the simplified real frequency technique (SRFT), originally developed for the design of wideband antennas [38], to systematically design the broadband matching networks. To adopt the SRFT technique in power amplifier design, we carry out extensive impedance analyses at the fundamental and harmonic frequencies

by applying the load-pull technique on large-signal device models across the design frequencies.

Since the amplifier efficiency is not very sensitive to the second harmonic terminations according to the class B/J design space analyses, we propose a broadband amplifier design technique where the fundamental matching networks are synthesized via the simplified real frequency technique and the harmonic impedances are placed in the high efficiency regions on the Smith chart by adjusting the bias line placements.

Although, the work in this chapter is originally meant to aid the design of broadband Doherty amplifiers in later chapters, subsequent analysis shows that the SRFT technique is not directly applicable to the bandwidth extension of the Doherty amplifier because broadband matching networks have poor impedance inverting properties. Nevertheless, the class B/J analyses give useful insights into the amplifier efficiency sensitivity to the second harmonic termination at the package reference plane. In fact, the insights enable subsequent Doherty amplifier designs to terminate the second harmonic using the bias lines alone.

3.2   Class B/J Design Space

3.2.1   Theory

The class B/J design space, introduced in [37,39], describes a set of voltage waveforms at the intrinsic drain that yields identical amplifier output power, efficiency, and linearity as the traditional class B amplifier. In theory, these additional voltage waveforms translate to many impedance terminations that provide flexibility in a broadband amplifier design. The current waveform is a half-rectified sine-wave for all voltage waveforms in the design space, while voltage waveforms are given by

$$v(\theta) = (1 - \cos\theta)(1 - \alpha\sin\theta), \quad -1 < \alpha < 1 \tag{3.1}$$

Since α in (3.1) is continuous from -1 to 1, a continuous set of voltage waveforms exists. In theory, a broadband design aiming to achieve constant efficiency versus frequency can utilize any of the continuous voltage waveforms across the band instead of being limited to the class B waveform. Three cases of α are given special designations with $\alpha = -1$ corresponding to class J^*, $\alpha = 0$ corresponding to class B, and $\alpha = 1$ corresponding to class J. The three voltage waveforms are illustrated in Figure 3.1.

In practice, a voltage waveform with a given α in the class B/J design space is synthesized by presenting the impedances Z_n (n denotes the harmonic number) associated that α as given by

$$Z_1 = R_{opt} + jX_1 \tag{3.2a}$$
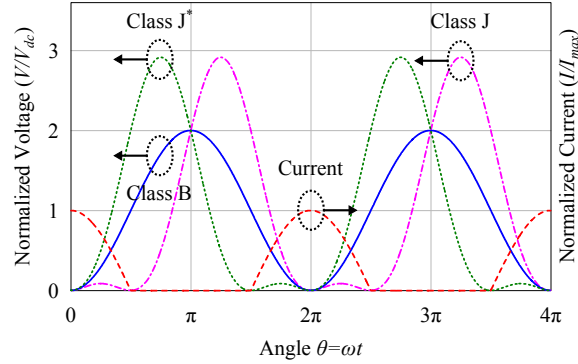
Figure 3.1: The normalized voltage waveforms of the class B, class J, and class J* mode of operation.

$$Z_2 = jX_2 \qquad (3.2b)$$

$$Z_n = 0, \quad n \geq 3 \qquad (3.2c)$$

with

$$R_{opt} = \frac{V_{dd}}{I_{max}/2} \qquad (3.3a)$$

$$X_1 = \alpha \frac{V_{dd}}{I_1} \qquad (3.3b)$$

$$X_2 = -\alpha \frac{V_{dd}}{2I_2} \qquad (3.3c)$$

where V_{dd} is the DC drain bias voltage, I_{max} is the device saturation current, and I_1 and I_2 are the fundamental and second harmonic components of the half-rectified sine-wave current.

3.2.2 Limitations

From Figure 3.1, a drawback of the class J and class J* modes is an increased peak voltage of approximately three times the normalized voltage. Therefore, designers have to ensure the voltage does not to exceed the device breakdown. The need for high breakdown voltage also translates to reduced device utilization factor.

Using (3.2), the class B/J design space can be visualize on the Smith chart as pairings of fundamental and second harmonic terminations. As an example, Figure 3.2 shows the fundamental
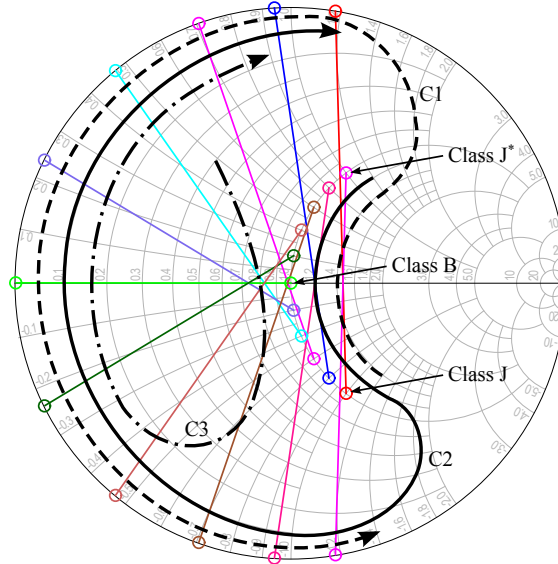
Figure 3.2: The class B/J design space visualized on the Smith chart.

and harmonic pairings connected by lines for various values of α for $R_{opt} = 50\ \Omega$ and $V_{dd} = 28$ V. The design space is static versus frequency because it is defined at the intrinsic drain. Therefore, to utilize the class B/J design space across the design frequency and satisfy (3.2) and (3.3), the broadband matching network should have an impedance versus frequency contour of either $C1$ or $C2$ as shown in Figure 3.2.

However, upon closer examination, the $C1$ and $C2$ impedance contours are not practically realizable because both contours require counter-clockwise rotation versus frequency, whereas all realizable passive and lossless networks rotate clock-wise [40]. The $C1$ contour rotates counter-clockwise at the second harmonic impedances, whereas the $C2$ contour rotates counter-clockwise at the fundamental impedances.

Therefore, a fundamental limitation exists in the utilization of the class B/J design space because any practical broadband matching network tracking the design space will always have some impedance mismatch. As an example, a practically realizable impedance contour that cannot exactly match all the impedances in the design space is shown as $C3$ in Figure 3.2. Given that mismatch is unavoidable in practical utilization, we now consider the amplifier efficiency sensitivity to impedance mismatch in the class B/J design space.

3.2.3 Efficiency Sensitivity to Impedance Mismatch

In the following analysis, we examine the efficiency degradation caused by mismatch in the fundamental and harmonic reactance in the class B/J design space. To aid our analysis, we
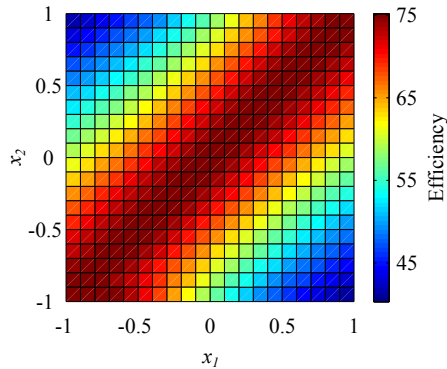
Figure 3.3: The amplifier efficiency as a function of the normalized reactance x_1 and x_2.

normalize the reactance X_1 and X_2 as x_1 and x_2, given by

$$x_1 = \frac{X_1}{V_{dd}/I_1} \tag{3.4a}$$

$$x_2 = \frac{X_2}{-V_{dd}/2I_2} \tag{3.4b}$$

The normalized reactance x_1 and x_2 have the same range as α in (3.1). If $x_1 = x_2$, then the fundamental and the second harmonic impedances are perfectly matched. To determine the efficiency degradation when $x_1 \neq x_2$, we sweep the two parameters and examine the amplifier efficiency using a harmonic balance simulator. Figure 3.3 illustrates the amplifier efficiency when x_1 and x_2 are varied.

From Figure 3.3, if $x_1 = 0$, corresponding to the class B fundamental reactance, and x_2 is either -1 or 1, corresponding to the class J* and class J second harmonic reactance, the efficiency is approximately 63%. In other words, if the fundamental matching is set at class B and the second harmonic is mismatched to either the class J* or class J reactance, one can expect a 15% efficiency degradation from the maximum efficiency of 78.5%.

On the other hand, if $x_1 = -1$ and $x_2 = 1$ or vice versa, corresponding to when a class J* fundamental is mismatched to a class J second harmonic or vice versa, we observe a 35% efficiency degradation from the maximum efficiency.

From this analysis, the efficiency degrades linearly versus the difference between x_1 and x_2. Moreover, if the absolute difference between x_1 and x_2 is kept below one normalized unit, then the efficiency degradation is less than 15%.
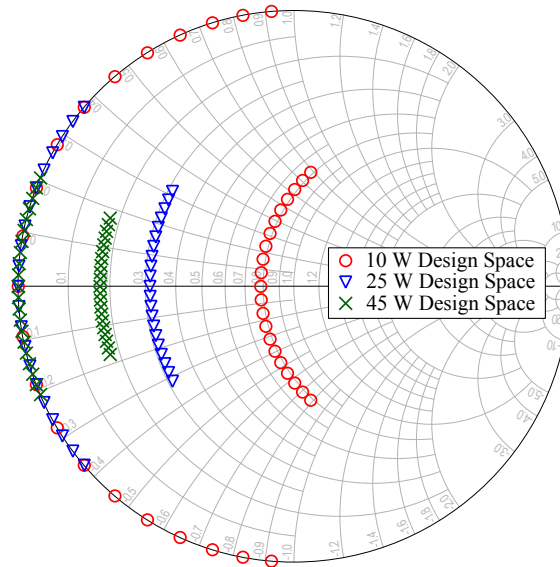
Figure 3.4: The class B/J design space as a function of the device power level.

3.3 Exploiting the Class B/J Design Space to Reduce the Efficiency Sensitivity

With the insights on the efficiency degradation versus mismatch, we now derive the class B/J design space at the package reference plane that shows how the amplifier efficiency sensitivity to the second harmonic terminations can be minimized.

To transform the class B/J design space from the intrinsic drain to the package reference plane, we account for the device power level, the output capacitance, as well as the device package. Figure 3.4 shows the class B/J design space as a function of the device power level. From Figure 3.4, as the power level increases, the design space compresses toward the left of the Smith chart with smaller impedances to match to, indicating higher matching challenges at larger power levels.

Using Cree Inc.'s CGH40045F 45 W GaN device as an example, which has an output capacitance of 4.0 pF, we transform the 45 W class B/J design space to the die reference plane as shown in Figure 3.5a at frequencies of 2.0, 2.5, and 3.0 GHz. To minimize the clutter, only the class J*, class B, and class J impedance pairings are shown. Like previously, the fundamental and second harmonic impedance pairings are connected with lines. From Figure 3.5a, the design space is now a function of frequency because of the output capacitance. Moreover, it is rotated counter-clockwise by almost 90°. The extent of the rotation is a function of the output capacitance value and the frequency.

49
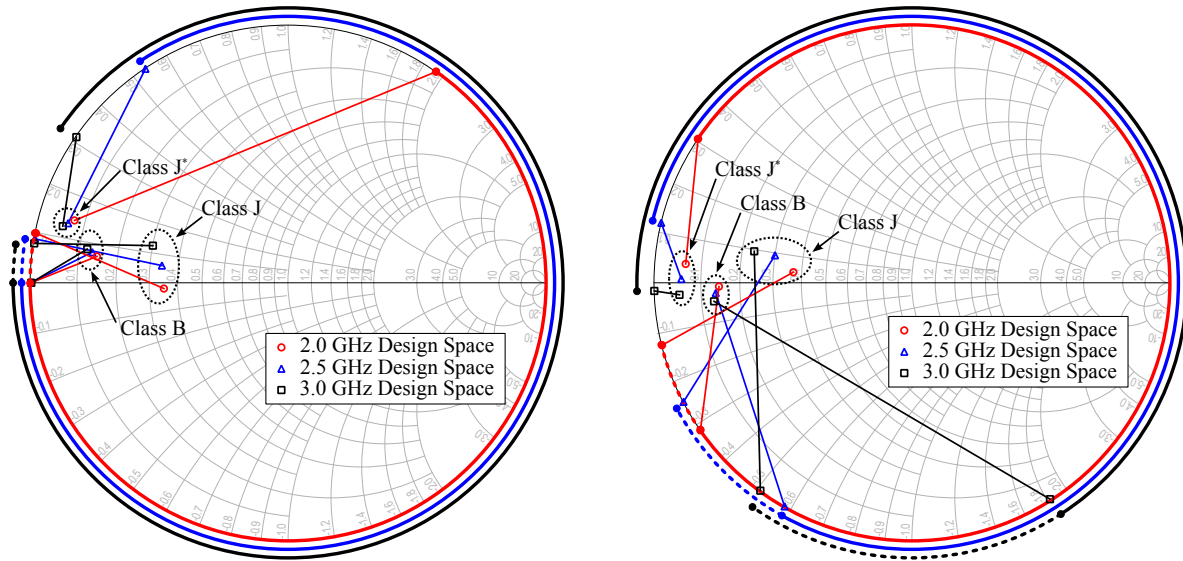
(a) The class B/J design space at the die reference plane in a 45 W GaN device with an output capacitance of 4.0 pF.

(b) The class B/J design space at the package reference plane in a 45 W GaN device when accounting for the output capacitance and the device package.

Figure 3.5: The class B/J design space of the 45 W GaN device at the die and package reference planes.

At first glance, the group of class J fundamental impedances seems optimal given its larger impedance value and its clockwise rotation versus frequency. However, when we examine the second harmonic transformation, it is apparent that the distribution of second harmonic termination around the edge of the Smith chart is uneven. From Figure 3.5a, the distance between the class B and class J second harmonic terminations is very close as indicated by dotted outer circles at each frequency. On the other hand, the class J* and the class B terminations are separated by almost the entire edge of the Smith chart as shown by the solid outer circles at each frequency. Therefore, if the class J* fundamental impedances are selected, the amplifier efficiency will be insensitive to second harmonic termination since a large portion of the Smith chart's edge will only result in a 15% efficiency degradation from the maximum efficiency. On the other hand, if the class J fundamental impedances are chosen, then the amplifier will be highly sensitive to the second harmonic termination. The fact that the choice of fundamental impedance can have a significant impact on the amplifier efficiency sensitivity to the second harmonic has not been highlighted in previous literature.

Similarly, when the output capacitance and device package are taken into account, the class B/J design space can be derived at the package plane as shown in Figure 3.5b. At the package reference plane, the design space is further rotated counter-clockwise and a similar trend exists in
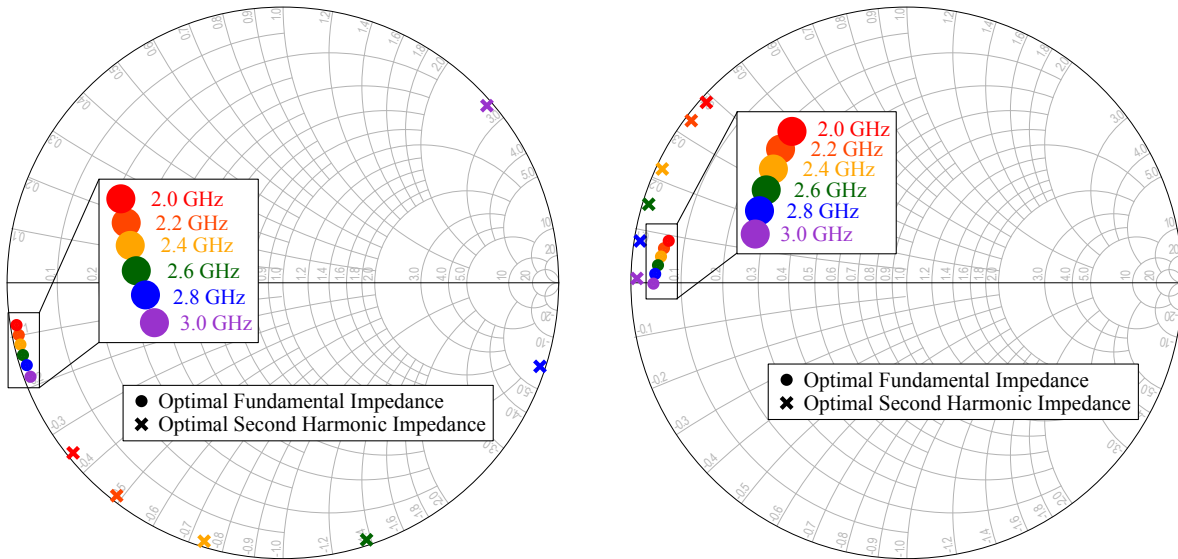
(a) The optimal fundamental and second harmonic source impedances at the package reference plane from source-pull simulation.

(b) The optimal fundamental and second harmonic load impedances at the package reference plane from load-pull simulation.

Figure 3.6: The source and load pull simulation of the 45 W GaN device from 2 to 3 GHz.

that the class J* fundamental impedances reduce the amplifier efficiency sensitivity to the second harmonic termination.

3.3.1 Load-pull Verification

To verify the proposed concept, we carried out load-pull simulations from 2 to 3 GHz in 0.2 GHz steps using the large signal model of the 45 W GaN device from Cree Inc. The device is biased at a drain voltage of 28 V and a drain current of 270 mA. The optimal fundamental and harmonic load impedances are shown in Figure 3.6b. In addition, second harmonic load-pull simulations are carried out at 4 and 6 GHz and shown in Figures 3.7a and 3.7b respectively. Each contour in Figures 3.7a and 3.7b indicates a 10% drop from the maximum efficiency. Each region between the contours is marked with the percentage efficiency degradation from the maximum efficiency.

By comparing to the optimal fundamental and harmonic impedances in Figure 3.6b to those in Figure 3.5b, we see that the load pull result contains exactly the class J* fundamental and harmonic pairings versus frequency. Additionally, the solid outer circles in Figure 3.5b that correspond to the harmonic sensitivity at 4 and 6 GHz show identical region of insensitivity as shown in the second harmonic load pull analyses in Figures 3.7a and 3.7b. As expected, the sensitivity analyses show large regions on the Smith chart with high efficiency at both 4 and

51
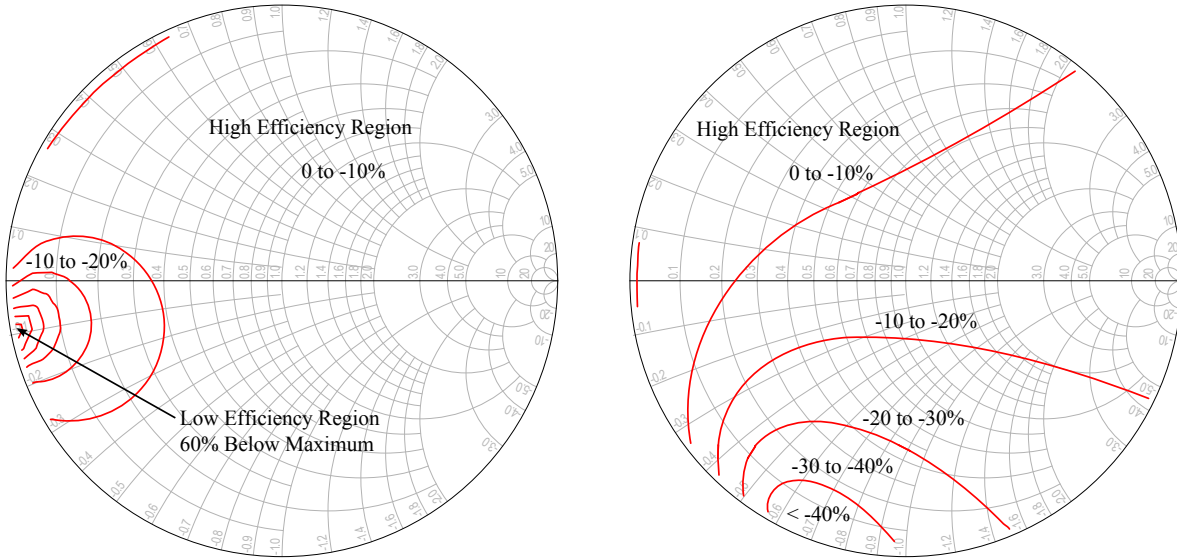
(a) The second harmonic load pull contours at 4 GHz indicating efficiency degradation below maximum efficiency in different region of the Smith Chart.

(b) The second harmonic load pull contours at 6 GHz indicating efficiency degradation below maximum efficiency in different region of the Smith Chart.

Figure 3.7: The second harmonic load-pull contours of the 45 W GaN device at 4 and 6 GHz.

6 GHz. Therefore, designers only have to explicitly match the fundamental impedances if the class J* set of impedances is chosen. For completeness, we also include the optimal fundamental and harmonic source-pull impedances in Figure 3.6a.

In short, although there are limitations in the utilization of the class B/J design space, the class J* mode of operation is nevertheless very useful because it relaxes the matching requirements at the second harmonic frequencies and thus enables designer to match only the fundamental impedances via techniques such as the simplified real frequency technique, which is briefly described in the next section.

3.4 Simplified Real Frequency Technique

The simplified real frequency technique (SRFT) is a numerical optimization algorithm that can determine the optimal broadband matching network when given a set of impedances across frequencies as input parameters. The single-ended matching problem is illustrated in Figure 3.8 where an arbitrary load that varies with frequency, expressed with $\Gamma_L(\omega)$, needs to be optimally matched to a fixed 50 Ω load across a frequency band. Ideally, a perfect match is achieved if the matching network S_{11} is exactly the conjugate of Γ_L across the frequency band. However,
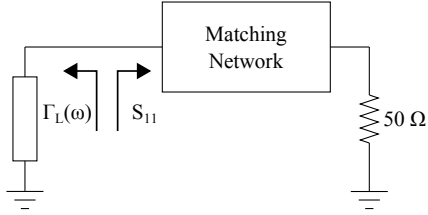
Figure 3.8: The matching of arbitrary loads across frequencies to a resistive termination.

because a physically realizable passive network's reactance always monotonically increases with frequency [40], assuming that Γ_L meets this criteria, the conjugate of Γ_L will have a reactance that monotonically decreases with frequency which a passive matching network cannot provide without using negative capacitors or inductors. A graphical equivalent can be shown on the Smith chart where Γ_L rotates clockwise versus frequency and its conjugate rotates counter-clockwise. And because a passive matching network's S_{11} rotates clockwise versus frequency, a perfect conjugate match across frequencies is not possible in practice.

Although analytical approaches exist to determine the network that yields the best gain-bandwidth product for matching a given set of impedances versus frequency to a resistive termination [41, 42], they generally require modelling of the load and must satisfy strict gain-bandwidth equalities that are difficult to process numerically except in highly simplified cases [43].

In 1982, Yarman proposed the simplified real frequency technique [44], an extension to the real frequency technique proposed by Carlin [43], that bypasses the analytical methods and uses the transducer power gain as the basis of an optimization algorithm to determine the optimal matching network given a set of impedances versus frequency. This method is shown to closely approximate the theoretical gain-bandwidth limit while being computationally friendly and easy to implement. The transducer power gain $T(\omega)$ of the matching problem in Figure 3.8 can be written as

$$T(\omega) = \frac{|S_{21}|^2(1 - |\Gamma_L|^2)}{|1 - S_{11}\Gamma_L|^2} \tag{3.5}$$

The transducer power gain is a key indicator of the "goodness of the match" since a transducer gain of unity implies a perfect match at that frequency. Therefore, the objective of the SRFT algorithm is to find the network whose S-parameter maximizes the transducer power gain for a given set of $\Gamma_L(\omega)$ across the design frequency band. A key result of [44] is the reformulation

53

of (3.5) such that it can be easily optimized using nonlinear optimization algorithms in modern computing software. The formulation also allows designers to use the optimization result to directly synthesize a realizable LC ladder network.

To reformulate (3.5), the *S*-parameter of the matching network, assumed to be lossless and reciprocal, is rewritten in the Belevitch form [45] on the *s*-plane using the polynomial $h(s)$, $g(s)$, and $f(s)$ given by

$$h(s) = h_0 + h_1 s + h_2 s^2 + \cdots + h_N s^N \tag{3.6}$$

$$g(s) = g_0 + g_1 s + g_2 s^2 + \cdots + g_N s^N \tag{3.7}$$

$$f(s) = f_0 + f_1 s + f_2 s^2 + \cdots + f_N s^N \tag{3.8}$$

For the special case where $f(s) = 1$, the *S*-parameter in Belevitch form is given as

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \frac{1}{g(s)} \begin{bmatrix} h(s) & 1 \\ 1 & -h(-s) \end{bmatrix} \tag{3.9}$$

Substituting the expression for S_{11} and S_{21} from (3.9) into (3.5) and utilizing the lossless condition given by

$$g(s)g(-s) = h(s)h(-s) + 1 \tag{3.10}$$

the transducer power gain versus frequency in terms of $h(s)$ and $g(s)$ can be derived as

$$T(\omega) = \left. \frac{1 - |\Gamma_L|^2}{h(s)h(-s)(1 + |\Gamma_L|^2) - 2\Re(\Gamma_L h(s)g(-s)) + 1} \right|_{s=j\omega} \tag{3.11}$$

For a given set of coefficients $h_0, h_1, h_2, \ldots, h_N$ in $h(s)$, the coefficients in $g(s)$ and the transducer power gain are uniquely defined via (3.10) and (3.11). Therefore, by using iterative nonlinear optimization routines available in MATLAB, the coefficients of $h(s)$ yielding the maximum transducer power gain across the frequency band can be determined. The solution is convergent and does not depend on the initial condition because the order of nonlinearity in terms of the real coefficient of $h(s)$ is always quadratic in nature [38].

Upon finding the optimal coefficient $h(s)$, the number of elements in the LC network corresponds directly with the order of $h(s)$. In addition, the elements of the low-pass LC ladder network can be determined by expanding the continued fraction of the driving impedance given by $S_{11} = h(s)/g(s)$.

Table 3.1: The ideal LC matching elements generated by the SRFT algorithm.

Element	Source		Load	
	Type	Value	Type	Value
#1	C	8.035 F	L	0.148 H
#2	L	0.645 H	C	8.412 F
#3	C	1.993 F	L	0.421 H
#4	L	0.907 H	C	2.659 F
Termination	R	1 Ω	R	1 Ω

3.5   Design and Validation

In this section, we outline the design of two broadband and highly efficient power amplifiers employing the SRFT technique using 45 W GaN and LDMOS devices. The prototypes demonstrate that the proposed technique can be applied independently of the technology and frequency range. In the two designs, we apply a systematic design method where the fundamental impedances are matched using the SRFT and the harmonic impedances are placed in the high efficiency regions of the Smith chart by adjusting placement of the bias lines.

3.5.1   A 2 to 3 GHz Broadband 45 W GaN Amplifier

Using the optimal fundamental impedances in Figures 3.6a and 3.6b as inputs to the SRFT optimization algorithm, Table 3.1 lists the generated LC ladder element values at a normalized frequency $\omega = 1$ and a reference impedance of 1 Ω. The results in Table 3.1 are subsequently scaled to a center frequency of 2.5 GHz with a 50 Ω reference impedance. The corresponding LC matching circuit is shown in Figure 3.9.

To verify that the SRFT algorithm generated proper matching networks, the impedance versus frequency of the LC ladder input and output networks are overlaid with the optimal fundamental impedances as shown in Figure 3.10. As expected, the synthesized networks have a clockwise rotation versus frequency. The optimal match circles around the optimal impedances with the black dots representing the impedances at the six frequencies evaluated in Figures 3.6a and 3.6b. Note that none of the six dots lies on its respective optimal impedance. This unavoidable impedance mismatch translates to efficiency degradation as well as lower amplifier gain due to the input mismatch.

To realize the circuit using microstrip lines, the LC ladder networks are converted to step impedance transmission lines following [31]. Upon conversion to transmission lines, the width and length of the lines are further fine tuned to account for the parasitic introduced by the step discontinuity. Finally, the bias line placements are designed to ensure that the second harmonic
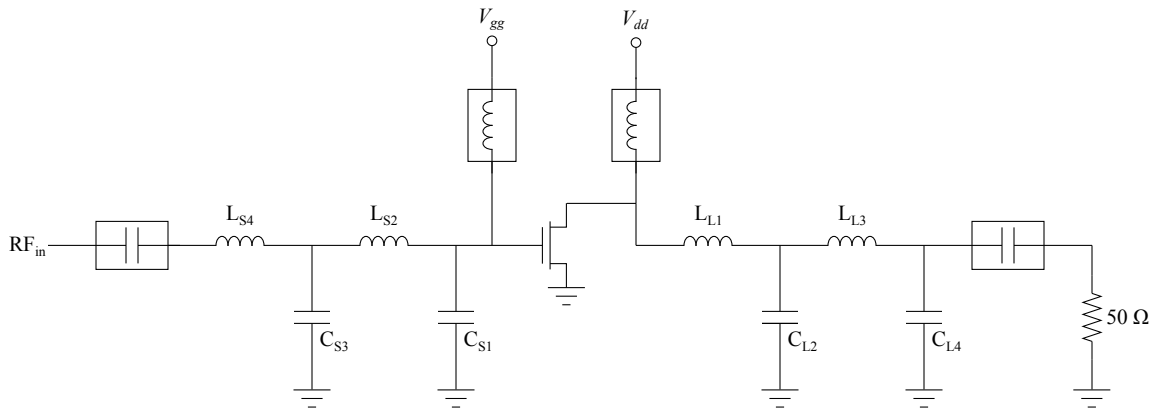
Figure 3.9: The low-pass LC input and output matching networks synthesized by the SRFT algorithm.
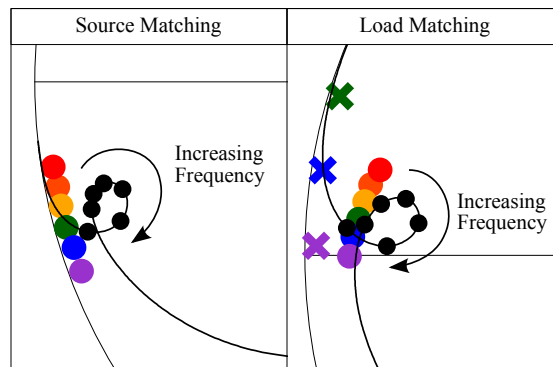
Figure 3.10: The impedance versus frequency of the source and load networks generated by the SRFT algorithm given the optimal source and load impedances as inputs.
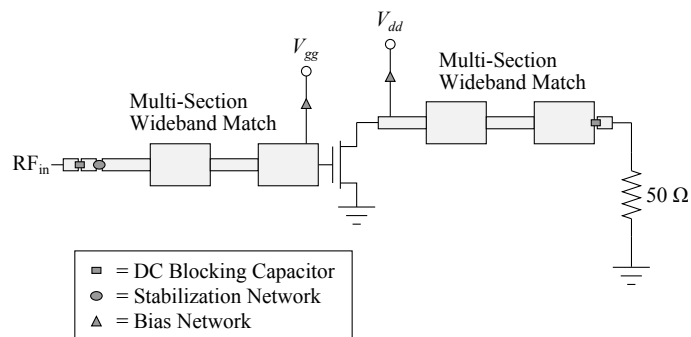
Figure 3.11: The microstrip equivalent of the LC input and output matching networks.

56
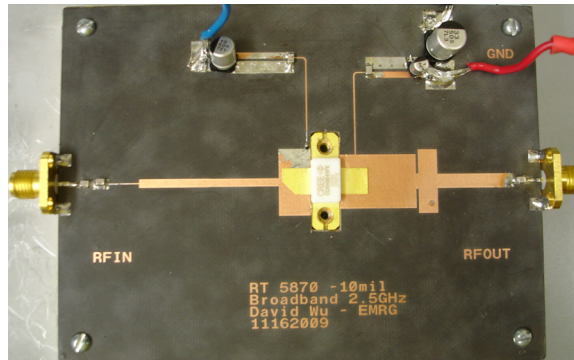
Figure 3.12: A picture of the 45 W GaN broadband amplifier.

terminations fall within the high efficiency regions shown in Figures 3.7a and 3.7b. The complete circuit diagram is shown in Figure 3.11. The fabricated input and output matching networks are shown Figure 3.12.

The measurement results are obtained without post production tuning of the amplifier. Figure 3.13a shows the measured versus simulated gain at the peak power from 1.8 to 3.1 GHz. The measured gain is about 2 dB lower than the simulated gain which is likely due to mismatch in the input matching network. Similarly, Figure 3.13b plots the measured versus simulated peak power, showing good agreement between the simulation and measurement. Lastly, Figure 3.14 shows the measured versus simulated drain efficiency. The measurement is shifted down by about 0.1 GHz when compared to the simulation, which is likely due to an error in the dielectric constant of the substrate. From 1.9 to 2.9 GHz (41.6% fractional bandwidth), the average gain, output power and drain efficiency are 10.8 dB, 45.8 dBm, and 63% respectively.

To assess the linearizability of the 45 W GaN broadband amplifier, a 20 MHz 1001 wideband code division multiple access (WCDMA) with 7.24 dB PAPR and a 10 MHz LTE signal with 9.2 dB PAPR are applied at 2.14 and 2.6 GHz respectively. Figures 3.15a and 3.15b show the output spectrum of the amplifier before and after memory polynomial digital pre-distortion (DPD) linearization for the WCDMA and LTE signals respectively.

When driven with the 20 MHz 1001 WCDMA signal, the adjacent channel power ratio (ACPR) improved from -30.95 to -50.14 dBc and the amplifier achieved an average output power of 37.78 dBm and an associated drain efficiency of 34.2%. Similarly, when driven with the 10 MHz LTE signal, the ACPR improved from -36.12 to -52.14 dBc and the amplifier achieved an average output power of 36.8 dBm with an associated drain efficiency of 27.0%.
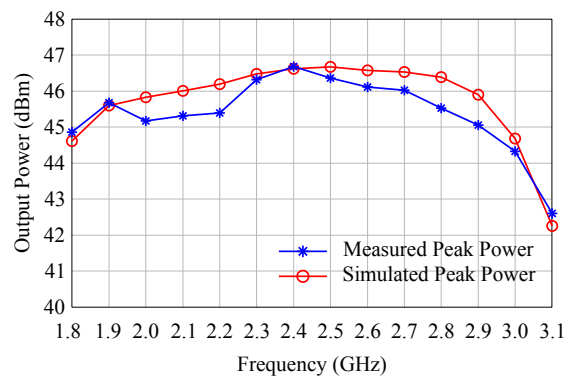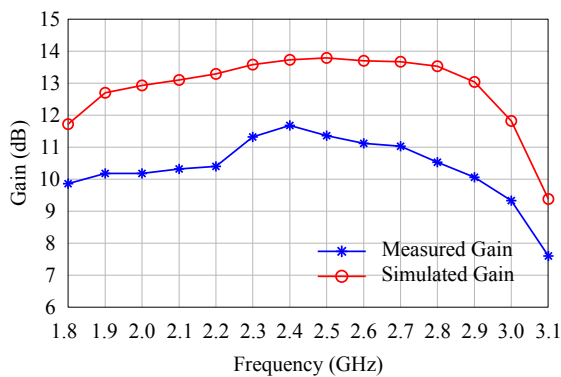
(a) The measured versus simulated gain of the 45 W GaN broadband amplifier.

(b) The measured versus simulated peak output power of the 45 W GaN broadband amplifier.

Figure 3.13: The measured versus simulated gain and output power of the 45 W GaN broadband amplifier from 1.8 to 3.1 GHz.
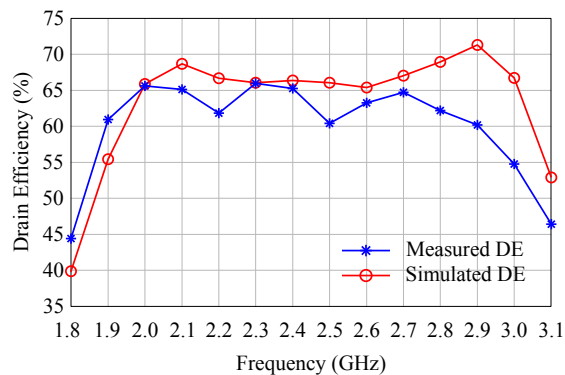
Figure 3.14: The measured versus simulated drain efficiency of the 45 W GaN broadband amplifier from 1.8 to 3.1 GHz.

3.5.2 A 650 to 1050 MHz Broadband 45 W LDMOS Amplifier

Following a similar approach as the GaN device analysis and design, a 650 to 1050 MHz (47% fraction bandwidth) broadband and highly efficient amplifier is designed using the 45 W MRF6S9045N LDMOS device from Freescale Semiconductor Inc. This prototype demonstrates that despite using a different technology with different device parasitic and package, a similar second harmonic insensitivity exists that enables the use of the SRFT for the fundamental matching. Source-pull and load-pull analyses were carried out from 650 to 1050 MHz with a device DC drain voltage of 28 V and a DC drain current of 350 mA. The SRFT algorithm is then used to synthesize the optimal matching network using the load-pull results. Similar to the 45 W GaN
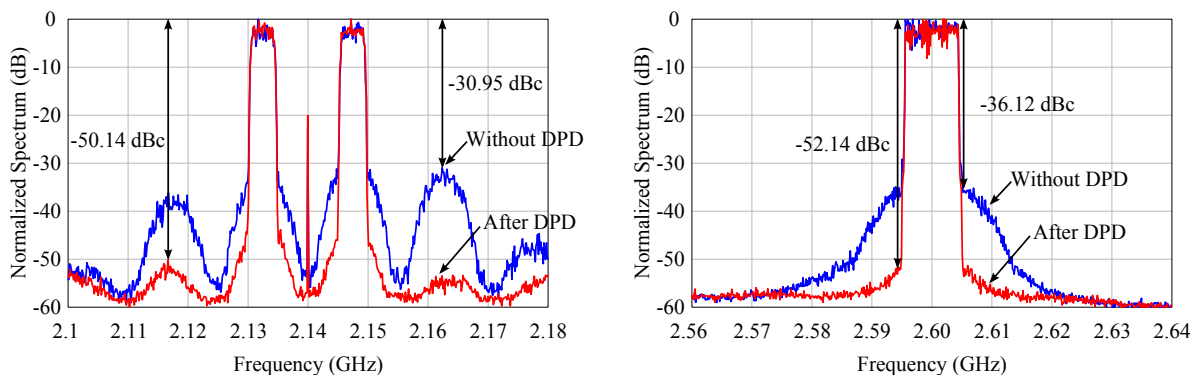
(a) The measured output spectra of the 45 W GaN broadband amplifier before and after the DPD linearization when driven with a 20 MHz WCDMA 1001 signal at 2.14 GHz.

(b) The measured output spectra of the 45 W GaN broadband amplifier before and after the DPD linearization when driven with a 10 MHz LTE signal at 2.6 GHz.

Figure 3.15: The measured output spectra of the 45 W GaN broadband amplifier before and after the DPD linearization when driven with 20 MHz WCDMA 1001 and 10 MHz LTE signals.
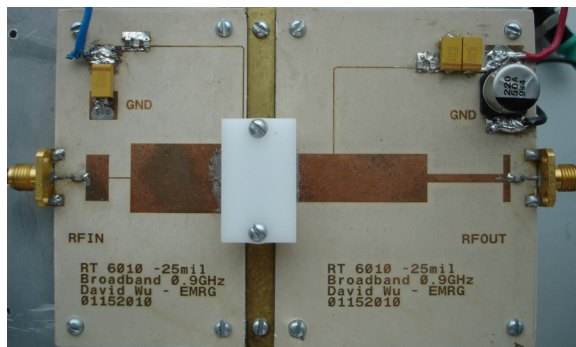
Figure 3.16: A picture of the 45 W LDMOS broadband amplifier.

design, the bias lines were placed such that the second harmonic impedances fell within the high efficiency regions on the Smith chart.

The amplifier is a first-pass design without post-production tuning. Figure 3.17a shows the measured versus simulated gain at the peak power from 0.6 to 1.1 GHz. Similarly, Figure 3.17b plots the measured versus simulated peak power. In Figure 3.18, the measured versus simulated drain efficiency is shown. The measurement is shifted down by about 50 MHz when compared to the simulation which is likely due to an error in the dielectric constant of the substrate. From 650 to 1050 MHz (47% fractional bandwidth), the average gain, output power and drain efficiency are 16.8 dB, 46.8 dBm, and 62.2% respectively.
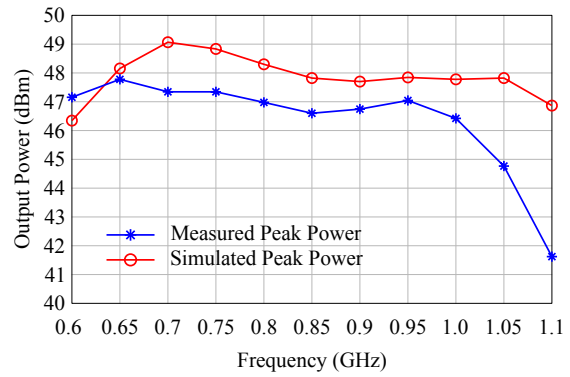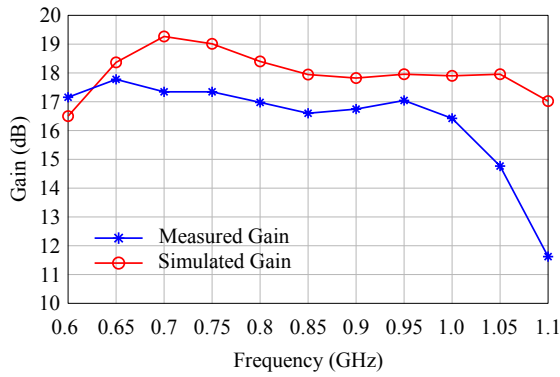
(a) The measured versus simulated gain of the 45 W LD-MOS broadband amplifier.

(b) The measured versus simulated peak output power of the 45 W LDMOS broadband amplifier.

Figure 3.17: The measured versus simulated gain and output power of the 45 W LDMOS broadband amplifier from 600 to 1100 MHz.
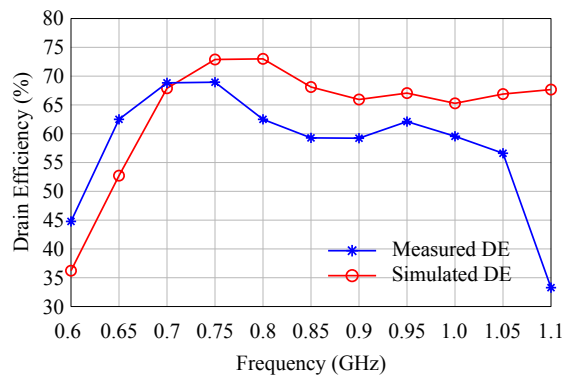
Figure 3.18: The measured versus simulated drain efficiency of the 45 W LDMOS broadband amplifier from 600 to 1100 MHz.

Chapter 4

Overview of Doherty Power Amplifier

4.1 Introduction

Although various techniques exist to enhance the peak efficiency of an amplifier as discussed previously, such an amplifier nevertheless exhibits a low average efficiency when driven with LTE or WiMAX signals which have a high peak-to-average ratio. Of the many approaches to improve the average efficiency of an amplifier, the Doherty power amplifier [4] has attracted significant interest because of its relative ease of implementation. In this chapter, we introduce the load modulation concept and derive the conventional Doherty amplifier characteristic. Despite its popularity, the conventional Doherty amplifier suffers from a number of shortcomings such as a need for advanced techniques to achieve proper load modulation as well as a limited operating bandwidth. To outline the state-of-the-art in the Doherty amplifier design, we review the traditional design method as well as conventional Doherty amplifiers in the literature. In subsequent chapters, we will present novel solutions to address the shortcomings of the conventional Doherty amplifier.

4.2 Theory of Operation

The Doherty amplifier consists of a main and an auxiliary device. Using the auxiliary device, the main device impedance is modulated to track a specific impedance profile that improves the efficiency at back-off power levels. For an ideal device biased in class B, the impedance R_o that results in the highest efficiency at a given the input voltage V_{in} is given by

$$R_o(V_{in}) = \frac{V_{dd}}{g_m V_{in}} \tag{4.1}$$
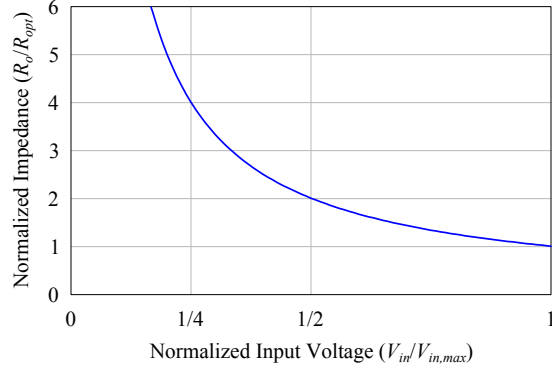
Figure 4.1: The impedance that yields the maximum efficiency versus the normalized input voltage v_{in} for a device biased in class B.

where g_m is the class B transconductance and V_{dd} is the DC drain bias voltage. At the maximum input voltage $V_{in,max}$, R_o is classically known as R_{opt} given by

$$R_{opt} = \frac{V_{dd}}{I_{max}/2} \tag{4.2}$$

Normalizing R_o by R_{opt} and V_{in} by $V_{in,max}$, Figure 4.1 plots the normalized R_o versus the normalized input voltage $v_{in} = V_{in}/V_{in,max}$.

From Figure 4.1, the impedance curve is nonlinear versus the input voltage. Therefore, although a class B amplifier that sees the impedance versus input profile in Figure 4.1 is highly efficient at all at power levels, the amplifier is nonlinear. This nonlinear transfer characteristic limits the application of single-ended amplifiers with reconfigurable matching networks that track the impedance curve in Figure 4.1. In contrast, the load modulation in a Doherty amplifier result in a linear transfer characteristic because of the output power contribution from the auxiliary device.

4.2.1 Load Modulation

The simplest circuit illustrating the load modulation concept is shown in Figure 4.2 where a voltage controlled voltage source (VCVS) is in parallel with a voltage controlled current source (VCCS) and a load resistor R. Using phasor notations (i.e. $\mathbf{X} = X\underline{/\theta_X}$), the impedance seen by the VCVS, $\mathbf{Z_1}$, can be modified using the current $\mathbf{I_2}$ as given by

$$\mathbf{Z_1} = \frac{\mathbf{V_1}}{\mathbf{I_1}} = \frac{\mathbf{V_1}}{\mathbf{I_R} - \mathbf{I_2}} \tag{4.3}$$

62
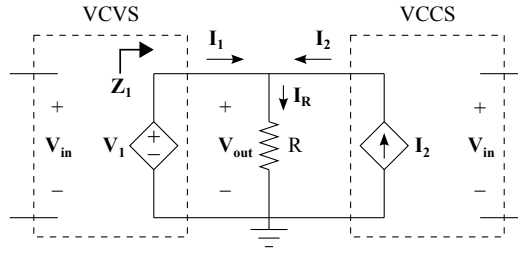
Figure 4.2: The load modulation concept illustrated using a VCVS and a VCCS.

Varying the current I_2 from zero to I_R corresponds to a Z_1 variation from R to ∞. In the Doherty amplifier, the ability to modulate Z_1 using I_2 is harnessed to track the optimal impedances that enable the amplifier to operate efficiently at the back-off power levels.

A key property of the circuit in Figure 4.2 is that the linearity of the overall system is solely determined by the linearity of the VCVS because the voltage V_{out} across the load R is equal to V_1. Therefore, linearity is guaranteed regardless of the value of I_2 as long as V_1 and V_{in} are linearly proportional.

Engineering the impedance Z_1 to track a given impedance profile versus V_{in} is achieved by specifying the I_2 versus V_{in} profile, a function that is defined piece-wise to target an efficiency enhancement up to a specific dB of back-off power. Although mathematically simple to define, realizing a given I_2 versus V_{in} profile in practice can be a challenge. As subsequent analysis will show, advanced techniques are needed in the conventional Doherty amplifier to satisfy its I_2 versus V_{in} profile.

In short, in the load modulation technique, the VCVS and VCCS each have an important role. The former ensures the linearity of the amplifier, while the latter acts as the load modulating device whose I_2 versus V_{in} profile determines the impedance Z_1 seen by the VCVS.

4.2.2   Load Modulation with VCCSs only

Because a transistor's output behaves intrinsically as a current source rather than a voltage source, to enable the load modulation technique in practice, a main VCCS is converted to a VCVS via a quarter-wave transmission line, and an auxiliary VCCS is used to modulate the impedance Z_m seen by the main device, as shown in Figure 4.3.

As a frequency dependent component, the quarter-wave transmission line introduces bandwidth constraint and input phase alignment requirement not present in Figure 4.2. Therefore, the complete description of the voltages and currents in Figure 4.3 needs to account for varying frequency (expressed via varying θ) as well as different phase relationships between I_m and I_a, or equivalently, between the input voltages V_{im} and V_{ia}.

63
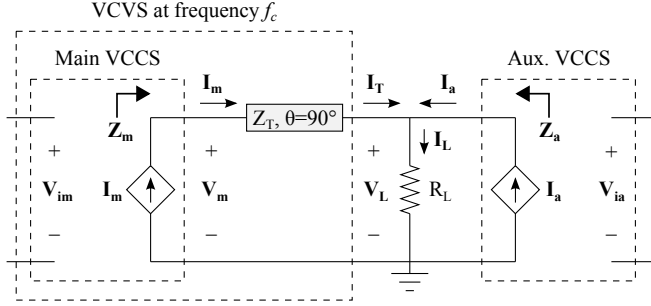
Figure 4.3: The Doherty amplifier load modulation scheme with VCVSs only.

To aid the analysis, we replace the transmission line in Figure 4.3 with its equivalent *ABCD*-parameter, yielding the following relations

$$\begin{bmatrix} \mathbf{V_m} \\ \mathbf{I_m} \end{bmatrix} = \begin{bmatrix} \cos\theta & jZ_T\sin\theta \\ j(1/Z_T)\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} \mathbf{V_L} \\ \mathbf{I_T} \end{bmatrix} \tag{4.4}$$

where Z_T and θ are the transmission line characteristic impedance and the electrical length respectively. At the center frequency f_c where $\theta = 90°$, the relationship between $\mathbf{V_L}$ and $\mathbf{I_m}$ reduces to

$$\mathbf{V_L} = -jZ_T\mathbf{I_m} \tag{4.5}$$

Assuming a linear relationship between $\mathbf{I_m}$ and $\mathbf{V_{im}}$, $\mathbf{V_L}$ can be considered as the output of a VCVS with an input voltage $\mathbf{V_{im}}$. Therefore, the key condition for load modulation is satisfied, albeit only at the frequency f_c.

For the complete description of the parameters in Figure 4.3 for any θ, we first replace $\mathbf{V_L}$ in (4.4) with

$$\mathbf{V_L} = R_L\mathbf{I_L} = R_L(\mathbf{I_a} + \mathbf{I_T}) \tag{4.6}$$

yielding

$$\begin{bmatrix} \mathbf{V_m} \\ \mathbf{I_m} \end{bmatrix} = \begin{bmatrix} \cos\theta & jZ_T\sin\theta \\ j(1/Z_T)\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} R_L(\mathbf{I_a} + \mathbf{I_T}) \\ \mathbf{I_T} \end{bmatrix} \tag{4.7}$$

Because $\mathbf{I_m}$ and $\mathbf{I_a}$ are known variables controlled via $\mathbf{V_{im}}$ and $\mathbf{V_{ia}}$, the two unknowns in (4.7) are $\mathbf{I_T}$, the current out of the transmission line, and $\mathbf{V_m}$, the voltage across the main device. With straightforward manipulations, $\mathbf{I_T}$ is determined as

$$\mathbf{I_T} = \frac{\mathbf{I_m} - j\mathbf{I_a}(R_L/Z_T)\sin\theta}{j(R_L/Z_T)\sin\theta + \cos\theta} \tag{4.8}$$

and $\mathbf{V_m}$ is given by

$$\mathbf{V_m} = \mathbf{I_a}R_L\cos\theta + \mathbf{I_T}(R_L\cos\theta + jZ_T\sin\theta) \tag{4.9}$$

64

Moreover, $\mathbf{Z_m}$ and $\mathbf{Z_a}$, the impedances seen by the main and auxiliary devices respectively, are given by

$$\mathbf{Z_m} = \mathbf{V_m}/\mathbf{I_m} \tag{4.10}$$

and

$$\mathbf{Z_a} = \mathbf{V_L}/\mathbf{I_a} \tag{4.11}$$

Substituting (4.8) into (4.6) and (4.9), the complete description of $\mathbf{V_m}$ and $\mathbf{V_L}$ (and consequently $\mathbf{Z_m}$ and $\mathbf{Z_a}$) for any θ can be expressed in terms of four key parameters, namely, $\mathbf{I_m}$, $\mathbf{I_a}$, Z_T, and R_L. For $\mathbf{Z_m}$ to track a specific impedance profile versus the input voltage, proper $\mathbf{I_m}$ and $\mathbf{I_a}$ profiles and an appropriate selection of Z_T and R_L are required.

The main and auxiliary device output power P_m and P_a can be calculated as

$$P_m = \frac{1}{2}\Re(\mathbf{V_m}\mathbf{I_m}^*) \tag{4.12}$$

and

$$P_a = \frac{1}{2}\Re(\mathbf{V_L}\mathbf{I_a}^*) \tag{4.13}$$

The efficiency of the main and auxiliary devices are given by

$$\eta_m = \frac{P_m}{P_{dcm}} \tag{4.14}$$

and

$$\eta_a = \frac{P_a}{P_{dca}} \tag{4.15}$$

where P_{dcm} and P_{dca} are the DC power consumption of the main and auxiliary devices respectively. The efficiency of the overall Doherty amplifier is given by

$$\eta = \frac{P_m + P_a}{P_{dcm} + P_{dca}} \tag{4.16}$$

4.3 Conventional Doherty Power Amplifier

4.3.1 Derivation

To enable $\mathbf{Z_m}$ to track R_o of Figure 4.1 up to 6 dB of power back-off from the peak power, W. H. Doherty proposed the circuit topology of Figure 4.3 with I_m and I_a versus V_{in} profiles shown in Figure 4.4a [4]. V_{in} denotes the magnitude of $\mathbf{V_{im}}$ and $\mathbf{V_{ia}}$, a valid simplification because the conventional Doherty amplifier splits the input power evenly.
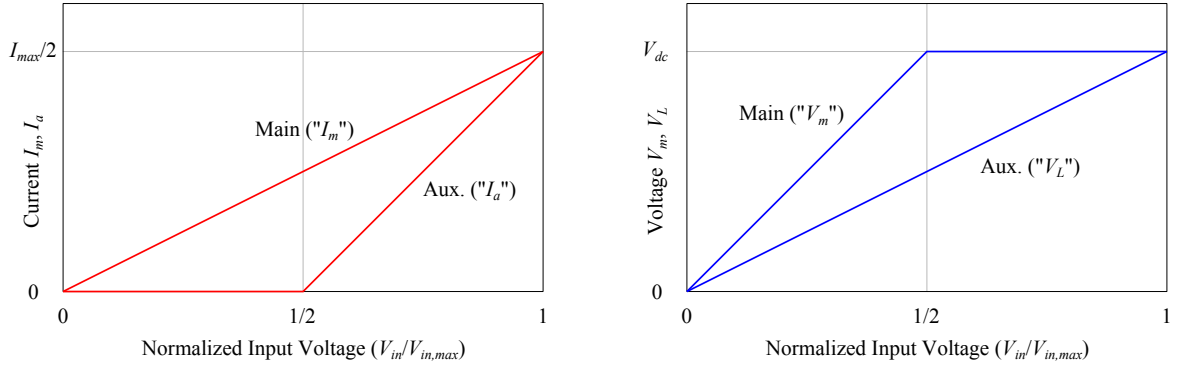
(a) The main device current I_m and the auxiliary device current I_a versus the normalized input voltage.

(b) The main device voltage V_m and the auxiliary device voltage V_L versus the normalized input voltage.

Figure 4.4: The output current and voltage profiles of the main and auxiliary devices in the conventional Doherty amplifier.

Mathematically, I_m and I_a can be described in terms of the normalized input voltage v_{in} given by

$$I_m = v_{in} \left(\frac{I_{max}}{2} \right) \tag{4.17}$$

and

$$I_a = \begin{cases} 0, & 0 \leq v_{in} < 0.5 \\ \left(v_{in} - \frac{1}{2} \right) I_{max}, & 0.5 \leq v_{in} \leq 1 \end{cases} \tag{4.18}$$

With the I_m and I_a profiles specified, the two parameters left to determine are Z_T and R_L which can be derived from (4.10) given (4.1), (4.17), and (4.18). At the center frequency f_c (i.e. $\theta = 90°$), assuming that $\mathbf{I_m} = I_m$ and $\mathbf{I_a} = -jI_a$, (4.10) reduces to

$$\mathbf{Z_m} = \left(\frac{Z_T}{R_L} - \frac{I_a}{I_m} \right) Z_T \tag{4.19}$$

and (4.11) reduces to

$$\mathbf{Z_a} = \frac{I_m Z_T}{I_a} \tag{4.20}$$

According to Figure 4.1, to track R_o, $\mathbf{Z_m}$ has to equal R_{opt} at the peak power and $2R_{opt}$ at the 6 dB back-off level. With the corresponding I_m and I_a from (4.17) and (4.18) at the two power levels, (4.19) yields

$$2R_{opt} = \frac{Z_T{}^2}{R_L} \tag{4.21}$$
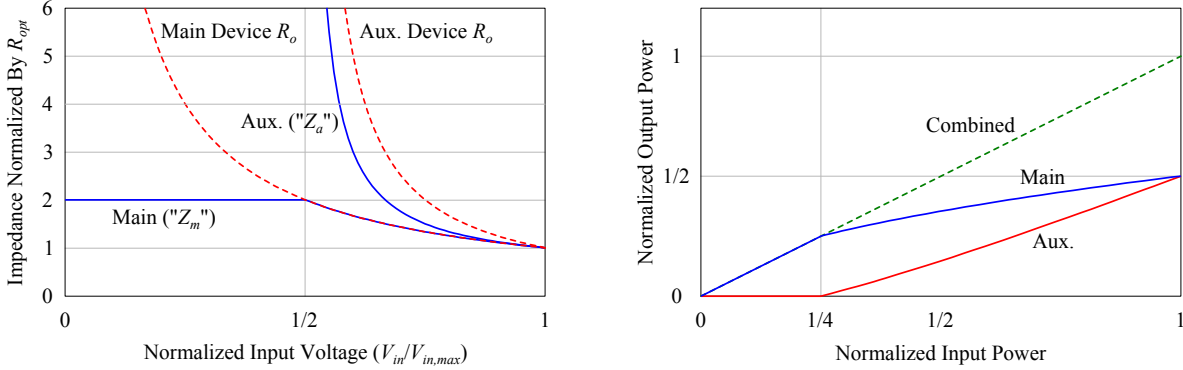
(a) The normalized impedances Z_m and Z_a seen by the main and auxiliary devices respectfully versus the normalized input voltage.

(b) The normalized output power P_m and P_a of the main and auxiliary devices versus the normalized input power.

Figure 4.5: The load modulation and the output power of the main and auxiliary devices in the conventional Doherty amplifier.

at the 6 dB back-off level, and

$$R_{opt} = \frac{Z_T{}^2}{R_L} - Z_T \qquad (4.22)$$

at the peak power. Solving for Z_T and R_L in (4.21) and (4.22) yields the classic results

$$Z_T = R_{opt} \qquad (4.23)$$

and

$$R_L = R_{opt}/2 \qquad (4.24)$$

The derivation of Z_T and R_L from the I_m and I_a profiles illustrates an important point. Namely, that though the circuit parameters of Figure 4.3 are described using four parameters, there are only two degrees of freedom. Once the I_m and I_a profiles are specified, a set of Z_T and R_L follows. Conversely, by specifying Z_T and R_L, one can derive the corresponding I_m and I_a profiles, a fact that is exploited in later chapters to derive a Doherty amplifier configuration with an extended bandwidth.

With R_L and Z_T determined, the voltages V_m and V_L across the main and auxiliary devices respectively are plotted in Figure 4.4b using (4.9) and (4.6). In the upper half input drive levels, V_m is held constant and prevented from saturating and distorting the current waveform. The impedances Z_m and Z_a seen by the main and auxiliary devices are plotted in Figure 4.5a using (4.19) and (4.20). As expected, Z_m tracks R_o for the upper half drive levels.

Using (4.12) and (4.13), the normalized output power P_m and P_a of the main and auxiliary devices respectively versus the normalized input voltage are plotted in Figure 4.5b. Because Z_m
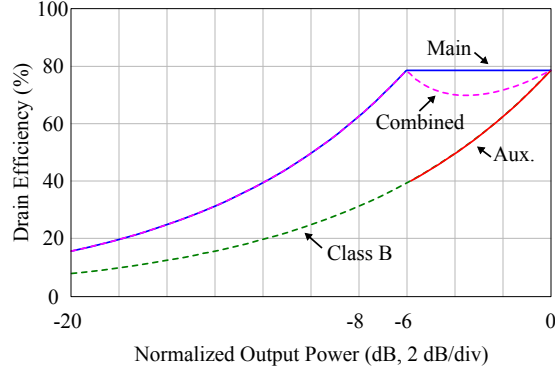
Figure 4.6: The efficiency of the main device, the auxiliary device, and the overall conventional Doherty amplifier.

and Z_a vary as a function of V_{in}, P_m and P_a are nonlinear with respect to the input power. However, the combined output power is linear with respect to the input because the VCVS ensures that the output load voltage V_L is a linear function of the input voltage.

Assuming class B power consumption, the DC power drawn by the main and auxiliary devices are given by

$$P_{dcm} = \frac{2I_m V_{dcm}}{\pi} \tag{4.25}$$

and

$$P_{dca} = \frac{2I_a V_{dca}}{\pi} \tag{4.26}$$

where V_{dcm} and V_{dca} are the DC drain bias voltages of the main and auxiliary devices respectively. In the conventional Doherty amplifier, the two bias voltages are equal.

Using (4.12), (4.13), (4.25) and (4.26), the efficiency of the main device, the auxiliary device, and the overall Doherty amplifier are calculated using (4.14), (4.15), and (4.16) and plotted versus the normalized output power in Figure 4.6. From Figure 4.6, the main device maintains its peak efficiency down to 6 dB of power back-off while the auxiliary device efficiency drops in a class B manner, shutting off at the 6 dB back-off level. As a result, the overall Doherty amplifier efficiency has peaks at 0 and 6 dB back-off levels and a minor efficiency drop in between. When compared to a class B amplifier, the conventional Doherty amplifier offers back-off efficiency improvements of about 40% and 20% at 6 and 10 dB back-off power levels respectively.

4.3.2 Frequency Behaviour

Having derived the conventional Doherty amplifier characteristic at the center frequency f_c, we now examine its characteristic when the frequency deviates from f_c. But prior to doing so, we

68
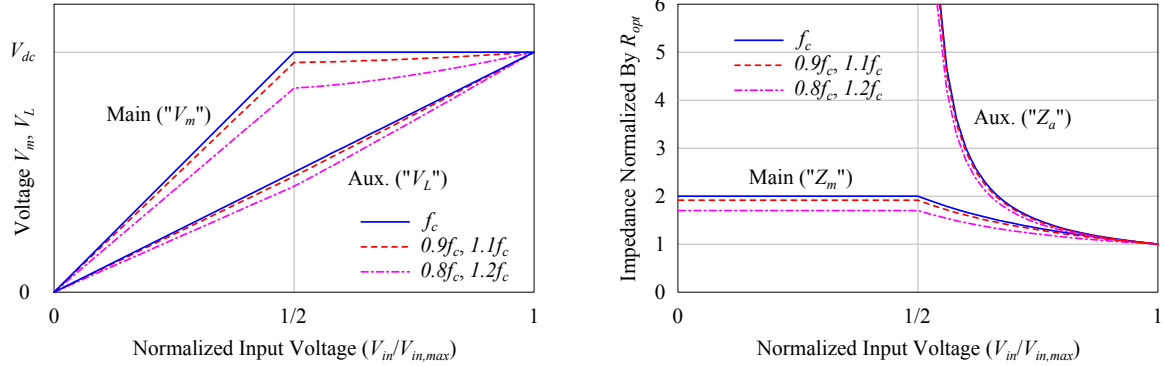
(a) The voltage V_m across the main device and the voltage V_L across the load and auxiliary device versus the normalized input voltage at various frequency deviations from f_c.

(b) The impedance Z_m and Z_a versus the normalized input voltage at various frequency deviations from f_c.

Figure 4.7: The output voltages and load modulation of the main and auxiliary devices in the conventional Doherty amplifier at various frequency deviations from f_c.

need to specify the relative phase of $\mathbf{I_m}$ and $\mathbf{I_a}$, or equivalently, of $\mathbf{V_{im}}$ and $\mathbf{V_{ia}}$, at frequency deviations from f_c. Practically, the $90°$ phase shift requirement between $\mathbf{I_m}$ and $\mathbf{I_a}$ at the center frequency f_c is synthesized via one of two methods: the use of an input $90°$ hybrid coupler, or a $90°$ transmission line inserted at the input of the auxiliary device. Although these two methods are equivalent at f_c, they yield different relative phase shifts when the frequency deviates from f_c. For the $90°$ hybrid coupler, the phase shift remains constant across the coupler's operating bandwidth given by

$$\underline{/\mathbf{I_m}} - \underline{/\mathbf{I_a}} = 90° \tag{4.27}$$

whereas the $90°$ transmission line method yields

$$\underline{/\mathbf{I_m}} - \underline{/\mathbf{I_a}} = \theta \tag{4.28}$$

where θ refers to the transmission line electrical length depicted in Figure 4.3.

The following frequency analysis of the conventional Doherty amplifier assumes (4.28) to be the phase relationship. Figure 4.7a illustrates the voltage V_m and V_L versus v_{in} at various frequency deviations from f_c plotted using (4.9) and (4.6). As the frequency deviation increases, the voltage V_m across the main device no longer saturates. More importantly, the voltage V_L, which appears across both the auxiliary device and the load R_L, is no longer linear with respect to v_{in}. This fundamental bandwidth-linearity trade-off in the conventional Doherty amplifier was not highlighted in previous publications.

Figure 4.7b illustrates the degradation from a load modulation perspective, where Z_m and Z_a, normalized by R_{opt}, are plotted versus v_{in} at various frequencies using (4.10) and (4.11). The fact
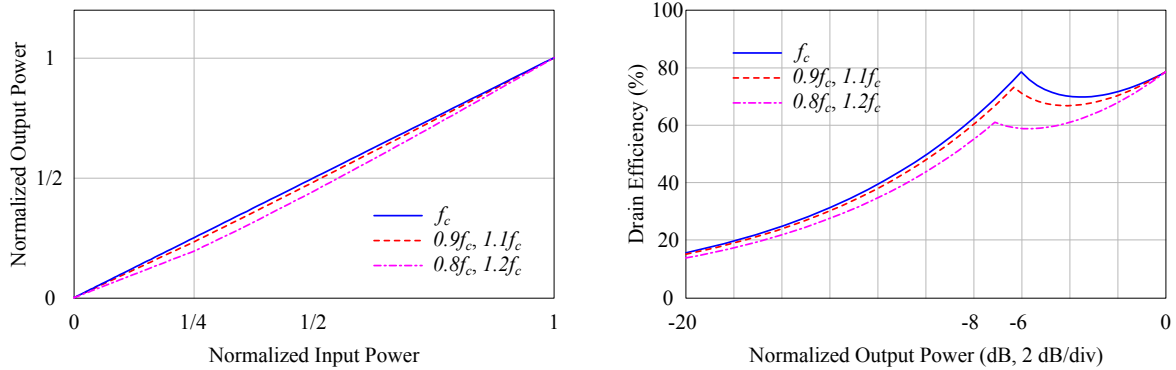
(a) The normalized output power versus the normalized input power at various frequency deviations from f_c.

(b) The efficiency versus normalized output power at various frequency deviations from f_c.

Figure 4.8: The output power and drain efficiency of the conventional Doherty amplifier at various frequency deviations from f_c.

that Z_m fails to reach $2R_{opt}$ at 6 dB back-off power explains the V_m degradation in Figure 4.7a, a problem that worsens as the frequency deviates further from f_c.

Using (4.12) and (4.13), the normalized output power versus input power at various frequency deviations from f_c is plotted in Figure 4.8a, further highlighting the bandwidth-linearity trade-off. Lastly, the efficiency versus normalized output power of the conventional Doherty amplifier at various frequency deviations from f_c is plotted in Figure 4.8b using (4.16). Clearly, the efficiency enhancement at the back-off power level degrades as the frequency deviates from f_c, illustrating the fundamental bandwidth limitation of the conventional Doherty amplifier. But interestingly, the peak power efficiency appears insensitive to frequency variations. Understanding this lack of bandwidth limitation for the peak power efficiency is exploited later in the formulation of the proposed broadband Doherty amplifier configuration.

4.4   Practical Design Considerations

4.4.1   Biasing of the Main and Auxiliary Devices

The practical implementation of a Doherty amplifier begins with the bias selection of the main and auxiliary devices. From Figure 4.4a, the main device current profile I_m requires a linear transfer characteristic, which can be exactly synthesized with a main device biased in class B. Figure 4.9a illustrates the synthesis of the I_m profile using the ideal FET model biased in class B.

On the other hand, the synthesis of the auxiliary device current profile I_a turns out to be a major challenge in the design of the conventional Doherty amplifier even though the I_a profile is
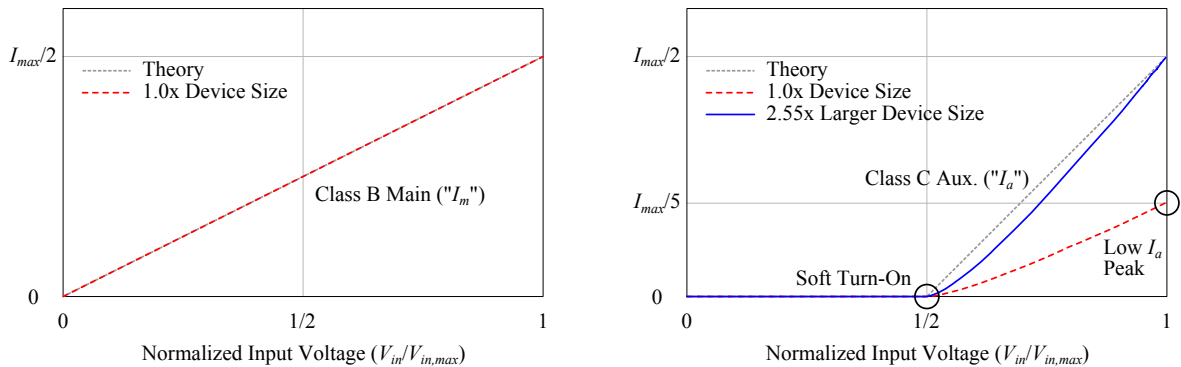
(a) The synthesis of the I_m profile with the main device biased in class B.

(b) The problems with synthesizing the I_a profile using an auxiliary device biased in class C.

Figure 4.9: The synthesis of the I_m and I_a current profiles in the conventional Doherty amplifier implemented using the ideal FET model biased in class B and class C respectively.

mathematically simple to define. To synthesize the I_a profile, a class C bias is chosen such that the auxiliary device turns on at $v_{in} = 1/2$. However, such a class C bias has two key shortcomings. Using the ideal FET model, Figure 4.9b shows that for an auxiliary device with the same size as the main device, I_a only reaches $I_{max}/5$ at the maximum input voltage instead of $I_{max}/2$ required by the theory. Moreover, the current I_a exhibits a gradual turn-on at $v_{in} = 1/2$ (a.k.a. soft turn-on) rather than an abrupt slope change required by the theory. These two deficiencies can be explained by the variation of the conduction angle of the class C current waveform as the drive level changes. The slow turn-on occurs because the output current conduction angle varies as a function of the input drive level, causing the slope of I_a to change above $v_{in} = 1/2$. Similarly, at the maximum input voltage, because of the smaller conduction angle of the class C current waveform when compared its class B counterpart, the peak current does not reach $I_{max}/2$.

A simple solution to mitigate the low peak current I_a is to use a larger auxiliary device. As Figure 4.9b shows, for an auxiliary device 2.55 times large larger than the main device, I_a reaches $I_{max}/2$ at the maximum input voltage. Similarly, a compromise can be made to alleviate the soft turn-on by adjusting the class C bias to turn on the auxiliary amplifier earlier than $v_{in} = 1/2$. However, turning on the auxiliary device earlier reduces the efficiency enhancement at the back-off power level. In the limiting case where the auxiliary device becomes class B biased, the Doherty configuration becomes a balanced class B amplifier with no efficiency enhancement at the back-off power level.

Aside from the aforementioned solutions, numerous other advanced techniques have been proposed in the literature with varying degrees of complexity to tackle the issue of slow turn-on and low I_a at peak power. These advanced techniques are discussed in later sections.
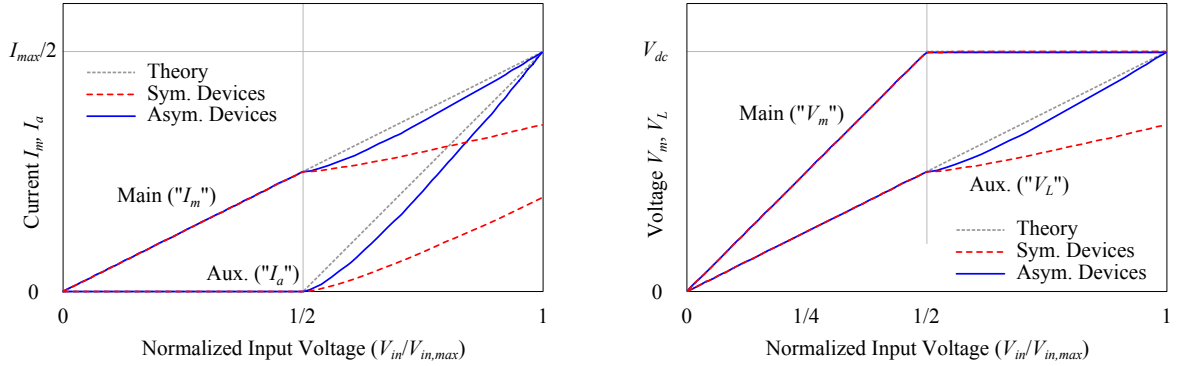
(a) The main device current I_m and auxiliary device current I_a in the symmetrical and asymmetrical Doherty configurations versus the normalized input voltage.

(b) The voltage V_m across the main device and the voltage V_L across the load and auxiliary device in the symmetrical and asymmetrical Doherty configurations versus the normalized input voltage.

Figure 4.10: The output current and voltage profiles of the main and auxiliary devices in the symmetrical and asymmetrical implementation of the conventional Doherty amplifier using the ideal FET model.

4.4.2 Implementations using Symmetrical and Asymmetrical Devices

To illustrate how the shortcomings of the class C bias of the auxiliary device affect the linearity, output power, and efficiency of the conventional Doherty amplifier, using the ideal FET model, we examine the symmetrical and asymmetrical Doherty configurations, where the auxiliary device is of the same size and 2.55 times that of the main device respectively.

Substituting (4.8) into (4.9) at the center frequency f_c (i.e. $\theta = 90°$) and with the assumption that $\underline{/I_m} - \underline{/I_a} = 90°$, we find the voltage across the main device as

$$\mathbf{V_m} = Z_T \left(\frac{I_m Z_T}{R_L} - I_a \right) \tag{4.29}$$

From (4.29), we see that if the realized auxiliary current I_a is lower than what the theory requires, then the main device voltage V_m increases. However, because of the device knee region, V_m is clipped at V_{dd} as shown in Figure 4.10b. The intrusion of V_m into the knee region reduces and distorts the main device current I_m, as shown in Figure 4.10a for the symmetrical and asymmetrical Doherty configurations. In both cases, the auxiliary device current I_a is lower than what the theory requires because of the soft turn-on at $v_{in} = 1/2$. However, the I_m reduction in the symmetrical Doherty configuration is significant because of the low peak auxiliary current I_a.

The degradation of the main device current I_m has a significant impact on the Doherty amplifier linearity, output power, and efficiency. Figure 4.10b shows the output voltage V_L across
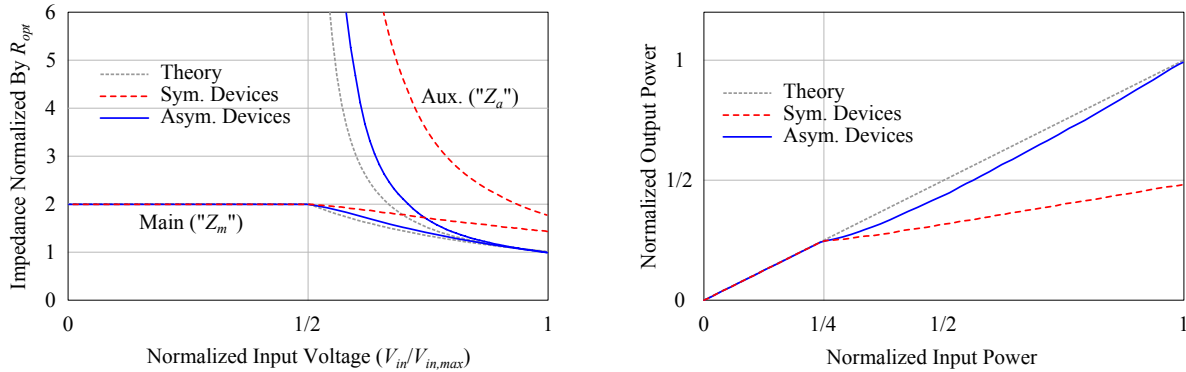
(a) The impedance Z_m and Z_a seen by the main and auxiliary devices respectively in the symmetrical and asymmetrical Doherty configurations versus the normalized input voltage.

(b) The normalized output power versus the normalized input power of the symmetrical and asymmetrical Doherty configurations.

Figure 4.11: The load modulation and transfer characteristic of the symmetrical and asymmetrical implementation of the conventional Doherty amplifier using the ideal FET model.

the auxiliary device and the load R_L. From Figure 4.10b, the voltage V_L, which mirrors the main device current I_m, is no longer linear with respect to the input because of the I_m distortion caused by inadequate I_a. The degradation is especially severe in the symmetrical Doherty configuration.

From a load modulation perspective, Figure 4.11a shows the impedance Z_m and Z_a seen by the main and auxiliary devices respectively in the two Doherty configurations. The soft turn-on and the low peak I_a in the case of the symmetrical Doherty cause Z_m and Z_a to be larger than what the theory requires, saturating the main and auxiliary devices and degrading their linearity and output power. These degradations can also be seen in the transfer characteristics of the two Doherty configurations as shown in Figure 4.11b. In the symmetrical Doherty amplifier, the peak output power is greatly reduced.

Lastly, the efficiency of the two configurations versus the output power are plotted in Figure 4.12. Because a class C bias consumes less DC power than the class B bias assumed in theoretical analyses, the efficiency of the asymmetrical Doherty configuration is higher than what the theory predicts. However, for the symmetrical configuration, the compromised output power results in reduced peak efficiency as well as poor back-off efficiency enhancement.

To summarize, the exact synthesis of the auxiliary device current is critical for a proper Doherty amplifier operation. However, even with the ideal FET model, the class C bias can only approximate the I_a profile required by the theory. In the next section, we explore other advanced techniques proposed in the literature to synthesize the proper auxiliary current profile.
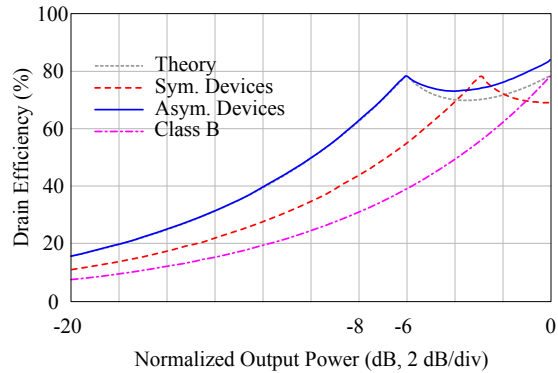
Figure 4.12: The efficiency of the symmetrical and asymmetrical conventional Doherty amplifiers implemented using the ideal FET model.

4.4.3 Advanced Techniques to Synthesize the Auxiliary Device Current

Previous analyses show that the exact synthesis of the auxiliary device current profile is critical to achieving the Doherty amplifier's theoretical linearity, output power, and efficiency. While the asymmetrical Doherty configuration is a simple and attractive solution, the required auxiliary to main device ratio of 2.55 is not always available in base station applications where the available device sizes are fixed by the device foundry. In this section, we present three advanced techniques that use symmetrical devices and are able to achieve the proper auxiliary device current profile.

Uneven Input Power Division

A conventional Doherty amplifier with symmetrical devices can use uneven input power division to achieve the required auxiliary current profile. By splitting the input power unevenly such that 13% goes to the main device and 87% goes to the auxiliary device, current profiles similar to those of the asymmetrical Doherty configuration can be obtained. A circuit diagram of a Doherty amplifier with uneven input power division is shown in Figure 4.13. This technique, however, suffers from some key shortcomings. Because only 13%, rather than 50%, of the power goes to the main device, the gain of the amplifier is reduced by 5.6 dB. Moreover, the increased drive of the auxiliary device means that for it to turn on at 6 dB back-off power, the auxiliary device has to be biased in deeper class C. In practice, the very deep class C bias can cause device breakdown or shorten the device lifetime. Lastly, the uneven input power division requires a special hybrid coupler or Wilkinson power splitter that adds to the design complexity.

74
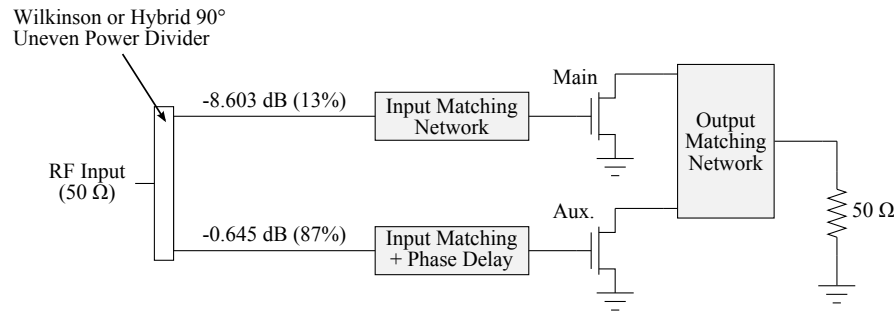
Figure 4.13: The circuit diagram of a symmetrical conventional Doherty amplifier with uneven input power division.

Adaptive Gate Bias for the Auxiliary Device

The adaptive gate bias technique adjusts the gate bias of the auxiliary device based on the envelope of the input signal in to obtain the theoretical auxiliary device current profile when symmetrical devices are used. A circuit diagram of a conventional Doherty amplifier using adaptive gate bias is shown in Figure 4.14. The RF input is sampled via a coupler and the signal envelope is extracted using an envelope detector. The envelope shaping circuit determines the appropriate auxiliary device gate bias $V_{g,aux}$ to apply based on the magnitude of the envelope signal. For example, at peak power, $V_{g,aux}$ is equal to the class B bias of the main device to obtain the same output current magnitude as the main device, whereas at 6 dB back-off and below $V_{g,aux}$ would be biased at deep enough class C to ensure the device is off. A delay line is added after the coupler to synchronize the two paths by accounting for the electrical delay of the envelope detector and shaping function.

Unlike the asymmetrical Doherty amplifier and the uneven input power division technique, the adaptive gate bias technique can eliminate the soft turn-on of the class C bias because the bias point is constantly being adjusted based on the envelope of the input signal. This technique is attractive because it can exactly synthesize the auxiliary device current profile. Although additional circuit elements and design complexity are needed, the higher cost may be justified given the potential performance gain.

Mixed-Signal Doherty Amplifier

The mixed signal Doherty amplifier, also known as the digital Doherty amplifier, eliminates the input power divider and instead uses two independently controlled inputs for the main and auxiliary devices. A circuit diagram of a mixed-signal Doherty with symmetrical devices is shown
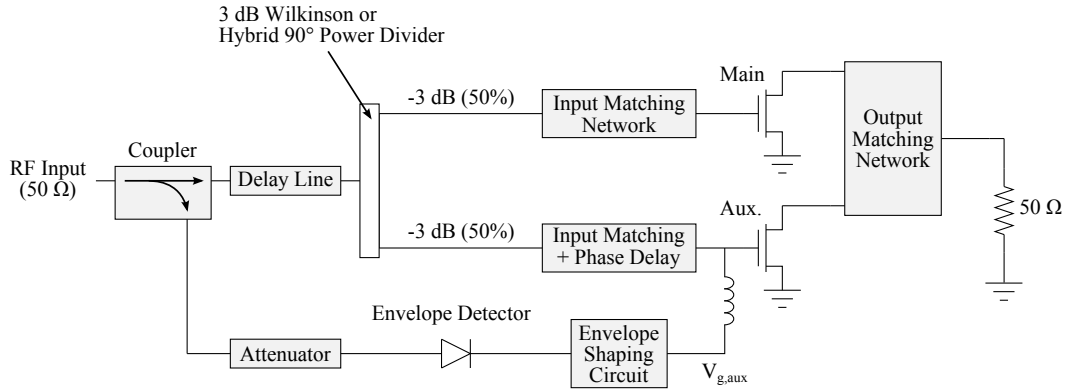
Figure 4.14: The circuit diagram of a symmetrical conventional Doherty amplifier with adaptive gate bias for the auxiliary device.

in Figure 4.15. The baseband signals are generated using a two channel arbitrary waveform generator and up-converted and filtered before being amplified by the drivers. The use of an arbitrary waveform generator allows for complete control of the magnitude of the main and auxiliary input signals, as well as their relative phases. As such, the auxiliary current profile can be exactly synthesized by shaping the input signal to cancel out the soft-turn on of the class C bias as well as to drive the device harder to reach the required current at peak power. The mixed-signal Doherty also has the advantage of being able to digitally tune out imperfections in the implementation. For example, if the auxiliary input matching network has more loss and an incorrect phase shift, the auxiliary input signal can be boosted and phase adjusted to compensate. Although the mixed-signal configuration is highly flexible and helps extract the maximum performance out of the amplifier, it requires twice the baseband hardware and driver amplifiers. Therefore, to fully assess the performance gain, one must account for the additional component cost as well as the power consumed by the baseband signal processing.

4.4.4   Matching Network Design

The purpose of the matching network in a Doherty amplifier is very similar to that of a single-ended amplifier. The network provides impedance matching to 50 Ω at the fundamental frequency and appropriate terminations at the harmonics. It also has to yield a high amplifier gain and stabilize the amplifier while having a low insertion loss. However, unlike a single-ended amplifier, the matching network in a Doherty amplifier also has to synthesize the proper phase relationship between the main and auxiliary devices. Moreover, at the output, an impedance inverter is needed between the main and auxiliary devices to achieve the proper load modulation. In this section, we outline key considerations in the design of the input and output matching networks in a Doherty amplifier.

76
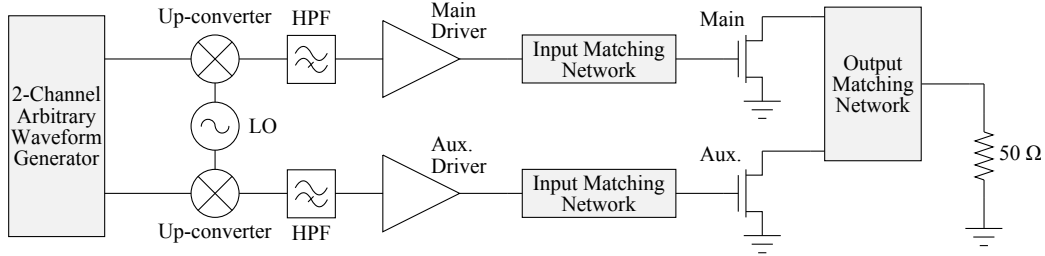
Figure 4.15: The circuit diagram of a symmetrical conventional Doherty amplifier with mixed-signal inputs.

Input Matching Network

As mentioned in Section 4.3.2, the 90° phase shift requirement between the main and auxiliary device inputs can be synthesize via one of two passive techniques: a 90° delay line inserted in the auxiliary input matching network, or a 90° hybrid coupler. The latter also acts as the input splitter for the main and auxiliary signals. When the 90° delay line is used, a Wilkinson power divider is needed to split the input signal with equal phases. As noted previously, these two passive techniques both yield 90° phase shift at the center frequency. However, away from the center frequency they yield different relative phase shifts that result in different Doherty amplifier frequency behaviours.

Aside from the phase requirement, the input matching also has to account for the different input impedances presented by the main and auxiliary devices. The impedances differ because of the class B and class C biases of the main and auxiliary devices. Moreover, if asymmetrical devices are used, the differences can be significant and different input networks as well as stabilization and bias networks may be necessary. For each of the main and auxiliary devices, the input matching to 50 Ω can be designed using the same procedure as that of a single ended amplifier.

Output Matching Network

To achieve load modulation, the output matching network in a Doherty amplifier has to provide an impedance inverter between the main and auxiliary devices. In addition, it must also provide fundamental matching to 50 Ω as well as appropriate harmonic terminations.

There are two approaches to achieving these objectives. In the traditional design approach,

the main and auxiliary devices are matched to 50 Ω first. The 50 Ω matched devices (now referred to as the main and auxiliary amplifiers) are then joined by a quarter-wave impedance inverter to form the Doherty amplifier. This approach is widely adopted because the main and auxiliary amplifiers can be designed separately as two single ended amplifiers where the load pull design technique can be readily applied. Moreover, each amplifier can be characterized separately before being inserted into a Doherty topology. However, as subsequent analyses will show, the resulting Doherty amplifier has a limited operating bandwidth and post production tuning is often needed to obtain the desired performance.

An alternative is to join the main and auxiliary devices with a quarter-wave impedance inverter first then provide impedance matching to 50 Ω. While this approach is actually more intuitive given the Doherty amplifier theory presented in the previous sections, there are two reasons why this approach is seldom used. First, the device parasitic and package does not permit the intrinsic current sources to be directly connected using a quarter-wave line. Second, the conventional Doherty amplifier theory requires $Z_T = R_{opt}$ and $R_L = R_{opt}/2$. For high power devices where R_{opt} is only a few ohms, the synthesis of the quarter-wave line characteristic impedance and matching to 50 Ω can be very difficult to achieve.

4.5   Traditional Design Method

In this section, we outline the traditional design method of the Doherty amplifier where the device outputs are matched to 50 Ω first then joined by a quarter-wave impedance inverter. In addition to outlining how the load modulation is achieved in this configuration, we highlight the shortcomings of this approach, namely, the limited operating bandwidth, an increased circuit size, and the requirement for post-production tuning.

Figure 4.16 illustrates the circuit topology used in the traditional design approach of the Doherty amplifier. The first step is to design the main and auxiliary amplifiers separately. Applying the load-pull technique, the main device, typically biased in class AB, is matched to 50 Ω at the input and output, forming the main amplifier between the reference planes A and B in Figure 4.16. Although the auxiliary amplifier can also be designed from scratch based on load-pull data, to ensure similar phase response in the two amplifiers, the auxiliary amplifier is often a replica of the main amplifier with the only difference being the class C bias of the auxiliary device. Once both amplifiers are tuned to satisfactory performance, they are inserted into the Doherty topology. The 90° phase delay in the auxiliary amplifier path is synthesized before the reference plane A with a hybrid coupler or a Wilkinson divider. On the output side, tuning lines, also known as offset lines, are inserted between the reference planes B and C. Empirically, the offset lines were found to be necessary for proper load modulation [46, 47]. Finally, the quarter-wave impedance inverter between the reference planes C and D joins the main and auxiliary amplifiers and the signals are combined with the output load at the reference plane D. Because the devices are
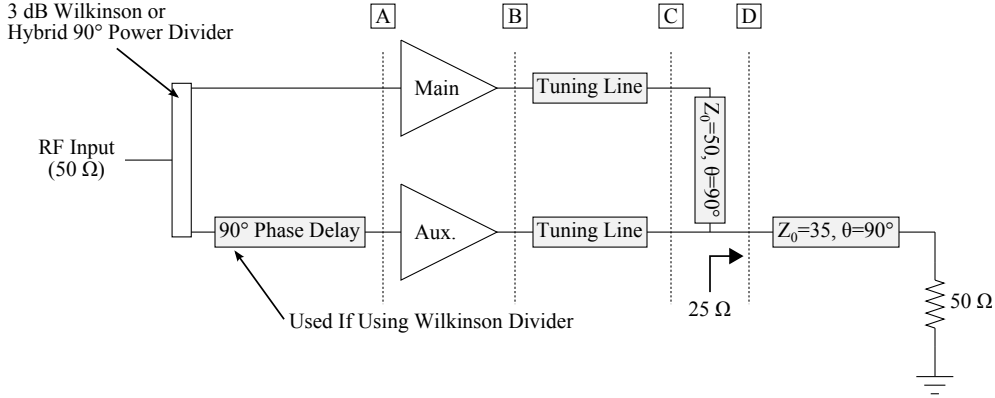
Figure 4.16: The circuit topology used in the traditional design approach of a Doherty amplifier.

matched to 50 Ω, a $R_{opt}/2$ of 25 Ω is synthesize from the 50 Ω load via another quarter-wave transmission line with a characteristic impedance of 35 Ω.

Although the procedures outlined are systematic and can be applied to the design of symmetrical and asymmetrical Doherty amplifier, exactly how the largely empirical approach achieves load modulation is not widely understood in the literature, especially given the offset lines which are not in the Doherty amplifier theory.

To understand how load modulation occurs in Figure 4.16, recall that in the Doherty amplifier theory, the quarter-wave line is connected to a current source at each end. Therefore, we can infer that the main and auxiliary amplifiers plus the offset lines must behave like current sources at the reference plan C. We can further deduce that the amplifier outputs at the reference plane B do not behave as current sources. Otherwise, the offset lines would not be necessary. The fact that a fully-matched amplifier output does not generally behave as a current source is easy to show. If we assume that the main amplifier output network $ABCD$-parameters are lossless and given by

$$\begin{bmatrix} V_i \\ I_i \end{bmatrix} = \begin{bmatrix} A_m & jB_m \\ jC_m & D_m \end{bmatrix} \begin{bmatrix} V_B \\ I_B \end{bmatrix} \tag{4.30}$$

where V_i, I_i, and V_B, I_B are the voltages and currents at the intrinsic drain and reference plane B respectively, and A_m, B_m, C_m, D_m are real numbers, then for I_B to be a purely a function of I_i (i.e. a current-controlled current source), C_m must be zero. However, without explicit design, a series of transmission line and lumped elements matching are unlikely to yield $C_m = 0$. Empirically, [46, 47] found that by tuning the offset line length, Doherty amplifier characteristics can be obtained in measurement.

To understand how the offset lines can produce current sources at the reference plane C, consider the combined $ABCD$-parameter when the output matching network given in (4.30) is

followed by an offset line with a characteristic impedance Z_c and length θ. The total *ABCD*-parameter is given by

$$\begin{bmatrix} A_t & jB_t \\ jC_t & D_t \end{bmatrix} = \begin{bmatrix} A_m & jB_m \\ jC_m & D_m \end{bmatrix} \begin{bmatrix} \cos\theta & jZ_c\sin\theta \\ j1/Z_c\sin\theta & \cos\theta \end{bmatrix} \tag{4.31}$$

The parameter C_t, which has to be zero for the amplifier to behave as a current source at the reference plane C, can be written as

$$C_t = jC_m\cos\theta + jD_m/Z_c\sin\theta = 0 \tag{4.32}$$

solving for θ yields

$$\theta = \tan^{-1}\frac{-C_mZ_c}{D_m} \tag{4.33}$$

As such, an offset line with a characteristic impedance Z_c and θ given by (4.33) will transform the non-current source output at the reference plane B to a current source at the reference plane C, thus enabling the Doherty operation as described in Section 4.2.

4.5.1 Limitations

A Doherty amplifier implemented with the traditional design technique suffers from several drawbacks, which include a need for post-production tuning, limited amplifier bandwidth and large circuit area. Post-production tuning is necessary because the *ABCD*-parameter from the intrinsic drain to the amplifier output is usually not available. Therefore, the length of the offset line cannot be calculated and has to be tuned after fabrication.

In terms of the bandwidth, the offset lines and quarter-wave line from the RF output to the combining node further degrade the amplifier bandwidth because the line lengths are frequency dependent. Moreover, contrary to intuition, using wideband output matching networks in the main and auxiliary amplifiers cannot improve the overall Doherty amplifier bandwidth. To illustrate this point, consider two different matching networks that match 50 Ω to 5 Ω as shown in Figure 4.17. In Figure 4.17a, a two-section quarter-wave matching is used while a four-section quarter-wave matching achieves a wider matching bandwidth in Figure 4.17b. For Doherty applications, the two networks are designed such that at the center frequency, each output at the 50 Ω load reference plane behaves as a current source. As such, the two networks resemble ideal matching networks that can be inserted between the intrinsic drain and the reference plane C in Figure 4.16.
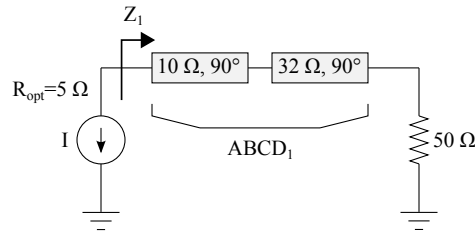
(a) 50 Ω to 5 Ω matching with two quarter-wave lines.
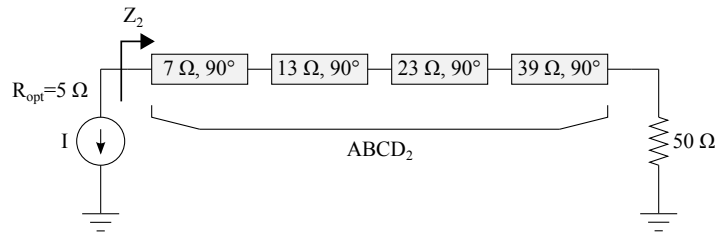
(b) 50 Ω to 5 Ω matching with four quarter-wave lines, achieving wider bandwidth.

Figure 4.17: Extending the matching bandwidth with multi-section transmission line.
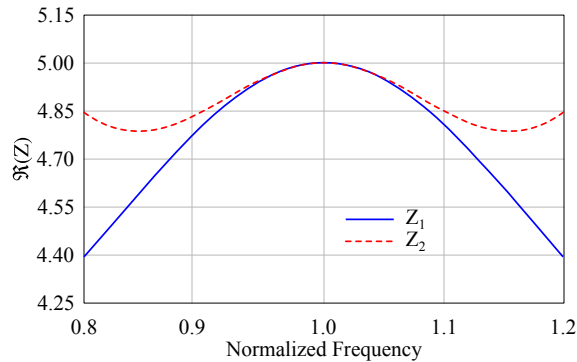
Figure 4.18: The impedances seen by the current sources in Figure 4.17 versus frequency.

Figure 4.18 shows the impedance Z_1 and Z_2 seen by the current sources in Figures 4.17a and 4.17b respectively versus the normalized frequency. As expected, the four-section matching deviates less from the intended 5 Ω impedance as the frequency deviates from the center frequency. However, when we compare the *ABCD* parameters of the two networks, we find that despite the wider impedance bandwidth of the four-section network, it is unsuitable for Doherty application because it has a narrower bandwidth over which the output at the 50 Ω reference plane behaves as a current source. To show the limited current source bandwidth, the *C* and *D* parameters of the *ABCD* parameter of the two and four section networks are plotted in Figure 4.18 with subscript 1 and 2 respectively. Ideally, the parameter *C* should be zero and the parameter *D* should be con-
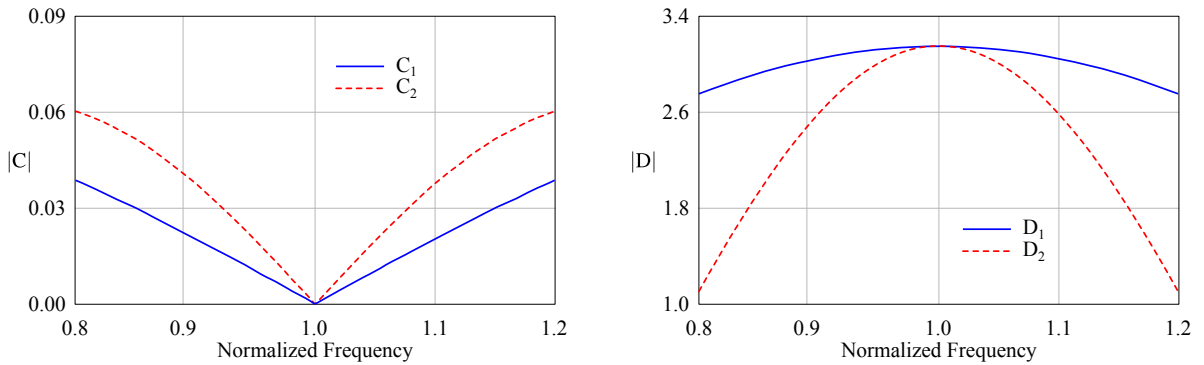
(a) The *C* parameter of the networks versus frequency.

(b) The *D* parameter of the networks versus frequency.

Figure 4.19: The *C* and *D* of the matching networks *ABCD* parameter in Figure 4.17.

stant so that the output current at the 50 Ω reference plane is strictly a function of the intrinsic current source. Comparing the *C* and *D* parameters versus normalized frequency in Figure 4.19a and 4.19b, we find that the two-section network has a wider bandwidth over which the output appears as a current source. But even in the two section network, the synthesis of the current source at the output is not ideal over frequency. The fact that a broadband matching network has a very narrowband impedance inverting property (i.e. poor *C* and *D* parameter bandwidth) was also discussed in [48].

Lastly, the offset lines and the quarter-wave line also increase the circuit size when compared to simple circuit presented in the Doherty amplifier theory, namely, a single quarter-wave line connecting the two devices and a load.

In summary, despite the widespread adoption by the industry and academia, the traditional design technique suffers from many limitations. In particular, it introduces band-limiting elements that are detrimental to the amplifier bandwidth. In subsequent chapters, we will propose an alternative design method that eliminates many of the shortcomings in the traditional design technique.

4.6 Conventional Doherty Power Amplifiers in the Literature

Table 4.1 summarizes the performances of conventional Doherty amplifiers found in the recent literature. The papers can be categorized into several area of focus. Many papers addressed the inadequate auxiliary current profile by using advanced techniques outlined in Section 4.4.3. For example, [49] used the adaptive input gate bias to mitigate the soft turn-on and the low peak auxiliary current in the symmetrical Doherty amplifier. Similarly, [50] used uneven input

Table 4.1: Conventional Doherty amplifiers in the literature.

Year [Ref.]	Device	f (GHz)	P_{out} (dBm)	Gain (dB)	η_{peak} (%)	η_{6dB} (%)	Note
2003 [49]	LDMOS	2.14	39	N/A	49[*]	26[*]	Adaptive gate
2005 [50]	LDMOS	2.14	40	14	N/A	40	Uneven input power
2008 [51]	HVHBT	2.14	53	9	72	57	HVHBT device
2008 [52]	GaN	2.14	43	N/A	68	54	Saturated mode
2009 [53]	GaN	2.14	35.1	4	55	44	Class F
2010 [54]	GaN	2.65	43.5	N/A	74	74	Saturated mode
2010 [55]	Si BJT	2.45	22.5	6	40[*]	27[*]	Uneven input power
2011 [56]	GaN	2.655	49.5	10	59	51	Knee region
2011 [57]	GaN	2.425	44.5	13	74	60	Mixed signal
2011 [58]	GaAs	9.5	29	6	49	42	Knee region
2011 [59]	LDMOS	2.14	53.2	N/A	53	50	Asymmetrical devices
2012 [60]	GaAs	2.14	31.6	9	74[*]	53[*]	Load optimization

[*] Power Added Efficiency

power division to achieve the proper auxiliary current profile for improved efficiency and linearity. Uneven input power division was also explored in [55] in the form of power-dependent power division by exploiting the nonlinear device input capacitance. In [59], the benefits of the asymmetrical Doherty amplifier was studied, which showed improved back-off efficiency when compared to the symmetrical Doherty amplifier. The use of a mixed-signal setup to improved the performance of the conventional Doherty amplifier was explored in [57].

Another area of research focused on improving the main amplifier efficiency by using high efficiency modes such as the saturated amplifier [52, 54] and the class F amplifier [53]. By using explicit harmonic control circuitry, the efficiency of the Doherty amplifier can be further improved at the cost of complexity and bandwidth.

In addition, conventional Doherty amplifiers implemented with emerging technologies such as GaN, high voltage hetero-junction bipolar transistor (HVHBT) [51], or integrated GaAs monolithic microwave integrated circuit (MMIC) technology [58, 60] have also been demonstrated in the literature. Papers such as [56, 58] also took into account the effect of the device knee region in their design to improve the linearity of the amplifier.

A common drawback of the papers listed in Table 4.1 is the limited bandwidth of the amplifier. Most papers did not include bandwidth results which suggest narrowband characteristics while those did report the bandwidth reported fractional bandwidth less than 8% [51, 54].

Chapter 5

Bandwidth Extension of the Doherty Power Amplifier

5.1 Introduction

From the analyses in Chapter 4, the conventional Doherty amplifier suffers from narrowband characteristics that can be attributed to theoretical and practical reasons. The conventional Doherty amplifier theory shows that, as a band-limited component, the quarter-wave line connecting the two devices results in back-off efficiency degradations when the operating frequency deviates from the center frequency. Moreover, the traditional Doherty amplifier design method introduces additional band-limited components such as the offset lines and the quarter-wave transformer to the RF output that further degrade the amplifier bandwidth. The limited bandwidth is confirmed in the literature review of the conventional Doherty amplifier where the highest reported fractional bandwidth is less than 8%.

To extended the Doherty amplifier bandwidth, we propose a new Doherty amplifier configuration with intrinsically broadband characteristics based on the analysis of the load modulation concept and the conventional Doherty amplifier. We also outline a different method to implement the proposed amplifier in practice that does not introduce any band-limited element so as to preserve the theoretical bandwidth potential of the proposed amplifier.

5.2 Previous Work

To differentiate the work presented in this chapter to those available in the literature, Table 5.1 lists the various attempts at the bandwidth extension of the Doherty amplifier in the recent literature. The approaches can be roughly divided into two categories: those that rely on a modified

Table 5.1: Extended bandwidth Doherty amplifiers in the literature.

Year [Ref.]	Device	f (GHz)	BW (%)	P_{out} (dBm)	Gain (dB)	η_{peak} (%)	η_{6dB} (%)	Note
2010 [65]	LDMOS[a]	1.7-2.3	30	~43	13	~55	~45	Mixed-signal
2011 [61]	GaN	1.7-2.6	41.9	~43	N/A	~50	~45[b]	Optimized matching
2012 [62]	GaN	2.2-2.96	29.5	~41	~6.5	~60	~40[b]	Optimized matching
2012 [63]	GaN	3.0-3.6	18.2	~43.5	~10	~60	~40	Optimized matching
2012 [66]	GaN	1.96-2.46	22.6	~43	~12	~60	~45	Mixed-signal
2012 [64]	GaN	1.96-2.46	22.6	~42	~10	~55	~40	Optimized matching
2012 [67]	GaN[a]	1.6-2.4	40	~42	~9	~63	~58	Mixed-signal[c]

[a] bare-die devices
[b] measured at 5-6 dB back-off
[c] asymmetrical drain bias

output matching network to achieve extended bandwidth, or those that rely on a mixed-signal setup which allows for input amplitude and phase adjustments across the design bandwidth. From Table 5.1, the papers that proposed various optimized output matching, namely [61–64], achieved peak efficiencies between 50% and 60% and back-off efficiencies between 40% and 45%. While these are encouraging results, the efficiency-bandwidth trade-off is significant when compared to a narrowband Doherty amplifier implemented with the same device at a similar frequency that achieved peak and back-off efficiencies of 74% [54]. Therefore, the literature suggests that output matching optimization alone is inadequate for effective bandwidth extension without significant performance trade-off.

On the other hand, [65–67] used the mixed-signal approach to improve the bandwidth of the Doherty amplifier. The efficiency results suggest that in certain cases, the mixed signal approach can be a viable candidate for the bandwidth extension of the Doherty amplifier. However, such an approach requires dual-path drivers as well as additional baseband processing for the adjustment of input amplitude and phase across the band. Of particular interest is [67] which achieved excellent results across a wide bandwidth. The work in [67], developed independently and published around the writing of this thesis, bears some similarity to this work in that asymmetrical drain bias is used. However, the theoretical derivation differs and a mixed-signal setup is mandatory in their approach.

In summary, the present literature lacks a simple solution that can effectively extend the bandwidth of the Doherty amplifier without introducing additional complexity. In the following sections, we propose a broadband Doherty amplifier configuration with an intrinsically broadband characteristic that can be implemented with commercially available packaged devices and does not require the use of a mixed-signal setup.
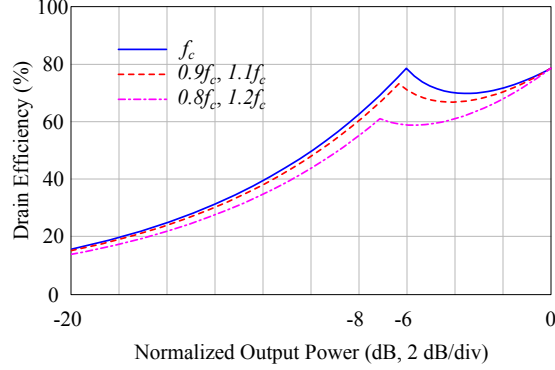
Figure 5.1: The conventional Doherty amplifier efficiency versus the normalized output power at various frequency deviations from f_c.

5.3 Proposed Doherty Amplifier with Extended Bandwidth

5.3.1 Derivation

The proposed broadband Doherty amplifier configuration is inspired by examining the conventional Doherty amplifier efficiency versus output power characteristics in Figure 4.8b, which is duplicated as Figure 5.1 for ease of reference.

From Figure 5.1, the efficiency enhancement at the back-off power level degrades as the frequency deviates from the center frequency f_c. But interestingly, the peak power efficiency appears insensitive to frequency variations. Understanding this lack of bandwidth limitation for the peak power efficiency in the conventional Doherty amplifier is a key step towards the formulation of the proposed broadband Doherty amplifier configuration.

To find the answer, we examine $\mathbf{Z_m}$, the impedance seen by the main device, in Figure 4.7b and find that at the peak power, $\mathbf{Z_m} = R_{opt}$ regardless of the frequency of operation, thus explaining the lack of efficiency degradations at the peak power. To understand how the supposedly narrowband quarter-wave transmission line in Figure 4.3 can present a constant R_{opt} at the peak power with no bandwidth restriction, we examine the load impedance seen by the transmission line, given by

$$\mathbf{Z_{load}} = \frac{\mathbf{V_L}}{\mathbf{I_T}} \tag{5.1}$$

Using (4.6) and (4.8), (5.1) simplifies to

$$\mathbf{Z_{load}} = \frac{R_L(\mathbf{I_m} + \mathbf{I_a}\cos\theta)}{\mathbf{I_m} - j(R_L/Z_T)\mathbf{I_a}\sin\theta} \tag{5.2}$$

86

With the conventional Doherty amplifier's Z_T and R_L from (4.23) and (4.24), and with $\mathbf{I_m}$ and $\mathbf{I_a}$ at the peak power given by

$$\mathbf{I_m} = \frac{I_{max}}{2} \tag{5.3}$$

and

$$\mathbf{I_a} = \frac{I_{max}}{2}\angle{-\theta} \tag{5.4}$$

(5.2) reduces to

$$\mathbf{Z_{load}} = R_{opt} \quad \forall\theta \tag{5.5}$$

at the peak power.

When we view (5.5) in light of the fact that the transmission line characteristic impedance Z_T in a conventional Doherty amplifier is also equal to R_{opt}, the reason $\mathbf{Z_m} = R_{opt}$ at the peak power for all frequencies becomes trivial to explain. Namely, that a transmission line terminated with a constant load equal to its characteristic impedance will have an input impedance equal to the load impedance regardless of the frequency.

With this key insight, we now derive the proposed broadband Doherty amplifier configuration. The proposed Doherty amplifier configuration is a synthesis of key ideas presented previously, which are summarized below:

1. The load modulation technique requires a VCVS and a VCCS in parallel with a load. In the Doherty amplifier, the VCVS is synthesized using a quarter-wave transmission line.

2. The operation of the Doherty amplifier can be completely described by four design parameters: $\mathbf{I_m}$, $\mathbf{I_a}$, Z_T, and R_L. These parameters are not independent: once the $\mathbf{I_m}$ and $\mathbf{I_a}$ are specified, Z_T and R_L can be derived.

3. The Doherty amplifier can exhibit broadband behaviour at a given power level if the load seen by the quarter-wave transmission line is equal to its characteristic impedance. For the conventional Doherty amplifier, this condition occurs at the peak power.

While 1) states the need to synthesize a VCVS for proper load modulation, we note that such a condition is irrelevant where load modulation does not occur, namely, below 6 dB back-off power. Combining this insight with 3), we propose a new Doherty configuration where

$$Z_T = R_L = 2R_{opt} \tag{5.6}$$

With (5.6), a broadband characteristic for the proposed Doherty amplifier is guaranteed at 6 dB back-off power and below.
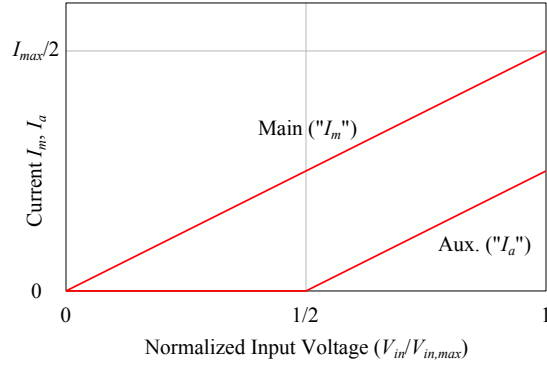
Figure 5.2: The main device current I_m and the auxiliary device current I_a versus the normalized input voltage of the proposed Doherty amplifier.

To complete the synthesis, we need to derive the corresponding $\mathbf{I_m}$ and $\mathbf{I_a}$ profiles versus V_{in} from Z_T and R_L. At the center frequency f_c, (4.19) can be applied with (5.6) to yield

$$I_a = I_m/2 \tag{5.7}$$

at the peak power, and

$$I_a = 0 \tag{5.8}$$

at 6 dB back-off power.

With (5.7) and (5.8), we propose the I_m and I_a profiles versus v_{in} shown in Figure 5.2, which are mathematically given as

$$I_m = v_{in}\left(\frac{I_{max}}{2}\right) \tag{5.9}$$

and

$$I_a = \begin{cases} 0, & 0 \leq v_{in} < 0.5 \\[2ex] \left(v_{in} - \frac{1}{2}\right)\left(\frac{I_{max}}{2}\right), & 0.5 \leq v_{in} \leq 1 \end{cases} \tag{5.10}$$

The proposed I_a versus v_{in} function in (5.10) is remarkable in that it can be easily realized in practice using an auxiliary device with the same size as the main device, except biased in class C. Therefore, advanced techniques outlined in Section 4.4.3 such as the asymmetrical Doherty, uneven input power division, or adaptive gate-biasing are no longer needed in the proposed Doherty amplifier.
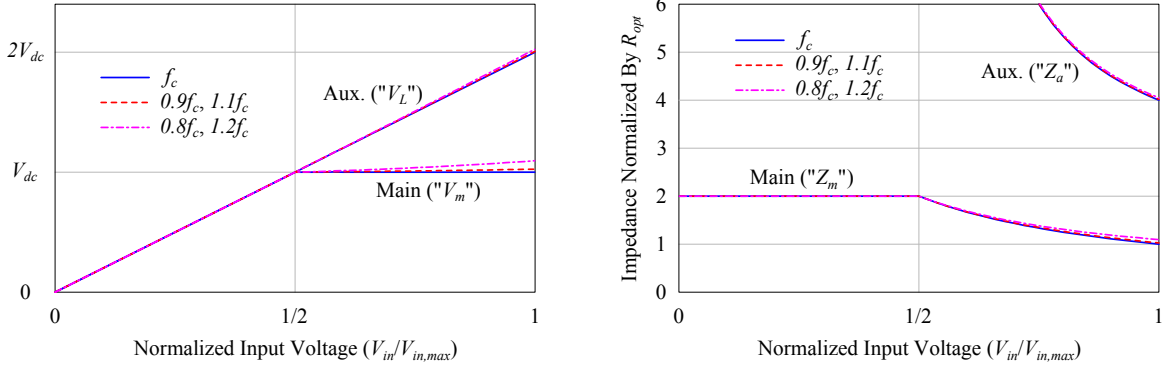
(a) The calculated main device voltage V_m and the voltage V_L across the load and the auxiliary device versus the normalized input voltage of the proposed Doherty amplifier at various frequency deviations from f_c.

(b) The calculated impedance Z_m and Z_a versus the normalized input voltage of the proposed Doherty amplifier at various frequency deviations from f_c.

Figure 5.3: The calculated voltage and impedance characteristics of the proposed Doherty amplifier versus the normalized input voltage at various frequency deviations from f_c.

5.3.2 Frequency Behaviour

Having defined the I_m and I_a profiles versus v_{in}, as well as Z_T, and R_L, we now derive the frequency behaviour of the proposed Doherty amplifier. Unlike the conventional Doherty amplifier, we will assume the phase relationship between $\mathbf{I_m}$ and $\mathbf{I_a}$ as defined in (4.27) instead of (4.28), a choice that is justified below.

Using (4.9), Figure 5.3a shows the voltage V_m across the main device versus v_{in}. At the center frequency f_c, the proposed V_m is identical to that of the conventional Doherty amplifier in Figure 4.7a. However, as the frequency deviates from f_c, V_m begins to swing with an amplitude greater than V_{dd}, the device drain bias voltage (with $V_m = 1.094V_{dd}$ at $0.8f_c$ and $1.2f_c$). This behaviour is problematic for a device biased in class B because the excess voltage swing will enter the device knee region and degrade the amplifier linearity. Selecting the $\mathbf{I_m}$ and $\mathbf{I_a}$ phase relationship of (4.27) instead of (4.28) minimizes this excess voltage swing. It is worth noting that with advanced modes of operation such as class F, the increased swing can theoretically be supported without linearity degradation for V_m up to $1.155V_{dd}$ [1, 10].

On the other hand, the voltage V_L across the auxiliary device and the load now swings twice as much as the V_L of the conventional Doherty amplifier in Figure 4.7a. As such, the DC drain bias of the auxiliary device needs to be twice that of the main device, given by

$$V_{dca} = 2V_{dcm} \tag{5.11}$$

From a practical perspective, the need for asymmetrical bias voltages implies the devices

89
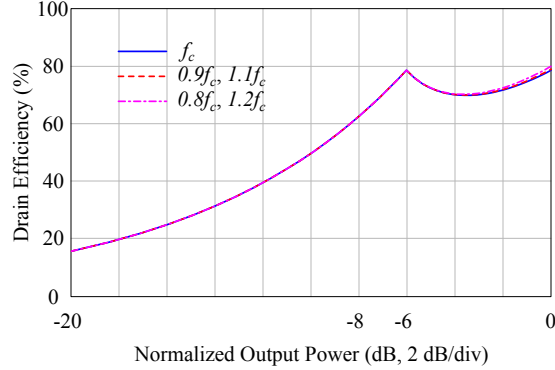
Figure 5.4: The calculated drain efficiency versus normalized output power of the proposed Doherty amplifier at various frequency deviations from f_c.

must have a high breakdown voltage. With the emergence of GaN devices where the latest reported breakdown voltage is around 300 V [68], we anticipate this disadvantage to be a non-issue in the near future. From a linearity perspective, a comparison between the V_L versus v_{in} transfer characteristics of Figure 4.7a and Figure 5.3a shows that the proposed Doherty amplifier also exhibits a better bandwidth-linearity trade-off than the conventional Doherty amplifier.

Figure 5.3b shows the load modulation in the proposed Doherty amplifier calculated using (4.10) and (4.11). At the center frequency f_c, Z_m, the impedance seen by the main device, is identical to that of the conventional Doherty with perfect tracking of R_o for up to 6 dB of back-off power. At the peak power, the auxiliary device now sees $4R_{opt}$ instead of R_{opt} because V_L is doubled while I_a is halved. Both Z_m and Z_a change little as the frequency deviates from f_c when compared to the conventional Doherty amplifier.

Finally, the efficiency versus normalized output power at various frequency deviations from f_c is plotted in Figure 5.4 using (4.16). At f_c, the efficiency curve and the peak output power are identical to that of the conventional Doherty power amplifier. There is no efficiency degradation at 6 dB back-off power as the frequency varies, whereas the peak efficiency is increased slightly because of an increased V_m. At 6 dB back-off power, the proposed Doherty amplifier is able to improve the efficiency by 5.4% at $0.9f_c$ and $1.1f_c$, and by 17.5% at $0.8f_c$ and $1.2f_c$ when compared to the conventional Doherty amplifier.

5.3.3 Advantages Beyond Bandwidth Extension

For clarity, the differences between the conventional and the proposed Doherty amplifier are summarized in Table 5.2. Aside from the extended bandwidth, there are two additional advantages in the proposed Doherty amplifier configuration:

Table 5.2: The conventional Doherty amplifier versus the proposed Doherty amplifier.

	Conventional Doherty	Proposed Doherty
I_m and I_a	See Figure 4.4a	See Figure 5.2
Z_T	R_{opt}	$2R_{opt}$
R_L	$R_{opt}/2$	$2R_{opt}$
Device sizes	Asymmetrical	Symmetrical
Bias voltages	Symmetrical	Asymmetrical
η vs. frequency	See Figure 4.8b	See Figure 5.4

Ease of Matching

From Table 5.2, the load resistance R_L of the proposed Doherty amplifier is four times that of the conventional Doherty amplifier. Therefore, the output matching to 50 Ω is easier to design because the impedance transformation ratio is reduced. Or equivalently, for the same matching network used in the conventional Doherty amplifier, the proposed Doherty amplifier is able to support a device with four times larger power.

Use of Symmetrical Devices

The use of symmetrical devices in the proposed Doherty amplifier is advantageous over the asymmetrical devices of the conventional Doherty amplifier for two reasons. From an output power perspective, symmetrical devices allow for higher output power because the largest device offered by a foundry can be used as the main device. In contrast, the conventional Doherty amplifier requires the largest device to be the auxiliary device and the main device to be 2.6 times smaller to obtain the desired I_m and I_a profile.

From a design perspective, because the symmetrical devices have similar device parasitic, circuit elements such as the bias network, input matching network, and stabilization network can be duplicated for the main and auxiliary devices, thus reducing the design complexity.

5.4   Building Blocks for Practical Implementation

To realize the proposed broadband Doherty amplifier in practice, we have to account for the device parasitic and package as well as the need for broadband input and output matching networks. To address the former, we expand upon the quasi-lumped transmission line concept in [65] by

Quasi-lumped quarter-wave TL at frequency f_c
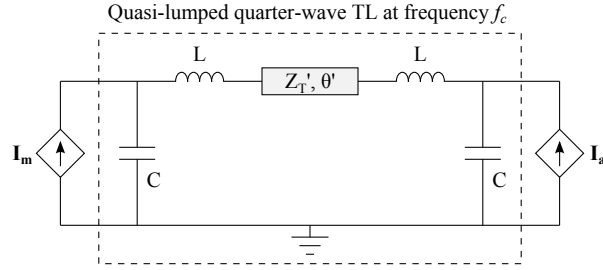
Figure 5.5: The absorption of the device output capacitance and bond-wire inductance to form the quasi-lumped quarter-wave transmission line.

formulating the absorption of arbitrary networks to form the quasi-lumped quarter-wave transmission line using the *ABCD*-parameters. For the latter, we explore the use of Klopfenstein taper to achieve broadband impedance matching. Unlike the conventional matching topology outlined in Section 4.5, the proposed matching structure does not include band-limited offset lines and quarter-wave transformers to the RF output. Therefore, the theoretical bandwidth potential of the proposed Doherty amplifier configuration is preserved. Finally, we discuss factors that cause practical Doherty amplifiers to deviate from the ideal characteristics outlined in the Section 5.5.

5.4.1 Quasi-lumped Quarter-wave Transmission Line

Because the intrinsic drain of a real transistor is embedded within the device parasitic and package, one cannot directly connect a quarter-wave transmission line between the intrinsic drains of the main and auxiliary devices. To approximate a quarter-wave transmission line between the intrinsic drains, [65] proposed a quasi-lumped quarter-wave transformer formed using the device output capacitances, bond-wires, and a modified transmission line, as shown in Figure 5.5.

To determine the parameter Z'_T and θ' of the modified transmission line such that the boxed circuit of Figure 5.5 approximates a quarter-wave transformer, we find the overall *ABCD*-parameter of the circuit and solve it against the *ABCD*-parameter of the ideal quarter-wave transmission line at the center frequency f_c. This approach is in contrast to the two-step solution presented in [65], which is simpler but not exact. Moreover, the method presented here can be generalized for any parasitic and package whose *ABCD*-parameters are known.

As an example, for the simplified model shown in Figure 5.5, the overall *ABCD*-parameter, $ABCD_Q$, is given by

$$ABCD_Q = ABCD_C * ABCD_L * ABCD_{TL} * ABCD_L * ABCD_C \tag{5.12}$$

where $ABCD_C$, $ABCD_L$, and $ABCD_{TL}$ are the *ABCD*-parameters of the device output capacitance C, the bond-wire inductance L, and the modified transmission line respectively. The assumption

92

of equal device parasitic and bond-wire for the main and auxiliary devices is valid because the proposed Doherty amplifier uses symmetrical devices. In fact, a symmetrical network has better impedance inverting properties than an asymmetrical network [48].

From (5.12), the matrix multiplication yields

$$A_Q = (1 - 2\omega^2 LC)\cos\theta' + \frac{\omega}{Z_T'}(\omega^2 L^2 C - L - CZ_T'^2)\sin\theta' \tag{5.13}$$

$$B_Q = j\{2\omega L\cos\theta' - \frac{1}{Z_T'}(\omega^2 L^2 - Z_T'^2)\sin\theta'\} \tag{5.14}$$

$$C_Q = j\{2\omega C(1 - \omega^2 CL)\cos\theta' + \frac{1}{Z_T'}(1 - 2\omega^2 CL + \omega^4 C^2 L^2 - \omega^2 C^2 Z_T'^2)\sin\theta'\} \tag{5.15}$$

$$D_Q = A_Q \tag{5.16}$$

From (4.4), at the center frequency f_c, the ideal quarter-wave transmission line has an ABCD-parameter, $ABCD_I$, given by

$$A_I = 0 \tag{5.17}$$

$$B_I = jZ_T \tag{5.18}$$

$$C_I = j(1/Z_T) \tag{5.19}$$

$$D_I = 0 \tag{5.20}$$

Although the two unknowns Z_T' and θ' appear to be overdetermined given the three equations (5.13) to (5.15), it can be shown that for the solution of Z_T' and θ' such that $A_Q = A_I = 0$, the equality $|B_Q| = 1/|C_Q|$ holds true. And given that $|B_I| = 1/|C_I|$ from (5.18) and (5.19), equations (5.14) and (5.15) are therefore not independent. As such, to solve for Z_T' and θ', we set $A_Q = A_I$ and $B_Q = B_I$ and use numerical method to determine the exact solution.

For practical designs, the *ABCD*-parameters of the complete parasitic and package model replace $ABCD_C$ and $ABCD_L$, thus enabling the calculation of Z_T' and θ' for any arbitrary networks to form the quasi-lumped quarter-wave transmission line.

5.4.2   Klopfenstein Taper for Broadband Impedance Matching

A key requirement unique to the proposed Doherty configuration is that R_L of Figure 4.3 must be broadband. Traditionally, R_L in the conventional Doherty is synthesized using a quarter-wave transformer that has a limited bandwidth.

In contrast, we synthesize the broadband R_L using a Klopfenstein taper that allows for a broadband real-to-real impedance matching above a given cutoff frequency [69]. In the implementation of the proposed Doherty amplifier, the Klopfenstein taper's cutoff frequency is set
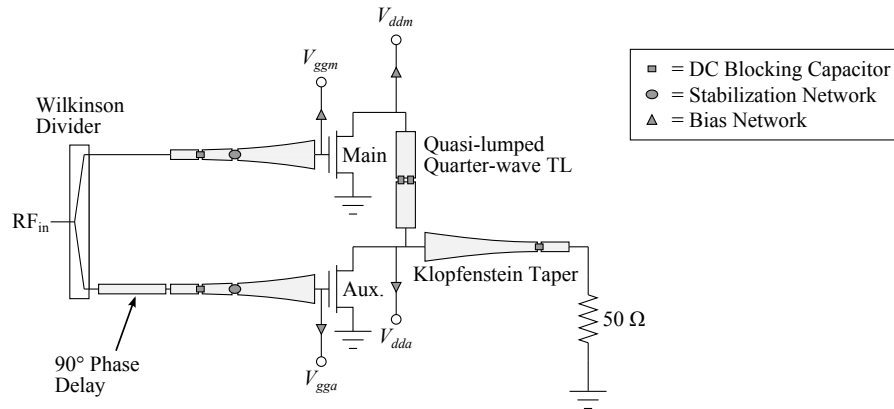
Figure 5.6: The circuit topology used to implement the proposed broadband Doherty amplifier.

lower than the amplifier's design frequency to achieve a constant R_L across the design frequency band. Together, the quasi-lumped quarter-wave transmission line and the Klopfenstein taper form the proposed output matching network shown in Figure 5.6.

Another unique requirement of the proposed Doherty amplifier is that the input matching network must maintain a proper phase relationship between the main and auxiliary devices across the design frequency band. In theory, such a network also has to absorb the device package and the input capacitance to provide good matching and high gain. To determine the best input matching topology, we carried out an empirical study that compared a multi-section network and the Klopfenstein taper. We found that while the multi-section network took up less area, the Klopfenstein taper was able to maintain the proper phase relationship over a broader bandwidth, though at the cost of lower amplifier gain. In addition, our study found that because the two GaN devices were biased in class AB and class C respectively, the different nonlinear input capacitances actually introduced additional phase shift between $\mathbf{I_m}$ and $\mathbf{I_a}$. As a result, we found that in practice, a Wilkinson divider with a phase delay line yielded better performance than a hybrid coupler. The chosen input matching topology, consisting of a 3 dB Wilkinson power divider, a 90° delay line, and two Klopfenstein tapers, is shown in Figure 5.6.

5.5   Factors Affecting the Doherty Amplifier Performance

Despite designers' best effort, practical Doherty amplifiers deviate from the ideal characteristics presented in Section 5.3 mainly because of two reasons: non-ideal device characteristics and matching network limitations.

94

Non-ideal Device Characteristics

From an efficiency perspective, the knee region in a real transistor limits the available voltage swing and can reduce the amplifier efficiency by 10% to 15% from the ideal value. Moreover, the class C biased auxiliary device exhibits a slow turn-on due to the varying conduction angle of the current versus the power, causing an efficiency degradation at the 6-dB back-off power level.

From a linearity perspective, the nonlinear transconductance g_m as well as voltage dependent capacitances cause the Doherty amplifier to be nonlinear in practice.

Matching Network Limitations

In the ideal analysis, the higher harmonics are assumed to be short circuit. In practice, such a condition is difficult to achieve without explicit harmonic stubs, which are inherently narrow-band. Instead, the output matching shown in Figure 5.6 relies on the output capacitance and the bias line adjustment to short out the harmonics. However, because of the imperfect harmonic matching, the efficiency deviates from the ideal characteristic, though current research suggests imperfect harmonic matching may still be optimized for high efficiency [70].

Moreover, although the device parasitic and package can be absorbed into the quasi-lumped quarter-wave transmission line, the load R_L cannot be directly connected to the intrinsic drain of the auxiliary device because of the package and parasitic. Therefore, the amplifier efficiency degrades due to the improper connection, especially at higher frequencies. The voltage dependent input capacitances also pose additional challenges because a varying capacitance cannot be resonated out using a static passive network.

Lastly, if the output matching network improperly allows the output voltage swing to enter the knee region, or if the matching results in improper load modulation, the amplifier linearity will also suffer. Finally, the insertion loss of the matching networks further degrades the efficiency of the amplifier.

5.6   Design and Validation

Based on the theoretical analysis presented in Section 5.3 and the practical design considerations discussed in Section 5.4, three broadband Doherty amplifier prototypes were designed using the circuit topology shown in Figure 5.6. A 90 W GaN broadband Doherty amplifier was initially fabricated to verify the proposed concept. Next, a 200 W GaN broadband Doherty amplifier demonstrated that the proposed technique can accommodate high power designs. Lastly, a 60 W LDMOS broadband amplifier was fabricated to show that the proposed technique is independent of technology. The prototype amplifiers targeted the 700 to 1000 MHz frequency range which
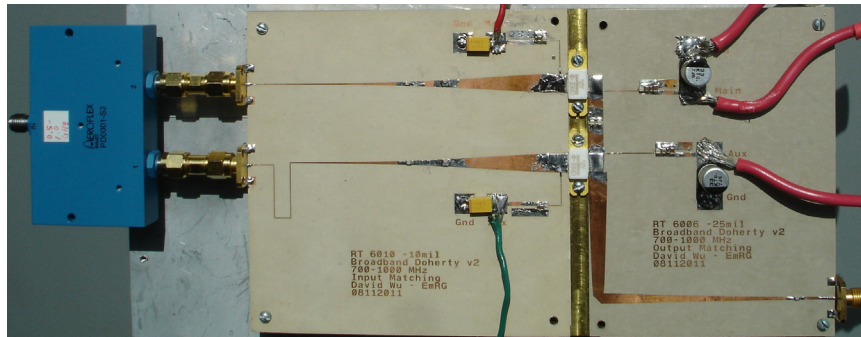
Figure 5.7: A picture of the fabricated 90 W broadband Doherty power amplifier.

included several LTE and UMTS frequency bands, as well as legacy GSM and CDMA bands [71].

5.6.1   A 90 W GaN Broadband Doherty Power Amplifier

The 90 W GaN broadband Doherty design used two commercially available 45 W CGH40045F packaged GaN transistor from Cree Inc. The main device was biased in deep class AB with a quiescent current of 400 mA and a drain voltage of 28 V. The auxiliary device was biased in class C with a gate voltage of -5.3 V and a drain voltage of 53.2 V. R_{opt} of 4.4 Ω was determined from the DC-IV simulation of the device and used to synthesize the quasi-lumped quarter-wave transmission line and the output Klopfenstein taper. The input matching network consisted of an external 3 dB Wilkinson power divider that operated from 500 to 1000 MHz, a delay line, and two Klopfenstein tapers which synthesized source impedances of 4 Ω for the main and auxiliary devices. Different substrates from Rogers Corp. were used to accommodate the impedance requirements of the input and the output matching networks. Figure 5.7 shows a picture of the fabricated 90 W broadband Doherty power amplifier with the input Wilkinson power divider.

Measurement

The fabricated broadband Doherty amplifier is measured without the use of a complex mixed-signal setup. Moreover, the amplifier was a first-pass design that did not require post-production tuning. Figure 5.8a shows the measured drain efficiency at the peak and 6 dB back-off power levels from 650 to 1050 MHz under a continuous-wave (CW) stimulus. Within the design frequency band from 700 to 1000 MHz, the average values of the peak efficiency and the 6 dB back-off efficiency were 67.3% and 60.6% respectively. The deviation from the ideal analysis can be primarily attributed to the soft turn-on of the auxiliary device and the knee region as discussed in Section 5.5. Figure 5.8b contains the measured peak output power and the associated

96
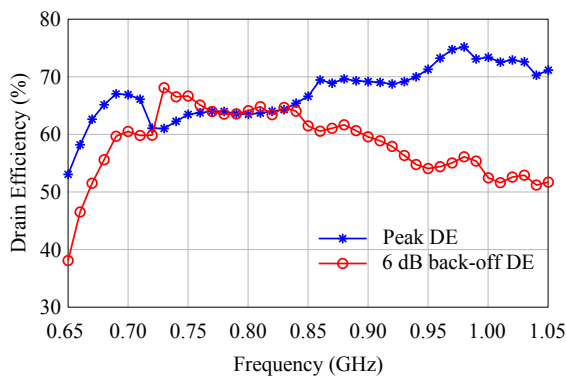
(a) The measured drain efficiency of the 90 W broadband Doherty amplifier at the peak power and 6 dB back-off power from 650 to 1050 MHz.
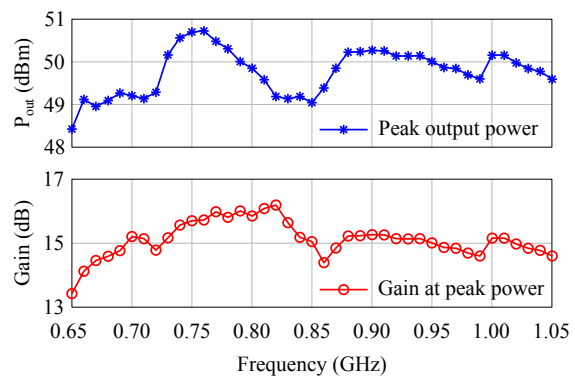
(b) The measured peak output power and the associated gain of the 90 W broadband Doherty amplifier from 650 to 1050 MHz.

Figure 5.8: The measured peak and 6 dB back-off drain efficiency, peak output power, and gain of the 90 W broadband Doherty amplifier from 650 to 1050 MHz.

(a) The simulated drain efficiency versus output power of the 90 W broadband Doherty amplifier at 700, 850, and 1000 MHz.
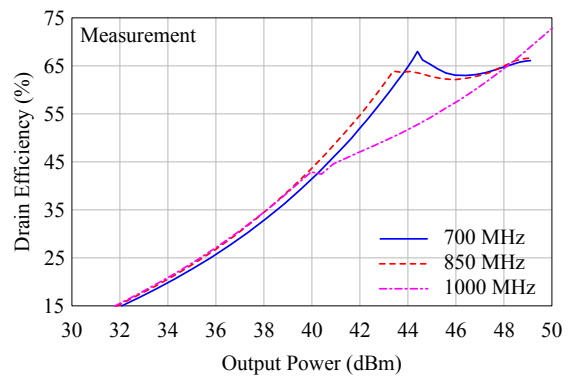
(b) The measured drain efficiency versus output power of the 90 W broadband Doherty amplifier at 700, 850, and 1000 MHz.

Figure 5.9: The simulated and measured drain efficiency versus output power of the 90 W broadband Doherty amplifier at 700, 850, and 1000 MHz.

gain versus frequency under a CW stimulus. From 700 to 1000 MHz, the average values of the peak output power and the associated gain were 49.9 dBm and 15.3 dB respectively.

To assess the efficiency enhancement at the back-off power levels, the drain efficiency versus output power was measured at different frequencies. Figures 5.9a and 5.9b show the simulated and measured drain efficiency versus output power at 700, 850, and 1000 MHz respectively. At 700 and 850 MHz, the measurements clearly show the two efficiency peaks as predicted by

97

(a) The simulated gain versus input power of the 90 W broadband Doherty amplifier at 700, 850, and 1000 MHz.

(b) The measured gain versus input power of the 90 W broadband Doherty amplifier at 700, 850, and 1000 MHz.

Figure 5.10: The simulated and measured gain versus input power of the 90 W broadband Doherty amplifier at 700, 850, and 1000 MHz.

the simulation. At 1 GHz, although the 6 dB back-off efficiency is still greater than 50%, the efficiency enhancement is reduced. The degradation can be attributed the non-ideal quasi-lumped quarter-wave transmission line and the improper load connection as discussed in Section 5.5.

To assess the linearity of the amplifier, we characterized the gain versus input power (i.e. AM–AM) at different frequencies. Figures 5.10a and 5.10b show the simulated and measured gain versus input power at 700, 850, and 1000 MHz respectively. Although the gains at the peak power for the three frequencies are similar, the small signal gains are higher at lower frequencies. These trends were predicted by the simulation. The nonlinear AM–AM characteristic of the amplifier can be attributed to the nonlinear device transconductance and the imperfect load modulation as stated in Section 5.5.

Linearization

To assess the linearizability of the 90 W GaN broadband Doherty amplifier at different frequencies, the amplifier was first driven with a four-carrier 20 MHz WCDMA 1111 modulated signal at 880 MHz, then characterized using a 20 MHz LTE signal at 740 MHz. The frequencies were selected to reflect the actual allocated frequencies of the respective wireless standards. The 20 MHz WCDMA and LTE input signals were clipped to PAPRs of 7.14 and 10.51 dB respectively.

For linearization, we used the digital pre-distortion (DPD) algorithm based on pruned Volterra series using Wiener G-functionals [72]. Figure 5.11a shows the measured output spectra before and after DPD linearization when the amplifier was driven with the 20 MHz WCDMA 1111 signal at 880 MHz. The ACPR improved from -29.57 to -51.26 dBc and the amplifier achieved
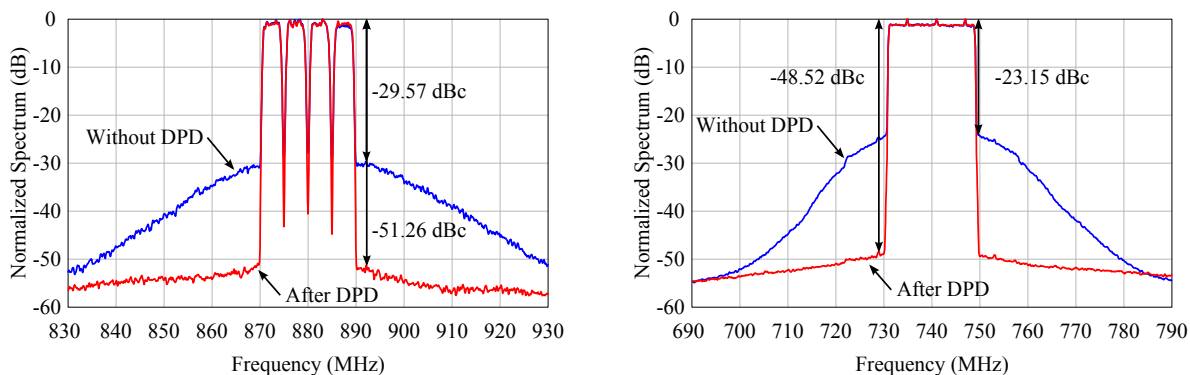
(a) The measured output spectra of the 90 W broadband Doherty amplifier before and after the DPD linearization when driven with a 20 MHz WCDMA 1111 signal at 880 MHz.

(b) The measured output spectra of the 90 W broadband Doherty amplifier before and after the DPD linearization when driven with a 20 MHz LTE signal at 740 MHz.

Figure 5.11: The measured output spectra of the 90 W broadband Doherty amplifier before and after the DPD linearization when driven with 20 MHz LTE and 20 MHz WCDMA 1111 signals.

an average output power of 42.74 dBm with an associated drain efficiency of 54.9%. Similarly, Figure 5.11b shows the output spectra before and after DPD when the amplifier was driven with the 20 MHz LTE signal at 740 MHz. The ACPR improved from -25.15 to -48.52 dBc and the amplifier achieved an average output power of 39.14 dBm with an associated drain efficiency of 44.9%. Moreover, the 10 ms LTE frame was captured and decoded to determine the data error vector magnitude (EVM) which has to be less than 8% for 64 QAM sub-carrier modulation. The EVM before and after DPD was 9.2% and 1.6% respectively, with the clipped input signal EVM being 1.2%.

The linearization result demonstrates that despite the nonlinear AM–AM characteristics, the 90 W GaN broadband Doherty amplifier is highly correctable even when driven with 20 MHz wideband signals.

5.6.2   A 200 W GaN Broadband Doherty Power Amplifier

The 200 W GaN broadband Doherty was designed to demonstrate that the proposed concept is suitable for high power designs where the device has a low matching impedance. The 200 W design used two commercially available 45 W CGH40120F packaged GaN transistor from Cree Inc. The main device was biased in deep class AB with a quiescent current of 500 mA and a drain voltage of 32 V. The auxiliary device was biased in class C with a gate voltage of -6.4 V and a drain voltage of 60.8 V. Figure 5.12 shows a picture of the fabricated 200 W broadband Doherty power amplifier with the input Wilkinson power divider.

Figure 5.12: A picture of the fabricated 200 W broadband Doherty power amplifier.
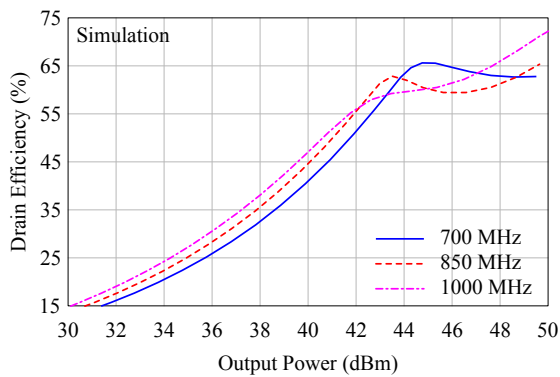

(a) The measured drain efficiency of the 200 W broadband Doherty amplifier at the peak power and 6 dB back-off power from 650 to 1050 MHz.

(b) The measured peak output power and the associated gain of the 200 W broadband Doherty amplifier from 650 to 1050 MHz.

Figure 5.13: The measured peak and 6 dB back-off drain efficiency, peak output power, and gain of the 200 W broadband Doherty amplifier from 650 to 1050 MHz.

Measurement

The 200 W GaN broadband Doherty amplifier was a first-pass design that did not require post-production tuning. Figure 5.13a shows the measured drain efficiency at the peak and 6 dB back-off power levels from 650 to 1050 MHz under a CW stimulus. Within the design frequency band from 700 to 1000 MHz, the average values of the peak efficiency and the 6 dB back-off efficiency were 61.3% and 55.9% respectively. Figure 5.13b contains the measured peak output power and the associated gain versus frequency under a CW stimulus. From 700 to 1000 MHz, the average values of the peak output power and the associated gain were 52.7 dBm and 14.9 dB respectively.

To assess the efficiency enhancement at the back-off power levels, the drain efficiency versus output power was measured at different frequencies. Figures 5.14a and 5.14b show the simulated

(a) The simulated drain efficiency versus output power of the 200 W broadband Doherty amplifier at 700, 850, and 1000 MHz.
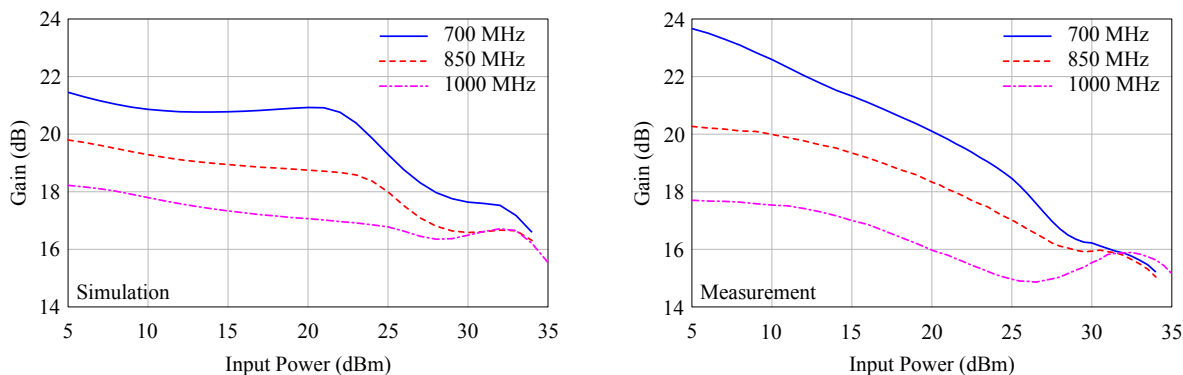
(b) The measured drain efficiency versus output power of the 200 W broadband Doherty amplifier at 700, 850, and 1000 MHz.

Figure 5.14: The simulated and measured drain efficiency versus output power of the 200 W broadband Doherty amplifier at 700, 850, and 1000 MHz.


(a) The simulated gain versus input power of the 200 W broadband Doherty amplifier at 700, 850, and 1000 MHz.

(b) The measured gain versus input power of the 200 W broadband Doherty amplifier at 700, 850, and 1000 MHz.

Figure 5.15: The simulated and measured gain versus input power of the 200 W broadband Doherty amplifier at 700, 850, and 1000 MHz.

and measured drain efficiency versus output power at 700, 850, and 1000 MHz respectively. Similar to the 90 W GaN broadband Doherty, at 700 and 850 MHz, the measurements show the two efficiency peaks as predicted by the simulation. However, at 1 GHz, measurement degradation can be observed due to reasons outlined in Section 5.5.

Figures 5.15a and 5.15b show the simulated and measured gain versus input power at 700, 850, and 1000 MHz respectively. The measurement trends were predicted by the simulation.
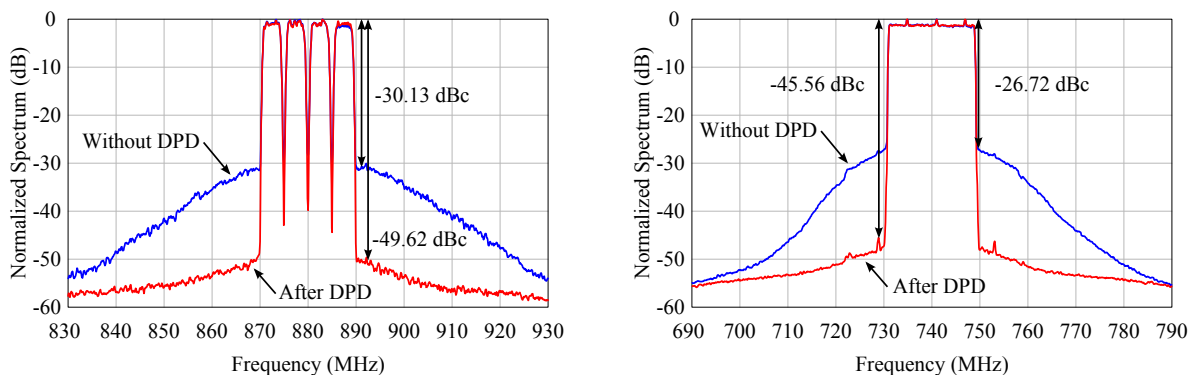
(a) The measured output spectra of the 200 W broadband Doherty amplifier before and after the DPD linearization when driven with a 20 MHz WCDMA 1111 signal at 880 MHz.

(b) The measured output spectra of the 200 W broadband Doherty amplifier before and after the DPD linearization when driven with a 20 MHz LTE signal at 740 MHz.

Figure 5.16: The measured output spectra of the 200 W broadband Doherty amplifier before and after the DPD linearization when driven with 20 MHz LTE and 20 MHz WCDMA 1111 signals.

Linearization

To assess the linearizability of the 200 W GaN broadband Doherty amplifier, the amplifier was driven with a four-carrier 20 MHz WCDMA 1111 modulated signal at 880 MHz and a 20 MHz LTE signal at 740 MHz. Figure 5.16a shows the measured output spectra before and after DPD linearization when the amplifier was driven with the 20 MHz WCDMA 1111 signal at 880 MHz. The ACPR improved from -30.13 to -49.62 dBc and the amplifier achieved an average output power of 45.01 dBm with an associated drain efficiency of 49.7%. Similarly, Figure 5.16b shows the output spectra before and after DPD when the amplifier was driven with the 20 MHz LTE signal at 740 MHz. The ACPR improved from -26.72 to -45.56 dBc and the amplifier achieved an average output power of 42.81 dBm with an associated drain efficiency of 41.9%. The 10 ms LTE frame was captured and decoded to determine the data EVM. The EVM before and after DPD was 6.9% and 2.3% respectively, with the clipped input signal EVM being 1.2%.

The linearization results demonstrate that the proposed technique can be used to design high power amplifier and that the 200 W GaN broadband Doherty amplifier is linearizable when driven with 20 MHz wideband signals.

5.6.3 A 60 W LDMOS Broadband Doherty Power Amplifier

The 60 W LDMOS broadband Doherty was designed to demonstrate that the proposed concept is independent of the technology used, despite the fact that GaN is more suitable given the higher
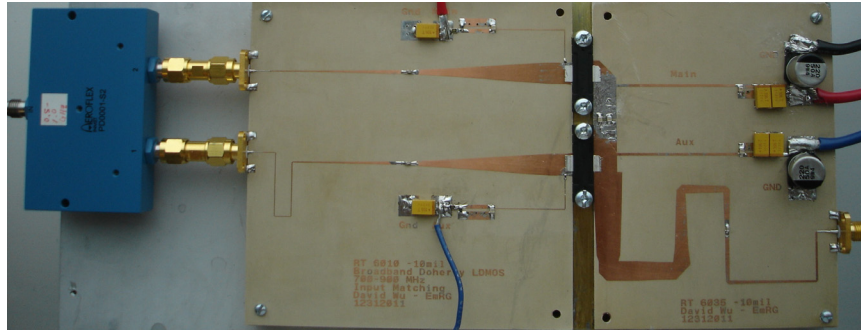
Figure 5.17: A picture of the fabricated 60 W broadband Doherty power amplifier.

breakdown voltage. The 60 W design used two commercially available 45 W MRFE6S9045N packaged LDMOS transistor from Freescale Semiconductor Inc. Because of the larger device parasitic in a LDMOS device, we chose a frequency of operation from 700 to 900 MHz. In addition, to accommodate the lower breakdown voltage of the LDMOS device, the main device was biased in deep class AB with a quiescent current of 350 mA and a down-biased drain voltage of 18 V. The auxiliary device was biased in class C with a gate voltage of 1.0 V and a drain voltage of 32.4 V. Because of the lower drain bias of the main device, the amplifier output was 60 W. Figure 5.17 shows a picture of the fabricated 60 W broadband Doherty power amplifier with the input Wilkinson power divider.

Measurement
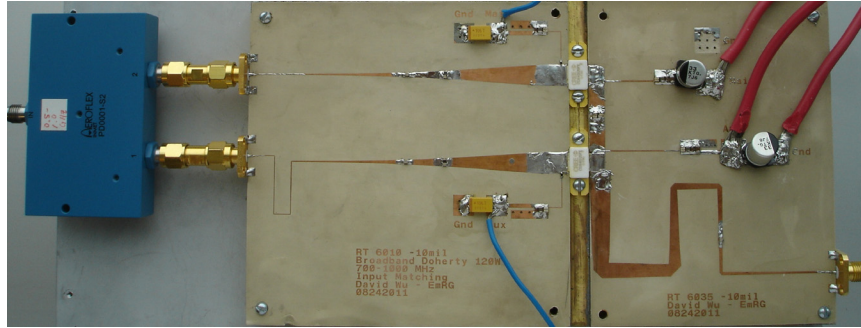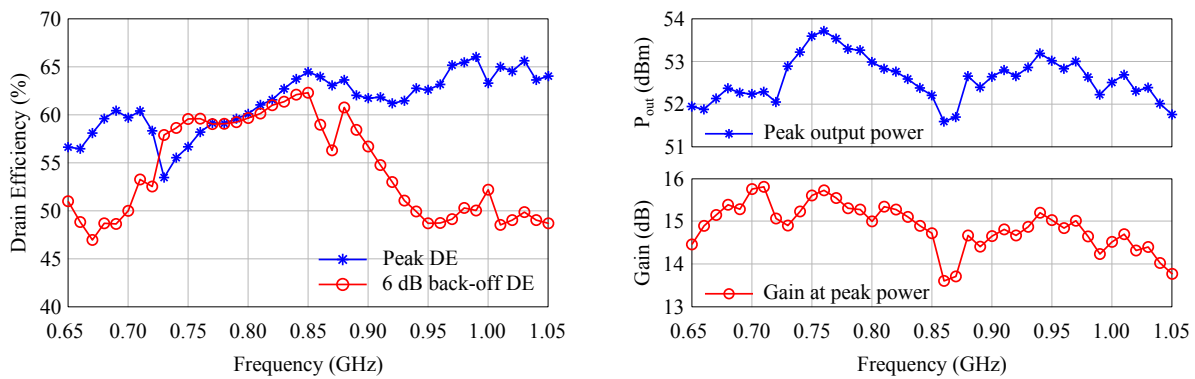
The 60 W LDMOS broadband Doherty amplifier was also a first-pass design that did not require post-production tuning. Figure 5.18a shows the measured drain efficiency at the peak and 6 dB back-off power levels from 650 to 950 MHz under a CW stimulus. Within the design frequency band from 700 to 900 MHz, the average values of the peak efficiency and the 6 dB back-off efficiency were 61.5% and 57.4% respectively. Figure 5.18b contains the measured peak output power and the associated gain versus frequency under a CW stimulus. From 700 to 900 MHz, the average values of the peak output power and the associated gain were 48.5 dBm and 11.5 dB respectively.

To assess the efficiency enhancement at the back-off power levels, the drain efficiency versus output power was measured at different frequencies. Figures 5.19a and 5.19b show the simulated and measured drain efficiency versus output power at 700, 800, and 900 MHz respectively. The measurement showed lower efficiency characteristic than the simulation. However, the measurement trends were well predicted by the simulation.

Figures 5.20a and 5.20b show the simulated and measured gain versus input power at 700, 800, and 900 MHz respectively. Although the measured shapes of the gain curve were well
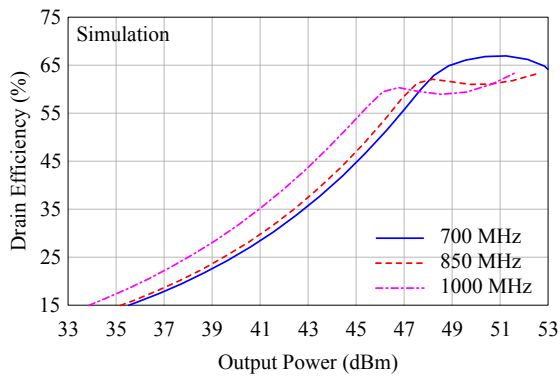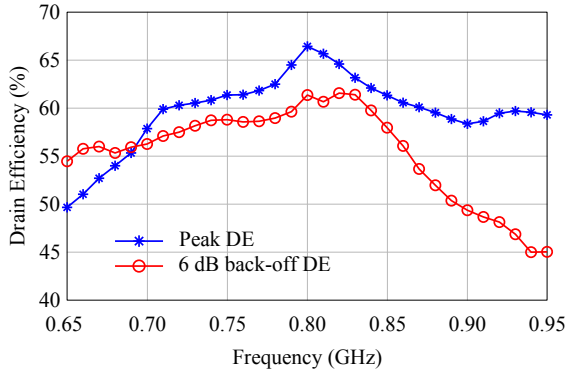
(a) The measured drain efficiency of the 60 W broad-band Doherty amplifier at the peak power and 6 dB back-off power from 650 to 950 MHz.
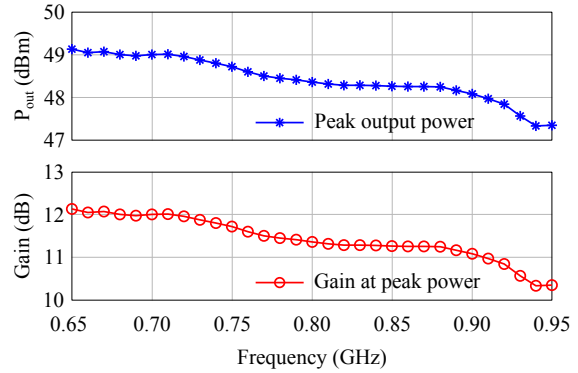
(b) The measured peak output power and the associated gain of the 60 W broadband Doherty amplifier from 650 to 950 MHz.

Figure 5.18: The measured peak and 6 dB back-off drain efficiency, peak output power, and gain of the 60 W broadband Doherty amplifier from 650 to 950 MHz.
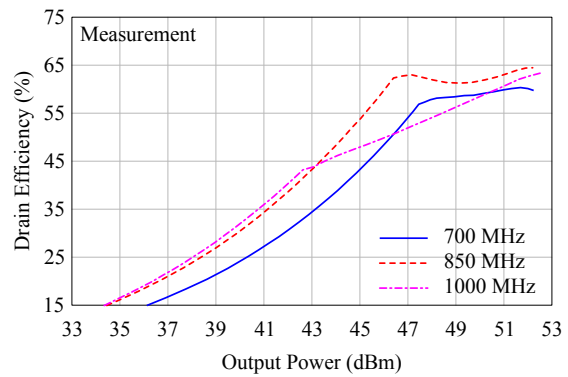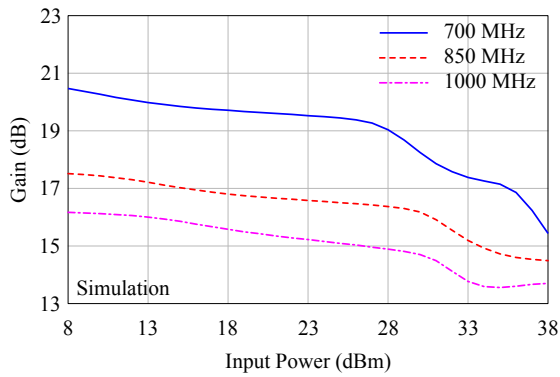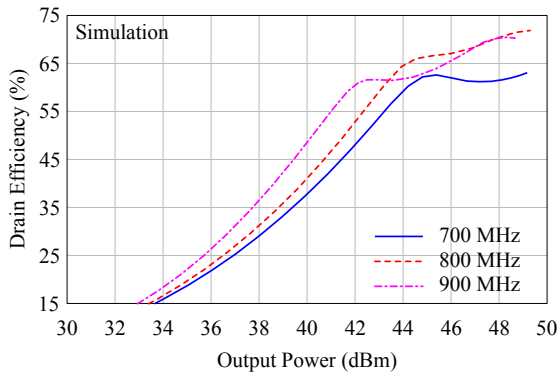

(a) The simulated drain efficiency versus output power of the 60 W broadband Doherty amplifier at 700, 800, and 900 MHz.
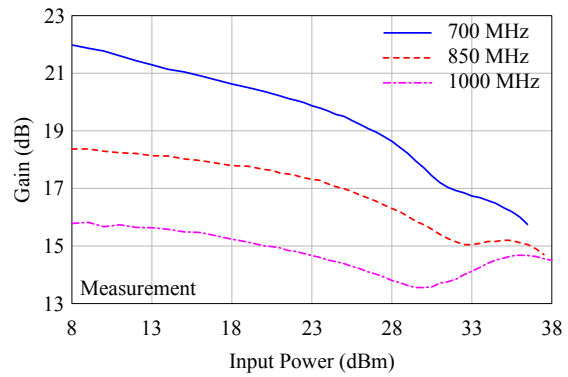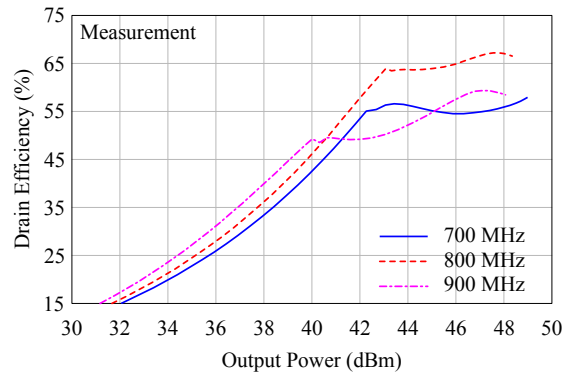
(b) The measured drain efficiency versus output power of the 60 W broadband Doherty amplifier at 700, 800, and 900 MHz.

Figure 5.19: The simulated and measured drain efficiency versus output power of the 60 W broadband Doherty amplifier at 700, 800, and 900 MHz.
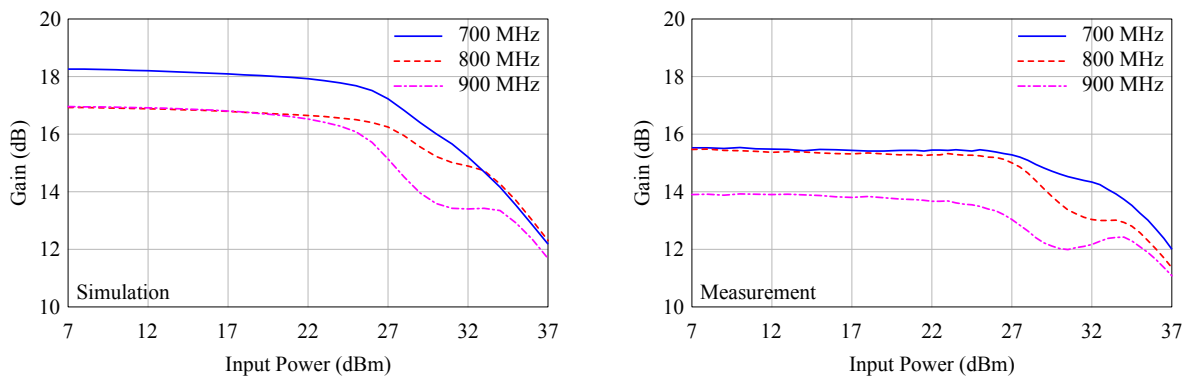
(a) The simulated gain versus input power of the 60 W broadband Doherty amplifier at 700, 800, and 900 MHz.

(b) The measured gain versus input power of the 60 W broadband Doherty amplifier at 700, 800, and 900 MHz.

Figure 5.20: The simulated and measured gain versus input power of the 60 W broadband Doherty amplifier at 700, 800, and 900 MHz.

predicted by the simulation, the small signal gain was off by about 2 dB. This discrepancy is likely due to the input matching network presenting inadequate matching over the bandwidth.

Linearization

To assess the linearizability of the 60 W LDMOS broadband Doherty amplifier, the amplifier was driven with a four-carrier 20 MHz WCDMA 1111 modulated signal at 880 MHz and a 20 MHz LTE signal at 740 MHz. Figure 5.21a shows the measured output spectra before and after DPD linearization when the amplifier was driven with the 20 MHz WCDMA 1111 signal at 880 MHz. The ACPR improved from -25.39 to -51.35 dBc and the amplifier achieved an average output power of 41.3 dBm with an associated drain efficiency of 48.4%. Similarly, Figure 5.21b shows the output spectra before and after DPD when the amplifier was driven with the 20 MHz LTE signal at 740 MHz. The ACPR improved from -37.32 to -53.0 dBc and the amplifier achieved an average output power of 38.03 dBm with an associated drain efficiency of 35.5%. The 10 ms LTE frame was captured and decoded to determine the data EVM. The EVM before and after DPD was 2.5% and 1.4% respectively, with the clipped input signal EVM being 1.2%.

The linearization results demonstrate that the proposed technique is independent of technology and that the 60 W LDMOS broadband Doherty amplifier is highly linearizable when driven with 20 MHz wideband signals.
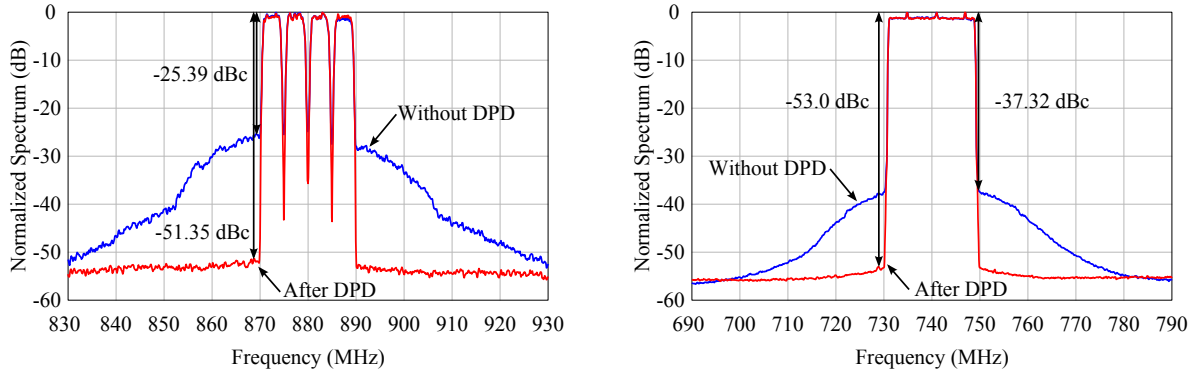
(a) The measured output spectra of the 60 W broadband Doherty amplifier before and after the DPD linearization when driven with a 20 MHz WCDMA 1111 signal at 880 MHz.

(b) The measured output spectra of the 60 W broadband Doherty amplifier before and after the DPD linearization when driven with a 20 MHz LTE signal at 740 MHz.

Figure 5.21: The measured output spectra of the 60 W broadband Doherty amplifier before and after the DPD linearization when driven with 20 MHz LTE and 20 MHz WCDMA 1111 signals.

Table 5.3: A performance summary of the three broadband Doherty amplifier prototypes.

Design	f (GHz)	BW (%)	P_{out} (dBm)	Gain (dB)	η_{peak} (%)	η_{6dB} (%)
90 W GaN broadband Doherty	0.7-1.0	35.3	49.9	15.3	67.3	60.6
200 W GaN broadband Doherty	0.7-1.0	35.3	52.7	14.9	61.3	55.9
60 W LDMOS broadband Doherty	0.7-0.9	25.0	48.5	11.5	61.5	57.4

5.6.4 Summary

Table 5.3 summarizes the measurement results of the three broadband Doherty amplifier prototypes. Although our design frequency bands are lower than those in the literature in Table 5.1, the larger device sizes mean the matching network design challenges are comparable. The 90 W broadband Doherty amplifier outperforms all others in terms of output power, gain, peak efficiency and back-off efficiency. This performance improvement is possible because the said prototype is designed base on a novel Doherty amplifier configuration with an intrinsically broadband characteristic. In addition, the proposed amplifier is simple and does not require a mixed signal setup to achieve broadband operation.

Chapter 6

Extended Doherty Power Amplifier with Reconfigurable Back-off Level

6.1   Introduction

As mentioned previously, modern wireless standards such as LTE and WiMAX have signals with a high PAPR in the range of 8 to 12 dB. Although the conventional Doherty amplifier enables back-off efficiency enhancements when compared to a single-ended amplifier, the auxiliary device in the conventional Doherty amplifier provides load modulation only up to 6 dB of back-off power from the peak power.

To address this shortcoming, we propose a Doherty amplifier with an extended back-off level greater than 6 dB by using insights derived in the previous chapters. This approach uses a combination of different current profiles and asymmetrical drain bias voltages to achieve extended back-off efficiency enhancements. Moreover, we show that the proposed amplifier not only has an extended bandwidth like in Chapter 5, but that its back-off power level can actually be reconfigured dynamically by adjusting the device bias points. Lastly, unlike a previous work [67], our approach does not require a complex mixed-signal setup.

In addition, we also address a shortcoming when asymmetrical drain bias voltages are used, namely, that when the main and auxiliary devices are implemented using the same technology, the device with the lower drain bias must be underutilized since the full available voltage swing is not achieved at the peak power. To overcome this problem, we propose a mixed-technology Doherty amplifier where the main and auxiliary devices are implemented with an LDMOS device and a GaN device respectively. By choosing technologies with suitable breakdown voltages for the main and auxiliary devices, the power utilization factor and the watts per dollar cost are improved. Lastly, we explore how the proposed amplifier can be optimally configured for a given modulated signal to achieve the highest average efficiency.

6.2 Previous Work

To distinguish our work from the previous work on extended back-off Doherty amplifiers, we briefly review the available literature. To achieve efficiency enhancement at back-off levels greater than 6 dB, two popular Doherty amplifier variants have been proposed, namely, the N-way Doherty amplifier [73–75] and the N-stage Doherty amplifier [76–79]. The N-way Doherty amplifier is a variant of the asymmetrical Doherty amplifier where $N-1$ auxiliary devices turn on simultaneously with specific current profiles to achieve an extended back-off efficiency enhancement [74]. Like the conventional Doherty amplifier, the N-way Doherty amplifier has two efficiency peaks.

The N-stage Doherty amplifier, on the other hand, achieves an extended back-off efficiency enhancement by load modulating the auxiliary device with more devices. For a three-stage Doherty amplifier, two auxiliary devices turn on at different back-off levels resulting in three efficiency peaks. The classical three-stage Doherty requires a mixed-signal setup due to the early saturation of the main device current [77, 80]. Recently, a novel three-stage Doherty amplifier has been proposed that can be implemented without using a mixed-signal setup [81]. However, adaptive gate biasing is still needed to mitigate the low peak current of the auxiliary devices when symmetrical devices are used [79].

Although the N-way and N-stage Doherty amplifiers enable extended back-off efficiency enhancements, a major drawback of these techniques is the increased design complexity. For example, the three-way and three-stage Doherty amplifiers require three-way input splitters as well as complex output combining schemes that also tend to reduce the amplifier bandwidth.

Recently in [67] and [82], Gustafsson *et al.* independently showed that asymmetrical drain bias voltages allowed for extended bandwidth as well as extended back-off efficiency enhancements. However, in their approach, a mandatory mixed-signal setup is needed to achieve reconfigurable back-off level with the adjustment of the main device drain bias voltage. In contrast, the proposed amplifier in the subsequent sections does not require a mixed-signal setup. Therefore, our approach significantly reduces the design complexity since dual path drivers and additional base-band processing are no longer needed.

A summary of Doherty amplifiers with extended back-off efficiency enhancements in the literature are outlined in Table 6.1.

Table 6.1: Doherty amplifiers with extended back-off efficiency enhancements in the literature.

Year [Ref.]	Device	f (GHz)	Back-off (dB)	P_{out} (dBm)	Gain (dB)	η_{peak} (%)	η_{bo} (%)	Note
2001 [74]	GaAs	0.95	9	27.5	10	46	45	Asym. devices
2005 [76]	GaAs	1.95	12	33	12.2	48.5	27	3-stage
2007 [77]	LDMOS	2.14	12	41	~12	64	43	3-stage mixed-signal
2008 [78]	GaN	2.14	12	50	~10	68	64	3-stage mixed-signal
2010 [79]	GaN	2.655	8	50.5	~9	~54	~55	3-stage adaptive-gate
2011 [83]	GaN	2.14	~ 8.5	44.5	~12	66	~50	Mixed-signal
2012 [67]	GaN[a]	1.6-2.4	~ 10	~42	~9	~63	~60	Mixed-signal[b]

[a] bare-die
[b] asymmetrical drain bias

6.3 Extended Doherty Amplifier with Reconfigurable Back-off Level

6.3.1 Derivation

A key insight from the previous analysis of the conventional Doherty amplifier is that the modulation of the impedance $\mathbf{Z_m}$ seen by the main device is completely described by four design parameters. This result is seen in (4.19), which is repeated as (6.1) for ease of reference.

$$\mathbf{Z_m} = \left(\frac{Z_T}{R_L} - \frac{I_a}{I_m} \right) Z_T \tag{6.1}$$

From (6.1), the modulation of the impedance $\mathbf{Z_m}$ is completely described by I_m, I_a, Z_T, and R_L. By properly choosing these four design parameters, $\mathbf{Z_m}$ can be engineered to track a given impedance profile up to any desired back-off power level as shown in the next section. The derivation eventually leads to to a surprising result, namely, the reconfigurability of the back-off power level without the need to redesign the matching networks.

6.3.2 Auxiliary Current Profile I_a for Extended Back-off Efficiency Enhancement

To aid our derivation, we briefly review the class B optimal impedance versus drive level. For the main device biased in class B, the optimal load R_o that maximizes the efficiency at a given

Figure 6.1: The impedance that yields the maximum amplifier efficiency versus the normalized input voltage v_{in} for a device biased in class B.

input voltage V_{in} is given by

$$R_o(V_{in}) = \frac{V_{dcm}}{I_m} = \frac{V_{dcm}}{g_m V_{in}} \tag{6.2}$$

where V_{dcm} is the main device drain bias voltage and g_m is the device transconductance in class B.

At the maximum input voltage $V_{in} = V_{in,max}$, corresponding to $I_m = I_{max}/2$, the optimal impedance, also known as R_{opt}, is given by

$$R_{opt} = \frac{2V_{dcm}}{I_{max}} \tag{6.3}$$

where I_{max} is the main device saturation current.

Normalizing R_o by R_{opt}, and setting $v_{in} = V_{in}/V_{in,max}$, R_o versus v_{in} is plotted in Figure 6.1. For the main device to maintain maximum efficiency as v_{in} is reduced, $\mathbf{Z_m}$ must perfectly track the impedance profile shown in Figure 6.1.

Although there are multiple combinations of I_m, I_a, Z_T and R_L that enable Z_m to track R_o of Figure 6.1 up to a specified back-off power level, we focus on the combinations with the unique properties of extended bandwidth as well as reconfigurable back-off efficiency enhancement. For the back-off efficiency peak to occur at X dB back-off from the peak power, the required auxiliary current profile I_a can be derived as follows,

Find R_o at X dB Back-off

At X dB back-off from peak power (where X is a positive number), the optimal load R_o is found from (6.2), given by

$$R_o(V_{in,X}) = \frac{V_{dcm}}{g_m V_{in,X}} = 10^{\frac{X}{20}} R_{opt} \tag{6.4}$$

where $V_{in,X}$ is given by

$$V_{in,X} = 10^{\frac{-X}{20}} V_{in,max} \tag{6.5}$$

Set Parameters Z_T and R_L

For a Doherty operation with extended and reconfigurable back-off level, we set $Z_T = R_L = R_o(V_{in,X})$, namely,

$$Z_T = R_L = 10^{\frac{X}{20}} R_{opt} \tag{6.6}$$

Determine I_a Profile

Replacing $\mathbf{Z_m}$ with R_o in (6.1) and solving for I_a yields

$$I_a = \left(\frac{Z_T}{R_L} - \frac{R_o}{Z_T} \right) I_m \tag{6.7}$$

Using (6.2) and (6.6), (6.7) simplifies to

$$I_a = I_m - \frac{10^{\frac{-X}{20}} I_{max}}{2} \tag{6.8}$$

From (6.8), I_a is simply I_m shifted by a constant. Since the range of I_m is given by

$$0 \leq I_m \leq \frac{I_{max}}{2} \tag{6.9}$$

I_a therefore has a range of

$$\frac{-10^{\frac{-X}{20}} I_{max}}{2} \leq I_a \leq \frac{I_{max}}{2}(1 - 10^{\frac{-X}{20}}) \tag{6.10}$$

The portion of I_a that is negative corresponds to the auxiliary device behaving as an active load rather than a power source. Therefore, although (6.8) enables Z_m to track R_o completely, the portion where I_a is negative actually degrades, rather than enhances, the amplifier efficiency. As such, where I_a is negative it should be set to zero. When input referred, (6.8) can be rewritten as

Figure 6.2: The calculated main device current I_m and auxiliary device current I_a for $X = 6, 8, 10, 12$ dB versus the normalized input voltage v_{in}.

$$I_a = g_m(V_{in} - V_{in,X}) \qquad (6.11)$$

Setting the negative portion of I_a in (6.11) to zero, the I_a profile as a function of V_{in} and $V_{in,X}$ can be expressed as

$$I_a = \begin{cases} 0, & \text{if } V_{in} \leq V_{in,X} \\ g_m(V_{in} - V_{in,X}), & \text{if } V_{in} > V_{in,X} \end{cases} \qquad (6.12)$$

Using (6.12), Figure 6.2 plots the I_m and I_a profiles for $X = 6, 8, 10, 12$ dB versus the input voltage v_{in}. From Figure 6.2 and (6.8), the I_m and I_a profiles have the same slope and therefore can be approximated using devices with similar size or periphery. Practical realization of the different I_a profiles at various back-off level X can be implemented in one of two ways. The mixed-signal approach is a possibility since it offers precise control of the turn-on voltage and I_a profile for a given back-off level X. However, the method we propose is to simply change the gate bias of the auxiliary device to various class C biases with the appropriate turn-on voltage for a desired back-off level X. The soft turn-on of the class C bias may be alleviated by using a slightly larger auxiliary device as implemented in the prototype in Section 6.7. The proposed technique offers a reduced design complexity since a mixed-signal setup with baseband processing and dual-path drivers is no longer needed.

6.3.3 Analysis with Fixed Main Device Bias Voltage V_{dcm}

Considering a fixed main device drain bias V_{dcm}, the voltage V_m across the main device and the voltage V_L across the auxiliary device are plotted in Figure 6.3 for $X = 6, 8, 10, 12$ dB. As the

112

Figure 6.3: The calculated main device voltage V_m and auxiliary device voltage V_L for $X = 6, 8, 10, 12$ dB versus the normalized input voltage v_{in} assuming a constant main device bias voltage V_{dcm}.

back-off level increases, the quarter-wave transformer characteristic impedance Z_T increases, resulting in a larger and larger swing of the auxiliary device voltage as given by

$$\mathbf{V_L} = -jZ_T\mathbf{I_m} \tag{6.13}$$

As a result, the auxiliary drain bias V_{dca} needs to be set at a higher voltage than the main drain bias voltage as given by

$$V_{dca} = 10^{\frac{X}{20}}V_{dcm} \tag{6.14}$$

Interesting insights can be drawn from Figure 6.3. If we assume that V_{dcm} is biased at half the main device breakdown voltage, then keeping the main bias voltage V_{dcm} fixed versus varying back-off level X ensures that the main device is fully utilized in all cases. However, because the auxiliary device voltage V_L swings at multiples of V_{dcm}, the auxiliary device requires a higher breakdown voltage and thus cannot be implemented using the same device as the main device. To address this, a mixed-technology scheme where the main device uses a lower breakdown LDMOS device and the auxiliary uses a higher breakdown GaN device is an attractive solution that improves the power utilization and lowers cost. With a mixed-technology scheme, the main and auxiliary devices are fully utilized from a voltage perspective. In contrast, if the main and auxiliary devices use the same device, then the main device must necessarily be underutilized since it must be down-biased.

Another interesting result is the ease of matching as the back-off level X increases. Because the design parameter Z_T and R_L increases with a larger back-off level X, realization of the microstrip network and matching to 50 Ω become easier at larger back-off level. Therefore, the

113
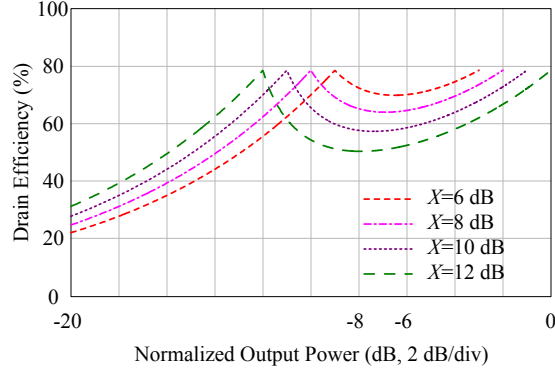
Figure 6.4: The calculated efficiency for $X = 6, 8, 10, 12$ dB versus the normalized output power assuming a constant main device bias voltage V_{dcm}.

ease of matching is no longer just dependent on R_{opt} but becomes both a function of R_{opt} and the back-off power level X as dictated by (6.4).

Figure 6.4 plots the efficiency versus normalized output power for $X = 6, 8, 10, 12$ dB. From Figure 6.4, the back-off and the peak power expand about the midpoint power level of $X/2$ as X increases. The back-off power decreases because the main device output power at the auxiliary device turn-on point is lower due to the lower I_m at that input drive level. Similarly, the peak power increases because both the peak I_a and V_L increase with larger X.

6.3.4 Analysis with Fixed Auxiliary Device Bias Voltage V_{dca}

From (6.14), only a specific V_{dca} to V_{dcm} ratio is needed to achieve a given back-off level X. In this section, we derive the voltage and efficiency characteristics when the auxiliary device bias voltage V_{dca} is held constant while the main device bias voltage is varied to satisfy the ratio given in (6.14).

Figure 6.5 plots the voltages across the main and auxiliary devices for $X = 6, 8, 10, 12$ dB when the auxiliary drain bias V_{dca} is fixed. From Figure 6.5, as the back-off level increases, the main device bias reduces accordingly and V_m saturates when $V_{in} = V_{in,x}$. Perhaps the most interesting result when V_{dca} is held constant while V_{dcm} varies is one regarding the optimal impedance R_o. When (6.14) is substituted into (6.4), the resulting R_o is a constant independent of the back-off level X as given by

$$R_o = \frac{2V_{dca}}{I_{max}} \quad \forall X \tag{6.15}$$

R_o stays constant because the two $10^{\frac{-X}{20}}$ terms in (6.5) and (6.14) cancel out. The practical
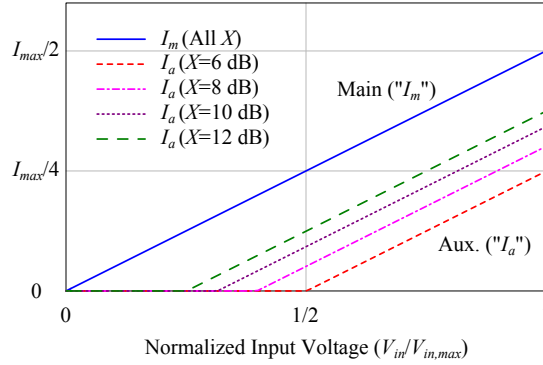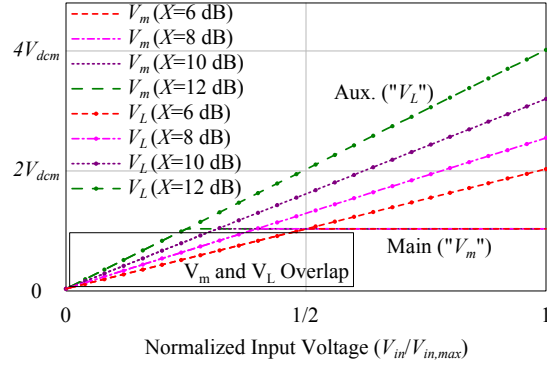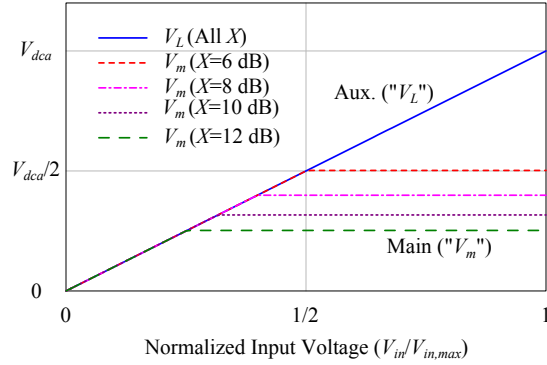
Figure 6.5: The calculated main device voltage V_m and auxiliary device voltage V_L for $X = 6, 8, 10, 12$ dB versus the normalized input voltage v_{in} assuming a constant auxiliary device bias voltage V_{dca}.
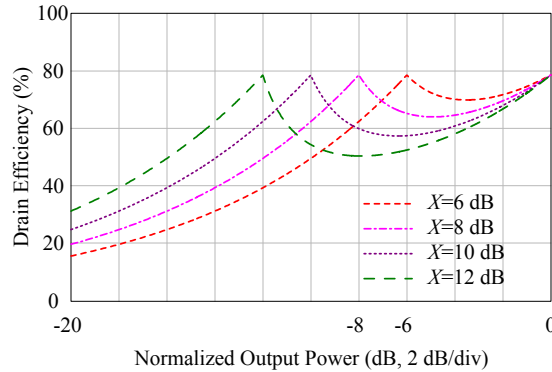
Figure 6.6: The calculated efficiency for $X = 6, 8, 10, 12$ dB versus the normalized output power assuming a constant auxiliary device bias voltage V_{dca}.

implication is that for a fixed output matching network with $Z_T = R_L = 2V_{dca}/I_{max}$, the back-off level can be reconfigured dynamically by adjusting the gate and drain bias of the auxiliary and main devices respectively to satisfy the required I_a profile and the voltage ratio in (6.14) for a desired back-off level X.

Finally, Figure 6.6 plots the efficiency versus normalized output power for $X = 6, 8, 10, 12$ dB. In Figure 6.6, the peak power stays constant regardless of the back-off level X because the decrease in the main device output power is compensated by an equal increase in the auxiliary device output power.

6.4   Device Utilization and Power Contribution

In the proposed asymmetrical voltage biasing scheme, the power utilization factor (PUF) of the Doherty amplifier is found by dividing its peak output power by the maximum power capability of the main and auxiliary device as given by

$$PUF = \frac{P_{max,DPA}}{P_{max,m} + P_{max,a}} \tag{6.16}$$

where the Doherty amplifier peak power $P_{max,DPA}$ is found by summing the peak power of the main and auxiliary device given by

$$P_{max,DPA} = \frac{2V_{dcm}I_{max} + 2V_{dca}I_{max}(1 - 10^{\frac{-X}{10}})}{8} \tag{6.17}$$

Using (6.14), (6.17) simplifies to

$$P_{max,DPA} = \frac{V_{dca}I_{max}}{4} \tag{6.18}$$

From (6.18), the Doherty amplifier peak power is independent of the back-off level X and is only a function of the auxiliary device drain bias V_{dca} and the main device saturation current I_{max}. This result follows because when the back-off level X is varied, the change in the main device utilization is compensated by an equal but opposite change in the auxiliary device utilization.

The maximum main device output power capability $P_{max,m}$ and the maximum auxiliary device output capability $P_{max,a}$ are given as

$$P_{max,m} = \frac{V_{br,m}I_{max}}{8} \tag{6.19}$$

and

$$P_{max,a} = \frac{V_{br,a}I_{max}}{8} \tag{6.20}$$

where $V_{br,m}$ and $V_{br,a}$ are the breakdown voltage of the main and auxiliary devices respectively. The two devices are assumed to have the same I_{max} because they should have similar g_m to achieve the current profiles in Figure 6.2.

When the asymmetrically biased Doherty amplifier is implemented with a single technology, the main and auxiliary devices have the same breakdown voltage $V_{br,m} = V_{br,a}$. Assuming that the auxiliary device bias V_{dca} is set at half the device breakdown voltage, then using (6.16), the device utilization can be calculated as

Table 6.2: Single versus mixed-technology Doherty amplifier.

Approach	Doherty PUF	Reconfigurable range
Single technology	$1/2$	$X \geq 0$
Mixed technology	$1/(1+m)$	$X \geq X_m$

$$PUF_{single} = \frac{1}{2} \tag{6.21}$$

In contrast, in the proposed mixed-technology Doherty amplifier, the different breakdown voltages of the main and auxiliary devices allow for an improved power utilization factor above 50%. Assuming that the main device breakdown voltage is lower than the auxiliary device breakdown as given by

$$V_{br,m} = mV_{br,a} \tag{6.22}$$

where $m < 1$, then using (6.16), the power utilization of the mixed-technology Doherty amplifier is given by

$$PUF_{mixed} = \frac{1}{1+m} \tag{6.23}$$

From (6.23), as m decreases, the power utilization of the mixed-technology Doherty amplifier improves. However, (6.22) in conjunction with (6.14) place a lower limit on the range of feasible back-off power level given by

$$X_m = -20\log(m) \tag{6.24}$$

In other words, for a given breakdown voltage ratio m, the amplifier can only have a reconfigurable back-off power range of $X \geq X_m$, since a back-off level less than X_m requires the main device drain bias V_{dcm} to be biased beyond what the main device breakdown voltage would allow.

Therefore, a fundamental trade-off exists between device utilization and the reconfigurable power range. When compared to a single-technology Doherty amplifier, the mixed-technology Doherty amplifier offers an improved device utilization factor at the cost of a reduced reconfigurable power range. A comparison between single and mixed-technology Doherty amplifier is summarized in Table 6.2.

Although the above analysis suggests that the Doherty amplifier PUF can be improved with a small m, the impact on the amplifier efficiency should be considered in such a scenario. From
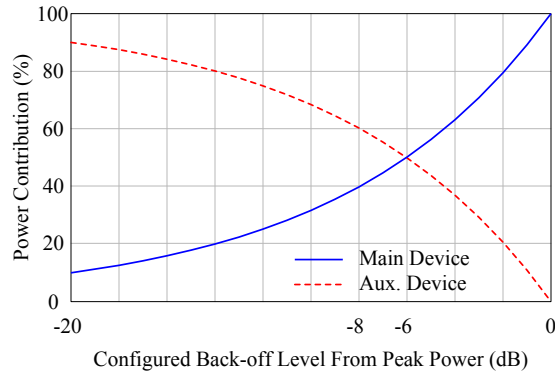
Figure 6.7: The calculated percentage power contribution of the main and auxiliary devices at peak power versus the configured back-off power level from the peak power.
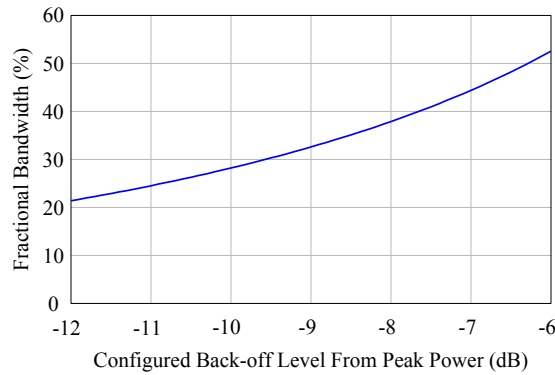
Figure 6.8: The calculated fractional bandwidth of the proposed amplifier versus the configured back-off power level from the peak power.

Figures 6.4 and 6.6, the dip between the efficiency peaks worsens at larger back-off level. The worsening dip is due to two reasons. First, the auxiliary device which isn't load modulated stays on longer since it turns on earlier. Second, the auxiliary device becomes the primary contributor of output power when the back-off level is large. Figure 6.7 shows the percentage power contribution of the main and auxiliary devices at the peak power versus the configured back-off levels. Because the auxiliary device contributes most of the output power when the back-off level is large, enhancing the efficiency of the main device whose power contribution is low does not yield an overall efficient Doherty amplifier. From Figure 6.7, the crossover back-off level where each device contributes half the output power occurs at $X = 6$ dB.

6.5   Bandwidth Analysis

In contrast to the work presented in [67] where a mixed-signal setup with adjustable input magnitude and phase is used to improve the bandwidth of the amplifier, we show that even without using a mixed-signal setup, the proposed amplifier is capable of extended bandwidth operation.

Following a similar analysis to Chapter 5, it can be shown that at the peak power, the main device voltage V_m in Figs. 6.3 and 6.5 begins to exceed V_{dcm} as the operating frequency deviates from the center frequency. In a class B amplifier, the excess V_m intrudes into the knee region and causes compression and efficiency degradation. However, recognizing that modes of operation such as class F and continuous class F [70] can support excess V_m swing up to $\frac{2}{\sqrt{3}}V_{dcm}$ or $1.155V_{dcm}$ without performance degradation, we derive the theoretical bandwidth of the proposed amplifier assuming that some excess V_m swing can be tolerated. Using $V_m < 1.155V_{dcm}$ as the limit, Figure 6.8 plots the theoretical fractional bandwidth of the proposed amplifier at various configured back-off power level. From Figure 6.8, the theoretical fractional bandwidth decreases when the amplifier is configured for a large back-off level, with 30% theoretical fractional bandwidth at $X = 9.5$ dB.

Although the proposed amplifier has less theoretical bandwidth than the mixed-signal approach in [67], it offers a much reduced design complexity since baseband processing and dual-path drivers are not required. Moreover, in practical designs, the device parasitic and package are often the dominant band-limiting components. Therefore, the two approaches may yield similar practical bandwidth once the other band-limiting components are taken into consideration. Lastly, as the analysis in Section 6.6 will show, the optimally configured back-off power level is generally less than the modulated signal's PAPR. Therefore, even signals with a high PAPR can achieve extended bandwidth when compared to the conventional Doherty amplifier.

6.6   Optimal Back-off Level for a Given Modulated Signal

The ability to adjust the back-off level dynamically enables an interesting possibility not explored in the previous literature, namely, the ability to configure the proposed amplifier for a given modulated signal to achieve the highest average efficiency.

From [84], given the probability density function (PDF) of the modulated signal p, the average efficiency η_{avg} can be computed as

$$\eta_{avg} = \frac{P_{out,avg}}{P_{dc,avg}} = \frac{\int p(P_{out}) * P_{out} dP_{out}}{\int p(P_{out}) * P_{dc}(P_{out}) dP_{out}} \tag{6.25}$$

where the DC consumption P_{dc} at a given output power P_{out} is found by

$$P_{dc}(P_{out}) = \frac{P_{out}}{\eta(P_{out})} \tag{6.26}$$

119

Table 6.3: A comparison of amplifier average efficiency when driven with different modulated signals.

Signal	PAPR (dB)	Conventional Doherty η_{avg} (%)	Proposed Doherty η_{avg} (%)
20 MHz WCDMA 1001	8.5	59.2	62.2 at X=8 dB
20 MHz LTE	10.5	52.0	59.0 at X=9 dB

Therefore, given the amplifier's efficiency versus output power profile and the PDF of the modulated signal, the average efficiency can be directly computed using (6.25) and (6.26).

Using the equations above, we sweep the back-off level X from 6 to 12 dB to determine the efficiency profile that results in the highest η_{avg} for a 20 MHz WCDMA 1001 signal with a 8.5 dB PAPR and a 20 MHz LTE signal with a 10.5 dB PAPR. The optimal efficiency profiles and the signal PDF for the WCDMA and the LTE signals are shown in Figure 6.9a and Figure 6.9b respectively. A key observation is that the optimal back-off levels are less than the respective signal's PAPR, with optimal levels of 8 and 9 dB for the 8.5 dB PAPR WCDMA and 10.5 dB PAPR LTE signals respectively. This result follows because the efficiency degradation due to the larger dip between the efficiency peaks outweighs the efficiency gain of having the back-off level at exactly the signal's PAPR.

Table 6.3 lists the average efficiency of the proposed amplifier when optimally configured for the two modulated signals. The conventional Doherty amplifier performance is also listed for comparison. From Table 6.3, the proposed amplifier improves the average efficiency by 3.0% and 7.0% for the WCDMA and LTE signals respectively when compared to the conventional Doherty amplifier. When compared to the novel three-stage Doherty amplifier [81], the optimally configured proposed amplifier has 7.1% and 6.7% lower average efficiency for the WCDMA and LTE signals respectively instead of the 10% lower average efficiency of the non-reconfigurable N-way Doherty amplifier reported in [79].

From the above comparison, a key judgement is therefore whether the complex and generally band-limited three-stage Doherty amplifier justifies the approximately 7% higher point in theoretical efficiency, especially when the insertion loss of the three-way input splitter and output combiners is taken into consideration.
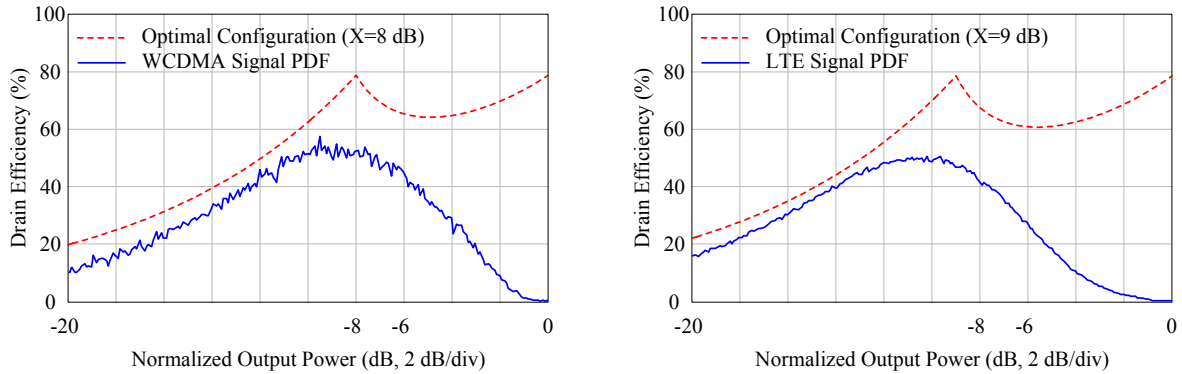
(a) The calculated optimal back-off level of the proposed amplifier when driven with a 20 MHz WCDMA 1001 signal with 8.5 dB PAPR.

(b) The calculated optimal back-off level of the proposed amplifier when driven with a 20 MHz LTE signal with 10.5 dB PAPR.

Figure 6.9: The optimal back-off level configurations of the proposed amplifier when driven with 20 MHz LTE and WCDMA 1001 signals with 10.5 and 8.5 dB PAPR respectively.

6.7 Design and Validation: A 180 W LDMOS/GaN Mixed-Technology Doherty Amplifier

6.7.1 Device Selection

To demonstrate the proposed concept in practice, we designed a 180 W mixed-technology Doherty amplifier using LDMOS and GaN technology. To ensure a proper load modulation in the proposed mixed-technology Doherty amplifier, the LDMOS and GaN devices should have similar transconductance g_m so that the main and auxiliary current profiles in Figure 6.2 can be realized. Based on this criterion, we selected the MRF6S9045N LDMOS transistor from Freescale Semiconductor Inc. as the main device and the CGH40120F transistor GaN from Cree Inc. as the auxiliary device. From the simulation, the maximum current capability of the MRF6S9045N transistor enables close to 90 W of peak output power while the CGH40120F is rated for 120 W of peak power at 28 V. The slightly larger auxiliary device allows the lower class C transconductance to equal the class B transconductance of the main device. It also helps mitigate the effect of the soft turn-on in a class C bias.

From the data sheets of the two devices, the breakdown voltage of the LDMOS and the GaN devices are estimated to be around 66 and 120 V respectively. Based on the approximately two to one ratio of the breakdown voltage, we design a Doherty amplifier with a reconfigurable back-off power range of greater than 6 dB back-off. From (6.23), the overall power utilization factor is about 66%. Biasing the LDMOS main device at 28 V and the GaN auxiliary device at 60 V, we expect to obtain approximately 180 W of peak output power. The LDMOS device is biased with

121

a quiescent current of 350 mA while the auxiliary gate bias varies depending on the back-off level. The combination of LDMOS and GaN devices also lowers the watts per dollar cost when compared to an amplifier implemented using GaN devices alone since the LDMOS device is less expensive.

6.7.2 Practical Design Considerations

To show that the proposed amplifier also exhibits extended bandwidth, we target a design frequency from 790 to 960 MHz, equivalent to a 20% fractional bandwidth. The output matching network consists of a quasi-lumped quarter-wave transformer that absorbs the device parasitic and package [65] and a two-section wideband matching network to 50 Ω that results in a very small PCB foot print. Although the LDMOS and GaN devices have different output capacitances and packages, the quasi-lumped quarter-wave transformer did not have issues absorbing these parasitic over the desired bandwidth. The impedance Z_T and R_L was found to be approximately 8 Ω.

An added design complexity in a mixed-technology Doherty amplifier is that different input matching networks are needed because the LDMOS and GaN devices have very different input impedances. Moreover, the electrical delay through the LDMOS device is found to be larger than the GaN device. To address the different input impedances, separate wideband matching networks are designed. The source impedances that result in the optimal performance were $1.8 + j1$ Ω and 6 Ω for the LDMOS and GaN devices respectively. To compensate for the different electrical delay through the two devices, additional phase delay is added to the standard $90°$ degree delay line. Figure 6.10 illustrates the chosen circuit topology to implement the proposed mixed-technology Doherty amplifier. A picture of the fabricated amplifier is shown in Figure 6.11.

6.7.3 Continuous Wave Characterization

Unlike [67], the proposed amplifier is measured without using a complex mixed-signal setup. To demonstrate the reconfigurability and the extended bandwidth capability of the proposed amplifier, we configure the amplifier for back-off level X of 6, 8, and 10 dB at 790, 870 and 960 MHz. The measurements are predicted by simulation. To reduce clutter, the simulations results are not shown. Figures 6.12a–6.12c show the measured drain efficiency versus output power of the fabricated mixed-technology Doherty amplifier for the three frequencies at the three different back-off levels. From the figures, the back-off efficiency drop slightly as the configured back-off level X increases. Despite different trends at the different frequencies, the measured peak and back-off efficiencies are all above 50% at the three frequencies and back-off levels. Due to thermal constraints in high power measurements, the true peak power capability is not obtained in the continuous-wave measurement.
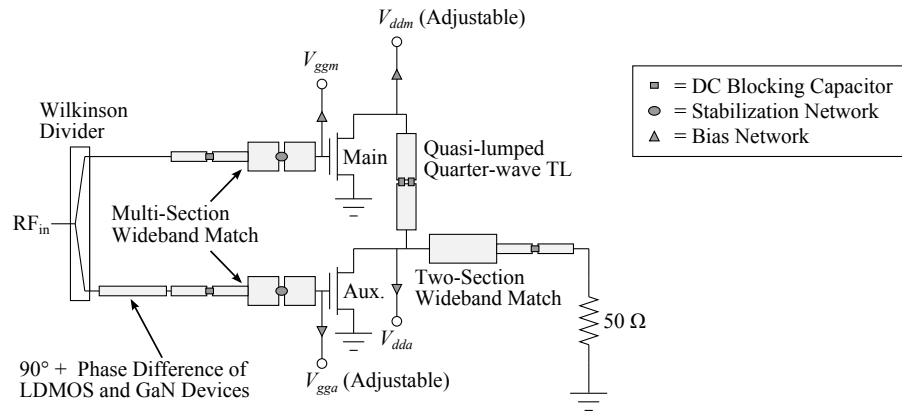
Figure 6.10: The circuit topology used to implement the proposed mixed-technology Doherty amplifier.
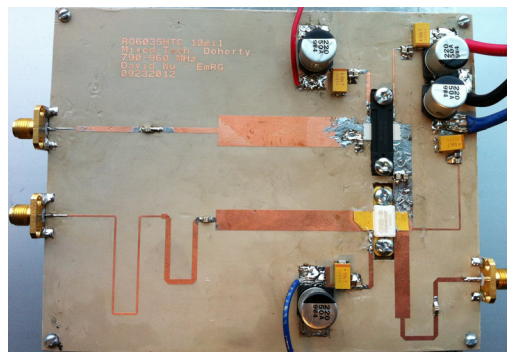
Figure 6.11: A picture of the fabricated 180 W mixed-technology, wideband and reconfigurable Doherty amplifier.

To assess the linearity of the proposed amplifier, the measured gain versus input power for the three frequencies and back-off power levels are shown in Figures 6.13a–6.13c. From the figures, the measured small signal gain varies from 15 to 17 dB across the three different frequencies and back-off power levels. The undesired inflection point in the gain curve when the auxiliary device turns on can be attributed to combining errors likely stemming from errors in the phase delay estimation of the two devices. From the gain versus input power plots, the amplifier is nonlinear and requires digital pre-distortion to achieve a linear response. The continuous wave measurements show that the proposed amplifier can support multiple standards with different PAPR across a 20% fractional bandwidth.
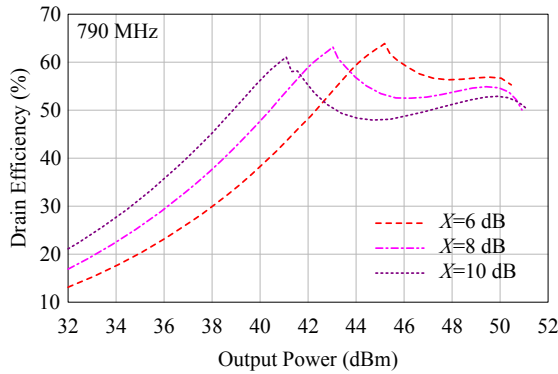
(a) The measured drain efficiency versus output power at 790 MHz for $X = 6, 8, 10$ dB.
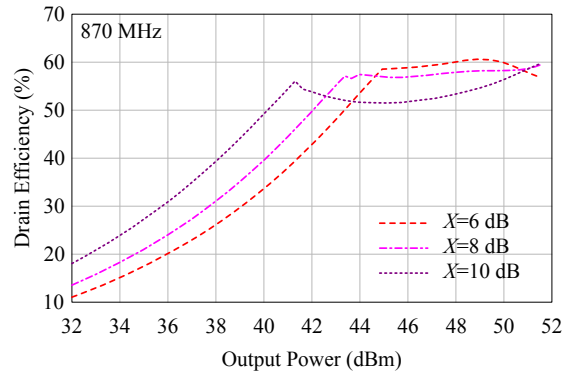
(b) The measured drain efficiency versus output power at 870 MHz for $X = 6, 8, 10$ dB.
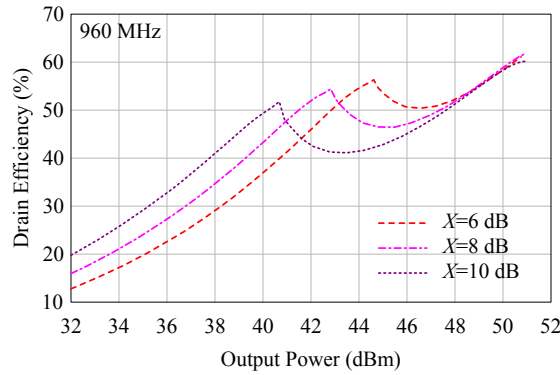
(c) The measured drain efficiency versus output power at 960 MHz for $X = 6, 8, 10$ dB.

Figure 6.12: The measured drain efficiency versus output power of the 180 W mixed-technology reconfigurable Doherty amplifier at 790, 870, and 960 MHz for $X = 6, 8, 10$ dB.

6.7.4 DPD Linearization

To assess the linearizability of the prototype amplifier for multi-standard application, we drive the amplifier with the 20 MHz LTE and 1001 WCDMA signals studied in Section 6.6 at 790 and 860 MHz respectively. Using the optimal configuration from Section 6.6, we configure the amplifier for $X = 8$ dB and $X = 9$ dB for the WCDMA and the LTE signals respectively to achieve the highest average efficiency.

For linearization, we use a digital pre-distortion (DPD) algorithm based on dynamic deviation reduction Volterra series with a static nonlinearity order of nine and kernels up to the fifth order with memory depths of 7, 5, 3, for the first, third, and fifth kernel respectively with a dynamic nonlinearity order $r = 2$ [85]. The gate bias of the auxiliary device was adjusted slightly
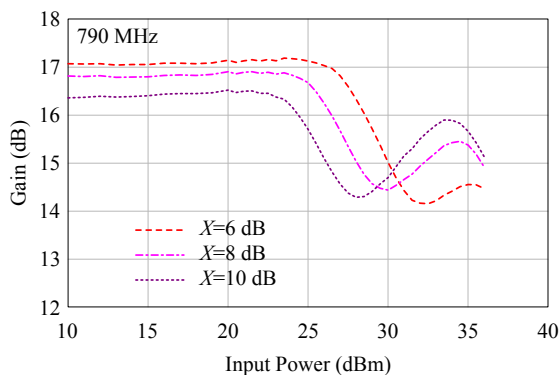
(a) The measured gain versus input power of at 790 MHz for $X = 6, 8, 10$ dB.
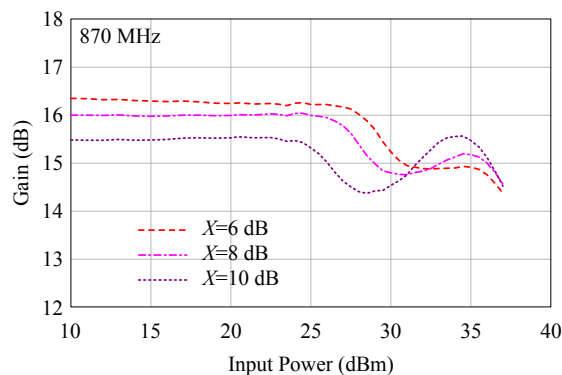
(b) The measured gain versus input power of at 870 MHz for $X = 6, 8, 10$ dB.
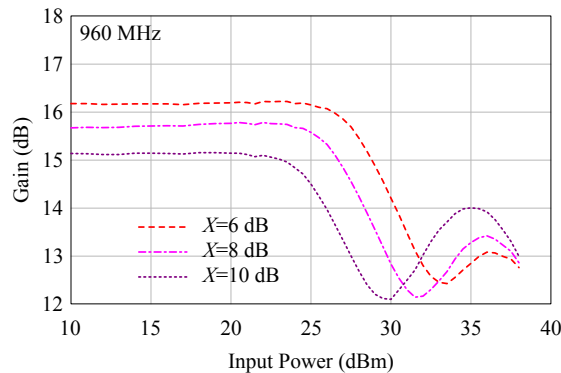
(c) The measured gain versus input power of at 960 MHz for $X = 6, 8, 10$ dB.

Figure 6.13: The measured gain versus input power of the 180 W mixed-technology reconfigurable Doherty amplifier at 790, 870, and 960 MHz for $X = 6, 8, 10$ dB.

to improve the linearizability of the amplifier at the cost of a minor reduction in the average efficiency. Figure 6.14a shows the measured output spectra before and after DPD linearization when the amplifier is driven with the 20 MHz LTE signal at 790 MHz. The ACPR improves from -26.68 to -50.16 dBc and the amplifier achieves an average output power of 42.4 dBm with an associated drain efficiency of 45.7%. Given that the LTE signal has a PAPR of 10.5 dB, we estimate that the amplifier is capable of the design peak power of 180 W when driven with a modulated signal. Similarly, Figure 6.14b shows the output spectra before and after DPD when the amplifier is driven with the 20 MHz 1001 WCDMA signal at 870 MHz. The ACPR improves from -28.31 to -50.90 dBc and the amplifier achieved an average output power of 43.6 dBm with an associated drain efficiency of 49.7%. The 1001 WCDMA signal has a PAPR of 8.5 dB.

Comparing the average efficiency achieved by the amplifier when driven with the WCDMA
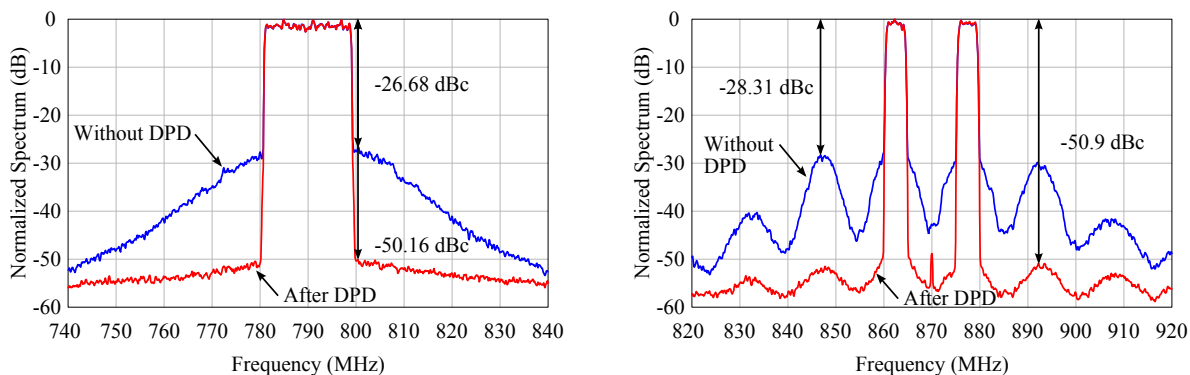
(a) The measured output spectra before and after the DPD linearization when driven with a 20 MHz LTE signal at 790 MHz.

(b) The measured output spectra before and after the DPD linearization when driven with a 20 MHz WCDMA 1001 signal at 870 MHz.

Figure 6.14: The measured output spectra of the 180 W mixed-technology Doherty amplifier before and after the DPD linearization when driven with 20 MHz LTE and 20 MHz WCDMA 1001 signals.

and LTE signals, the difference of 4% between 45.7% and 49.7% is close to the theoretical difference of 3.2% predicted in Table 6.3. From the linearization results, the amplifier achieved excellent DPD correction with ACPR better than -50 dBc.

6.8 Summary

In this chapter, a mixed-technology, extended Doherty amplifier based on asymmetrical drain bias voltages was implemented using LDMOS and GaN as the main and auxiliary devices respectively to improve the power utilization factor and watts per dollar cost. In contrast to previous work, the proposed amplifier can achieve extended and reconfigurable back-off level without the use of a mixed-signal setup, thus reducing the system level complexity and cost of implementation. The analysis also highlighted a trade-off between the device utilization and reconfigurable power range. Lastly, we showed that the proposed amplifier can be optimally configured for a given modulated signal to obtain the highest average efficiency. We found that the optimally configured back-off power level is generally less than the signal's PAPR.

A 180 W LDMOS/GaN mixed-technology prototype amplifier operating from 790 to 960 MHz demonstrated the proposed concept. The amplifier achieved peak and back-off efficiencies greater than 50% when configured for 6, 8, and 10 dB of back-off power level at 790, 870, and 960 MHz under continuous wave stimulus. The amplifier is highly linearizable when driven with wideband 20 MHz LTE and WCDMA signals with 10.5 and 8.5 dB PAPR respectively, achieving ACPR of

better than -50 dBc after DPD linearization with average efficiency greater than 45%. Although the proposed amplifier has slightly lower peak and back-off efficiencies when compared to several amplifiers in the literature outlined in Table 6.1, it uses a low cost LDMOS main device and has a low design complexity as well as an extended bandwidth and reconfigurable back-off power level. The result may also be improved by using the latest generation of LDMOS devices.

Chapter 7

Conclusion

The high cost to license wireless spectra has led to emerging wireless standards with an improved spectral efficiency and a high peak-to-average ratio that negatively affect the base station RF power amplifier efficiency. In this thesis, we began by outlining the multitude of requirements of a modern base station power amplifier that include high gain, output power, linearity, peak efficiency, back-off efficiency, and bandwidth. From first principles, we derived the underlying power amplifier theory that related these requirements to one another. With practical amplifier design techniques and device technology insights, we designed a narrowband, harmonically-tuned 3.3 GHz, 10 W GaN high efficiency amplifier that demonstrated the high efficiency amplifier theory in practice.

Next, we explored how to simultaneously achieve broadband and highly efficient amplifier operation. With load-pull results from 2 to 3 GHz, we harnessed the simplified real frequency technique to systematically design broadband matching networks for a 45 W GaN device. Moreover, by analyzing the class B/J design space, we found that the choice of output fundamental impedances can affect the amplifier efficiency sensitivity to the second harmonic termination at the package reference plane. To demonstrate that the proposed broadband matching technique is independent of the device technology, we also designed a 650 to 1050 MHz, 45 W LDMOS broadband amplifier.

To achieve back-off efficiency enhancements, broadband, and highly efficient amplifier operation, we analyzed the conventional Doherty amplifier to ascertain the reasons behind its narrow bandwidth as observed in the literature. We found that the narrow bandwidth was caused by the theoretical limitation of the quarter-wave transmission line as well as the widely adopted traditional design technique. As an original contribution to knowledge, we proposed a novel Doherty amplifier configuration using asymmetrical drain voltage biases that enabled a broadband Doherty amplifier operation. Moreover, when symmetrical devices are used, the proposed amplifier does not require advanced techniques to synthesize the auxiliary device current profile or a complex mixed-signal setup. To demonstrate the proposed concept in practice, we designed a 700

to 1000 MHz, 90 W GaN broadband Doherty amplifier. To show that the proposed concept is applicable to high power designs, we designed a 200 W GaN broadband Doherty amplifier in the same band. Lastly, to demonstrate that the technique is independent of the device technology, we designed a 700 to 900 MHz, 60 W LDMOS broadband Doherty amplifier. The three prototypes were shown to be highly linearizable using DPD when driven with wideband 20 MHz LTE and WCDMA modulated signals.

Lastly, using the insights from the previous analyses, we proposed a novel mixed-technology Doherty amplifier with an extended and reconfigurable back-off power level as well as an improved power utilization factor. The reconfigurability of the proposed amplifier made it possible to customize the back-off level to achieve the highest average efficiency for a given modulated signal without redesigning the matching networks. A 790 to 960 MHz, 180 W LDMOS/GaN Doherty amplifier was designed to demonstrate the extended bandwidth and reconfigurability. The amplifier was highly linearizable when driven with wideband 20 MHz LTE and WCDMA modulated signals. The proposed amplifier addresses many shortcoming of the conventional Doherty amplifier and satisfies the multitude of requirements of a base station power amplifier.

7.1   Summary of Contribution

To highlight the contribution of this thesis, we list the thesis sections that, to the best knowledge of the author, provide either new insights into existing concepts, or a new contribution to knowledge.

In Chapter 2, the class F waveform synthesis relied on the knee region nonlinearity alone to produce the desired third harmonic current required for the voltage shaping. This approach is simpler than previous work that biased the device in class AB [12] or relied on the sloping of the device DC-IV curve [86]. For the design of the matching networks, we determined that $\lambda/8$ open circuited stubs minimize the impedance variation to manufacturing errors. In the 3.3 GHz, 10 W GaN amplifier design that was also published in [33], we highlighted the efficiency sensitivity to the input second harmonic termination and proposed techniques to mitigate the effect.

In Chapter 3, we were the first to adopt the simplified real frequency technique to systematically synthesize the matching networks for highly efficient and broadband amplifiers [87]. Analyzing the class B/J design space, we identified class J* as the mode of operation that minimizes the amplifier efficiency sensitivity to the second harmonic termination at the package reference plane.

In Chapter 4, we showed that the load modulation in a Doherty amplifier is completely described by four key design parameters. Unlike previous work that attributed the narrow bandwidth solely to the quarter-wave transmission line, we also identified the traditional Doherty amplifier design technique as a key source of bandwidth limitation. We also provided closed-form

equation to determine length of the offset tuning lines which are typically determined empirically post fabrication.

In Chapter 5, we outlined the main contribution of this thesis on the bandwidth extension of the Doherty amplifier. Using a different set of the four design parameters, we proposed a new Doherty amplifier configuration with an intrinsically broadband characteristics. Moreover, we proposed a different circuit topology that preserves the theoretical bandwidth potential of the proposed amplifier in practical implementations. The results were published in [88].

In Chapter 6, we exploited the concept further and derived sets of the four design parameters that allowed for extended back-off efficiency enhancement in the Doherty amplifier. Unlike a previous work [67] that relied on a mixed-signal setup to synthesize the required current profiles to achieve reconfigurable back-off power level. We showed that by adjusting the gate bias of the auxiliary device, the reconfigurability can be achieved without the use of a mixed-signal setup. Moreover, we proposed a mixed-technology solution to improve power utilization factor and lower the watts per dollar cost.

7.2   Future Work

The work presented in this thesis can benefit from future research to further address the requirements of next generation base station power amplifiers.

In particular, there is a need to demonstrate the proposed broadband Doherty amplifier at higher frequencies where the device parasitic and package become the dominant band-limiting elements. This research is particularly challenging for high power and packaged devices that are standard in the industry today.

Another interesting research topic is the optimization of the device and package for a given Doherty amplifier configuration that accounts for the required current profiles, breakdown voltages, parasitic, etc. This approach of designing the Doherty amplifier from the device level up has a good potential to significantly improve the back-off efficiency.

Lastly, with advanced digital pre-distortion techniques in recent years, designers are more able to trade-off linearity for an improved efficiency while still satisfying the requirements of the wireless standard after linearization. However, designers currently have little insights into the linearizability of their designs until the amplifiers are on the test bench. Therefore, it will be very interesting if the linearization capability can be brought in during the design stage for the optimal trade-off between efficiency and linearity in practical designs.

7.3   List of Publications

Peer-Reviewed Journal Papers

1. <u>D. Y.-T. Wu</u> and S. Boumaiza, "Reduction of power amplifier efficiency sensitivity by exploiting the class B/J design space," submitted to *IEEE Transactions on Circuits and Systems I*, Dec. 2012. (Based on Chapter 3)

2. <u>D. Y.-T. Wu</u> and S. Boumaiza, "A mixed-technology, asymmetrically-biased extended and reconfigurable Doherty amplifier with improved power utilization factor," accepted to *IEEE Transactions on Microwave Theory and Techniques* Feb. 2013. (Based on Chapter 6)

3. <u>D. Y.-T. Wu</u> and S. Boumaiza, "A modified Doherty configuration for broadband amplification using symmetrical devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 10, pp. 3201–3213, Oct. 2012. (Based on Chapter 4 and 5)

4. <u>D. Y.-T. Wu</u> and S. Boumaiza, "Comprehensive first-pass design methodology for high efficiency mode power amplifier," *IEEE Microwave Magazine*, vol. 11, no. 1, pp. 116–121, Feb. 2010. (Based on Chapter 2)

Papers in Refereed Conference Proceedings

1. H. Sarbishaei, <u>D. Y.-T. Wu</u>, and S. Boumaiza, "Linearity of GaN HEMT RF power amplifiers - a circuit perspective," in *IEEE MTT-S International Microwave Symposium Digest*, Jun. 2012.

2. F. Mkadem, <u>D. Y.-T. Wu</u>, and S. Boumaiza, "Wiener G-functionals for nonlinear power amplifier digital predistortion," in *IEEE MTT-S International Microwave Symposium Digest*, Jun. 2012.

3. <u>D. Y.-T. Wu</u>, F. Mkadem, and S. Boumaiza, "Design of a broadband and highly efficient 45W GaN power amplifier via simplified real frequency technique," in *IEEE MTT-S International Microwave Symposium Digest*, Anaheim, CA, May 2010.

4. <u>D. Y.-T. Wu</u>, D. Frebrowski, and S. Boumaiza, "First-pass design of high efficiency power amplifiers using accurate large signal models," in *IEEE Wireless and Microwave Technology Conference*, Apr. 2010.

5. M.-C. Fares, <u>D. Y.-T. Wu</u>, and S. Boumaiza, "Inward nonlinear characterization of Doherty power amplifiers," in *IEEE MTT-S International Microwave Symposium Digest*, Jun. 2009.

6. <u>D. Y.-T. Wu</u> and S. Boumaiza, "10 W GaN inverse class F PA with input/output harmonic termination for high efficiency WiMAX transmitter," in *IEEE Wireless and Microwave Technology Conference*, Apr. 2009.

References

[1] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Artech House, 2006.

[2] P. Aaen, J. Pla, and J. Wood, *Modeling and Characterization of RF and Microwave Power FETs*. Cambridge University Press, 2007.

[3] K. Chang, *RF Microwave Wireless Systems*. Wiley-Interscience, 2000.

[4] W. H. Doherty, "A new high efficiency power amplifier for modulated waves," *Proceedings of the Institute of Radio Engineers*, vol. 24, pp. 1163–1182, Sep. 1936.

[5] D. F. Kimball, J. Jeong, C. Hsia, P. Draxler, S. Lanfranco, W. Nagy, K. Linthicum, L. E. Larson, and P. M. Asbeck, "High-efficiency envelope-tracking W-CDMA base-station amplifier using GaN HFETs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 11, pp. 3848–3856, Nov. 2006.

[6] F. H. Raab, "Class-F power amplifiers with maximally flat waveforms," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 11, pp. 2007–2011, Nov. 1997.

[7] F. H. Raab, "Class-E, class-C, and class-F power amplifiers based upon a finite number of harmonics," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 8, pp. 1462–1468, Aug. 2001.

[8] F. H. Raab, "Maximum efficiency and output of class-F power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 6, pp. 1162–1166, Jun. 2001.

[9] S. Gao, "High-efficiency class F RF/microwave power amplifiers," *IEEE Microwave Magazine*, vol. 7, no. 1, pp. 40–48, Feb. 2006.

[10] J. D. Rhodes, "Output universality in maximum efficiency linear power amplifiers," *International Journal Of Circuit Theory And Applications*, vol. 31, no. 4, pp. 385–405, Jul. 2003.

[11] C. J. Wei, P. DiCarlo, Y. A. Tkachenko, R. McMorrow, and D. Bartle, "Analysis and experimental waveform study on inverse class class-F mode of microwave power FETs," in *IEEE MTT-S International Microwave Symposium Digest*, vol. 1, Boston, MA, Jun. 2000, pp. 525–528.

[12] P. Colantonio, F. Giannini, G. Leuzzi, and E. Limiti, "On the class-F power amplifier design," *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 9, no. 2, pp. 129–149, Mar. 1999.

[13] D. M. Snider, "A theoretical analysis and experimental confirmation of the optimally loaded and overdriven RF power amplifier," *IEEE Transactions on Electron Devices*, vol. 14, no. 12, pp. 851–857, Dec. 1967.

[14] B. Ingruber, J. Baumgartner, D. Smely, M. Wachutka, G. Magerl, and F. A. Petz, "Rectangularly driven class-A harmonic-control amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 11, pp. 1667–1672, Nov. 1998.

[15] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 7, pp. 1151–1159, Jul. 1988.

[16] M. Berroth and R. Bosch, "High-frequency equivalent circuit of gaas fets for large-signal applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 39, no. 2, p. 224, Feb. 1991.

[17] R. Tayrani, J. E. Gerber, T. Daniel, R. S. Pengelly, and U. L. Rohde, "A new and reliable direct parasitic extraction method for MESFETs and HEMTs," in *Proc. IEEE 23rd European Microwave Conference*, Madrid, Spain, Sep. 1993, p. 451.

[18] E. S. Mengistu, "Large-signal modeling of GaN HEMTs for linear power amplifier design," Ph.D. dissertation, University of Kassel, 2007.

[19] R. G. Brady, C. H. Oxley, and T. J. Brazil, "An improved small-signal parameter-extraction algorithm for GaN HEMT devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 7, p. 1535, Jul. 2008.

[20] L. Dunleavy, C. Baylis, W. Curtice, and R. Connick, "Modeling GaN: Powerful but challenging," *IEEE Microwave Magazine*, vol. 11, no. 6, pp. 82–96, Oct. 2010.

[21] C. Fager, J. C. Pedro, N. B. de Carvalho, and H. Zirath, "Prediction of IMD in LDMOS transistor amplifiers using a new large-signal model," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 12, pp. 2834–2842, Dec. 2002.

[22] H. Sarbishaei, D. Y.-T. Wu, and S. Boumaiza, "Linearity of GaN HEMT RF power amplifiers - a circuit perspective," in *IEEE MTT-S International Microwave Symposium Digest*, Jun. 2012, pp. 1–4.

[23] M. Maeda, H. Masato, H. Takehara, M. Nakamura, S. Morimoto, H. Fujimoto, Y. Ota, and O. Ishikawa, "Source second-harmonic control for high efficiency power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 43, no. 12, pp. 2952–2957, Dec. 1995.

[24] S. Watanabe, S. Takatuka, K. Takagi, H. Kuroda, and Y. Oda, "Simulation and experimental results of source harmonic tuning on linearity of power GaAs FET under class AB operation," in *IEEE MTT-S International Microwave Symposium Digest*, vol. 3, San Francisco, CA, Jun. 1996, pp. 1771–1774.

[25] K. ik Jeon, Y. se Kwon, and S. cheol Hong, "Input harmonics control using non-linear capacitor in GaAs FET power amplifier," in *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, Denver CO, Jun. 1997.

[26] P. M. White, "Effect of input harmonic terminations on high efficiency class-B and class-F operation of PHEMT devices," in *IEEE MTT-S International Microwave Symposium Digest*, vol. 3, Baltimore, MD, Jun. 1998, pp. 1611–1614.

[27] P. Colantonio, F. Giannini, E. Limiti, and V. Teppati, "An approach to harmonic load and sourcepull measurements for high-efficiency PA design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 1, pp. 191–198, Jan. 2004.

[28] S. Gao, P. Butterworth, S. Ooi, and A. Sambell, "High-efficiency power amplifier design including input harmonic termination," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 2, pp. 81–83, Feb. 2005.

[29] S. C. Cripps, "A theory for the prediction of GaAs FET load-pull power contours," in *IEEE MTT-S International Microwave Symposium Digest*, Boston, MA, May 1983, pp. 221–223.

[30] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, 2nd ed. Prentice Hall, 1996.

[31] D. M. Pozar, *Microwave Engineering*, 3rd ed. Wiley, 2005.

[32] M. Helaoui and F. M. Ghannouchi, "Optimizing losses in distributed multiharmonic matching networks applied to the design of an RF GaN power amplifier with higher than 80% power-added efficiency," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 2, pp. 314–322, Feb. 2009.

[33] D. Y.-T. Wu and S. Boumaiza, "Comprehensive first-pass design methodology for high efficiency mode power amplifier," *IEEE Microwave Magazine*, vol. 11, no. 1, pp. 116–121, Feb. 2010.

[34] T. Heima, A. Inoue, A. Ohta, N. Tanino, and K. Sato, "A new practical harmonics tune for high efficiency power amplifier," in *Proc. IEEE 29th European Microwave Conference*, Munich, Germany, Oct. 1999, pp. 271–274.

[35] Y. Y. Woo, Y. Yang, and B. Kim, "Analysis and experiments for high-efficiency class-F and inverse class-F power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 5, pp. 1969–1974, May 2006.

[36] J. H. Kim, G. D. Jo, J. H. Oh, Y. H. Kim, K. C. Lee, and J. H. Jung, "Modeling and design methodology of high-efficiency class-F and class-F^{-1} power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 1, pp. 153–165, Jan. 2011.

[37] S. C. Cripps, P. J. Tasker, A. L. Clarke, J. Lees, and J. Benedik, "On the continuity of high efficiency modes in linear RF power amplifiers," *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 10, pp. 665–667, Oct. 2009.

[38] B. Yarman, *Design of Ultra Wideband Antenna Matching Networks*. Springer, 2008.

[39] P. Wright, J. Lees, J. Benedikt, P. J. Tasker, and S. C. Cripps, "A methodology for realizing high efficiency class-J in a linear and broadband PA," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, pp. 3196–3204, Dec. 2009.

[40] R. M. Foster, "A reactance theorem," *Bell Systems Technical Journal*, vol. 3, pp. 259–267, 1924.

[41] R. M. Fano, "Theoretical limitations on the broadband matching of arbitrary impedances," *Journal of The Franklin Institute*, vol. 249, no. 1, pp. 57–83, Jan. 1950.

[42] D. Youla, "A new theory of broad-band matching," *IEEE Transactions on Circuit Theory*, vol. 11, pp. 30–50, Mar. 1964.

[43] H. J. Carlin, "A new approach to gain-bandwidth problems," *IEEE Transactions on Circuits and Systems*, vol. 24, no. 4, pp. 170–175, Apr. 1977.

[44] B. S. Yarman and H. J. Carlin, "A simplified real frequency technique applied to broad-band multistage microwave amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 30, no. 12, pp. 2216–2222, Dec. 1982.

[45] V. Belevitch, "Topics in the design of insertion loss filters," *IRE Transactions on Circuit Theory*, vol. 2, no. 4, pp. 337–346, Dec. 1955.

[46] B. Kim, Y. Yang, J. Yi, J. Nam, Y. Y. Woo, and J. H. Cha, "Efficiency enhancement of linear power amplifier using load modulation technique," in *International Microwave Optical Technology Symposium Digest*, Jun. 2001, pp. 505–508.

[47] Y. Yang, J. Yi, Y. Y. Woo, and B. Kim, "Optimum design for linearity and efficiency of a microwave Doherty amplifier using a new load matching technique," in *Microwave Journal*, vol. 44, no. 12, Dec. 2001, pp. 20–36.

[48] S. Cripps, "Inverted logic," *IEEE Microwave Magazine*, vol. 9, no. 5, pp. 30–38, Oct. 2008.

[49] Y. Yang, J. Cha, B. Shin, and B. Kim, "A microwave Doherty amplifier employing envelope tracking technique for high efficiency and linearity," *IEEE Microwave and Wireless Components Letters*, vol. 13, no. 9, pp. 370–372, Sep. 2003.

[50] J. Kim, J. Cha, I. Kim, and B. Kim, "Optimum operation of asymmetrical-cells-based linear Doherty power amplifiers–uneven power drive and power matching," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 5, pp. 1802–1809, May 2005.

[51] C. Steinbeiser, T. Landon, C. Suckling, J. Nelson, J. Delaney, J. Hitt, L. Witkowski, G. Burgin, R. Hajji, and O. Krutko, "250 W HVHBT Doherty with 57% WCDMA efficiency linearized to - 55 dBc for 2c11 6.5 dB PAR," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 10, pp. 2218–2228, Oct. 2008.

[52] J. Kim, J. Moon, Y. Y. Woo, S. Hong, I. Kim, J. Kim, and B. Kim, "Analysis of a fully matched saturated Doherty amplifier with excellent efficiency," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 2, pp. 328–338, Feb. 2008.

[53] P. Colantonio, F. Giannini, R. Giofr, and L. Piazzon, "Theory and experimental results of a class F AB-C Doherty power amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 8, pp. 1936–1947, Aug. 2009.

[54] J. Kim, J. Son, J. Moon, , and B. Kim, "A saturated Doherty power amplifier based on saturated amplifier," *IEEE Microwave and Wireless Components Letters*, vol. 20, no. 2, pp. 109–111, Feb. 2010.

[55] M. Nick and A. Mortazawi, "Adaptive input-power distribution in Doherty power amplifiers for linearity and efficiency enhancement," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 11, pp. 2764–2771, Nov. 2010.

[56] J. Moon, J. Kim, J. Kim, I. Kim, and B. Kim, "Efficiency enhancement of Doherty amplifier through mitigation of the knee voltage effect," *IEEE Transactions on Microwave Theory and Techniques*, vol. 1, no. 1, pp. 143–152, Jan. 2011.

[57] R. Darraji, F. M. Ghannouchi, and O. Hammi, "A dual-input digitally driven Doherty amplifier architecture for performance enhancement of Doherty transmitters," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 5, pp. 1284–1293, May 2011.

[58] P. Colantonio, F. Giannini, R. Giofr, and L. Piazzon, "Increasing Doherty amplifier average efficiency exploiting device knee voltage behavior," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 9, pp. 2295–2305, Sep. 2011.

[59] J. Kim, B. Fehri, S. Boumaiza, and J. Wood, "Power efficiency and linearity enhancement using optimized asymmetrical Doherty power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 2, pp. 425–434, Feb. 2011.

[60] S. Chen and Q. Xue, "Optimized load modulation network for Doherty power amplifier performance enhancement," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 11, Nov. 2012.

[61] K. Bathich, A. Z. Markos, and G. Boeck, "Frequency response analysis and bandwidth extension of the Doherty amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 4, pp. 934–944, April 2011.

[62] G. Sun and R. H. Jansen, "Broadband Doherty power amplifier via real frequency technique," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 1, pp. 99–111, Jan. 2012.

[63] J. M. Rubio, J. Fang, V. Camarchia, R. Quaglia, M. Pirola, and G. Ghione, "33.6-GHz wideband GaN Doherty power amplifier exploiting output compensation stages," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 8, pp. 2543–2548, Aug. 2012.

[64] M. Akbarpour, M. Helaoui, and F. M. Ghannouchi, "A transformer-less load-modulated (TLLM) architecture for efficient wideband power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 9, pp. 2863–2874, Sep. 2012.

[65] J. H. Qureshi, N. Li, W. C. E. Neo, F. Rijs, I. Blednov, and L. C. N. de Vreede, "A wide-band 20W LMOS Doherty power amplifier," in *IEEE MTT-S International Microwave Symposium Digest*, Anaheim, CA, May 2010, pp. 1504 – 1507.

[66] R. Darraji, F. M. Ghannouchi, and M. Helaoui, "Mitigation of bandwidth limitation in wireless Doherty amplifiers with substantial bandwidth enhancement using digital techniques," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 9, pp. 2875–2884, Sep. 2012.

[67] D. Gustafsson, C. M. Andersson, and C. Fager, "A novel wideband and reconfigurable high average efficiency power amplier," in *IEEE MTT-S International Microwave Symposium Digest*, Montreal, Canada, Jun. 2012.

[68] F. Yamaki, K. Inoue, , N. Ui, A. Kawano, and S. Sano, "A 65 % drain efficiency GaN HEMT with 200 W peak power for 20 V to 65 V envelope tracking base station amplifier," in *IEEE MTT-S International Microwave Symposium Digest*, Baltimore, MD, Jun. 2011.

[69] R. W. Klopfenstein, "A transmission line taper of improved design," *Proceedings of the Institute of Radio Engineers*, vol. 44, no. 1, pp. 31–35, Jan. 1956.

[70] V. Carrubba, A. L. Clarke, M. Akmal, J. Lees, J. Benedikt, P. J. Tasker, and S. C. Cripps, "On the extension of the continuous class-F mode power amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 1, pp. 1294–1303, May 2011.

[71] *Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment (UE) Radio Transmission and Reception*, 3GPP TS 36.101 V11.0.0, 2012 Std.

[72] F. Mkadem, S. Boumaiza, J. Staudinger, and J. Wood, "Systematic pruning of Volterra series using Wiener G-functionals for power amplifier and predistorter modeling," in *2011 European Microwave Integrated Circuits Conference (EuMIC)*, Oct. 2011, pp. 482–485.

[73] F. H. Raab, "Efficiency of Doherty RF power-amplifier systems," *IEEE Transactions on Broadcasting*, vol. 3, pp. 77–83, Sep. 1987.

[74] M. Iwamoto, A. Williams, P.-F. Chen, A. G. Metzger, L. E. Larson, and P. M. Asbeck, "An extended Doherty amplifier with high efficiency over a wide power range," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 12, pp. 2472–2479, Dec. 2001.

[75] Y. Yang, J. Cha, B. Shin, and B. Kim, "A fully matched N-way Doherty amplifier with optimized linearity," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 3, pp. 986–993, Mar. 2003.

[76] N. Srirattana, A. Raghavan, D. Heo, P. E. Allen, and J. Laskar, "Analysis and design of a high-efficiency multistage Doherty power amplifier for wireless communications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 3, pp. 852–860, Mar. 2005.

[77] W. C. E. Neo, J. Qureshi, M. J. Pelk, J. R. Gajadharsing, and L. C. N. de Vreede, "A mixed-signal approach towards linear and efficient N-way Doherty amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 5, pp. 866–879, May 2007.

[78] M. J. Pelk, W. C. E. Neo, J. R. Gajadharsing, R. S. Pengelly, and L. C. N. de Vreede, "A high-efficiency 100 W GaN three-way Doherty Amplifier for base-station applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 7, pp. 1582–1591, Jul. 2008.

[79] I. Kim, J. Moon, S. Jee, and B. Kim, "Optimized design of a highly efficient three-stage Doherty PA using gate adaptation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 10, pp. 2562–2574, Oct. 2010.

[80] B. Kim, I. Kim, and J. Moon, "Advanced Doherty architecture," *IEEE Microwave Magazine*, vol. 11, no. 5, pp. 72–86, Aug. 2010.

[81] J. Gajadharsing, "Recent advances in Doherty amplifiers for wireless infrastructure," in *IEEE MTT-S International Microwave Symposium Workshop WSC*, 2009.

[82] D. Gustafsson, "Theory and design of wideband Doherty power amplifiers," Licentiate Thesis, Chalmers University of Technology, Gothenburg, Sweden, 2012.

[83] R. Darraji and F. M. Ghannouchi, "Digital Doherty amplifier with enhanced efficiency and extended range," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 11, pp. 2898–2909, Nov. 2011.

[84] G. Hanington, P.-F. Chen, P. M. Asbeck, and L. E. Larson, "High-efficiency power amplifier using dynamic power-supply voltage for CDMA applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 8, pp. 1471–1476, Aug. 1999.

[85] A. Zhu, J. C. Pedro, and T. J. Brazil, "Dynamic deviation reduction-based Volterra behavioral modeling of RF power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, pp. 4323–4332, 2006.

[86] S. C. Cripps, "Indeterminate inversion," *IEEE Microwave Magazine*, vol. 12, no. 7, pp. 32–129, Dec. 2011.

[87] D. Y.-T. Wu, F. Mkadem, and S. Boumaiza, "Design of a broadband and highly efficient 45W GaN power amplifier via simplified real frequency technique," in *IEEE MTT-S International Microwave Symposium Digest*, Anaheim, CA, May 2010, pp. 1090–1093.

[88] D. Y.-T. Wu and S. Boumaiza, "A modified Doherty configuration for broadband amplification using symmetrical devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 10, pp. 3201–3213, Oct. 2012.