Noise Analysis and Measurement of Integrator-based Sensor Interface Circuits for Fluorescence Detection in Lab-on-a-chip Applications

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Lab-on-a-chip (LOC) biological assays have the potential to fundamentally reform healthcare. The move away from centralized facilities to Point-of-Care (POC) testing of biological assays would improve the speed and accuracy of these, thereby improving patient care. Before LOC can be realized, a number of challenges must be addressed: the need for expert users must be abstracted away; the manufacturing cost of $5 per test threshold must be met; and the supporting infrastructure must be integrated down to an easily portable size. These challenges can be addressed with the deposition of microfluidics on CMOS chips. By designing application specific integrated circuits (ASICs) much of the automation and the supporting infrastructure needed to run these assays can be integrated into the chip. Additionally, CMOS fabrication is some of the most optimized manufacturing in industry today.

One of the central challenges with LOC on ASIC is the signal acquisition from the microfluidics into the CMOS. Optical sensing of fluorescence is one form of sensing used for LOC assays. Despite a large literature, there has not been a strong demonstration of monolithic LOC fluorescence detection (FD) for low concentration samples. This work explores the limit-of-detection (LOD) for LOC FD through analysis of the signal and noise of a proposed acquisition channel.

The proposed signal acquisition channel consists of an on chip photodiode and integrator based amplification circuits. A hand analysis of the signal propagation through the channel and the noise sources introduced by the circuitry, is performed. This analysis is used to establish relationships between different circuit parameters and the LOD of a hypothetical LOC device. The hand analysis is verified through simulation and the acquisition channel is implemented in: (i) the Austrian Microsystems 350nm CMOS process, (ii) discrete components. Testing of the CMOS chip revealed several issues not identified in extracted simulation; however, the discrete integrator demonstrated many of the trends predicted by the hand analysis and simulations and achieved a LOD of $7.2\mu M$. This analysis provides insight into the engineering trade-offs required to improve the LOD, to enable more wide spread application of LOC FD.

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Dedication

To my family, present and future.

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List of Symbols

LCE_E Light Collection Efficiency of Excitation

LCE_{Fl} Light Collection Efficiency of Fluorescence

μTAS Micro Total Analysis System

APD Avalanche Photodiode

ASIC Application Specific Integrated Circuit

CTIA Capacitive Transimpedance Amplifier

FCC Folded Cascode

FD Fluorescence Detection

FIFO First In-First Out Buffer

FLIM Fluorescence Lifetime Imaging

FWHM Full Width Half Maximum

LCE Light Collection Efficiency

LIF Laser Induced Fluorescence

LOC Lab-on-a-Chip

MSPS Mega-sample per second

NA Numerical Aperture

OD Optical Density

PCB Printed Circuit Board

PMT Photo-Multiplier Tube

POC Point-of-Care

PSD Power spectral density

S/H Sample-and-hold

SBR Signal to Baseline Ratio

SNR Signal-to-Noise Ratio

SPAD Single-Photon Avalanche Diode

TIA Transimpedance Amplifier or Resistive Transimpedance Amplifier

Chapter 1

Introduction

The development and evaluation of biological assays has long been carried out using centralized testing facilities. The requirements for large-scale bench-top infrastructure, expert operators and costly reagents has restricted assay analysis to large, well-funded laboratories. In recent years, however, there has been a surge in the development of point-of-care (POC) diagnostic devices for applications in medicine [1], forensics [2] and food safety [3].

In 1990, micro total analysis systems (μTAS) emerged suggesting that when some biological assays are miniaturized, they operate faster, require less reagent and become more sensitive [4]. With the advances in microfabrication, spurred by Moore's law, it was conceivable to integrate an entire assay onto a "lab-on-a-chip" (LOC) device. These devices address the challenges preventing the migration of biological assays from centralized testing facilities to POC testing by reducing platform size, shortening the time required to carry out an assay and removing the need for expert operators.

The most common signal-acquisition [1, 3, 5] in conventional biological assays are optical and electrochemical detection. Although the latter has been successfully employed in a number of commercial POC products [6, 7], it has found less commercial use in genetic analysis or other low concentration immunoassays due to its limited sensitivity. However, of the variety of optical methods available, fluorescence detection (FD) has been widely used in large-scale automated platforms for genome sequencing and protein microarrays due to

its superior specificity and sensitivity compared to electrochemical detection techniques [8, 9].

While many research groups have focussed on constructing FD-based POC devices, FD has not yet reached the level of integration and cost suitable for commercial POC devices [5]. Market research has suggested that for LOC devices to be successful in the current marketplace, they need to reach a manufacturing cost of $5 per test [10]. Additionally, these devices must be nearly fully integrated, abstracting away the complexity of the assay to allow for easy training and repeatable use [11]. Conventional FD systems require confocal optics, stabilized laser sources, photo-multiplier tubes (PMTs) and high-quality optical filters. Not only are these components expensive [12], but they are too bulky to fit in a hand-held or easily-portable device [13, 14]. Alternative approaches, such as proximity-based detection have demonstrated improved integration by eliminating the need for collection optics [15, 16, 17], these devices still require substantial support infrastructure such as external light sources and discrete electronic control and signal-acquisition circuits.

Platform size and cost in FD-based POC systems can be reduced by integrating the optical and electronic components. To reduce the impact that discrete electronic components have on POC device size, some research groups have integrated these using application-specific integrated circuit (ASIC) technology [18, 19, 20, 21]. Other investigators have also demonstrated various ways of integrating light sources into silicon devices such as light-emitting diodes (LEDs) [22, 23], organic LEDs (OLEDs) [24, 25] and lasers [26]. A monolithic LED and complementary metal-oxide-semiconductor (CMOS) detection circuit has also been demonstrated [27], however no experimental results were provided. The absence of an optical filter is suspected for this omission. Later publications by the same group demonstrated optical detection using a two-chip solution, with the light-source chip placed down on the detection chip with the sample and high-quality optical filter placed in between [28]. A hypothetical hybrid ASIC/microfluidic LOC device for FD detection is shown in Figure 1.1. By depositing photo-polymer microfluidics on the surface of an ASIC chip a monolythic LOC device can be made. Running an analyte through a micro-channel located in the microfluidics, the sample can be optically interrogated by the ASIC below.

While reductions in platform form factor and cost are necessary to ensure widespread use of FD-based POC devices, these systems must also provide sufficient detection limit to be used for personal diagnostics. A review by Dandin *et al.* examined various μTAS FD devices and concluded that, despite many demonstrations of this technology, none has achieved sufficient sensitivity for low-brightness samples [5]. The metric of sensitivity for FD is the limit of detection (LOD) which is the concentration of fluorophore measurable at a given minimum signal-to-noise ratio (SNR).

This thesis focuses on the design of integrated and discrete signal-acquisition circuits for a FD-based LOC device that would be appropriate for the system shown in Figure 1.1. The noise performance of these circuits is analyzed and compared to simulated and experimental results in order to better understand the factors affecting the LOD and how this metric can be improved. Chapter 2 provides additional background on fluorescence, detection hardware, and LOC devices. In Chapter 3, the necessary optical signal strengths are derived and a signal-acquisition-channel architecture is proposed. Analysis of the circuit functions and noise of this architecture help to establish a model for improving the LOD of FD-based LOC devices. Simulations of the acquisition channel in Chapter 4 validate the derived noise calculations and circuit functions. The proposed signal-acquisition channel is implemented (i) as an integrated circuit using the Austria Microsystems (AMS) 350 nm CMOS process and (ii) using discrete components. Experimental results demonstrating the circuit operation and noise performance of these devices are presented in Chapter 5.

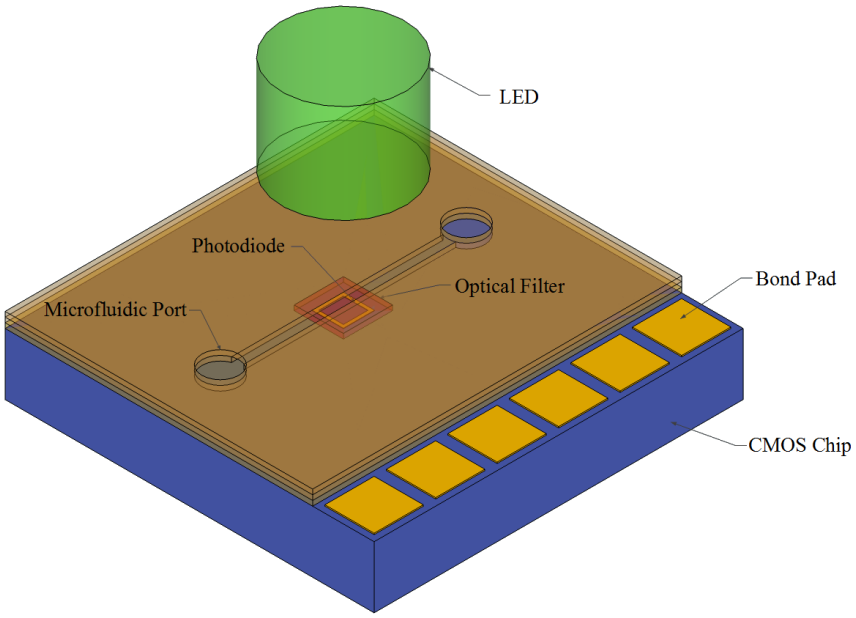


Figure 1.1: A possible implementation of an FD-based LOC device.

Chapter 2

Background

Constructing an FD-based LOC device while providing adequate detection limit poses many engineering challenges. This chapter presents some of these challenges and lays out a framework for the design decisions made later in this thesis.

Fluorescence detection requires three steps: excitation, emission and detection. Excitation is the process of optically exciting the fluorescent molecule into a state. Emission is the process by which the molecule returns to its resting state by re-emitting light at a higher wavelength then the excitation light. Detection refers to the measurement of fluorescent light using a photodetector and measurement circuitry.

The following sections provide a brief introduction to different fluorescent analytes which can be used in biological assays. Additional background is given on matching fluorescent molecules to excitation sources. Various solutions to the challenge of separating the excitation light from the emitted fluorescent light are then discussed. Following this, some of the many optical detectors are examined. Only methods which can be practically integrated into a monolithic device are examined.

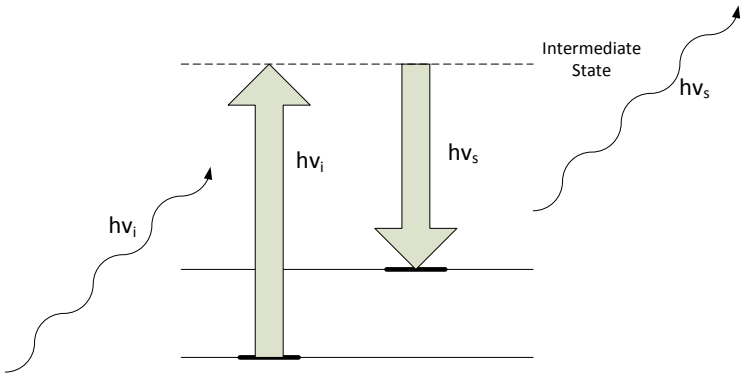


Figure 2.1: Energy state diagram of a fluorescent molecule. The difference between the absorption and emission wavelengths is called the Stokes shift. Adapted from [30]

2.1 Fluorophores

Many molecules have fluorescent properties. A fluorophore is a type of fluorescent molecule commonly used in biological assays. In these assays, fluorophores are chemically attached to biomarkers such as antibodies, DNA primers or other proteins which react with the bio-analyte resulting in a change in the intensity of emitted fluorescent light [29].

The process of fluorescence can be explained using the simplified model of absorbed photons forcing electrons into intermediate higher-energy states. After some period, called the fluorescence lifetime, the electron will fall to a lower energy state and re-emit the photon as shown in Figure 2.1. Each molecule will absorb and re-emit light depending on their distribution of the energy bands of the molecule, however the emission will always be of higher wavelength than the absorption band. The difference between the absorption and emission wavelengths is known as the Stokes shift.

The propagation of light in aqueous solutions is described by the Beer-Lambert Law which states that the initial intensity of the light (I_o) is exponentially attenuated as a function of the wavelength dependent absorbance coefficient ($\varepsilon(\lambda)$), the concentration of

the absorbent molecule (c) and the distance the light has propagated through the solution (x), as described by Eq. 2.1:

$$I_{Tx} = I_o \cdot 10^{-\varepsilon(\lambda)\cdot c\cdot x} \tag{2.1}$$

The power density of light absorbed can then be described as $I_{Ab} = I_o - I_{Tx}$ however examination of the typical values of the exponent allow for a Taylor approximation to be performed reducing the absorption to a linear equation[1]:

$$I_{Ab} = I_o \cdot ln(10) \cdot \varepsilon(\lambda) \cdot c \cdot x \tag{2.2}$$

Not all photons that are absorbed are re-emitted as fluorescence. There is a scaling factor called the quantum yield (ϕ) which determines the total emission intensity (I_{Fl}). The quantum yield varies from fluorophore to fluorophore but is typically in the range of 0.2-0.7. This results in the total emission light intensity to be described by:

$$I_{Em} = I_o \cdot \phi \cdot ln(10) \cdot \varepsilon(\lambda) \cdot c \cdot x \tag{2.3}$$

There are many higher order effects which influence fluorophore emission. Fluorescence lifetime denotes the time constant of the decay from the higher intermediate state down to the final resting state of the electron [32]. This has applications in fluorescence lifetime imaging (FLIM) where to separate the excitation light from the fluorescence, the excitation source is extinguished fast enough that the fluorescence is the only light present. Anisotropy also can have an influence when dealing with polarized light sources and slow rotational time-constants of the molecule [32]. When fluorophores are exposed to high-intensity light, they can also undergo a process called photobleaching in which the fluorophores simply stop re-emitting photons due to chemical changes.

[1] Factoring out I_o, the equation becomes $1-10^{-A}$. A Taylor Expansion of $10^{-A} = 1-A\cdot ln(10)+1/2\cdot A^2\cdot ln^2(10)+...$ however as $A = c\cdot\varepsilon(\lambda)\cdot x$ and a typical value of $A = 10nM\cdot 250000[1/(cm\cdot M)]\cdot 30\mu m = 7.5\cdot 10^{-6}$, the coefficient of the third term $A^2 << A$ and the approximation becomes $1 - 10^{-A} = A \cdot ln(10)$ [31].

2.2 Excitation Sources

A good pairing between the excitation light source and fluorophore is important for the generation of a strong fluorescent signal. Additionally, as will be discussed in the next section, the fluorescence emission spectrum should be as distinct from the excitation source spectrum as possible. This means that 'white' sources such as metal-halide lamps, are not generally appropriate.

The following subsections will provide an overview of different types of lasers, LEDs, and OLEDs suitable as excitation sources. Some of the key physical parameters associated with these devices include the spectral full width half maximum (FWHM), optical power density and relative stability, as well as their scalability for monolithic integration.

2.2.1 Lasers

Lasers are the most commonly used excitation sources to induce fluorescence[2]. The coherent light emitted from the laser results in a huge advantage in power density and small FWHM (typically < 1 nm). This narrow spectrum makes it extremely easy to select optical filters, which will be discussed more in Section 2.3.

While there are many types of lasers available, only semiconductor diode lasers are appropriate for use as an integrated light source. Other types of lasers, such as diode, pumped and dye, require a pressurized Fabry-Perot optical-resonating chamber or external pumping laser to stimulate light emission [34].

Due to the well-established use of laser induced fluorescence (LIF), many fluorophores have been optimized for use with the common laser-diode wavelengths (such as 405 nm, 532 nm, 635 nm and 670 nm [12]). The output power of diode lasers is typically on the order of 5mW. Lasers can also be focused to the optical confinement limit of their particular wavelength, allowing for maximum intensity.

[2] A simple search of Laser Induced Fluorescence in the Web of Knowledge Database yields approximately 24,000 results [33]

The drawbacks associated with using diode lasers include optical stability and integration. Diode laser output is extremely temperature dependent and prone to jitter. Although feedback stabilization can be used to improve stability to around 1%, low-frequency drift (0.1 to 1 Hz) is still a common issue [35]. This presents a problem in biological assays because fluorescent signal changes typically occur in the same signal bandwidth.

2.2.2 LEDs

The use of LEDs as excitation sources is becoming increasingly common [36]. LEDs demonstrate several advantages over lasers such as lower cost, higher efficiency and better intensity stability. There are disadvantages, however, mainly associated with the near isotropic light emission pattern.

When a LED is forward biased, the current flow causes electrons and holes to recombine, resulting in photon emission determined by the bandgap of the substrate. The variation in energies of the electrons and holes result in variations in the wavelength of photons emitted, giving LEDs a slightly larger FWHM (15 to 25 nm) than lasers. The large angle of light emission from LEDs means that the power density of any fluorescent excitation becomes geometry dependent. In integrated devices where the relative angles between the analytes and the samples are large, this is less of a concern. However, it presents a geometric challenge if any spacial filtering of the excitation light is to be employed. Calculations provided in Appendix B.1 provide a power estimate of around 300μW for geometries typical of microfluidic fluorescent detection.

Various groups have demonstrated the use of integrated LEDs for fluorescent detection. Rae *et al.* showed LEDs deposited on an ASIC and used in conjunction with a single-photon avalanche diode (SPAD) array to measure fluorescent dye [28]. Chediak *et al.* provided a more compact implementation where a small LED was deposited on a PIN photodiode below a microfluidic channel [37]. The most complete work to date has been the Ohta group, which demonstrated a single ASIC beside a micro-LED on a polyimide substrate [38].

2.2.3 OLEDs

Organic LEDs are a rapidly-developing technology and are very promising for use as integrated excitation sources. The basic physics of OLED light emission are very similar to that of LEDs, however instead of using crystalline inorganic semiconductors such as GaAs or GaN, they utilize organic compounds which exhibit similar properties. This presents significant fabrication advantages in that instead of flip-chip bonding, as required for LEDs, deposition processes compatible with conventional lithography can be used. Similar to conventional LEDs, OLEDs have a broad spectral emission and emission angle.

There have been a number of demonstrations of OLEDs used as excitation sources for fluorescence measurement devices. Pais *et al.* utilized an OLED and organic photodiode to measure fluorescence detection in a thin film microfluidic device [39]. There have been some very elaborate demonstrations of OLEDs on CMOS suggesting that this is a fairly mature fabrication process. Levy *et al.* demonstrated a full 852x600 pixel three colour OLED display on the surface of an ASIC [24]. Pais demonstrated output levels up to 1000cd/m^2. Assuming a pixel size of 200x200 μm and a viewing angle of 90^o, this provides 107 nW of optical power (Appendix B.1).

2.3 Fluorescent Separation

A key to increasing the sensitivity of circuits for FD is the use of optical methods to eliminate the excitation light from the light measured by the detector. As Roulet *et al.* explained, in a "typical" FD situation the fluorescent signal is 250,000 times weaker than the baseline excitation light [40]. A measurement of the combined excitation and fluorescent signal would require an 18-bit analog-to-digital converter (ADC), and only a single bit would represent the signal. In order to improve this signal-to-baseline ratio (SBR), optical methods for separating these two signals must be employed. Various options will be explored in the following subsections.

There are three key features of the fluorescent light which can be exploited to separate

it from the excitation. Spectrally, there is a difference in wavelength between the excitation and fluorescent light. Geometrically, the excitation light will come from the direction of its source; the fluorescent light can be emitted in any direction. Finally, there is a temporal difference between the excitation of the fluorophore and the re-emission of the fluorescence.

2.3.1 Spectral Separation

Exploiting the spectral differences between excitation and fluorescent light, it is possible to select optical filters which will attenuate the former light while transmitting the latter. The effectiveness of the transmittance of the filter is measured in either optical density (OD), decibels or percent. This work will use optical density which is described mathematically by Eq. 2.4 [40].

$$OD(\lambda) = -log_{10}\left(\frac{I_{Tx}(\lambda)}{I_o(\lambda)}\right) \tag{2.4}$$

As the excitation and the fluorescence will have distinct spectral profiles, both will have a different effective transmission through the filter. This work will use the notation OD_E and OD_{Fl} for the effective optical densities of the excitation and fluorescent light, respectively. The effective OD can be found by replacing the wavelength dependent intensities in Eq. 2.4 with the total intensities. An ideal optical filter would provide a large OD_E and an OD_{Fl} of zero.

Absorbance filters utilize Beer-Lambert's Law to selectively filter specific wavelengths dependent on the chemical structure of the filter. The thickness of these filters will ultimately determine the attenuation. A challenge with this type of filter is autofluorescence. The chemical structure of these pigments may end up re-emitting the photons at higher wavelengths to dissipate the energy absorbed. As the material is made thicker eventually the amount of re-emitted light will become greater than the increased absorbed light, limiting the performance of the filter.

Interference filters are commonly used commercially available filters. These filters contain multiple layers of different index materials which cause components of the light to

reflect and destructively interfere with the incoming light. By precisely depositing these layers, sharp cut off frequencies can be achieved by such filters [5]. These filters also typically provide incredible high attenuation ($OD_E < 5$). Groups such as Burns [41, 15] have deposited such filters directly onto photodiodes for use with fluorescence detection.

The main disadvantage with interference filters is that they do not work very well if the light is not normal to the surface [18]. Richard *et al.* looked to combat this problem by developing a hybrid filter consisting of both an absorbance filter and interference filter [42]. Their hybrid filter achieved a stopband OD of 4.3 at 532nm and a passband OD of 0.13.

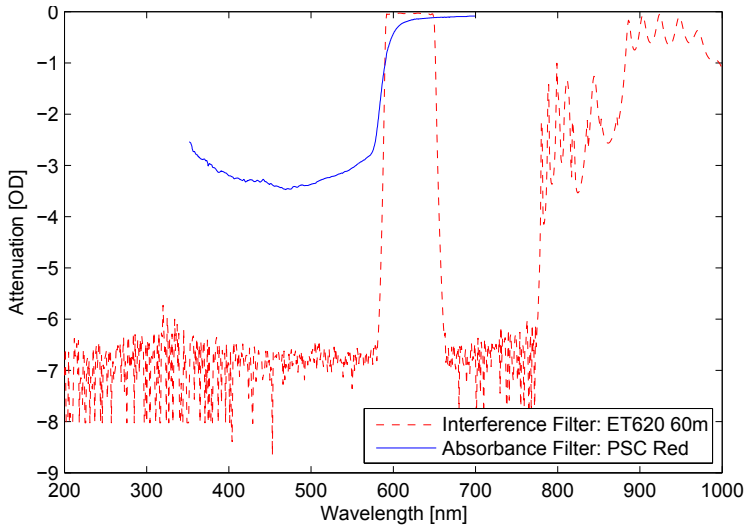


Figure 2.2: Comparison between performance of absorbance filter [42] and interference filter [43].

Another optical trick which can be utilized for fluorescence and excitation separation is to use the polarization of the light. By pre-polarizing the excitation light and then cross polarizing the resulting signal, the excitation light will be removed and the fluorescence will be transmitted. This scheme however assumes that the fluorescence is unpolarized (resulting in $OD_{Fl} = 0.3$ or 50% attenuation) which is not always an acceptable assumption due to anisotropic fluorescence. Such schemes however make a wavelength independent

fluorescent filter, allowing for multiplexed fluorophores to be used without further design consideration being given to the filter. These filters typically achieve OD_E of 2.5 - 2.9 [39, 44]. Some groups have also explored hybrid polarizer-filter techniques and have seen OD_E as high as 8 at some wavelengths [45].

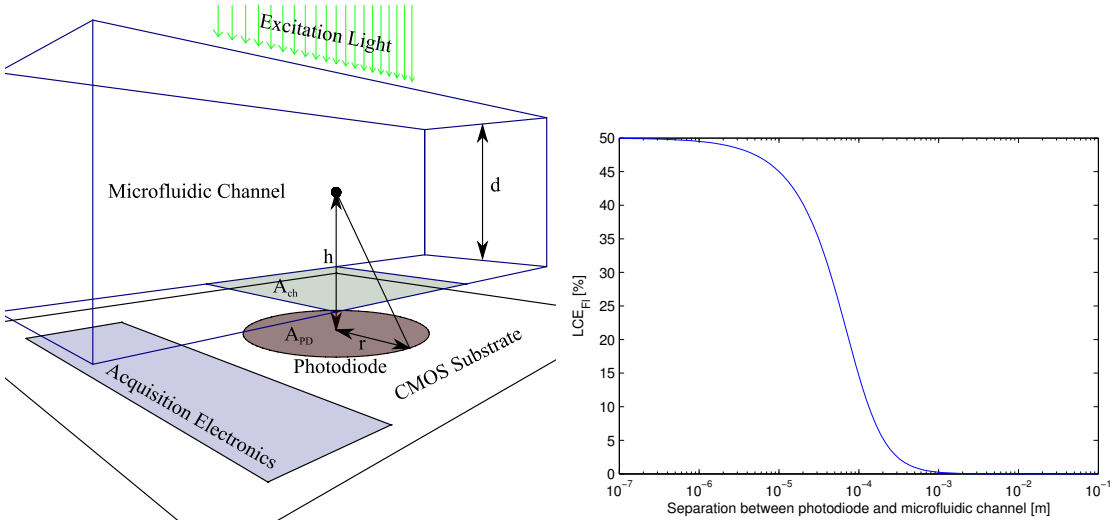
2.3.2 Geometric separation

To geometrically separate the fluorescent light from the excitation light is fairly easy when using a laser excitation light source. As the laser only propagates along a single path and the fluorescence emits isotropically, the detector can simply be placed out of the path of the laser. As the devices scale however this becomes more difficult. Using isotropic light sources such as LEDs or OLEDs, this becomes much more complicated.

With photo-lithography and laser ablation being the most common form of microfluidic fabrication, the devices are usually constrained to being two dimensional. This has largely limited the excitation sources to being either shining directly into the detector, orthogonal to the detector or to illuminating from the same plane as the detector.

To abstract away much of the optical modelling required to accurately predict the amount of fluorescence or excitation light collected, a coefficient is introduced: the Light Collection Efficiency (LCE), which is defined as the total power incident normalized by the total power input. In confocal optical systems the LCE is dictated by the Numerical Aperture (NA) of the device optics [18]. In integrated devices, such as the one presented by Burns *et al.* [41] where the detector is placed directly below the microfluidic channel, the LCE of Fluorescence (LCE_{Fl}) is determined by the size of the detector and the distance between the detector and the channel [5]. By modelling the fluorescences as an isotropic source (as shown in Figure 2.3a) it can be shown that the LCE will follow the relationship shown in Eq. 2.5, where r is the radius of a circular photo-detector and h is the separation between the fluorophore and detector. In the limit where the height becomes small or the size of the photodiode large the LCE_{Fl} converges to 50%. This relationship between the separation distance and LCE_{Fl} (as shown in Figure 2.3b) provides additional motivation for LOC integration.

$$LCE_{Fl} = \frac{1}{2}\left(1 - \frac{h}{\sqrt{h^2 + r^2}}\right) \tag{2.5}$$



(a) (b)

Figure 2.3: (a) Diagram of fluorescent point source light collection by photodiode. (b) Plot of LCE_{Fl} as a function of the dimension h for a photodiode with a $100\mu m$ radius.

This provides additional motivation for integrating fluorescence detection on-chip. In order to maximize LCE_{Fl} the separation must be minimized, which means that the ideal situation is to have the microfluidic deposited directly onto the surface of the photodiode. This however imposes a trade off between LCE_{Fl} and Excitation Light Collection Efficiency (LCE_E).

The LCE_E has a significant influence on the strength of the excitation background signal. In discrete FD devices, it is possible to implement fluidic configurations which limit the LCE_E to less than 1%. When FD is scaled an integrated, it comes increasingly difficult to illuminate the microfluidic channel without increasing LCE_E to near unity.

Some groups have elected to ignore this trade off and simply maximize the LCE_{Fl} and collect nearly all the excitation light ($LCE_E \approx 1$) [17, 45, 46, 47]. Others illuminate the microfluidics orthogonal to the detector, reducing the LCE_E to 0.3-5% [13, 16, 18,

48, 49, 50] with either the use of waveguides or using focused excitation. Chediak *et al.* demonstrated an excitation source built into the same GaAs substrate as the detector [37]. An other group demonstrated a wave-guide etched into the substrate which then reflected the light up into the channel from below and collected the fluorescence through a similar structure [51]. Other groups have employed wavelength dependent diffraction to send the excitation a different direction from the fluorescence [52, 53].

2.3.3 Temporal

The delay between the excitation of the fluorophore and the re-emission of the photon is a decay with a time constant on the order of nanoseconds. With suitably fast electronics it is possible to shutter the light source and record the decay of the fluorescence [28, 54, 55]. This form of detection could soften the requirement of other forms of optical separation, however this increases the complexity and speed required by the photo-detector and light source.

2.4 Photodiodes

A photodetector is required to convert emitted photons to electrons which can be measured by a signal-acqusition circuit. The most common form of on-chip photodetectors are photodiodes. Photodiodes are simple, well-characterized devices with good optical properties and can be implemented in almost any CMOS process.

Silicon photodiodes are formed from a p-n junction and are normally operated under reverse-bias conditions. When a photon is absorbed in the depletion region, an electron-hole pair is created. Due to the applied electric field, the electron is swept to the cathode and the hole is swept to the anode. This charge separation results in a capacitance across the photodiode along with a light-dependent current. A greater light intensity on the photodiode results in a larger current flow. There is a large shunt resistance across the diode which results in a leakage path across the diode. Photodiodes exhibit limited gain

as a single photon can only produce, at most, a single electron-hole pair. As a result, for low light intensities, noise can dominate over the photocurrent.

The photocurrent produced by the photodiode I_{PD} is given by:

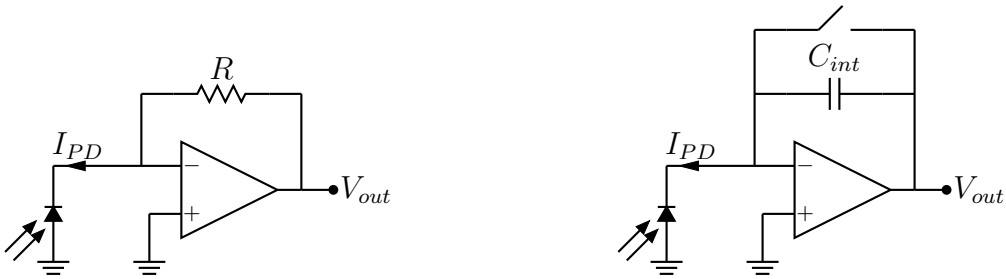
$$I_{PD} = e^{-}\eta\left(\frac{P \cdot \lambda}{h \cdot c}\right) \tag{2.6}$$

where e^{-} is the charge of an electron, η is the quantum efficiency of the photodiode, P is the power incident on the photodiode, λ is the wavelength of light, h is Planck's constant, and c is the speed of light [34]. It is common to reduce these terms to a linear scaling factor called the responsivity ($Resp$) measured in units of A/W. The conversion from incident power to output current can be described by:

$$I_{PD} = Resp \cdot P \tag{2.7}$$

2.5 Measurement Electronics

Two types of of current measurement circuits are considered in this thesis: the resistive transimpedance amplifier (TIA), shown in Figure 2.4a; and the capacitive transimpedance amplifier (CTIA), shown in Figure 2.4b.



(a) Resistive transimpedance amplifier (b) Capacitive transimpedance amplifier

Figure 2.4: Circuit architectures of two types of transimpedance amplifiers.

2.5.1 Resistive Transimpedance Amplifier

A resistive TIA amplifies current signals by driving them across a resistive load using an op-amp. The TIA output voltage is described by Eq. 2.8.

$$V_{out} = R \cdot i(t) \tag{2.8}$$

where t is time. This function shows that the transimpedance (i.e., the ratio of output voltage to signal input current) is fixed by the value of the feedback resistor (R). Although the gain can be manipulated using a bank of on-chip resistors of different values, this would require digital logic to control and would need additional interface pins. The linear relationship between the transimpedance and the resistance also makes the gain proportional to the resistor area. This is a serious drawback in integrated circuits as transimpedance values of 10MΩ would occupy a prohibitively large area.

2.5.2 Capacitive Transimpedance Amplifier

In the CTIA shown in Figure 2.4b, the current is integrated on to a capacitor (C_{int}). The output voltage is given by:

$$V_{out} = \frac{1}{C_{int}} \int_0^{T_{int}} I_{PD}(t)\ dt \tag{2.9}$$

For a fixed value of C_{int}, this architecture allows the gain to be adjusted by changing the integration period (T_{int}). The $1/C_{int}$ relationship also allows for high gain to be achieved using a very small capacitor, reducing the circuit area overhead.

Chapter 3

Design

This chapter presents the analysis and design of a signal acquisition channel for the ASIC CMOS of a LOC FD chip, such as the one shown in Figure 1.1. The design requirements are for a transimpedance amplifier integrated with a single on-chip photodiode. This channel must have adequate sensitivity/limit of detection (LOD) to be used for fluorescence detection, as well as a small chip area and minimal pin count.

A low pin count is important as interfacing with CMOS with microfluidic post-processing provides a significant design challenge. For example Abbott Point of Care's i-STAT cartridge system utilizes pogo-pins to create electrical contact, each pin requiring roughly $1mm^2$. In a full CMOS process this would be prohibitively expensive and thus a minimal pin-count should be maintained.

Of the variety of FD based biological assays, this work will focus on its application for genetic analysis. Genetic analysis assays make extensive use of fluorophore labels. Using labelled DNA sequences, called primers, to bind to a DNA sample, information can be gained about the order and length of the target. Polymerase chain reaction (PCR) is the standard way to genetically amplify DNA samples, where each amplified copy becomes tagged with a fluorophore. In a typical PCR reactions, a starting concentration of fluorescently labelled primers is around 100 nM and the relative PCR yield (conversion of primers to product) is usually between 5-50% depending on how optimized the reaction is. Thus

a low-end signal strength would be around 10 nM concentration. Thus the target LOD for this device is 10 nM. The fluorophore of choice will be AF532, which is commercially available attached to DNA primers.

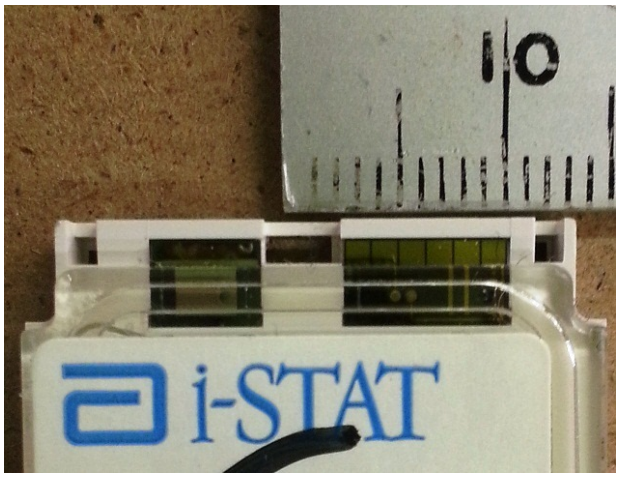


Figure 3.1: Photograph of Abbott Point of Care i-STAT Cartridge. The gold coloured squares located directly below the ruler are the pogo-pin pads. The lower half of the chip is covered by a microfluidic capillary through which a sample and reagents are passed as part of the assay. An application of this research would be to develop a fluorescent detection chip which could be used in place of the electrochemical chip shown here.

In the following sections propose an acquisition channel which contains a photodiode and a capacitive transimpedance amplifier (CTIA) for measurement of the optical signals. Next, the complete transfer function of the photodiode signal is determined and the total noise introduced by the circuit is calculated. This information is then used to find the SNR and LOD of the proposed LOC device.

3.1 Signal Characteristics

The key challenge in fluorescence detection is the separation of the emitted fluorescent light from the background excitation. The light recorded by an on-chip photodiode is modelled

as having two separate components: background excitation light P_B and fluorescent emission light P_{Fl}, both measured in watts. Based on the review by Dandin [5], these can be described analytically as:

$$P_B = I_{LED} \cdot A_{PD} \cdot LCE_B \cdot 10^{-OD_B} \tag{3.1}$$

$$P_{Fl} = I_{LED} \cdot A_{Ch} \cdot LCE_{Fl} \cdot 10^{-OD_{Fl}} \cdot ln(10) \cdot \varepsilon \cdot c \cdot d \cdot \phi \tag{3.2}$$

where A_{PD} is the photodiode area; A_{Ch} is the illuminated area of the microfluidic channel containing the fluorescent molecules; I_{LED} is the intensity of the LED; LCE_E and LCE_{Fl} are the light collection efficiency of the photodiode for the background and fluorescence light respectively (a geometric parameter); OD is the attenuation due to optical filters; c is the concentration of the fluorophore; d is the optical path length of the channel; ε is the extinction coefficient of the fluorophore; and ϕ is the quantum yield of the fluorophore.

Table 3.1 provides a set of model parameters which can be expected for a LED top-illuminated FD system as shown in Figure 1.1. Equations 3.2 and 3.1 predict the background and fluorescent optical signal power to be 400 nW and 10.5 pW respectively. This illustrates the challenge of measuring a signal that is four orders of magnitude smaller than the baseline.

The conversion from optical power to electric current is described by Eq. 2.7. A typical value of responsivity is around 0.29 A/W for optical wavelengths around 500 nm. This gives an electrical current of 3.06 pA for the fluorescent signal and 116nA for the background current.

The frequency content of the fluorescent signal in conventional FD applications, is typically fairly low. For example, the fluorescent signal in Capillary Electrophoresis, is a function of the change in concentration (c in Eq. 3.2) which fluctuates at a rate of 10-50Hz. These slowly changing fluctuations mean that circuit speed is not critical. The background excitation signal is DC.

Table 3.1: Typical parameter values for an integrated fluorescent detection system

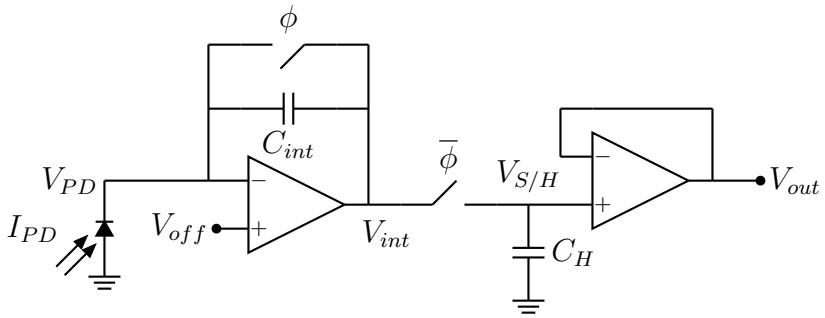
Parameter	Value	Reference
A_{Pd}	200x200μm^2	
A_{Ch}	100x100μm^2	[18]
LCE_{Fl}	40%	[5, 19]
LCE_B	100%	[5, 15]
I_{LED}	$10000W/m^2$	Measured
OD_{Fl}	0.76	[5]
OD_B	3	[5]
c	$10nM$	
d	$40\mu m$	[18, 41]
ϕ	0.61	[56]
ε_{Eff}	$27000(cm \cdot M)^{-1}$	[5, 56]

3.2 Acquisition channel

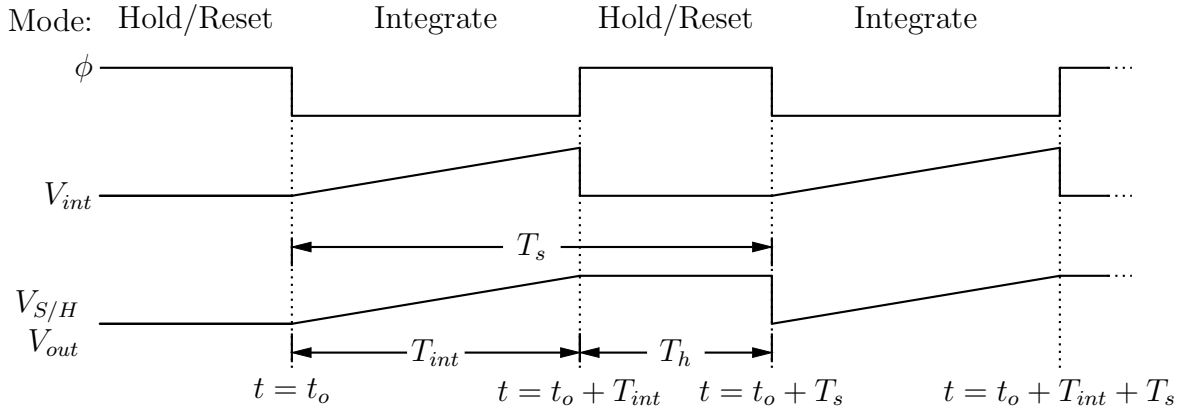
The following subsections describe the circuit selected for signal acquisition, the design choices which resulted in the selection of this circuit, the transfer function and the noise present in this circuit.

3.2.1 Architecture

The architecture for the signal acquisition channel was selected to be as shown in Figure 3.2a. A CTIA was selected due to its adjustable gain with minimal interface, as well as a smaller area requirement. To avoid timing challenges with off-chip measurement circuitry a sample-and-hold (S/H) circuit and buffer is added to the output of the CTIA. The hold signal is configured to operate on complementary signals to the integrator reset signal. This means that while the integrator capacitor is being discharged, the output voltage at the end of the integration period is held by the output buffer, as shown in Figure 3.2b. This circuit is designed for the AMSP35 350nm process, which was selected for its optical process option.



(a) Acquisition channel circuit



(b) Timing diagram

Figure 3.2: The implemented circuit and timing diagram for the signal acquisition channel. The switches are closed when the gate signal is high.

3.2.2 Channel Components

Provided in the following sections is an explanation and justification for the selection of this acquisition channel circuit architecture, along with a derivation of their respective transfer functions.

Photodiode

The main consideration with regards to the photodiode is the area sizing. The sizing is heavily dependent on the geometry of fluorescent sample to be measured. In the tar-

geted microfluidic applications such as CE, the channel width is typically around 100 μm [48]. With the targeted implementation of the microfluidics being a post-processed photopolymer, the separation between the photodiode and the channel is expected to be on the order of 20-50 μm [57].

The geometric parameter which determines the sizing of the photodiode is the light collection efficiency (LCE_{Fl}) (shown in Eq. 2.5). As the limit of this equation provides a maximum value of 50%, a diameter of the photodiode should be selected to give a value close to this. By selecting an edge length of 200μm, the LCE_{Fl} is close to its maximum without occupying excessive area.

Although the AMSP35 process kit comes with a photodiode standard cell, its dimensions are limited to a maximum of 150μm. This photodiode is a p-sub/n-well structure with a guard ring on all sides. As the standard cell does not provide layouts of sufficient size, a scaled version of this cell was laid out by hand.

The photodiode responsivity is specified to be 0.29 A/W (at a wavelength of 500nm) in the AMSP35 process [58]. This wavelength provides a sufficiently accurate approximation of the responsivity for all optical signals considered in this thesis.

The photodiode is electrically modelled as shown in Figure 3.3. The sizing of the photodiode influences its effective capacitance and resistance. The small size of the photodiode and large number of substrate contacts allows R_s to be neglected. The AMSP35 process is specified to have a diode area capacitance of $0.08fF/\mu m^2$. Typical values of R_{PD} for discrete photodiodes are extremely large ($100M\Omega$ to $10G\Omega$ [12]). With the small junction area of the on-chip photodiode, the resistance will be even larger, making the photodiode effectively a current source in parallel with a capacitor.

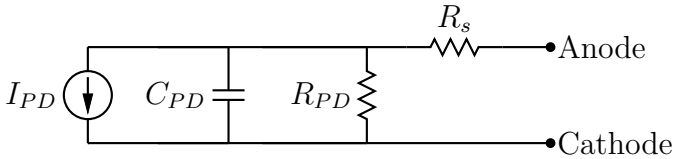


Figure 3.3: Photodiode equivalent circuit.

Capacitive Transimpedance Amplifier

The CTIA is made up of three components: an op-amp, feedback capacitor and switch. For the op-amp a folded cascode NMOS input architecture is used. The full analysis of this op-amp is provided in Appendix A. The op-amp open-loop transfer function is modelled as a single pole response described by:

$$A(f) = \frac{A_o}{1 + \frac{j \cdot f}{f_{3dB}}} \tag{3.3}$$

where A_o is the open loop gain ($R_{out} \cdot G_m$) and f_{3dB} is the corner frequency of the op-amp. The feedback switch is implemented using a NMOS and PMOS pass transistor with dummy transistors for charge injection reduction. A more complete analysis of this is provided in the Sample and Hold Section.

The periodic reset of the CTIA is necessary to prevent saturation of the op-amp. This results in a sinc-response profile of the transimpedance function. The complete response of the CTIA in Figure 3.2a is described by Eq. 3.4 which is derived in Appendix D.

$$\frac{V_{int}(f)}{I_{PD}(f)} = \frac{T_{int}}{C_{int} + \frac{C_{PD}+C_{int}}{A(f)}} \cdot sinc\left(f \cdot T_{int}\right) \tag{3.4}$$

The op-amp response results in a single pole located at:

$$f \approx \frac{C_{int} \cdot A_o \cdot f_{3dB}}{(C_{PD} + C_{int})} \tag{3.5}$$

Noting however, that the $sinc(f \cdot T_{int})$ has an effective 3dB frequency located at $f = 0.44/T_{int}$ it can safely be assumed that:

$$\frac{0.44}{T_{int}} \ll \frac{C_{int} \cdot A_o \cdot f_{3dB}}{(C_{PD} + C_{int})} \tag{3.6}$$

allowing for Eq. 3.4 to be reduced to:

$$\frac{V_{int}(f)}{I_{PD}(f)} = \frac{T_{int}}{C_{int}} \cdot sinc\left(f \cdot T_{int}\right) \tag{3.7}$$

Sample and Hold

Although there are many varieties of S/H circuits available in the literature, an architecture consisting of a transmission gate and hold capacitor is used in this work. A challenge with this style of S/H is charge injection which results from the charge being ejected from the transmission gate channel when the switch is opened. Various charge cancellation techniques can be used to mitigate this non-ideality. This work will make use of the architecture shown in Figure 3.4 because it minimizes the impact of charge injection and its ability to pass voltages close to ground and V_{DD} without losing a threshold drop. The effects of charge injection will be explored further in Section 3.2.4.

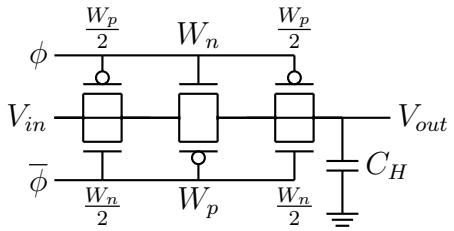


Figure 3.4: S/H circuit using a 6T transmission gate and capacitor.

When the transmission gate is closed, the applied voltage (V_{in}) is transferred to the hold capacitor C_h. When the switch is opened the voltage present on the capacitor is effectively sampled. In the context of the signal path described in Figure 3.2a, the time-domain representation of the sampled-and-held signal is [59]:

$$V_{S/H}(t) = \left(V'_{S/H}(t) \cdot \sum_{k=-\infty}^{\infty} \delta(t - (t_0 + k \cdot T_s + T_{int}))\right) * rect\left(\frac{t}{T_h}\right) \tag{3.8}$$

where $V'_{S/H}(t)$ is the time domain output signal when the switch is closed and $rect(t/T) =$

$u(t+T/2)-u(t-T/2)$, where $u(t)$ is the Heaviside step function. Times t_0, T_s, T_{int}, and T_h are all described by the timing diagram given in Figure 3.2b. It is possible to describe $V_{S/H}(t)$ in the frequency domain by noting that convolution by a *rect* function becomes a multiplication by a *sinc* and that multiplication by a Dirac delta function becomes a convolution by a delta function. To simplify variables, $f_k = f - k/T_s$. The frequency-domain response at the S/H output is given by:

$$V_{S/H}(f) = V'_{S/H}(f) * \sum_{k=-\infty}^{\infty} \delta(f_k) \cdot \frac{T_h}{T_s} \cdot sinc(f \cdot T_h) \cdot e^{-j2\pi f \cdot (t_0+T_{int})} \tag{3.9}$$

$$= \frac{T_h}{T_s} \cdot sinc(f \cdot T_h) \cdot e^{-j2\pi f \cdot (t_0+T_{int})} \cdot \sum_{k=-\infty}^{\infty} V'_{S/H}(f_k) \tag{3.10}$$

where$V'_{S/H}(f)$ is $V_{int}(f)$ after it is passed through the RC filter of S/H. This is given by:

$$V'_{S/H}(f) = \frac{V_{int}(f)}{1 + j2\pi \ f \ R_{SW} \ C_H} \tag{3.11}$$

where R_{SW} is the on resistance of the transmission gate.

Output Buffer

The purpose of the output buffer is to drive the voltage from across the hold capacitor off-chip without drawing charge from this capacitor. A basic unity feedback op-amp configuration is therefore implemented, using the same FCC op-amp as for the CTIA. The differential open-loop response of the op-amp is described by Eq. 3.3. Using the voltage definitions described in Figure 3.2a, the unity feedback configuration forces the output to be:

$$V_{out}(s) = A(s) \cdot (V_{S/H}(s) - V_{out}(s)) \tag{3.12}$$

resulting in the transfer function:

$$\frac{V_{out}(s)}{V_{S/H}(s)} = \frac{A(s)}{A(s)+1} \tag{3.13}$$

Sampling of Acquisition Channel Output

Implicit in the derivation of the CTIA frequency response is that the output of the amplifier is sampled during the hold mode of operation. This will transform the signal from a continuous time equation into a discrete time equation as described by:

$$V_{out}(t) = V'_{out}(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - n\ T_s) \tag{3.14}$$

where $V'_{out}(t)$ is the output of the buffer prior to sampling. This aliases the frequency spectrum coming out of the output buffer and limits the measurable spectrum to less than $1/(2\ T_s)$.

To allow for a more intuitive explanation the circuit will first be simplified by assuming that the pole resulting from the S/H is high frequency and output buffer does not contribute to the frequency response. Consider a current input tone of frequency F_{tone} and unit magnitude applied to the input of the CTIA. The magnitude of the output of the CTIA will be described by:

$$V_{int}(f) = \frac{T_{int}}{C_{int}} sinc(T_{int}F_{tone}) \cdot \delta(f - F_{tone}) \tag{3.15}$$

as shown in the top of Figure 3.5. When the switch of the sample and hold is opened the tone will be copied around the spectrum and scaled by a sinc function and the duty cycle of the hold period as given by:

$$V_{S/H}(f) = \frac{T_h}{T_s} sinc(T_h f) \sum_{k=-\infty}^{\infty} \frac{T_{int}}{C_{int}} sinc(T_{int}F_{tone}) \cdot \delta(f - F_{tone} - \frac{k}{T_s}) \tag{3.16}$$

as shown in the middle of Figure 3.5. When the S/H output is sampled by an ADC the spectrum is folded down into the baseband and all the copied tones from the middle plot

of Figure 3.5 are summed. Using the identity [60]:

$$\sum_{n=-\infty}^{\infty} \frac{sin((n-a)\theta)}{n-a} = \pi \tag{3.17}$$

where $0 < \theta < 2\pi$ and a is unbounded, it can be shown that the sum of these tones will equal the magnitude of the output of the CTIA as shown by:

$$\frac{T_{int}}{C_{int}} sinc(T_{int}F_{tone}) = \frac{T_{int}}{C_{int}} sinc(T_{int}F_{tone}) \frac{T_h}{T_s} \sum_{n=-\infty}^{\infty} sinc(T_h(F_{tone} - \frac{n}{T_s})) \tag{3.18}$$

The location of the tone in the measured output is determined by the relationship:

$$f_{out} = F_{tone} - \frac{p}{T_s} \tag{3.19}$$

where p is an integer which force f_{out} to lie between 0 and $F_s/2$. As a result of the aliasing f_{out} does not map one-to-one with F_{tone}. Multiple values of F_{tone} can be placed at the same frequency of f_{out}. Thus, when superposition is applied and F_{tone} is allowed to be a continuum of frequencies, the sum of all values of p must be taken. This results in the output spectrum of the sampled results being described by:

$$V_{out}(f) = \sum_{p=-\infty}^{\infty} \frac{T_{int}}{C_{int}} sinc(T_{int}(f - \frac{p}{T_s})) \cdot I_{PD}(f - \frac{p}{T_s}) \tag{3.20}$$

The infinite summation and limitations on the output frequency values for which $V_{out}(f)$ can be evaluated, makes it difficult to attain intuitive understanding of the mathematical relationships of aliased functions. As a result, it will be more helpful in coming sections to plot the output magnitude as a function of the input frequency.

Removing the assumptions of a high gain of the output buffer and high pole frequency

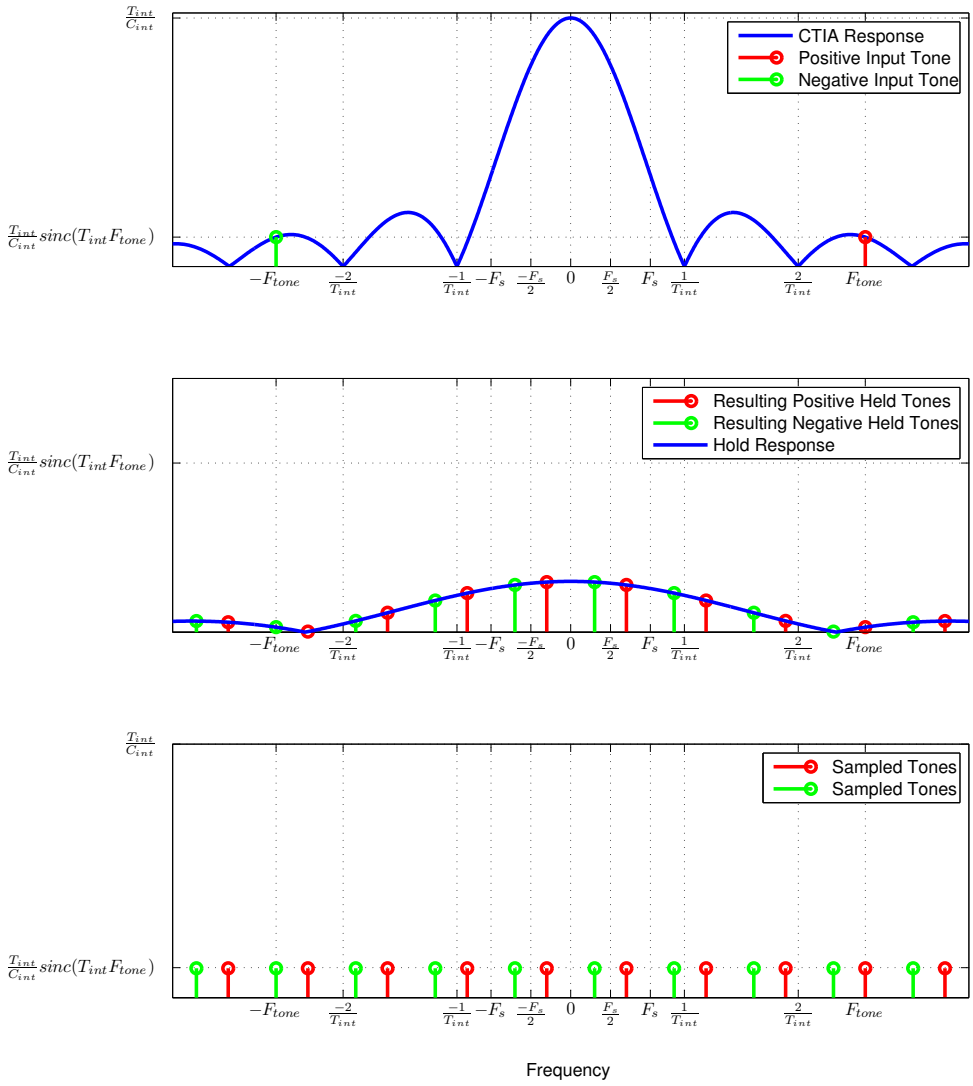


Figure 3.5: Top: The output spectrum of the CTIA to a current tone applied across the photodiode. Middle: When the S/H switch is opened the tone from the plot above is copied to frequency multiples of $1/T_s$ and scaled by a sinc function. Bottom: When the S/H is sampled by an ADC all the tones from the middle plot are summed and result in the same magnitude as the top plot.

of the S/H, the output spectrum is described by:

$$V_{out}(f) = \sum_{p=-\infty}^{\infty} \frac{V_{int}(f - \frac{p}{T_s})}{1 + j2\pi(f - \frac{p}{T_s}) \cdot R_{SW}C_H} \frac{A(f - \frac{n}{T_s})}{A(f - \frac{n}{T_s}) + 1} \tag{3.21}$$

provided $sinc(A_v \cdot f_{3dB} \cdot T_h) \approx 0$.

3.2.3 Voltage Magnitude Spectrum of Complete Signal Acquisition Channel

The complete voltage magnitude spectrum describing the signal acquisition channel is described in this section. The signal acquisition begins in the CTIA where the photodiode current charge is accumulated on the capacitor. Assuming that the inequality in Eq. D.28 is satisfied, the magnitude of the transimpedance is described by Eq. 3.7. When plotted, nulls can be seen at integer multiples of $1/T_{int}$ (Figure 3.6).

When the CTIA output is propagated through the S/H circuit it is aliased by the sampling and copies of the integrator output spectra are shifted to integer multiples of the sampling frequency. As a result of the hold period, an additional sinc function filters the aliased spectrum over a passband related to the hold duration. The spectrum is additionally scaled by T_h/T_s because as T_h becomes smaller, the pass-band of the hold sinc function becomes larger and more copies of the CTIA output are passed to the buffer. As no additional power is added to the signal due to the sampling, the spectrum needs to be scaled by T_h/T_s. The voltage magnitude spectrum at the S/H output is given by:

$$\left\|V_{S/H}(f)\right\| = \left\| \frac{T_h \cdot T_{int}}{T_s \cdot C_{int}} \cdot sinc(f \cdot T_h) \cdot \sum_{k=-\infty}^{\infty} \frac{I_{PD}(f_k) \cdot sinc\left(f_k \cdot T_{int}\right)}{1 + j2\pi f_k \cdot R_{SW}C_H} \right\| \tag{3.22}$$

where, $f_k = f + k/T_s$.

As a result of the op-amp frequency response, the output buffer places a bandwidth

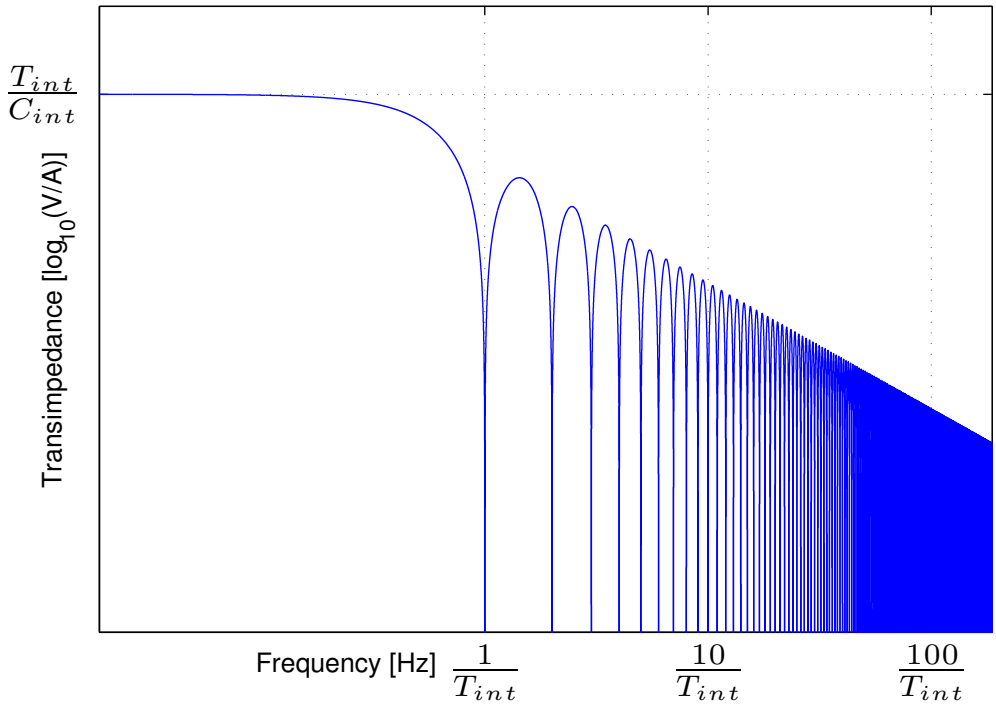


Figure 3.6: Transimpedance magnitude of the CTIA (Eq. 3.7). Both the x and y axes are plotted on a logarithmic scale.

limit on the signal output resulting in a output voltage magnitude of:

$$\|V_{out}(f)\| = \left\| \frac{T_h \cdot T_{int}}{T_s \cdot C_{int}} \cdot sinc(f \cdot T_h) \cdot \sum_{k=-\infty}^{\infty} \frac{I_{PD}(f_k) \cdot sinc\left(f_k \cdot T_{int}\right)}{1 + j2\pi f_k \cdot R_{SW} C_H} \cdot \frac{A_o \cdot f_{3dB}}{f_{3dB} \cdot (A_o + 1) + j \cdot f} \right\| \tag{3.23}$$

As a result of frequency aliasing from the ADC, the spectrum is folded over when sampled. This results in a measured frequency domain spectrum of:

$$V_{out}(f) = \frac{T_{int}}{C_{int}} \sum_{p=-\infty}^{\infty} \frac{sinc\left((f - \frac{p}{T_s}) \cdot T_{int}\right) \cdot I_{PD}(f - \frac{p}{T_s})}{1 + j2\pi(f - \frac{p}{T_s}) \cdot R_{SW} C_H} \cdot \frac{A(f - \frac{p}{T_s})}{A(f - \frac{p}{T_s}) + 1} \tag{3.24}$$

3.2.4 Acquisition Channel Interference

Non-idealities in the operation of the acquisition channel result in systematic addition of unwanted signals. Different from noise, these interfering signals are not generated by random processes and could, in principle, be determined and removed. The two sources of interference that are discussed in the following sections are: charge injection by the transmission gates and interference generated by the photodiode while the integrating capacitor is being reset.

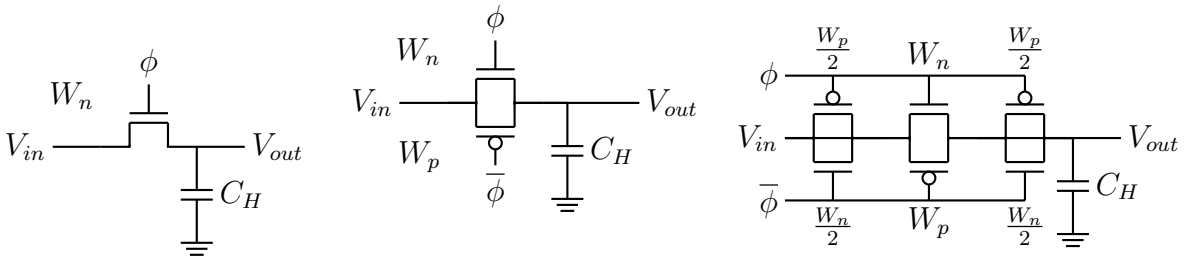
Switch Charge injection

The chief problem with simple transmission gates is charge injection. When the gate is closed, charge is forced out of the MOSFET channel and injected onto the trace on either side of the FET [61]. Should a capacitor be located at one or both ends of the transmission gate, the injected charge will affect the voltage on the capacitor. In the case of the S/H circuit shown in Figure 3.7a, the charge injected by a single NMOS results in a change of voltage described by:

$$\Delta V = \frac{W_n \cdot L_n \cdot C_{ox}(V_\phi - V_{in} - V_{TH})}{2C_H} \tag{3.25}$$

where W_n and L_n are the dimensions of the transistor, C_{ox} is the gate oxide capacitance per unit area, V_ϕ is the gate voltage, V_{in} is the voltage being passed by the gate, V_{TH} is the transistor threshold voltage and C_H is the hold capacitor value of the S/H.

One technique for reducing charge injection is to use parallel PMOS and NMOS transistors as the switch as shown in Figure 3.7b. When the gate is switched off, the PMOS will eject holes and the NMOS will eject electrons which will ideally cancel the total injected charge. This configuration provides the additional advantage of passing both a hard 0 and a hard V_{DD}. One issue with this is that the charge injected by the PMOS and NMOS do not cancel completely because the charge from each is a function of V_{in}. However, if the transistors are sized such that a midrange value of V_{in} provides no charge injection, this non-ideality can be minimized. By first setting the charge ejected from each transistor



(a) 1T transmission gate with hold capacitor

(b) 2T transmission gate with hold capacitor

(c) 6T transmission gate with hold capacitor

Figure 3.7: Three different styles of transmission gates used in a S/H.

equal, the dimensions can be selected using the following equation [61]:

$$W_n \cdot L_n \cdot C_{ox}(V_\phi - V_{in} - V_{THN}) = W_p \cdot L_p \cdot C_{ox}(V_{in} - |V_{THP}|) \tag{3.26}$$

Then by optimizing the charge cancellation for $V_{in}/2$:

$$\begin{aligned} W_n \cdot L_n(3.3 - 3.3/2 - 0.46) &= W_p \cdot L_p(3.3/2 - 0.68) \\ W_n \cdot L_n \cdot 1.19 &= W_p \cdot L_p 0.97 \\ W_n \cdot L_n \cdot 1.22 &= W_p \cdot L_p \end{aligned}$$

However, in simulation when the input voltage was increased to 3.3V for a $1\mu m$ width NMOS, a charge injection of $10.25fC$ ($20.5mV$ on a $0.5pF$ capacitor) was observed, which is too large to be acceptable.

An alternative method to reduce charge injection is to place a 'dummy' transistor with its source and drain connected to the input or output trace to sink the injected charge by running it on complementary signals, as shown in Figure 3.7c. Using the first-order approximation that equal charge is injected on either side of the pass transistor, a PMOS and NMOS dummy of half the width of the pass transistor is placed on either side. The PMOS and NMOS dummy gate signals will be complementary to the pass transistors PMOS and NMOS respectively. Theoretically, this provides perfect charge cancellation. Layout mismatch, however, will result in some excess charge accumulating. This style of

transmission gate has superior performance and will therefore be used for the S/H and CTIA reset switch.

Reset Interference

During the reset phase of signal acquisition (Figure 3.2a), the photodiode drives current across the reset switch introducing a voltage onto C_{int}. The circuit conditions under which this happens is shown in Appendix G in Figure G.1. This voltage will be stored and transferred to the output when the circuit returns to the integrate phase (Figure G.2). This section will derive the total voltage stored on C_{int} and the transfer function to the circuit V_{out}.

The voltage resulting from the photodiode current during reset is described by:

$$V'_{cap}(f) = I_{PD}(f) \cdot \frac{R_{SW}}{1 + j2\pi f R_{SW} C_{int}} \tag{3.27}$$

which is very close to the response of a TIA amplifier discussed in Section 2.5.1. When the circuit changes back into integrate mode, this voltage is sampled and held. In the frequency domain this is represented by a multiplication by a sinc function and spectral copies being moved to multiples of the sampling frequency as described by:

$$V_{cap}(f) = \frac{T_h}{T_s} sinc(f \cdot T_h) \sum_{k=-\infty}^{\infty} V'_{cap}(f - \frac{k}{T_s}) \tag{3.28}$$

In integrate mode, the voltage of the capacitor is forced across the S/H circuit resulting in a frequency response described by:

$$V_{S/H}(f) = V_{cap}(f) \frac{A(f)}{A(f) + 1} \cdot \frac{1}{1 + j2\pi f \ R_{SW} C_h} \tag{3.29}$$

When this is sampled again by the S/H circuit, the frequency response is shaped by another sinc, aliased again and passed through the buffer. When the buffer output is finally sampled by the ADC, the various sinc functions cancel (as was previously shown in Section 3.2.2)

and the transfer function from the reset mode capacitor voltage to the output is described by:

$$V_{out}(f) = \sum_{p=-\infty}^{\infty} \frac{V_{cap}(f - \frac{p}{T_s})}{1 + j2\pi(f - \frac{p}{T_s})R_{SW}C_h} \left(\frac{A(f - \frac{p}{T_s})}{A(f - \frac{p}{T_s}) + 1} \right)^2 \tag{3.30}$$

The output as a function of the photodiode current is described by:

$$V_{out}(f) = \sum_{p=-\infty}^{\infty} \frac{1}{1 + j2\pi f_p R_{SW}C_h} \cdot \left(\frac{A(f_p)}{A(f_p) + 1} \right)^2 \cdot \frac{I_{PD}(f_p) \cdot R_{SW}}{1 + j2\pi f_p R_{SW}C_{int}} \tag{3.31}$$

where $f_p = f - \frac{p}{T_s}$.

3.2.5 Acquisition Channel Noise

The characterization of the noise of the acquisition channel is critical for determining the LOD of the FD system. There are a number of different noise sources which contribute to the output-referred noise PSD. These include: photon shot noise, photodiode dark current shot noise, photodiode thermal noise, op-amp noise (flicker and thermal), and the flicker and thermal noise of the switches. The following sections will derive the output referred noise PSD for each of the noise sources in the acquisition channel.

The noise sources in the circuit contribute in different ways to the total noise during the integrate and reset phases of operation. During the integrate phase, the circuit and noise sources are as shown in Figure 3.8a. During reset, no noise is passed directly to the output; however, noise is placed across the integrating capacitor. This results in a random initial condition of the CTIA which is then passed to the output. During the reset phase, the circuit noise sources are as shown in Figure 3.8b.

The following convention will be uesd to indicate the noise variables: Noise PSDs generated by individual circuit elements are denoted with an over line (-). All transformed noise will be denoted as $S^{Mode}_{Location\ \ Source}(f)$, where *Location* is the in the circuit described by the PSD (S/H, out, Cap), *Source* is the noise source generating the PSD (i_{SW1}, v_{n1} etc.), and *Mode* refers to what mode the circuit was in while generating the noise PSD (rs

for reset *int* for integrate). The integrated output noise voltage will be similarly denoted with $v_{Location\ Source\ Mode}$.

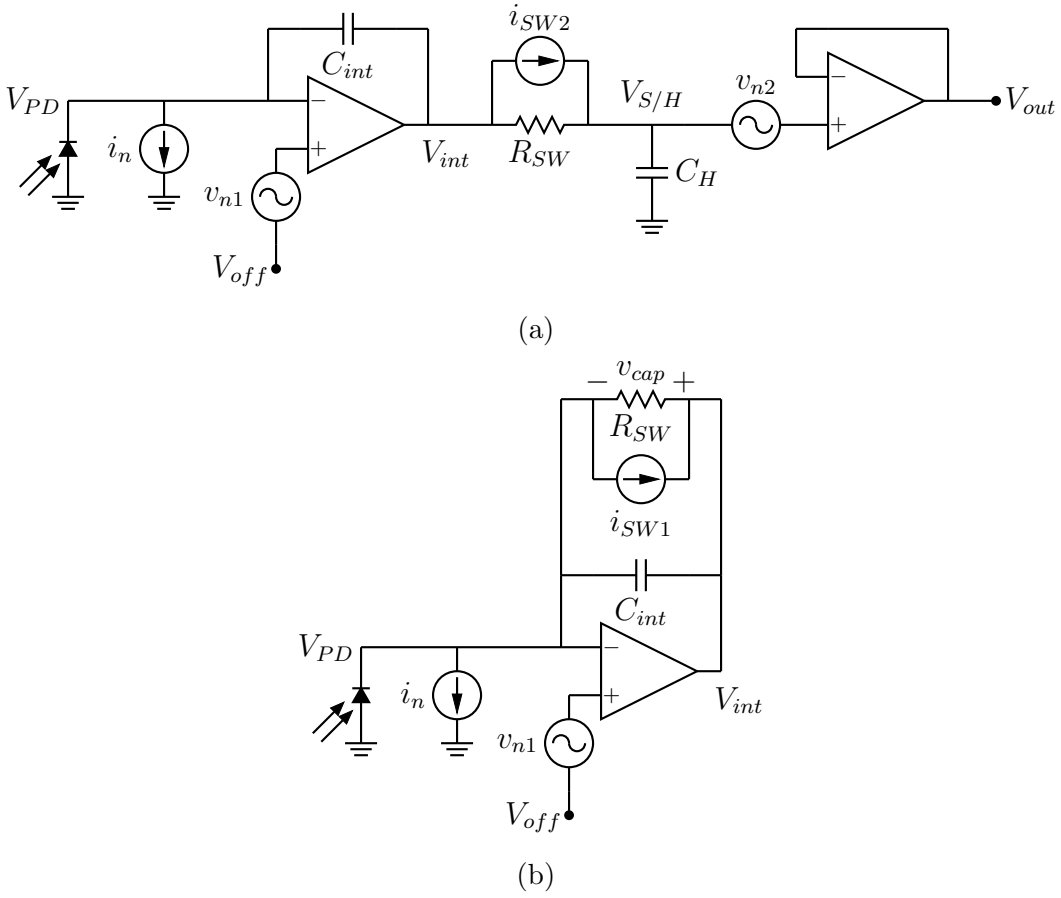


Figure 3.8: (a) Noise sources in the acquisition channel during the integration phase (b) Noise sources in the acquisition channel during the reset phase

Photon Shot Noise

Photon shot noise results from the random arrival of individual photons. The time between photon arrivals is modelled by a Poisson distribution, which means that the standard deviation between photon arrival events is equal to the square root of the mean number of

photons per counting period [21]. The shot noise current PSD, denoted by $\overline{i_n}^2$ in Figure 3.8a is described by:

$$\overline{i_n}^2 = 2 \cdot e^- I = 2 \cdot e^- P_{PD} \cdot resp \tag{3.32}$$

where e^- is the charge of an electron, I is the average current, P_{PD} is the average power and $resp$ is the photodiode responsivity. In the limit of detection, P_{PD} is expected to be dominated by the background excitation light and thus, $P_{PD} = P_B$. Substituting Eq. 3.1 in to Eq. 3.32 results in:

$$\overline{i_n}^2 = 2 \cdot e^- I_{LED} \cdot A_{PD} \cdot LCE_B \cdot 10^{-OD_B} \cdot resp \tag{3.33}$$

Since the photon shot noise source is located at the same point in the circuit as the input signal, the output referred noise voltage PSD can be found using Eq. 3.24 as follows:

$$S^{int}_{out\ i_n}(f) = \left\| \frac{T_{int}}{C_{int}} \sum_{p=-\infty}^{\infty} \frac{sinc\left((f - \frac{p}{T_s}) \cdot T_{int}\right)}{1 + j2\pi(f - \frac{p}{T_s}) \cdot R_{SW} C_H} \cdot \frac{A(f - \frac{p}{T_s})}{A(f - \frac{p}{T_s}) + 1} \right\|^2 \cdot \overline{i_n}^2 \tag{3.34}$$

During the reset phase, the shot noise undergoes the same interference effect as the photodiode signal described in Eq. 3.31. As the circuit is only in reset for a fraction of the sampling period, the output voltage PSD is scaled by the reset duty cycle. The output shot noise PSD will therefore also contribute:

$$S^{rs}_{out\ i_n}(f) = \frac{T_h}{T_s} \cdot \left\| \sum_{p=-\infty}^{\infty} \frac{1}{1 + j2\pi f_p R_{SW} C_h} \cdot \left(\frac{A(f_p)}{A(f_p) + 1} \right)^2 \cdot \frac{R_{SW}}{1 + j2\pi f_p R_{SW} C_{int}} \right\|^2 \cdot \overline{i_n}^2 \tag{3.35}$$

Photodiode Noise

The photodiode contributes dark current shot noise and thermal noise to the output of the signal acquisition channel. The dark current shot noise differs from the photon shot noise discussed before in terms of the source of the current. The dark current of the photodiode

is an intrinsic DC current resulting from random generation of electron/hole pairs and is a function of the photodiode area [58]. The dark current shot noise PSD is described by:

$$\overline{i_n}^2 = 2 \cdot e^- I_{Dark} = 2 \cdot e^- \cdot \rho_{Dark} \cdot A_{PD} \tag{3.36}$$

where ρ_{Dark} is the dark current per unit area and A_{PD} is the area of the photodiode.

The thermal noise current PSD of the photodiode is a function of the diode resistance R_{PD} and is given by:

$$\overline{i_n}^2 = \frac{4 \cdot k \cdot T}{R_{PD}} \tag{3.37}$$

where k is the Boltzmann constant and T is the temperature.

Both of these noise sources are introduced as a current source in parallel with the photodiode. Thus both of these noise sources will be subject to the same frequency shaping as for the photon shot noise described in Eq. 3.34 and Eq. 3.35.

CTIA Op-amp Noise

The FCC op-amp used in the signal acquisition channel has an input referred noise $\overline{v_n}$ PSD made up of thermal and flicker noise. The full description and derivation of this noise is provided in Appendix A.3. The op-amp noise contributes to both the reset phase noise and the integration phase noise.

During reset, v_{n1} contributes to the random initial condition of V_{cap} as shown in Figure 3.8b. The transfer function from the op-amp input terminal to the integrating capacitor during reset can be described by:

$$\frac{V_{cap}(f)}{v_{n1}(f)} = \frac{A(f)(1 + j2\pi R_{SW}(C_{int} + C_{PD}))}{(A(f) + 1)(1 + j2\pi C_{int} R_{SW}) + j2\pi R_{SW} C_{PD}} \tag{3.38}$$

As a result of the periodic switching between the reset and integrate modes, the actual noise stored on V_{cap} is scaled by the reset duty cycle. The output-referred noise voltage PSD from this capacitor follows the same transfer function as described by Eq. 3.30, resulting

in the output noise voltage PSD being described by:

$$S^{rs}_{outv_{n1}}(f) = \frac{T_h}{T_s} \cdot \left\| \sum_{p=-\infty}^{\infty} \frac{V_{cap}(f - \frac{p}{T_s})}{1 + j2\pi(f - \frac{p}{T_s})R_{SW}C_h} \left(\frac{A(f - \frac{p}{T_s})}{A(f - \frac{p}{T_s}) + 1} \right)^2 \right\|^2 \tag{3.39}$$

During the integration phase, the CTIA op-amp noise is driven out through the S/H circuit and to the output as shown in Figure 3.8a. The transfer function from v_{n1} to $V_{S/H}$ is described by:

$$\frac{V_{S/H}(f)}{\overline{v_{n1}}(f)} = \frac{A(f) \cdot (1 + Z_{PD} \cdot s \cdot C_{int})}{1 + (A(f) + 1) \cdot Z_{PD} \cdot s \cdot C_{int}} \cdot \frac{1}{1 + R_{SW}C_H s} \tag{3.40}$$

Due to the periodic switching, the magnitude of the ADC sampled output referred noise PSD is scaled by the integration mode duty cycle. When the capacitor value is sampled by opening the S/H transmission gate and sampled again by the ADC it results in the output-referred noise voltage PSD described by:

$$S^{int}_{outv_{n1}}(f) = \frac{T_{int}}{T_s} \cdot \left\| \sum_{p=-\infty}^{\infty} \left(\frac{A(f - \frac{p}{T_s})}{A(f - \frac{p}{T_s}) + 1} \right)^2 \cdot \left(1 + \frac{C_{PD}}{C_{int}} \right) \cdot \frac{\overline{v_{n1}}(f - \frac{p}{T_s})}{1 + j2\pi(f - \frac{p}{T_s})R_{SW}C_h} \right\|^2 \tag{3.41}$$

Reset Transmission Gate Noise

The transmission gate noise is made up primarily of thermal noise. Minimal flicker noise is present as the current flowing through the transistor is very small. The total current noise PSD is described by:

$$\overline{i_{SW1}}^2 = \frac{8}{3} \cdot k \cdot T \cdot (g_m + g_{ds} + g_{mb}) \tag{3.42}$$

where: g_m, g_{ds}, and g_{mb} are all small signal parameters of the transistor; k is the Boltzmann constant; and T is the temperature. This noise current results in a voltage across the

integrating capacitor during the reset phase that is given by:

$$V_{cap}(f) = \frac{R_{SW}(A(f)+1)}{j2\pi f C_{PD} R_{SW} + (A(f)+1)(j2\pi f R_{SW} C_{int} + 1)} \cdot \overline{i_{SW1}} \tag{3.43}$$

This offset is then transformed by the magnitude squared of Eq. 3.30, scaled by the duty cycle of the reset mode, as described by:

$$S_{outi_{SW1}R}(f) = \frac{T_h}{T_s} \cdot \left\| \sum_{p=-\infty}^{\infty} \frac{V_{cap}(f - \frac{p}{T_s})}{1 + j2\pi(f - \frac{p}{T_s}) R_{SW} C_h} \left(\frac{A(f - \frac{p}{T_s})}{A(f - \frac{p}{T_s}) + 1} \right)^2 \right\|^2 \tag{3.44}$$

where $f_p = f - p/T_s$.

The noise contribution during the integration phase is negligible as the values of g_m, g_{ds}, and g_{mb} are extremely small.

Sample and Hold Transmission Gate Noise

The noise contributed by the S/H transmission gate during the sample/integration stage is represented by i_{SW2}. The value of $\overline{i_{SW2}}$ follows the same relationship as in Eq. 3.42. The transfer function to refer this to a voltage PSD across the S/H capacitor is described by:

$${V_{S/H}}^2 = \left\| \frac{R_{SW}}{1 + sC_H R_{SW}} \right\|^2 \cdot \overline{i_{SW2}}^2 \tag{3.45}$$

This noise is scaled by the integration mode duty cycle and then output referred by:

$$S^{int}_{outi_{SW2}}(f) = \frac{T_{int}}{T_s} \cdot \left\| \sum_{p=-\infty}^{\infty} \frac{A(f - \frac{p}{T_s})}{A(f - \frac{p}{T_s}) + 1} \frac{R_{SW}}{1 + j2\pi(f - \frac{p}{T_s}) C_H R_{SW}} \right\|^2 \cdot \overline{i_{SW2}}^2 \tag{3.46}$$

Output Buffer Op-amp Noise

The output buffer noise needs to be treated a little differently because this noise source is not switched. It is simply added to all signals presented to the output. Taking the input

referred noise of the op-amp as calculated in Appendix A.3, it is possible to calculate the resulting output noise from a unity feedback configuration. By placing the op-amp in unity feedback the output noise PSD is described by:

$$S_{outv_{n2}}^{int\ rs}(f) = \left\| \sum_{p=-\infty}^{\infty} \frac{A(f-\frac{p}{T_s})}{A(f-\frac{p}{T_s})+1} \cdot \overline{v_{n2}}(f-\frac{p}{T_s}) \right\|^2 \tag{3.47}$$

3.2.6 Component design

The design choices for the various circuit components are made based on the parametrized equations from the previous sections. To minimize the chances of mistakes, the previously submitted folded cascode op-amp is used for both the output buffer and the CTIA. The analysis of this op-amp is available in Appendix A. This limits the design choices required to the sizing of: C_{int}, C_h and the transmission gate transistors. To limit complexity, the same transmission gate sizing will be used for both the S/H and the CTIA reset gates.

CTIA

As was shown in Section 3.2.2 the gain of the integrator is tied to two parameters: the integration period and the capacitor size. As was discussed in Section 3.1, the baseline current from the excitation light is expected to be 116 nA. To accommodate variation in the excitation intensity and possibly highly concentrated fluorescent samples, the capacitor will be sized to allow for integration of currents up to 130nA without saturating.

Although the bandwidth of these signals is fairly low (10-50Hz), a sampling rate of 4 kHz was selected to help keep the capacitor size low. The AMSP35 technology is a 3.3V process and thus the integrator will saturate at this voltage. Assuming a DC input signal, integration time of $T_{int} = 250\mu s$, and a maximum integration range of 3.3V, the capacitor value needs to be 9.85pF based on Eq. 3.7. To keep things simple, this value was rounded up to 10pF.

Transmission Gate

The two transmission gates in the acquisition channel must facilitate fast reset of the CTIA capacitor, high bandwidth transmission for the S/H. The bandwidth of the S/H can also be adjusted by the sizing of C_h, thus the speed of the CTIA reset is the primary constraint.

The CTIA integrating capacitor was sized to be 10pF in the section above, thus the transmission gate resistance must be low enough that several RC time constants can pass without interfering with the 4kHz sampling rate. Five time constants(τ) are sufficient to return the voltage to less than 1% of the reset value. By placing the requirement that 5τ must pass in less than $1\mu s$, R_{SW} must satisfy:

$$5 \cdot R_{SW} \cdot C_{int} < 1\mu s \tag{3.48}$$

$$R_{SW} < 20k\Omega \tag{3.49}$$

Using the transmission gate resistance equations from [61], the gate resistance is described by:

$$R_{SW} = R_p || R_n \tag{3.50}$$

$$R_n = \frac{L_n}{\mu_n \cdot C_{ox} \cdot W_n \cdot (V_{DD} - V_{in} - V_{THN})} \tag{3.51}$$

$$R_p = \frac{L_p}{\mu_p \cdot C_{ox} \cdot W_p \cdot (V_{in} - |V_{THP}|)} \tag{3.52}$$

where L and W are the dimensions of the transistor, $V_{DD} = 3.3V$, V_{THN} and V_{THP} are the transistor threshold voltages, μ_n and μ_p are the carrier mobilities and C_{ox} is the gate capacitance per unit area. For $1\mu m$ length and width of both transistors, the gate resistance is estimated to be $3.9k\Omega$. In simulation the value of $R_{SW} = 1.67k\Omega$.

Sample and Hold

The sizing of the sample and hold capacitor determines the bandwidth of the signal allowed to pass through to the output buffer. Using a small capacitor reduces the total foot print

used; however, giving a large capacitor helps reduce the noise. A value of $C_h = 100fF$ was selected as it is a compromise between small area and low noise. This sizing places the 3dB frequency of the S/H at 953MHz; which is high enough to allow the photodiode signal to propagate without attenuation.

3.3 Predicted System Performance

Using the parametrized equations and component sizing determined in the previous sections, this section will identify the total gain, noise output voltage PSD and system SNR for the acquisition channel. By determining the SNR, the LOD of the system can be determined and ways of improving the LOD can be identified.

3.3.1 Output Signal Magnitude

The output voltage magnitude of the acquisition channel is given by:

$$V_{out}(f) = \frac{T_{int}}{C_{int}} \sum_{p=-\infty}^{\infty} \frac{sinc\left((f - \frac{p}{T_s}) \cdot T_{int}\right) \cdot I_{PD}(f - \frac{p}{T_s})}{1 + j2\pi(f - \frac{p}{T_s}) \cdot R_{SW}C_H} \cdot \frac{A(f - \frac{p}{T_s})}{A(f - \frac{p}{T_s}) + 1} \tag{3.53}$$

as was described in Eq. 3.24. Taking the acquisition channel parameters given in Section 3.2.6 (summarized in Table 3.2), the output magnitude response for a given input frequency is plotted in Figure 3.9.

By taking the photodiode current signal strengths predicted in Section 3.1, the total output voltage is predicted to have 2.90V of baseline and $76\mu V$ of signal for a fluorophore concentration of 10nM.

3.3.2 Total Output Noise

In the previous sections, the output noise PSD for the different noise sources in the signal acquisition channel were calculated. The noise PSD provides insight into the profile of the

$T_s = 500\mu s$	$T_{int} = 250\mu s$
$T_h = 250\mu s$	$C_{int} = 10pF$
$C_h = 100fF$	$R_{SW} = 1.67k\Omega$
$A_o = 2408V/V$	$f_{3dB} = 1045Hz$

Table 3.2: Summary of Parameters used for Eq. 3.53

noise however does not provide a good measure for the identifying the sensitivity for FD. This section will numerically calculate and analytically approximate the total noise to help identify ways in which the noise of the complete device can be reduced.

Input Noise Current during Integration Phase

There are three current noise sources located at the input to the signal acquisition channel that follow the shaping function described by Eq. 3.34. They are: the baseline shot noise, photodiode thermal noise and dark current shot noise. When the output referred noise PSD is plotted for these sources (Figure 3.10), it can be seen that the baseline shot noise is the dominant source of noise for part of the low frequency measurements.

It can be seen that the shaping of the PSD is dominated by the sinc function from the CTIA. By assuming that the other poles do not contribute the noise PSD can be simplified to:

$$S^{int}_{out_n}(f) = \left\| \frac{T_{int}}{C_{int}} \sum_{p=-\infty}^{\infty} sinc\left((f - \frac{p}{T_s}) \cdot T_{int} \right) \right\|^2 \cdot \overline{i_n}^2 \tag{3.54}$$

The total noise contributed from these noise sources can then be approximated by:

$$v_{out_n I}{}^2 = \int_0^{0.5/T_s} S^{int}_{out_n}(f) df \tag{3.55}$$

$$= \frac{T_{int}}{2\ C_{int}{}^2} \cdot \overline{i_n}^2 \tag{3.56}$$

When Eq. 3.34 is numerically integrated from 1Hz to 10MHz, it predicts the total noise contributed by the excitation light shot noise (given by Eq. 3.33) to be $215\mu V_{RMS}$. When Eq. 3.56 is evaluated, it approximates the total noise to be $304\mu V_{RMS}$. This is sufficiently

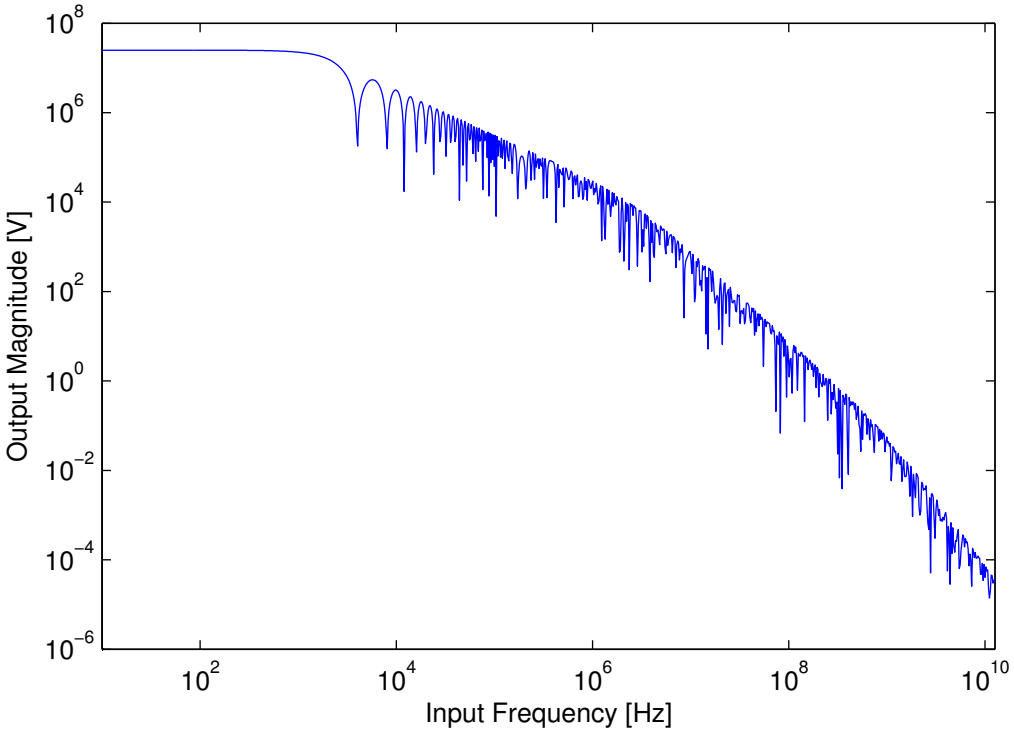


Figure 3.9: The output magnitude for different input frequency sinusoidal current signals of 1A amplitude.

close to the numerically integrated value to provide insight into methods for improving the noise performance. The photodiode dark current shot noise is numerically integrated to be $54\mu V_{RMS}$ compared to the approximated value of $77\mu V_{RMS}$. The photodiode thermal noise is numerically found to be $0.72\mu V_{RMS}$ and approximated to be $1.01\mu V_{RMS}$.

Input Noise Current during Reset Phase

The noise sources located at the input to the acquisition channel also contribute during the Reset phase as described by Eq. 3.35. By assuming that the op-amp has high bandwidth and that the dominant pole of this response is from $C_{int}||R_{SW}$, the integral can be taken

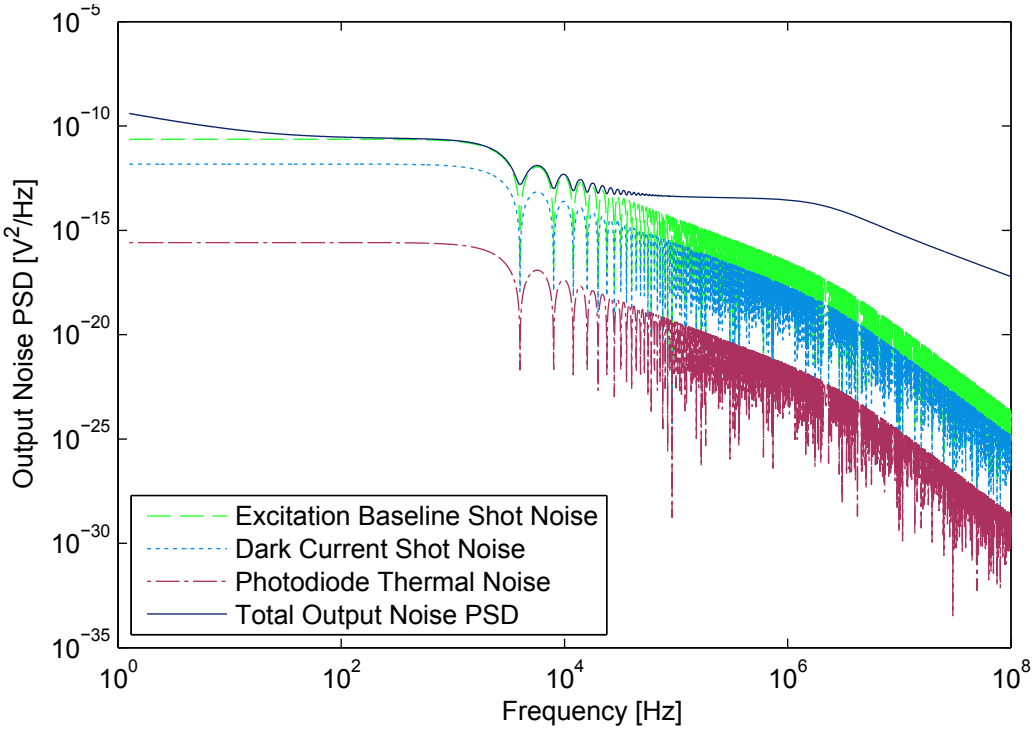


Figure 3.10: The output referred noise PSDs for the baseline shot noise, photodiode thermal noise and dark current shot noise during the integration phase, in comparison to the total noise PSD of the acquisition channel.

to find the total noise contributed:

$$v_{out_nR}{}^2 = \int S^{rs}_{out_n}(f)df \tag{3.57}$$

$$= \int \frac{T_h}{T_s} \frac{R_{SW}{}^2}{1+(2\pi f_p R_{SW} C_{int})^2} \cdot \overline{i_n}^2 df \tag{3.58}$$

$$= \frac{R_{SW} \cdot T_h}{4 \cdot C_{int} \cdot T_s} \cdot \overline{i_n}^2 \tag{3.59}$$

This approximation is not always ideal as the op-amp pole may be dominant for some designs. However when Eq. 3.35 is numerically integrated from 1Hz to 10MHz, the total output noise contributed by the excitation light shot noise is predicted to be $0.31\mu V_{RMS}$ which is reasonably close to the value of $1.76\mu V_{RMS}$ predicted by Eq. 3.59, despite the op-

amp being the dominant pole in this configuration. Similarly, the integrated value for the photodiode dark current shot noise during reset is calculated to be $0.079\mu V_{RMS}$, compared to the approximated value of $0.44\mu V_{RMS}$. The integrated value for the photodiode thermal noise during reset is calculated to be $1.04nV_{RMS}$ and the approximated calculation predicts $5.88nV_{RMS}$. As can be seen in Figure 3.11, the total noise contributed by these sources during the reset phase is insignificant compared to their contribution during the integration phase.

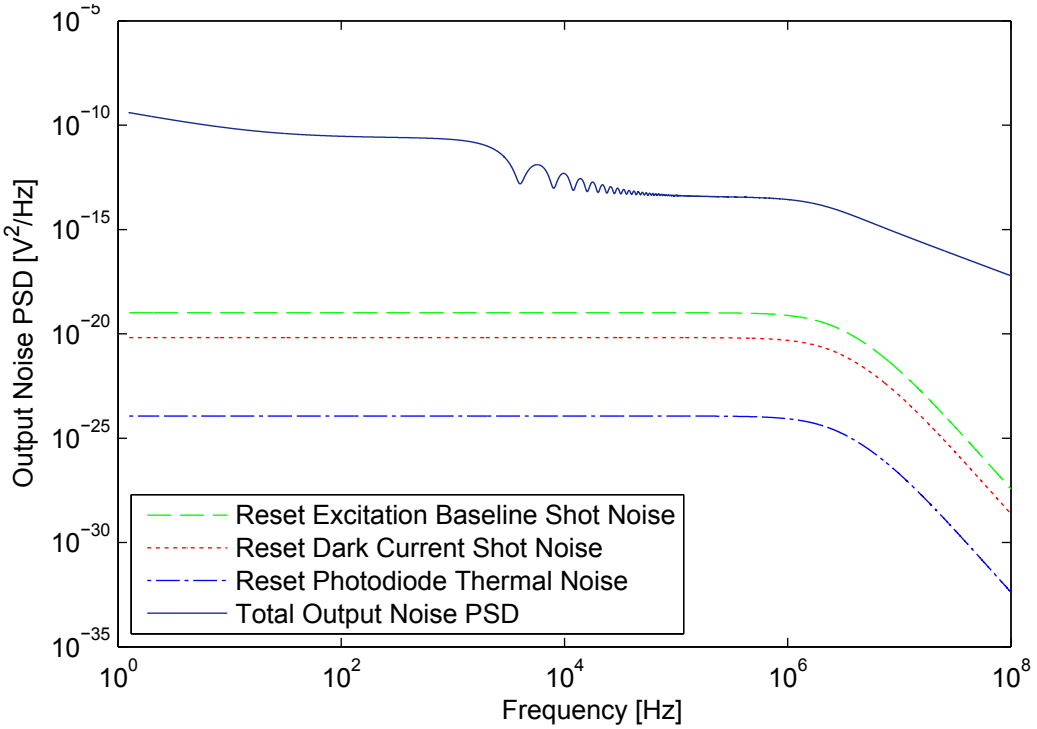


Figure 3.11: The output referred noise PSDs for the baseline shot noise, photodiode thermal noise and dark current shot noise during the reset phase, in comparison to the total noise PSD of the acquisition channel.

Op-amp Noise

Two identical FCC op-amps are used in the signal acquisition channel. The total noise generated by these op-amps is calculated in Appendix A.3 to be $197\mu V_{RMS}$. For the output buffer op-amp, no further shaping of the noise is applied on chip. The CTIA op-amp noise is shaped by Eq. 3.40 during the integrate phase and Eq. 3.39 during the reset phase. The output referred noise voltage PSDs are plotted in Figure 3.12.

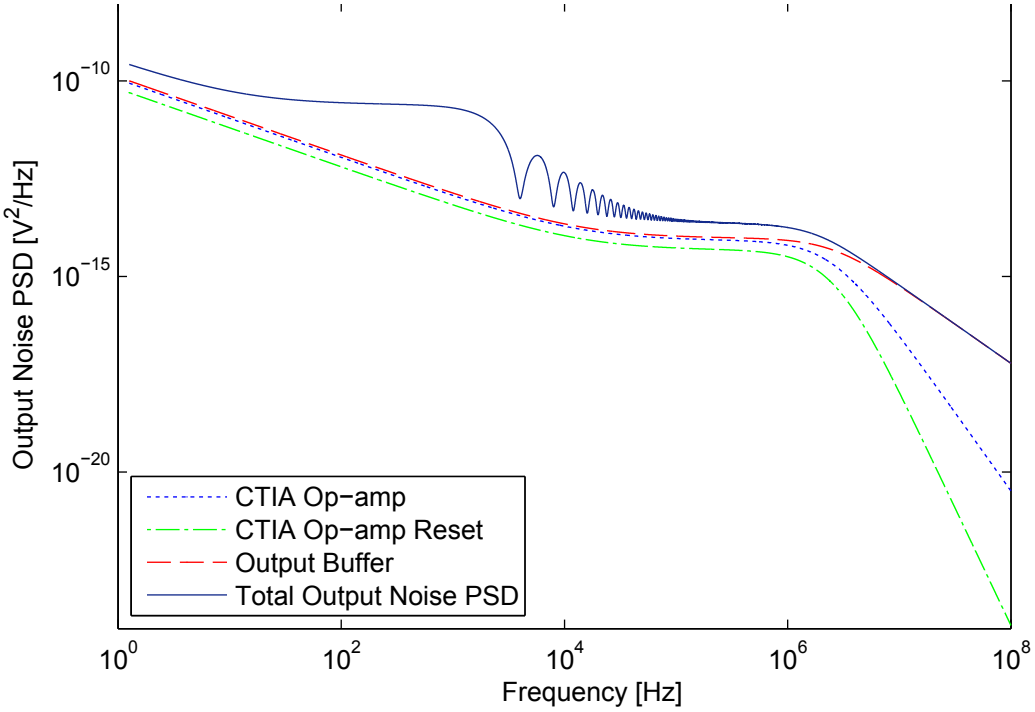


Figure 3.12: The output referred noise PSDs for the output buffer and CTIA op-amp during the integration phase and the reset phase of operation. It can be seen that these three noise PSDs contribute are dominant for low frequencies and high frequencies as their shape conforms closely to that of the total noise PSD.

Examining Eq. 3.40, it can be identified that the majority of the noise shaping comes from the amplification due to the configuration of C_{int} and C_{PD}. Thus the total noise

contributed during the integrate phase can be approximated to:

$$v_{outv_{n1}I}{}^2 = \frac{T_{int}}{T_s} \cdot (1 + \frac{C_{PD}}{C_{int}}) \cdot v_{n1}{}^2 \tag{3.60}$$

where v_{n1} is the input referred noise of the op-amp. Similarly, an examination of Eq. 3.39 shows that the transformations of the noise are effectively unity until a bandwidth beyond the 3dB of the amplifier, allowing the output referred noise to be summarized by:

$$v_{outv_{n1}R}{}^2 = \frac{T_h}{T_s} \cdot v_{n1}{}^2 \tag{3.61}$$

Comparison between the numerically calculated (between 1Hz and 10MHz) integration phase noise from the CTIA op-amp and the approximated calculation provide values of $134\mu V_{RMS}$ and $130\mu V_{RMS}$ respectively. For the CTIA op-amp noise during reset provide an numerically calculated value of $90.4\mu V_{RMS}$ and an approximated value of $98.6\mu V_{RMS}$.

Switch Noise

There are two transmission gates in the acquisition channel that contribute noise. The reset switch for the CTIA has a noise PSD described by Eq. 3.44. The S/H switch has an output referred noise PSD described by Eq. 3.46. When plotted it can easily be seen that these switches contribute negligibly to the total output noise (Figure 3.13). Examining the reset switch noise PSD, it can be seen that if the the $R_{SW}||C_{int}$ pole is dominant, the total noise contributed is effectively time averaged kT/C noise:

$$v_{outi_{SW1}R}{}^2 = \frac{T_h}{T_s}\frac{R_{SW}}{4C_{int}}\overline{i_{SW1}}^2 \tag{3.62}$$

$$= \frac{T_h}{T_s} \cdot \frac{2kT}{3C_{int}} \tag{3.63}$$

Similarly for the S/H switch, if the dominant pole is assumed to be from $R_{SW}||C_h$, the total output noise is:

$$v_{outi_{SW2}I}{}^2 = \frac{T_{int}}{T_s} \cdot \frac{2kT}{3C_h} \tag{3.64}$$

When comparing the numerically integrated results to the approximated equations, the reset switch numerically works out to $5.1\mu V_{RMS}$ compared to the approximated value of $11.7\mu V_{RMS}$. The S/H switch numerically is calculated to be $7.33\mu V_{RMS}$ compared to the approximated value of $114\mu V_{RMS}$. The large difference between the values for the S/H switch is because the assumption that C_h is violated as the unity gain frequency of the output buffer is much less then the S/H pole.

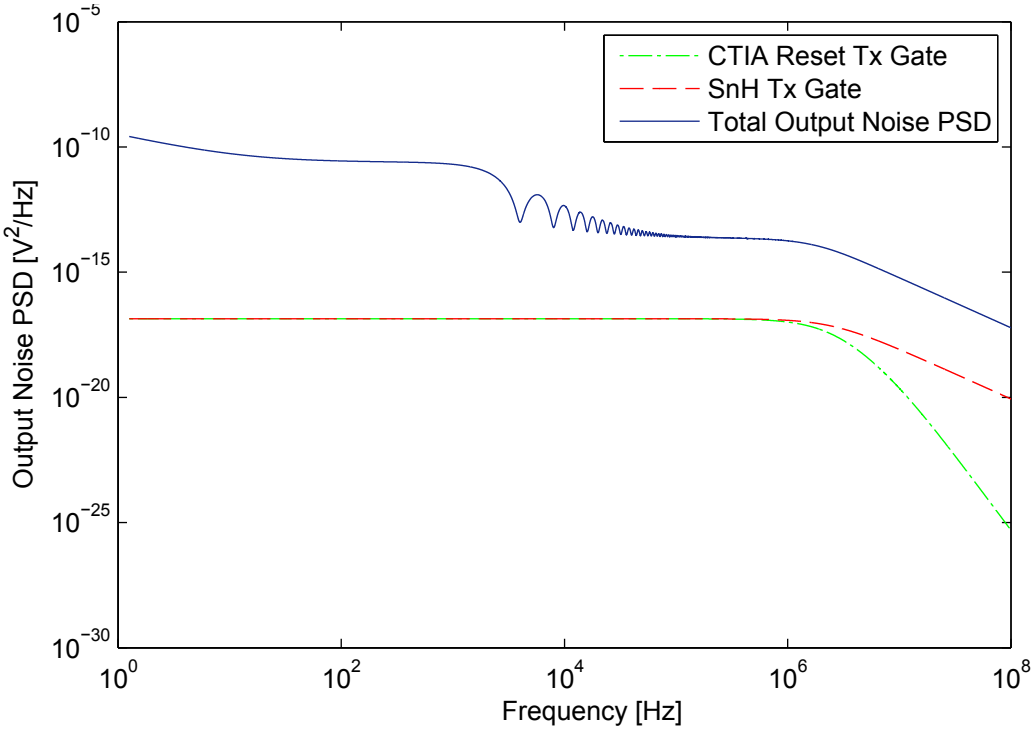


Figure 3.13: The output referred noise PSDs for the reset and S/H switches. Both these noise sources do not contribute significantly to the total output noise PSD profile.

3.3.3 Limit of Detection

The metric by which LOC FD is compared is the LOD. The LOD is determined as the fluorophore concentration at which the fluorescent signal falls below three times the measurement noise floor [62].

Source	Noise Contribution [μV_{RMS}]
Integration Phase Excitation Light Shot Noise	215
Integration Phase Photodiode Dark Current Shot Noise	54.2
Integration Phase Photodiode Thermal Noise	0.72
Reset Phase Excitation Light Shot Noise	30.5
Reset Phase Photodiode Dark Current Shot Noise	0.142
Reset Phase Photodiode Thermal Noise	0.0018
Output Buffer	197
CTIA Op-amp Integration Phase	134
CTIA Op-amp Reset Phase	90.4
Reset Transmission Gate	5.10
Sample and Hold Transmission Gate Noise	7.33
Total Noise	$338\mu V_{RMS}$

Table 3.3: The summation of the noise sources present in the acquisition channel.

The optical signal strength in this case is only that resulting from the fluorescence. The measured excitation signal is constant and can easily be removed. The optical signal strength for the proposed FD device is described by Eq. 3.2. Assuming that the frequency components of I_{PD} are small compared to the integration time, the voltage output signal for this device is described by:

$$V_{sig} = \frac{T_{int}}{C_{int}} \cdot resp \cdot I_{LED} \cdot A_{Ch} \cdot LCE_{Fl} \cdot 10^{-OD_{Fl}} \cdot ln(10) \cdot \varepsilon \cdot d \cdot \phi \cdot c \tag{3.65}$$

The noise in the measurement signal has been derived in the previous section. The noise can be approximated by the following equation:

$${V_n}^2 = {v_{outi_nI}}^2 + {v_{outi_nR}}^2 + {v_{outv_{n1}I}}^2 + {v_{outv_{n1}R}}^2 + {v_{outv_{n2}IR}}^2 + {v_{outi_{SW1}R}}^2 + {v_{outi_{SW2}I}}^2 \tag{3.66}$$

The LOD is defined in terms of SNR, as the point where the fluorophore concentration results in:

$$SNR = 3 = \frac{{V_{sig}}^2}{{V_n}^2} \tag{3.67}$$

Noise Source	Transformation Function
Integration Phase Photodiode and Photon Shot Noise	$S^{int}_{outi_n}(f) = \left\| \frac{T_{int}}{C_{int}} \sum_{p=-\infty}^{\infty} \frac{sinc\left((f-\frac{p}{T_s})\cdot T_{int}\right)}{1+j2\pi(f-\frac{p}{T_s})\cdot R_{SW}C_H} \cdot \frac{A(f_p)}{A(f_p)+1} \right\|^2 \cdot \overline{i_n}^2$
Reset Phase Photodiode and Photon Shot Noise	$S^{rs}_{outi_n}(f) = \frac{T_h}{T_s} \cdot \left\| \sum_{p=-\infty}^{\infty} \frac{1}{1+j2\pi f_p R_{SW}C_h} \cdot \left(\frac{A(f_p)}{A(f_p)+1}\right)^2 \cdot \frac{R_{SW}}{1+j2\pi f_p R_{SW}C_{int}} \right\|^2 \cdot \overline{i_n}^2$
Integration Phase CTIA Op-amp Noise	$S^{int}_{outv_{n1}}(f) = \frac{T_{int}}{T_s} \cdot \left\| \sum_{p=-\infty}^{\infty} \left(\frac{A(f_p)}{A(f_p)+1}\right)^2 \cdot \left(1+\frac{C_{PD}}{C_{int}}\right) \cdot \frac{\overline{v_{n1}(f_p)}}{1+j2\pi f_p R_{SW}C_h} \right\|^2$
Reset Phase CTIA Op-amp Noise	$S^{rs}_{outv_{n1}}(f) = \frac{T_h}{T_s} \cdot \left\| \sum_{p=-\infty}^{\infty} \frac{V_{cap}(f_p)}{1+j2\pi f_p R_{SW}C_h} \left(\frac{A(f_p)}{A(f_p)+1}\right)^2 \right\|^2$ $V_{cap}(f) = \frac{A(f)(1+j2\pi R_{SW}(C_{int}+C_{PD}))}{(A(f)+1)(1+j2\pi C_{int}R_{SW})+j2\pi R_{SW}C_{PD}} \cdot \overline{v_{n1}(f)}$
Reset Phase CTIA Reset Switch Noise	$S^{rs}_{outi_{SW1}}(f) = \frac{T_h}{T_s} \cdot \left\| \sum_{p=-\infty}^{\infty} \frac{V_{cap}(f_p)}{1+j2\pi f_p R_{SW}C_h} \left(\frac{A(f_p)}{A(f_p)+1}\right)^2 \right\|^2$ $V_{cap}(f) = \frac{R_{SW}(A(f)+1)}{j2\pi f C_{PD}R_{SW}+(A(f)+1)(j2\pi f R_{SW}C_{int}+1)} \cdot \overline{i_{SW1}}$
Integration Phase S/H Reset Switch Noise	$S^{int}_{outi_{SW2}}(f) = \frac{T_{int}}{T_s} \cdot \left\| \sum_{p=-\infty}^{\infty} \frac{A(f_p)}{A(f_p)+1} \frac{R_{SW}}{1+j2\pi f_p C_H R_{SW}} \right\|^2 \cdot \overline{i_{SW2}}^2$

Table 3.4: Output Noise PSD Equation Summary. $f_p = f - p/T_s$

Noise Source	Noise PSD Equation
Excitation Light Photon Shot Noise	$\overline{i_n}^2 = 2 \cdot e^- I_{LED} \cdot A_{PD} \cdot LCE_B \cdot 10^{-OD_B} \cdot resp$
Photodiode Dark Current Shot Noise	$\overline{i_n}^2 = 2 \cdot e^- I_{Dark} = 2 \cdot e^- \cdot \rho_{Dark} \cdot A_{PD}$
Photodiode Thermal Noise	$\overline{i_n}^2 = \frac{4 \cdot k \cdot T}{R_{PD}}$
Folded Cascode Op-amp Noise	$\overline{v_{n1}}^2 = \overline{v_{n2}}^2 = \frac{2}{{g_{m_{N2}}}^2} \cdot ({I_{n_{N2}}}^2 + {I_{n_{N10}}}^2 + 2 \cdot {I_{n_{P4}}}^2) \cdot 1A(f)^2$
	$\overline{I_n}^2 = \frac{K_f \cdot {I_d}^{AF}}{C_{ox} \cdot w \cdot l} \cdot \frac{1}{f} + \frac{8}{3} \cdot k \cdot T \cdot (g_m + g_{ds} + g_{mb})$
Transmission Gate Switch Noise	$\overline{i_{SW}}^2 = \frac{8}{3} \cdot k \cdot T \cdot (g_m + g_{ds} + g_{mb})$

Table 3.5: Noise Input Equations

which can then be manipulated into:

$$c_{LOD} = \frac{\sqrt{3} \cdot V_n \cdot C_{int}}{T_{int} \cdot resp \cdot I_{LED} \cdot A_{Ch} \cdot LCE_{Fl} \cdot 10^{-OD_{Fl}} \cdot ln(10) \cdot \varepsilon \cdot d \cdot \phi} \tag{3.68}$$

In this form a sensitivity analysis can be performed to identify parameters which can be optimized to improve the LOD. Some interesting parameters to examine are: A_{PD}, T_{int}, C_{int} and v_{n1+n2}. When the photodiode area is increased, a minimum is seen where the increased light collection efficiency is eventually over come by the increased baseline light collected resulting in a larger shot noise component (Figure 3.14a). This result proposes that there is an optimal size for the photodiode for LOC FD.

By decreasing the op-amp noise by a factor of 10, it the op-amp no longer contributes meaningfully to the total noise and no further advantage is received (Figure 3.14b). Similarly for the value of C_{int}, by decreasing its value an increase in signal gain is achieved however for values much below 10pF, the dominant source of noise becomes the op-amp

(Figure 3.14c). The integration period is the most interesting parameter as it ties into both the signal gain and the noise gain. By increasing the integration period, the gain of the signal increases, however the gain of the noise increases. As the noise scales with the square of the integration period, the SNR is improved despite the increased noise. The slight correction in the slope of Figure 3.14d is produced by the op-amp noise being dominant to the excitation baseline shot noise being dominant. The challenge with increasing T_{int} is that, in order to avoid saturation a larger value of C_{int} is required, which comes with increased associated noise.

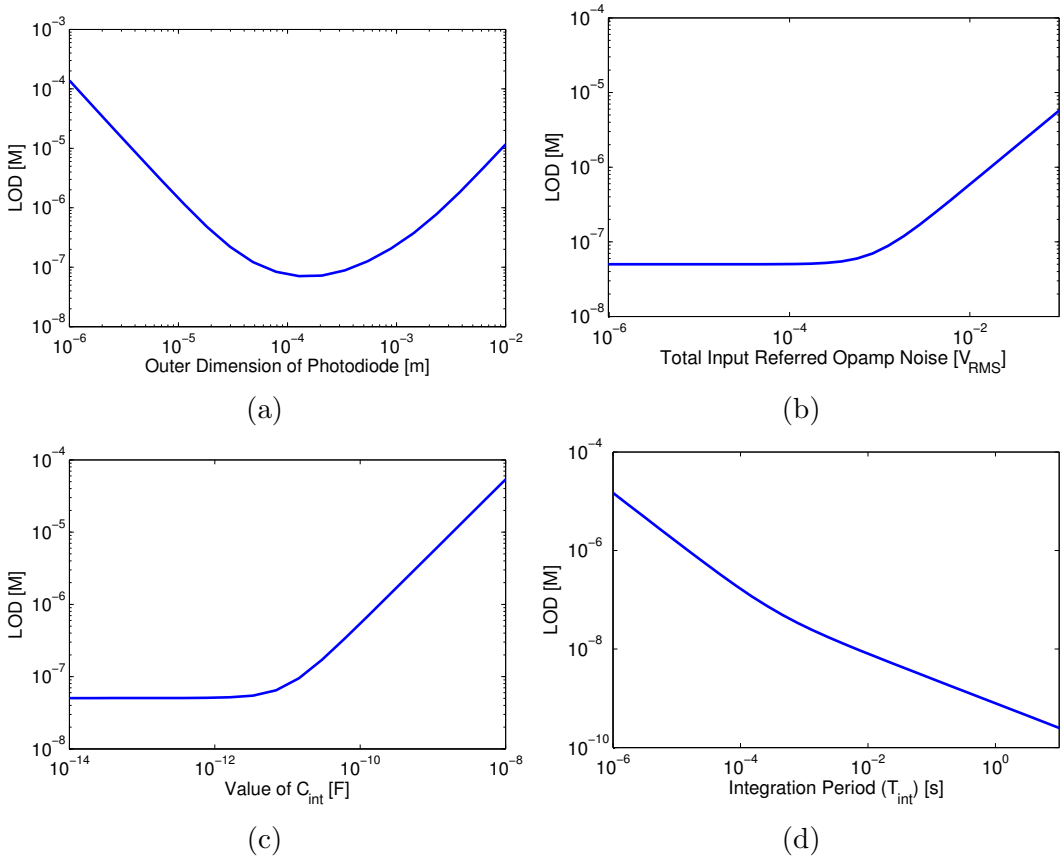


Figure 3.14: Sweeps of individual variables and the effect on the LOD

Chapter 4

Circuit Simulation Results

To validate the equations derived in Chapter 3 the acquisition channel circuits are simulated using the AMSP35 v4.00 kit from CMC. The simulations are done using SpectreRF from Cadence. The following sections simulate the acquisition channel to observe: the integrator transfer function, the interference models, and the predicted output noise PSD.

4.1 Simulations of Acquisition Channel

The following simulations of the CTIA, S/H and output buffer demonstrate good agreement between the predicted frequency domain output and the analysis results derived in Chapter 3. The simulated time-domain output signals are also in good agreement with the expected (Figure 3.2b) outputs, as demonstrated in Figure 4.1.

4.1.1 Behavioural Simulations

The equations derived in Chapter 3 are formed around idealized approximations of switches and op-amp functions. To verify that these equations are correct, an idealized implementation of the acquisition channel is simulated. This allows for validation of the models

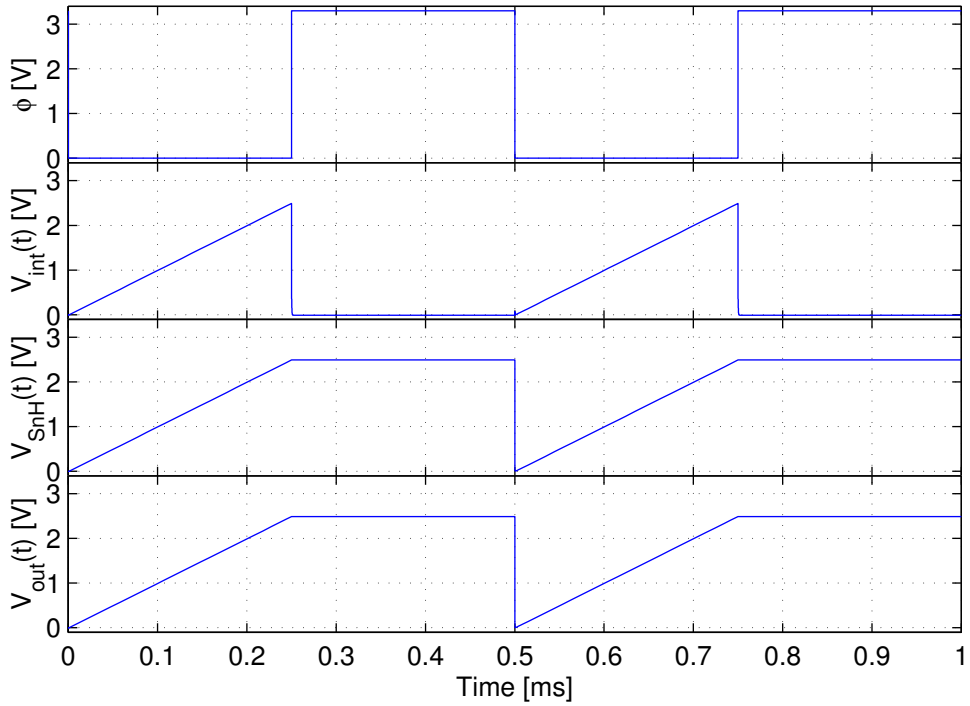


Figure 4.1: Acquisition channel transient voltage profiles. A DC current of 100nA was applied to the anode of the diode to model the photocurrent.

without interference from higher order effects. The simplified circuit is implemented using ideal switches with infinite off resistance and on resistance of R_{SW} of $1.76k\Omega$.

CTIA

As derived in section 3.2.2, the CTIA is expected to follow the transimpedance described by Eq. 3.7. By running a transient simulation with a 100nA sine-wave applied across the photodiode, the magnitude response shown in Figure 4.2 was measured. All circuit parameters were set as described in Table 3.2. A good agreement between the calculated and simulated results is observed. A slight low frequency offset is observed, however this is a simulation artefact resulting from the initial charging of the capacitors[1]. Nulls are

[1]This artefact is because of the switched nature of the circuit, the DC analysis to find the simulator starting points does not calculate the correct starting values.

observed at internals of $1/T_{int}$ as predicted.

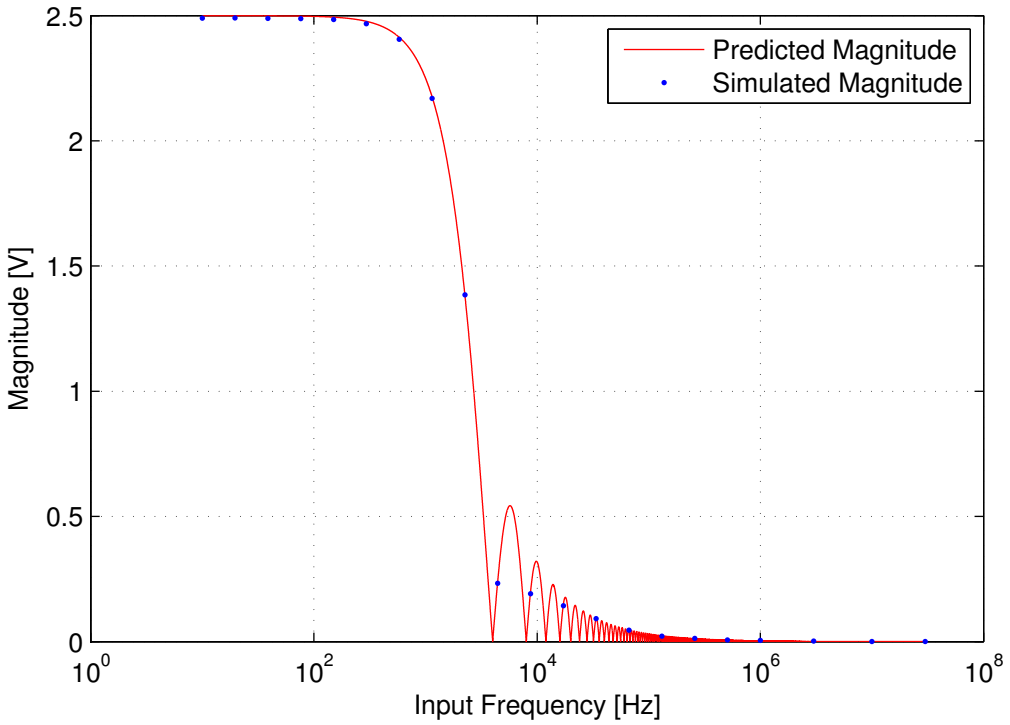


Figure 4.2: Comparison between simulation results and values predicted by Eq. 3.7.

Sample and Hold

In Section 3.2.2 the magnitude function from the photodiode input current to the S/H is described by Eq. 3.10. To validate this equation, a sine-wave current is applied across the photodiode and the output voltage magnitude is measured. The FFT of the output values sampled during the hold phase is calculated in MATLAB to find the magnitude and output frequency. The input frequencies were selected to be prime multiples of the bin frequency of the simulation to ensure sharp FFT spectra and accurate amplitudes.

The output frequency is different from the input frequency as a result of the aliasing introduced by the sampling. The output frequencies shown in Figure 4.3 match that

predicted by Eq. 3.19. The magnitude of the response at the output of the S/H also matches that predicted by the Eq. 3.21 when high op-amp gain is assumed.

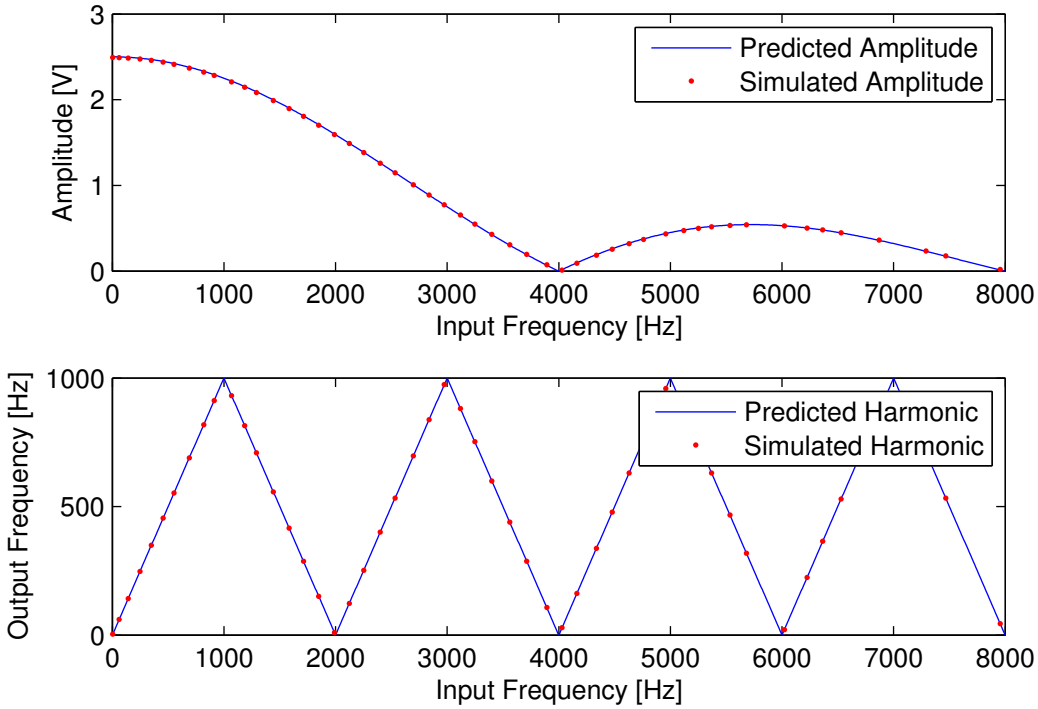


Figure 4.3: Comparison between calculated and simulated S/H output magnitudes and frequencies as a function of the photodiode current input frequency.

Output Buffer

As the output buffer is the final stage of signal propagation, this simulation demonstrates the complete propagation from photodiode current input to measured output. This was previously described in Section 3.2.3 by Eq. 3.24. To validate this equation a similar simulation to that of the S/H is performed. As the unity gain frequency of the op-amp is up around $1MHz$, the addition of the op-amp does not dramatically influence the performance of the channel and thus the results look nearly identical to that of the S/H.

4.1.2 Transistor Level Circuit Simulations

To further validate the mathematical model derived for the signal acquisition channel, transistor level and extracted simulations of the complete circuit are performed. The transistor level simulations differ from the behavioural simulations in the non-ideal op-amp, the pass transistor gate switches and physical diode characteristics. The extracted simulations are performed on the calibre layout extracted equivalent circuit. This simulation should provide the results closest to the physical implementation.

The FCC op-amp used for both the CTIA and output buffer is also simulated. The FCC gain was simulated to be $A_V = 2511V/V$ with the corner frequency at $f_{3dB} = 100kHz$, placing $R_{out} = 162M\Omega$ and $g_m = 19.5\mu S$. The complete results are in Appendix A.

The behavioural acquisition channel model simulations demonstrated that the transfer functions derived in Section 3 provide a valid mathematical representation of the circuit. The transistor level simulations will not match as closely as the ideal circuit models as these simulations take into account the FCC op-amp characteristics as well as charge injection, off resistance of the pass transistors and various other circuit effects. To allow proper operation of the circuit, an offset voltage of 0.7V needs to be applied to the non-inverting terminal of the FCC op-amp. This is due to the NMOS input transistors. Additionally, photodiodes can only drive photo-current from the anode to the cathode, thus a DC bias current must be applied in addition to any sine-waves. For these simulations a 50nA DC current with a 50nA sine component will be applied to the anode of the photodiode. Running the signal acquisition channel under this modified context, the circuit transfer function demonstrates good agreement with the simplified simulations, as demonstrated in Figure 4.4.

The introduction of the FCC op-amp introduces harmonic distortion as the output of the integrator approaches the power rails. It can be seen in Figure 4.4 that the op-amp does not drive the output to 3.2V as expected by the behavioural simulation but instead distorts the sine-wave to a maximum value of roughly 2.7Vs. This is due to the PMOS cascode transistor entering the triode region when the output voltage approaches the supply rail. When examining the frequency domain response of the output this distortion can be seen

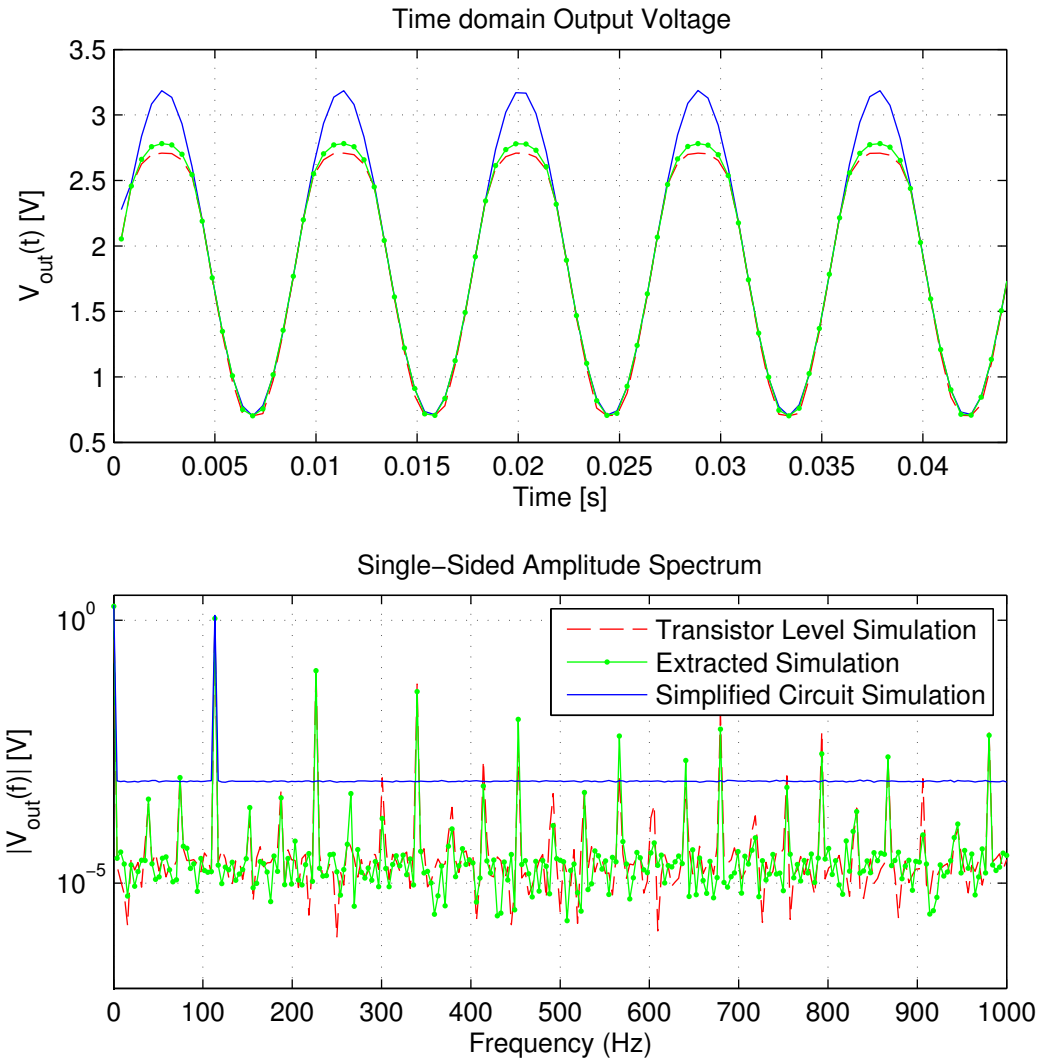


Figure 4.4: Comparison of the sampled simplified circuit simulation results to the transistor level and extracted simulations. A 50nA, 113Hz sine-wave with a 50nA DC offset current was injected onto the photodiode for all three simulations. An integration time of $250\mu s$ was used with a total period of $500\mu s$.

as extra tones at integer multiples of the input frequency. Higher-order harmonics can be seen to be aliased down into the baseband as well.

There was good agreement between the transistor level simulation and the extracted

simulations. The extracted simulation demonstrated slightly less harmonic distortion as the FCC op-amp didn't clip the output until 2.8V however the harmonic distortion is still a challenge which should be addressed in future iterations of the chip as this restricted operating range of the amplifier reduces the total output range of the CTIA to only 2.1V.

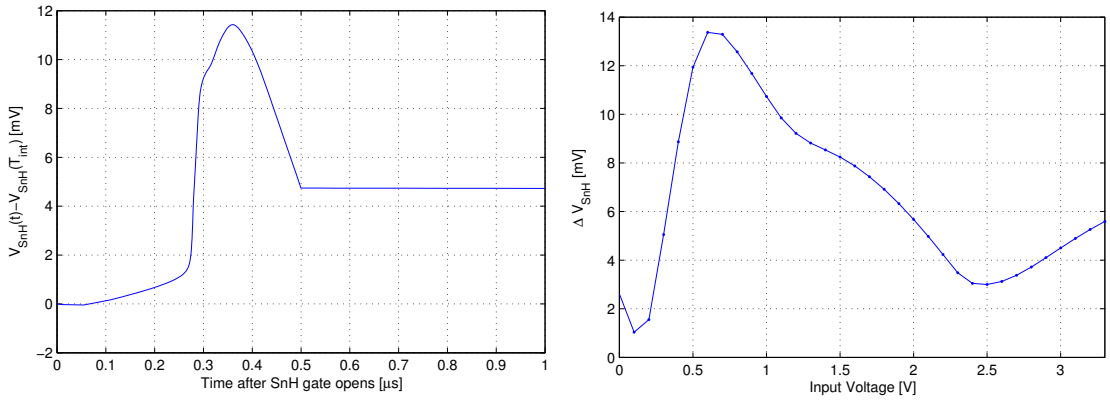
4.2 Acquisition Channel Interference

There are two sources of signal interference which are discussed in Section 3.2.4: transmission gate charge injection, and interference from the signal while the CTIA is in reset. The following subsections will simulate these interference effects to validate their predicted impact.

4.2.1 Charge Injection

Despite the design of the transmission gates to be matched PMOS and NMOS to allow for charge cancellation, charge injection still takes place. The idealized model which suggests that dummy transistors will sink all charge expelled by the transmission gate, does not account for many of the higher order effects which are included in SpectreRF simulations. However, the charge injection is a highly repeatable process and thus can be accounted for during operation of the acquisition channel.

Of the two transmission gates used in this acquisition channel, only the S/H gate needs to be accounted for. The gate located across the CTIA capacitor will inject charge equally onto both sides of the gate. As equal charge is placed on either side of the capacitor, no voltage is introduced. The S/H however injects charge on to C_h which is then buffered off chip. Figure 4.5a demonstrates the addition of charge after the signal to close the transmission gate is sent at $t = T_{int}$. The charge injection peaks at 11.4mV, however this is mitigated down to 4.74mV as the dummy transistors begin to sink the excess charge. This injection value is for $V_{int} = 1.95V$.



(a) (b)

Figure 4.5: (a) Transient charge injection on $V_{S/H}$ for $V_{int} = 1.95V$. (b) Total charge injection onto output of S/H circuit in isolation, as a function of input voltage.

4.2.2 Signal Interference

As was described in Section 3.2.4, when in reset, the CTIA behaves like a conventional TIA amplifier. As a result, when the CTIA comes out of reset, charge is sampled onto the integrating capacitor. This charge is then propagated through the acquisition channel to the output resulting in interference.

The magnitude of the voltage placed across the integrating capacitor is described by:

$$\frac{V_{Cap}(f)}{I_{PD}(f)} = \frac{Z_{SW} \cdot Z_{PD} \cdot (g_m \cdot Z_o \cdot +1)}{Z_o \cdot Z_{PD} \cdot g_m + Z_o + Z_{PD} + Z_{SW}} \tag{4.1}$$

where $Z_{SW} = R_{SW}||1/(sC_{int})$, $Z_{PD} = R_{PD}||1/(sC_{PD}) \approx 1/(sC_{PD})$, $Z_o = R_o||1/(sC_o)$ and g_m is the transconductance of the amplifier. At DC this equation reduces to:

$$\frac{V_{Cap}(f=0)}{I_{PD}(f=0)} = R_{SW} \tag{4.2}$$

By running a transistor level DC simulation, the value of R_{SW} was measured to be $2.165k\Omega$. To evaluate the entire transimpedance function a transistor level AC simulation was per-

formed (Figure 4.6). The equation accurately predicts the low frequency gain and first pole location. The simulation however, has a much steeper roll off past the cut off frequency. This is possibly due to internal poles in the FCC op-amp which are not modelled in the single pole op-amp equivalent circuit used to derive the transimpedance equation.

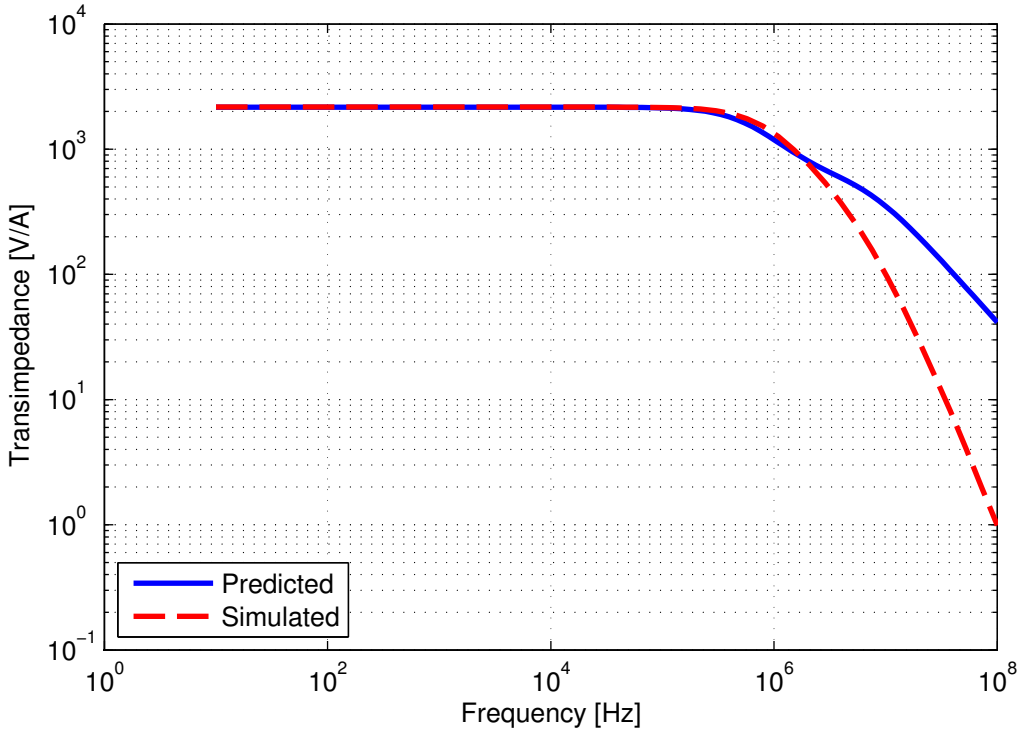


Figure 4.6: Comparison between hand calculated and simulated transimpedance values for the photodiode current while the CTIA is in reset.

The transformation from a voltage across C_{int} to the output is described in Section 3.2.4) by Eq. 3.30. To measure this from a transient simulation is difficult as this is a secondary effect resulting from the same source as the input signal. The output should however be effectively described by the sum of Eq. 3.24 and Eq. 3.30, an approximated form of this relationship is:

$$V_{out}(f) = (\frac{T_{int}}{C_{int}} sinc(T_{int}f) + R_{SW}||C_{int})I_{PD}(f) \tag{4.3}$$

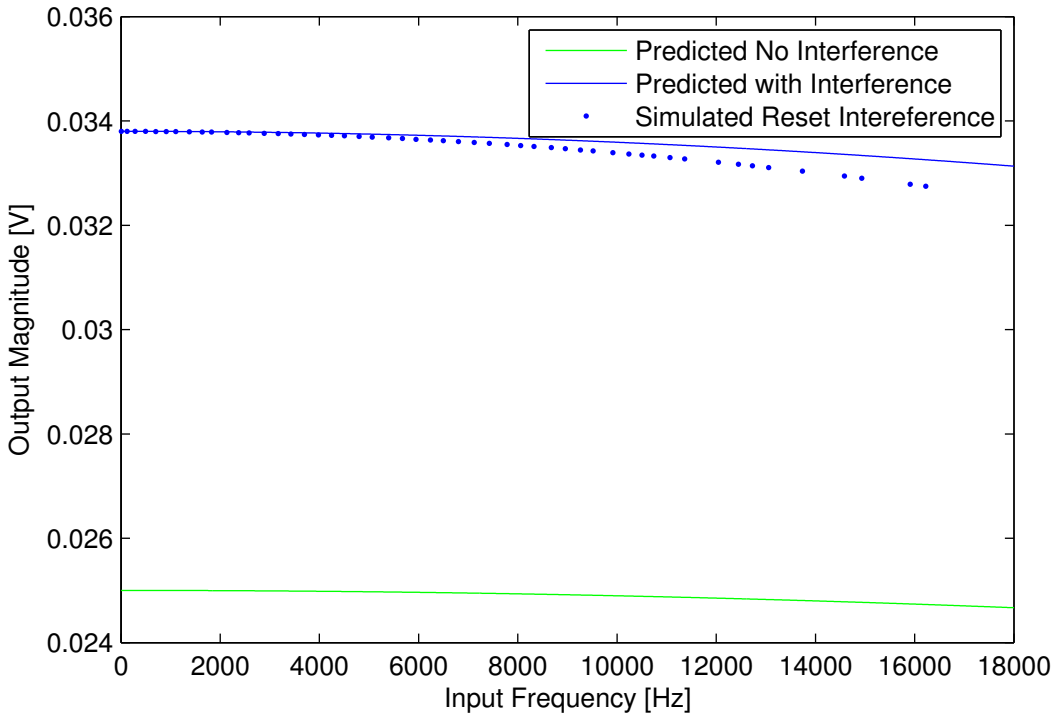


Figure 4.7: Comparison of integrator output for different current input frequencies, with and without accounting for the reset interference. It can be seen that the reset interference does contribute to the output, however the derived model does not completely explain the higher frequency effects taking place.

By making the integration time to be extremely small, the contribution from Eq. 3.24 will be small. As the interference is independent of timing parameters, the relative contribution should increase. To make the influence more obvious, the reset switch resistance is increased to $176k\Omega$. This is simulated using the behavioural model to minimize the effects of other higher order effects. Figure 4.7 plots the simulated output described by Eq. 4.3; it can be seen that there is good agreement is achieved for low frequency values, however the equation begins to diverge as frequency increases. This is due to two poles not properly accounted for in this equation: the photodiode capacitance and the op-amp transfer function pole. These poles are also less significant when using the measured R_{SW} value.

4.3 Noise Transfer Function Simulations

The noise generated by various noise sources in the circuit have unique shaping functions for how they propagate through the acquisition channel to the output. These functions are described in Section 3.2.5. Analysis of these equations demonstrated that only a few of the noise sources contribute significantly to the total output noise. To validate this assertion, each of the noise shaping functions are simulated using sinusoidal sources and the magnitude at the output is measured.

These simulations are done using transient simulations due to the switched nature of the circuit. The behavioural model of the acquisition channel circuit is used to limit the computational load of these simulations.

4.3.1 Photodiode

The photodiode current noise follows the same transfer function as the input signal. Thus noise at this point will experience the full gain of the acquisition channel. Three sources of noise are introduced at the photodiode: Excitation light shot noise, Dark current shot noise and photodiode thermal noise. Upon sampling, these noise sources will have the noise PSD described by Eq. 3.34. The magnitude response of this equation is previously verified in Section 4.1.1.

4.3.2 CTIA Op-amp

The FCC op-amp has a input referred noise PSD described in Appendix A.3. This noise PSD will be shaped by the transfer function derived in Section 3.2.5. To validate this transfer function a $100\mu V$ sinusoidal voltage input is applied to the non-inverting terminal of the CTIA op-amp[2]. In Figure 4.8, the sampled output is compared against the predicted sampled output, which is described by Eq. 3.41.

[2]The amplitude of this tone has been selected arbitrarily as this serves to validate the transfer functions not measure the total noise.

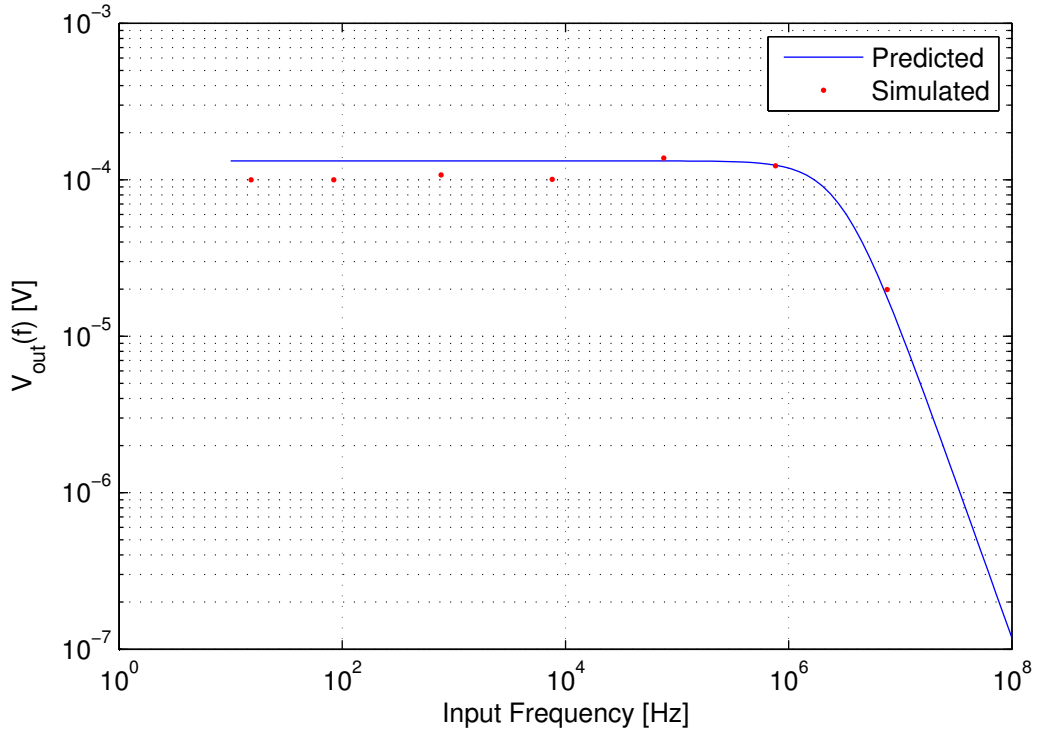


Figure 4.8: The amplitude of various input tones (Red dots) correspond to the amplitude of that predicted by the transfer function.

Good agreement is seen between the predicted and simulated results. Some slight deviation from the equation is observed in the lower frequencies; however, the corner frequency corresponds are predicted.

4.3.3 CTIA Reset Transmission Gate

The thermal noise generated by the CTIA reset transmission gate does not introduce noise during the integration phase as the values of g_m and g_{ds} are too small to be significant. During the reset phase however, the thermal noise PSD results in a reset noise (V_{Cap}) being placed across C_{int} which is sampled when the CTIA returns to the integrate phase of operation. The value of V_{Cap} is determined largely by the RC filter of the switch impedance

and the value of C_{int}, which is mathematically described by Eq. 3.43.

When the CTIA returns to the integrate phase, the noise across C_{int} is effectively sampled and held. The held voltage is then propagated across the sample and hold register and onto the output during the integration phase. The output signal is finally sampled resulting in an output voltage magnitude described by Eq. 3.44.

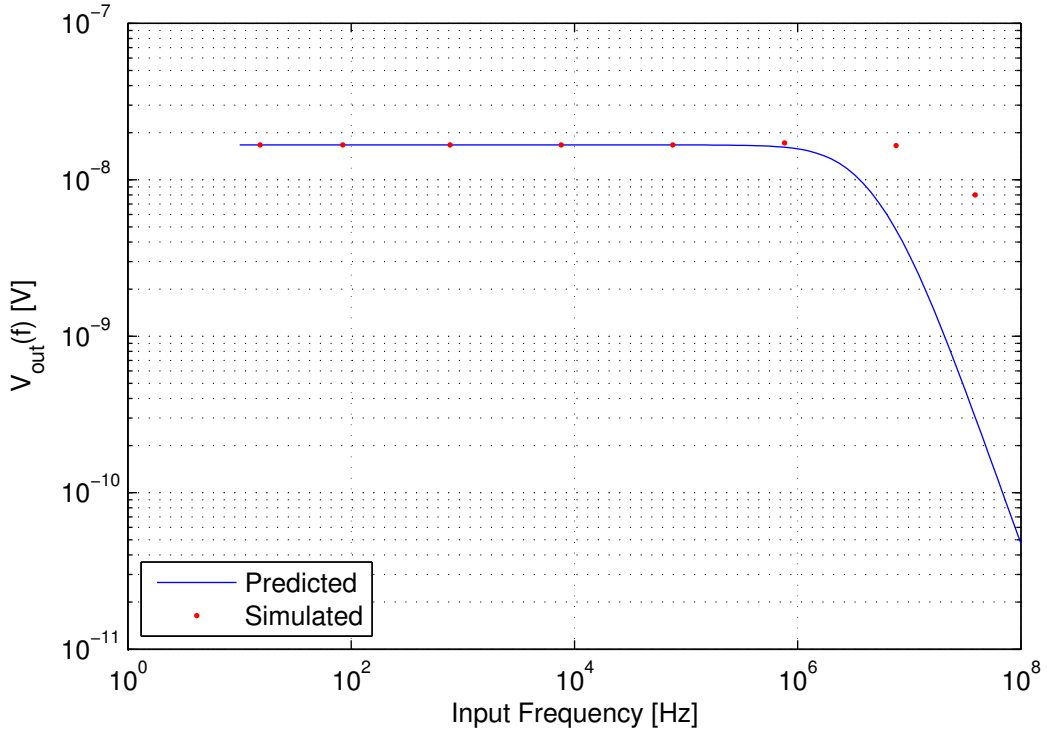


Figure 4.9: The amplitude of various input tones (Red dots) correspond to the amplitude of that predicted by the transfer function. The spectra for the highest frequency simulated tone was not able to be plotted due to simulator related issues, however the magnitude of the sinusoid was measured from the transient V_{out} signal by hand.

Transient simulations of the behavioural circuit were performed to validate the predicted transimpedance function. These simulations were performed by applying an current sine-wave of different frequencies an 10pA amplitude across the reset switch resistor with ideal switches located on either side. The circuit was operated with a $250\mu s$ reset and integration period for a total period of $500\mu s$. The Fourier transform was performed on the

data sampled from the output buffer during the reset phase. These simulations demonstrated that the low frequency amplitudes and locations predicted by Eq. 3.44 match closely with the output spectra. Figure 4.9 shows that the first pole is located slightly lower than in simulation. To perform accurate simulations at such high frequencies however presents extremely large computational requirements. Despite error in the pole location, the magnitude of the transimpedance demonstrate that the noise contributed during the reset phase is not significant compared to the noise contributed during the integration phase.

4.3.4 Sample and Hold Transmission Gate

Behaviourally, the sample and hold transmission gate behaves as a resistor during the integration phase and as a open circuit during the reset phase. This was mathematically described in Section 3.2.5 by Eq. 3.46.

This equation represents the transimpedance of the equivalent current noise of the transmission gate to the output. To avoid running extremely large simulations, the transimpedance function can be validated against a sinusoidal current input in parallel with the transmission gate. Figure 4.10 plots the sampled output of the buffer against the input frequency, demonstrating that Eq. 3.46 is in good agreement with the behavioural simulations.

4.3.5 Output Buffer

The output buffer consists of the FCC op-amp in a unity feedback configuration. This means that the noise contributed by this op-amp will be the equivalent of the input referred noise of the op-amp transformed by the unity gain function. Mathematically this is described by:

$$S_{Buff}(f) = \left\| \frac{A(f)}{A(f)+1} \right\|^2 \cdot S_{Input}(f) \tag{4.4}$$

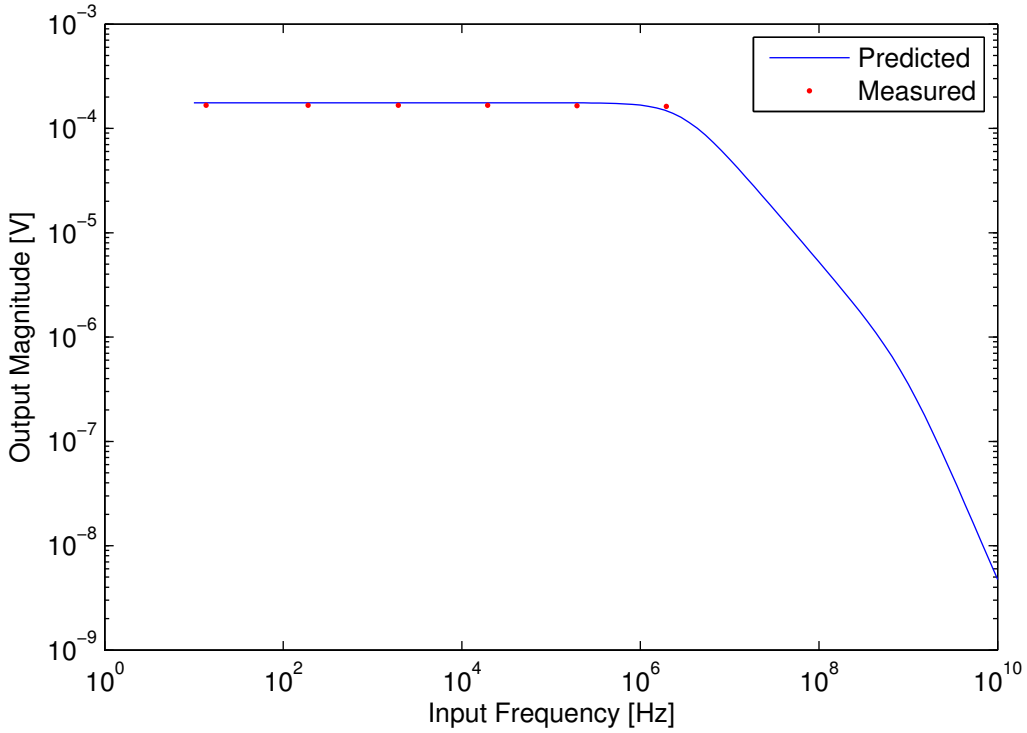


Figure 4.10: Comparison between predicted and simulated noise transfer function for S/H transmission gate. This plot assumes a 100nA input sine-wave current.

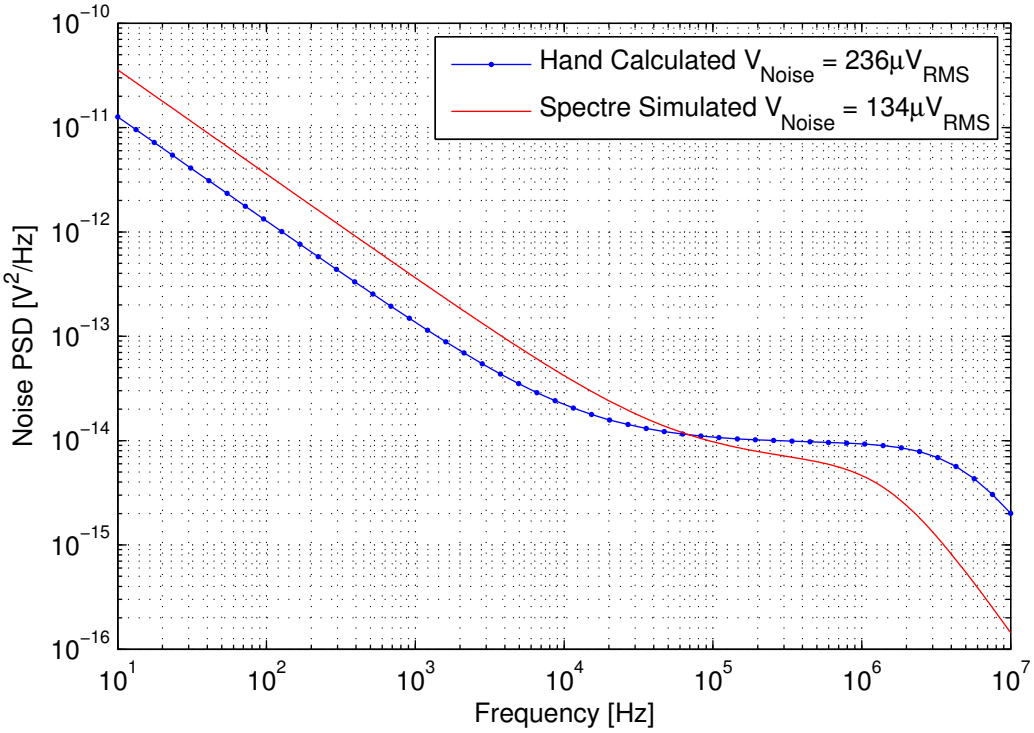


Figure 4.11: Comparison between simulated and calculated output noise PSD of FCC output buffer in unity feedback.

Where $A(f)$ is the frequency response of the op-amp and $S_{Input}(f)$ is the input referred noise PSD derived in Appendix A.3. Figure 4.11 compares the transistor level simulation of the FCC op-amp output noise PSD in unity feedback against the hand calculated values. Some discrepancies are seen between the corner frequencies of the two. This is explained by the internal node capacitance which is included in the spectre simulations but omitted in the hand calculations. Additionally the 1/f noise is somewhat higher in simulation than predicted by the calculations. This is because the actual equations used by SpectreRF for the 1/f noise are not provided but the AMS process documentation does specify that a non-linear fitted equation is used.

4.4 Transient Noise Simulations

The total noise of the measurement is the only noise value that matters when the LOD of the device is determined. Section 3.3.2 determines that of the various noise sources, only four contribute significantly to the total output noise: The integration phase excitation light shot noise; the CTIA op-amp integration phase noise; the CTIA op-amp reset phase noise; and the output buffer noise. The total noise contributed by the output buffer was determined in Section 4.3.5. The transfer functions for the different noise sources were validated in the previous section, however the total noise contribution is not determined.

This section will perform transient noise simulations on the behavioural model of the signal acquisition channel. The noise generated by the CTIA op-amp and the shot noise generated by the excitation photo-current are simulated. These results are compared against the equations derived in Section 3.3.2.

4.4.1 CTIA Op-amp Transient Noise Simulation

The total output noise generated by the CTIA op-amp is comprised of two components: that generated during the reset phase, and that generated during the integrate phase. As these generate from a common source, the total output noise power will be described by the sum of the powers of these signals:

$$v_{outv_{n1}IR}{}^2 = v_{outv_{n1}R}{}^2 + v_{outv_{n1}I}{}^2 \tag{4.5}$$

where $v_{outv_{n1}I}$ and $v_{outv_{n1}R}$ are described by Eq. 3.60 and Eq. 3.61 respectively.

To simplify the simulation, a white thermal noise was assumed for the input referred noise PSD. A value of $1.21 \cdot 10^{-}8V^2/Hz$ was assumed for the PSD amplitude. This value was selected as it matched the thermal noise floor from the op-amp noise PSD simulations, however it was realized later that this was a value for output referred noise instead of input referred. This increases the total noise measured but the trend predicted by Eq. 4.5

should match. The 3dB bandwidth of the op-amp is estimated to be 1MHz. This provides a rough total noise of the op-amp to be:

$$v_{n1}{}^2 = 1.21 \cdot 10^-8 \frac{V^2}{Hz} \cdot 1MHz = 0.0121V^2 \tag{4.6}$$

The first simulation was run at $F_{MAX} = 10MHz$ as this is 10 times the maximum frequency of the op-amp. $F_{MIN} = 3.9Hz$ as the this was one over the simulation period. The simulation period was 256ms. $T_{int} = 250\mu s$ and $T_h = 250\mu s$ for a $T_s = 500\mu s$. These parameters give a predicted total noise of $128.8mV_{RMS}$. The simulated noise from the op-amp for these parameters was measured to be $122mV_{RMS}$. To ensure that the simulation was run for sufficient duration, the standard deviation of the output was plotted against the number of samples in Figure 4.12. It can be seen that the noise converges to within approximately 3% after 100 samples. Thus the simulation time will be reduced to 50ms.

The total noise generated for different values of T_{int} is simulated, with all other parameters are held constant ($T_s = 500\mu s$ with T_h adjusted). Figure 4.13a plots the predicted and measured value of the noise. A divergence from the predicted trend is thought to be a result of correlation between noise contributions during reset and integrate. In Eq. 4.5 the two noise sources are assumed to be uncorrelated; however, examining the time domain signal this can be thought of as a bad approximation. During reset, the output will be described by:

$$V_{out}(t) = v_{n1}(t) \tag{4.7}$$

When the circuit returns to integrate mode at some time t_o, Eq. 4.7 is sampled onto the capacitor C_{int} and added to the now amplified op-amp noise, as described by:

$$V_{out}(t) = v_{n1}(t_o) + (1 + \frac{C_{pd}}{C_{int}}) \cdot v_{n1}(t) \tag{4.8}$$

As a result, the noise sum of the two terms will be described by the autocorrelation of $v_{n1}(t)$. When the model is modified to include a correlation coefficient, a 50% correlation provides a good fit to the measured output noise, as shown in Figure 4.13a.

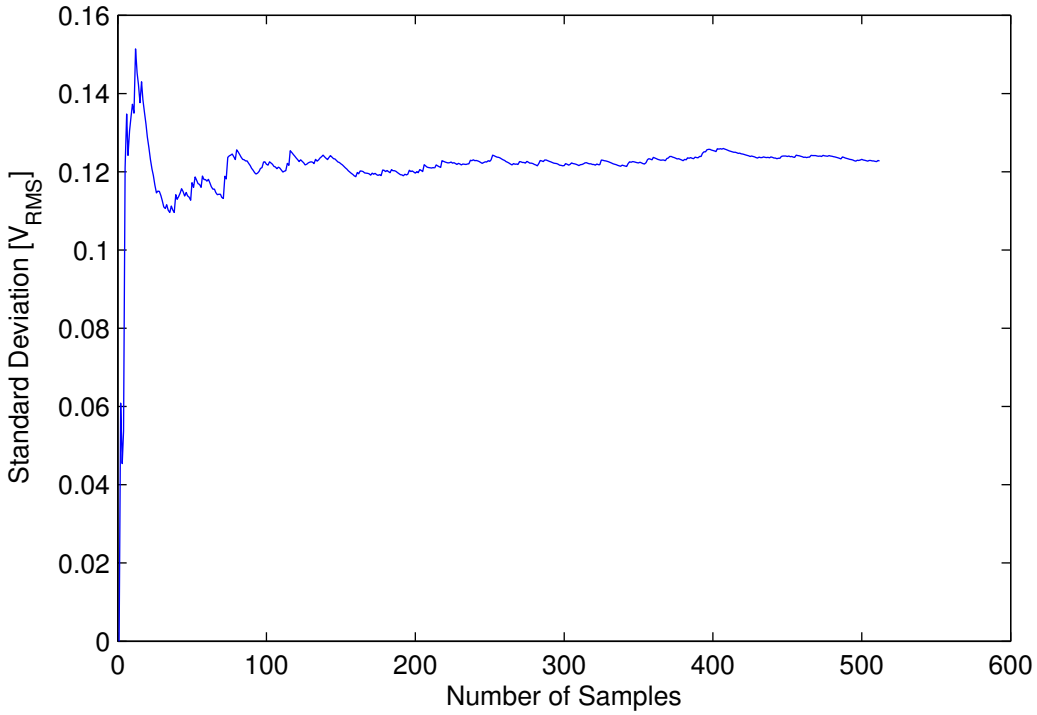
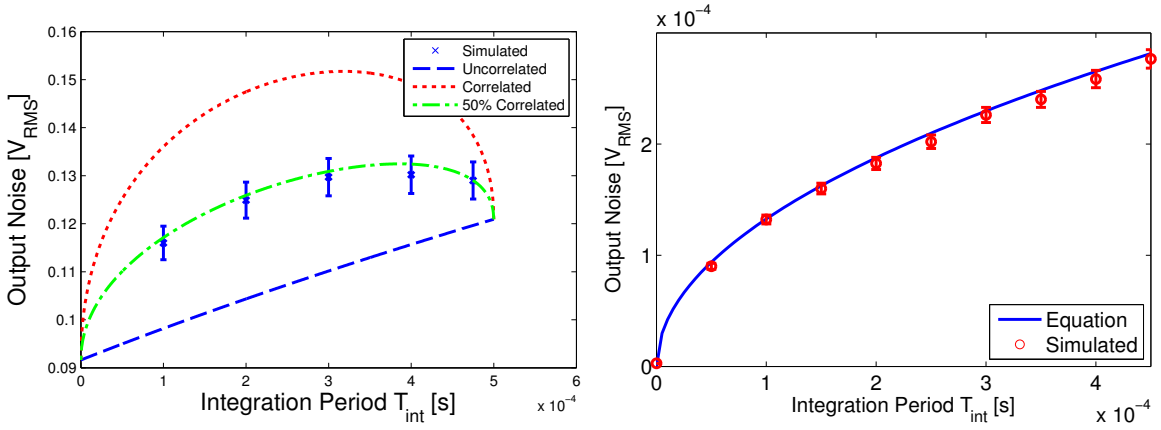


Figure 4.12: The standard deviation of the sampled output as a function of the number of samples taken. It can be seen that 100 samples is sufficient to provide an accurate value for the standard deviation.

4.4.2 Photodiode Transient Noise Simulation

The total output noise of the acquisition channel that is generated by the photodiode is described by Eq. 3.56. It was previously shown that the noise contributed during the reset phase is negligible in comparison. To validate the noise predicted by Eq. 3.56, a transient noise simulation is run. The photodiode noise is expected to be dominated by the excitation light shot noise, thus the input noise will be described by the shot noise equation. For a baseline current of 110nA, the input noise PSD is $\overline{i_n}^2 = 3.52 \cdot 10^{-26} A^2/Hz$. As was demonstrated by Figure 4.12 the measured noise is accurate after 100 samples, for a sampling period of 500ms the simulation needs to be run for 50ms. The transient noise simulation was run with a $F_{MAX} = 10MHz$ and $F_{MIN} = 10Hz$. The simulations are



(a) (b)

Figure 4.13: (a) Comparison between the calculated and simulated output noise generated by the CTIA op-amp. (b) Comparison between the calculated and simulated output noise generated by noise sources located across the photodiode.

run for integration periods from $0\mu s$ to $450\mu s$ as shown in Figure 4.13b. The error in the simulated output noise is taken to be 3%, as was determined in Figure 4.12.

Figure 4.13b demonstrates excellent agreement to the values predicted by Eq. 3.56. This validates the derivation of the total output referred noise resulting from the photodiode input noise.

Chapter 5

Experimental Results

This chapter describes the experimental results measured from the CMOS and a discrete circuit implementation of the acquisition channel described and simulated in the previous chapters. This chapter: outlines how each circuit was implemented, explains the test setup for the measurements, and tries to validate the acquisition channel transfer functions and noise analysis.

The CMOS and discrete implementations of the acquisition were initially developed to allow for a comparison in the performance. Initial testing demonstrated several implementation problems with the operation of CMOS of the circuit. This forces most of the analysis to be on the discrete implementation, for which modifications to the noise equations are needed. An effort is made to identify the reasons that the CMOS doesn't operate as expected however no exact cause has been identified.

5.1 ASIC Integrator

This section provides the measured results from the ASIC implementation of the acquisition channel. The implementated design is provided along with the test setup. Measurements of the FCC op-amp is provided along with the transient output and measurement of the fre-

quency dependent transimpedance function. Many of the issues identified in the operation of this circuit are discussed here.

5.1.1 Design

The physical implementation of the acquisition channel requires five interface signals: V_{DD}, V_{SS}, V_{Off}, V_{Out} and $Reset$. An extra signal was added connected directly to a 200μm x 200μm top metal layer pad, which is intended for running an OLED in the future. The acquisition channel circuit was laid out in Cadence using the Virtuoso tool suite and a DRC was run using Calibre. The layout was implemented using the AMSP35 C35 process standard cells. As the circuit is relatively small, it was implemented in the South-West corner of OR1. It was implemented on a separate ground plane and power rails then the other circuits on the chip to prevent any catastrophic faults rendering the entire chip unusable. A copy of the FCC op-amp was connected directly to pins to allow for measurement of its noise and gain. A photodiode is connected directly to pins to allow for characterization. The chip was packaged in a 44 pin quad-flat-package. The top of the package was not adhered closed to allow for light signals to be injected into the photodiodes.

5.1.2 Test Setup

Two custom PCBs and a FPGA development board are used to control and power the OR1 chip. One of the custom PCBs provided all the electrical interfaces to the OR1 chip, the other provided a low noise LED light source which was used to optically probe the OR1. Both PCBs were fabricated using a four layer process by Siber Circuits using PCLFR370HR laminate.

The OR1 interface PCB was designed to supply separate power supplies to the digital and analog power domains of the chip. A 16-bit 2.5MSPS ADC was used to measure the output of the integrator. The OR1 reset signal comes from the FPGA which was connected to the underside of the OR1 PCB by a high density connector. The V_{off} pin is connected to a 16-bit low noise DAC.

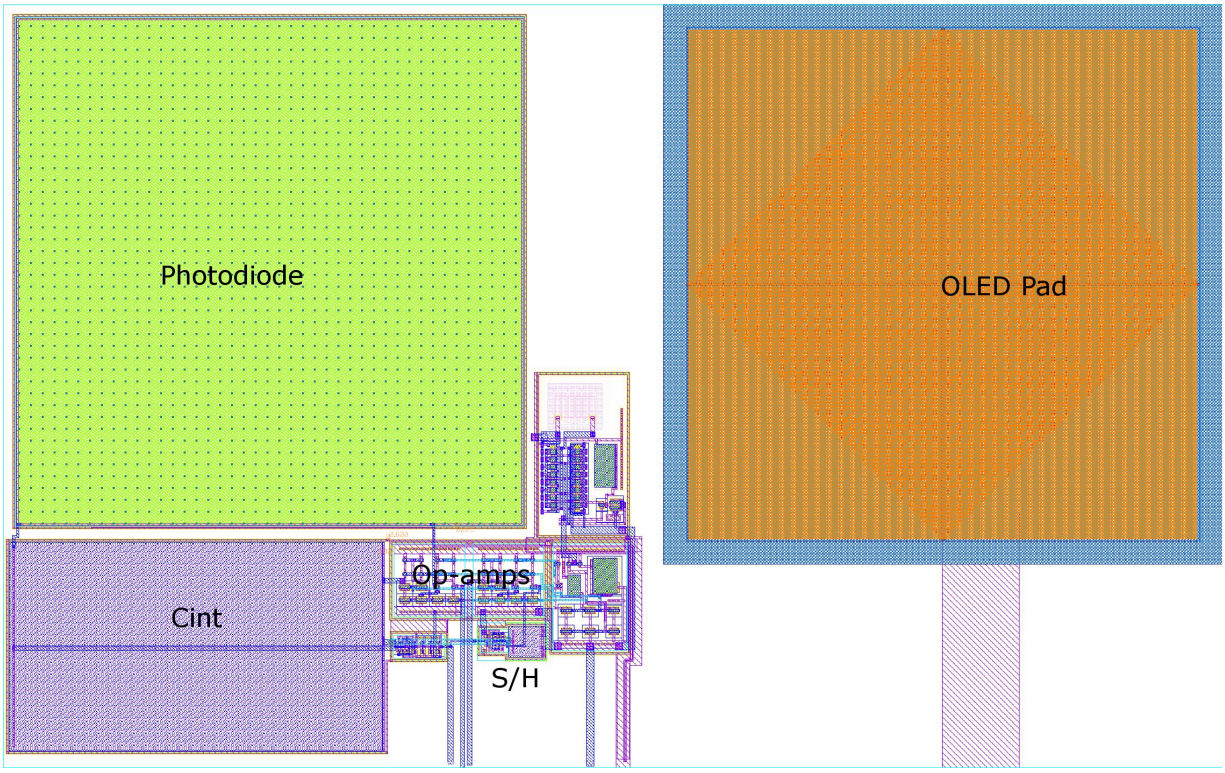


Figure 5.1: Complete layout of acquisition channel.

The LED PCB was mounted directly above the OR1 chip such that the LED was centred above the die. A 8 bit DAC was used to drive a NPN transistor which pulled current through the LED. This provided a low noise linear response for the amount of current flowing through the LED. The DAC was controlled by the FPGA through a connector on the OR1 PCB.

The FPGA development board is an Opal Kelly XEM6010 Spartan 6 development board. The purpose of the FPGA is to provide the digital interface to support the DACs and ADCs of the OR1 interface PCB. The data from the ADCs was feed into a FIFO buffer which was read by a MATLAB GUI. A more complete set of the PCB performance specifications is provided in Appendix E.

5.1.3 Op-amp Characterization

The FCC op-amp is critical to the performance of the acquisition channel. For this reason a copy of the FCC op-amp was connected to pins to allow for verification of its performance. Two of the bias voltages were also connected to pins; both were measured to be less than 1% different from simulation.

To measure the frequency response of the op-amp a common mode voltage of 1.65V was applied to the inverting terminal of the op-amp. The output of the op-amp balanced mid rail when the non-inverting terminal was placed at 1.648V. This gives the offset voltage of the amplifier to be 2mV.

A single frequency tone was then added to one of the rails and the gain was measured. Initially, the gain was measured to be much lower than expected. It was realized that due to the large output impedance of the op-amp, the loading placed on the op-amp by the oscilloscope, compromised the gain. A high input impedance OP129 op-amp was spliced into the trace in unity feedback to reduce the load current draw. Despite much effort to remove any residual flux, the parasitic resistance from the solder flux and PCB substrate, the maximum op-amp gain achieved was $A_V = 335V/V$. This is an order of magnitude smaller than predicted by simulation. The 3dB frequency was measured to be $f_{3dB} = 1.166kHz$. A single pole frequency response was observed. The addition of the addition of the OP129 buffer did not significantly contribute to the frequency response.

The noise of the op-amp was measured by leaving the op-amp in open loop and recording the output with the ADC. The corner frequency of the noise was found to be 20% higher than predicted by the unloaded simulation. When the simulation was repeated with loading that results in approximately the same gain, a much better agreement between the measured and simulated noise was observed (Figure 5.2). The total output referred noise from the FCC op-amp is measured to be $48.78mV_{RMS}$. Input referring the noise PSD gives a total input referred noise of $1.02mV_{RMS}$.

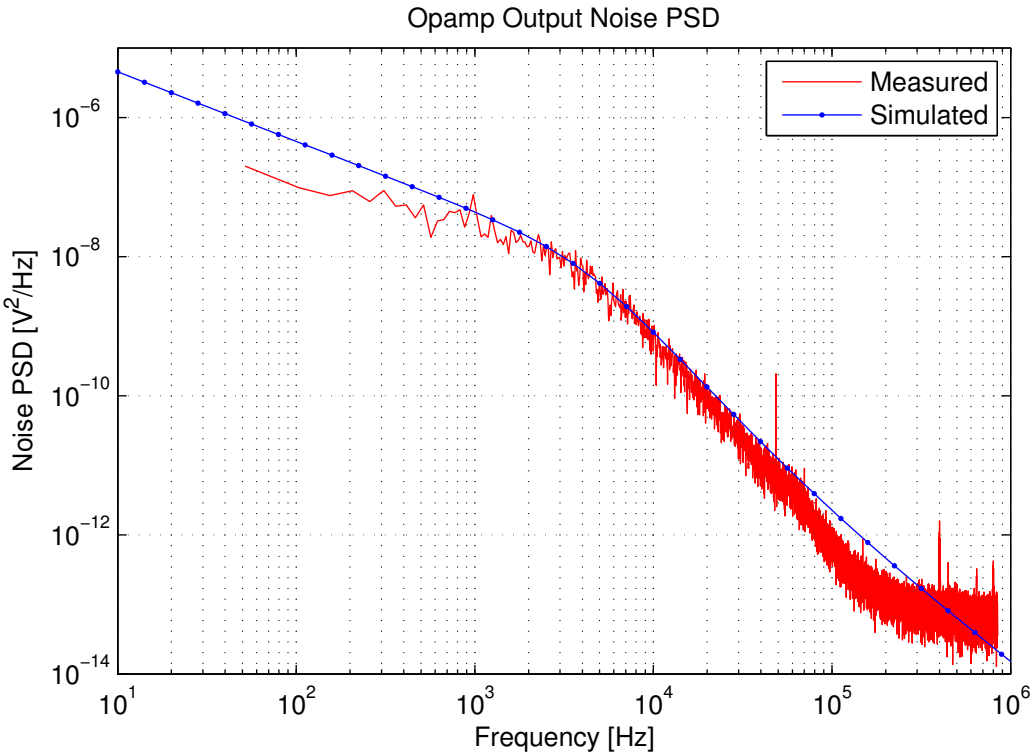


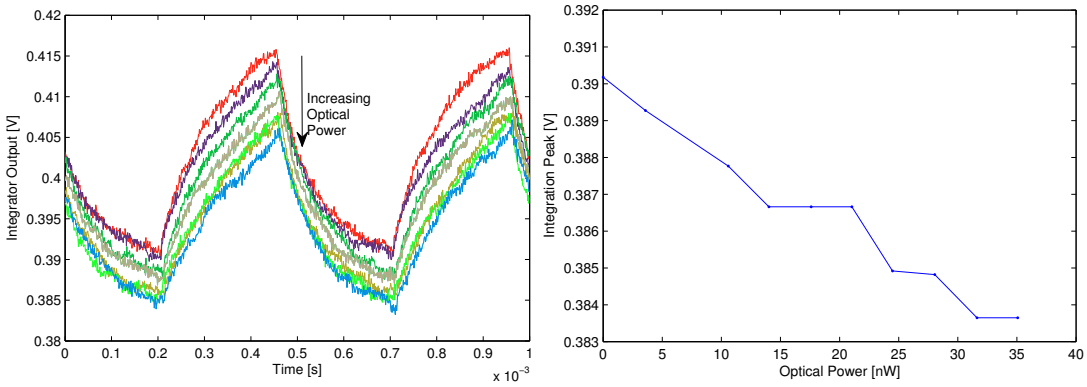
Figure 5.2: Comparison between measured and the loaded simulation of the output referred noise PSD of the FCC op-amp. The slope of the low frequency gain is determined by the flicker noise where as the high frequency slope is determined by the gain roll off of the op-amp. The plateau at the high frequency of the measured results is from the noise floor of the measurement which occurs at $10^{-13}V^2/Hz$.

5.1.4 Transient Output

To test the acquisition channel three parameter sweeps are made: vary the light intensity and measure the integrator output magnitude, vary the integration time and measure the integrator output, and vary the offset voltage and measure the integrator output. All measurements of the OR1 integrator output are made using a using Agilent Technologies MSO-X 3015A oscilloscope. This is because the digital signals used to control the OR1 PCB ADC corrupt the measurement of the signal.

To measure the output dependence on the light intensity, the LED provides a DC light signal at a controlled intensity. The time is set to: $T_{int} = 250\mu s$ and $T_h = 250\mu s$. The non-inverting terminal is set to $V_{off} = 0.693V$, meaning the op-amp should be in a high gain region. Ten different light intensities between 0 and 35nW are recorded in Figure 5.3. It can be seen that the acquisition channel fails to match the output voltage profile predicted in the Design or Simulation sections. The first problem is that during the hold/reset mode of operation, the peak output voltage is not maintained. This suggests that there is a parasitic resistance drawing current off of the capacitor C_h. A simulation with a $1G\Omega$ resistor placed in parallel with C_h demonstrates sufficient current draw to match the measured output profile. The other inconsistency with the previous sections is the decreasing integration peak magnitude with increased optical power. The hand calculations predict that an optical power of 35nW should cause the integrator peak to increase by 253mV; instead the peak decreases by 8mV. This is thought to be a result of the light incident on the analog components of the acquisition channel. With the increased light intensity, more carriers are also generated inside the op-amp, op-amp bias circuitry and pass transistors. This could result in unpredictable operating conditions of the circuitry and resulting in the improper operation of the CTIA. This hypothesis is given support by the decreased peak height but also decreased minimum voltage reached by the output. In typical circumstances, the minimum voltage should be determined by the offset voltage applied to the CTIA, however with increased light intensity the minimum voltage drops suggesting that this is a light dependence in the operation of the op-amp.

As the incorrect operation of the CTIA is expected to be explained by the light incident on the analog circuitry, in dark conditions it is expected that the integrator will still operate. To test this the ambient light is extinguished and different values of V_{Off} are applied to the CTIA. The photodiode was modelled in previous sections to have an large resistance value. By applying increasing bias voltages through the CTIA, the leakage current through the photodiode increases. This current can then be measured using the CTIA integrator as shown in Figure 5.4. A linear increase in the integrator output is observed for bias voltages up to 1.14V. Beyond this bias voltage the current increases rapidly and saturates the integrator. The exact cause of this sudden increase in current is not known as the



(a) (b)

Figure 5.3: (a) The output of the integrator as a function of time at 10 different optical powers on the photodiode. (b) The maximum integrator value for each applied optical power.

breakdown voltage of a n well-p sub diode in this process is 24V. Similar results however are also seen for a discrete photodiode, as will be discussed in Section 5.2.

5.2 Discrete Integrator

Due to problems with the ASIC implementation of the acquisition channel, a circuit similar to the acquisition channel was implemented using discrete components. The purpose of the discrete implementation is to demonstrate the transimpedance characteristics of a CTIA and partially validate the noise calculations derived in Section 3. This section will outline expected performance of the circuit and give measured results of the noise and transimpedance characteristics.

5.2.1 Design

The implementation of the discrete CTIA is based around the Texas Instruments IVC102 chip. This is a CTIA with integrated capacitors and reset and hold switches. Used in

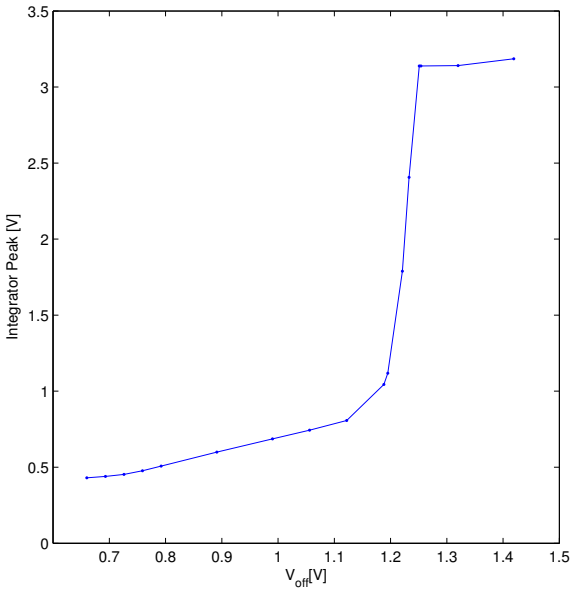


Figure 5.4: The maximum integrator value at T_{int} for values of V_{off}.

conjunction with a discrete photodiode, the circuit shown in Figure 5.5 is implemented. The discrete circuit implements the same transimpedance function as OR1, without the higher order poles introduced by the S/H and the output buffer. The transimpedance function is effectively described by:

$$V_{out}(f) = I_{PD}(f) \cdot \frac{T_{int}}{C_{int}} \cdot sinc(f \cdot T_{int}) \tag{5.1}$$

The IVC102 is specified to contribute $150\mu V_{RSM}$ for input capacitance of $45pF$ (the specified capacitance of the photodiode). The PCB has been characterized to contribute between $465\mu V_{RMS}$ and $930\mu V_{RMS}$ depending on the measurement (Appendix E). Assuming worst case noise the total predicted output noise is $887.4\mu V_{RMS}$.

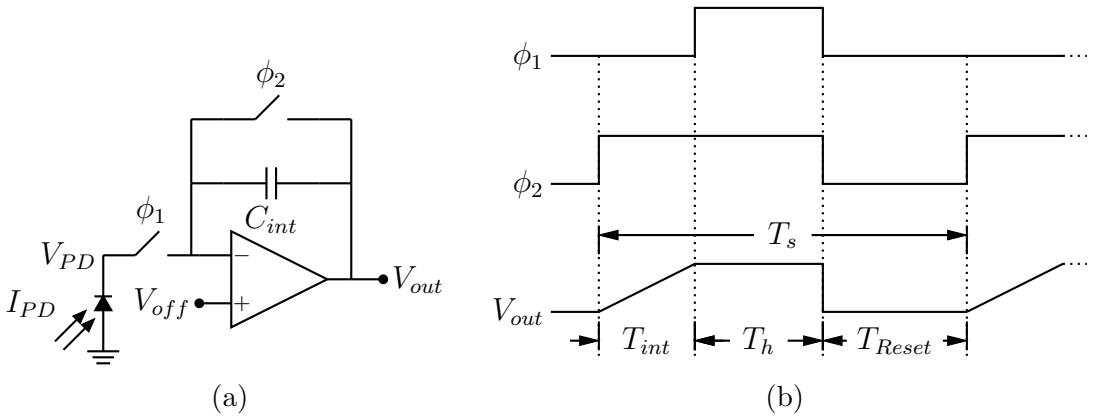


Figure 5.5: (a) The discrete circuit implementation of CTIA. (b) Timing diagram for discrete CTIA. Switches ϕ_1 and ϕ_2 are open on logic high.

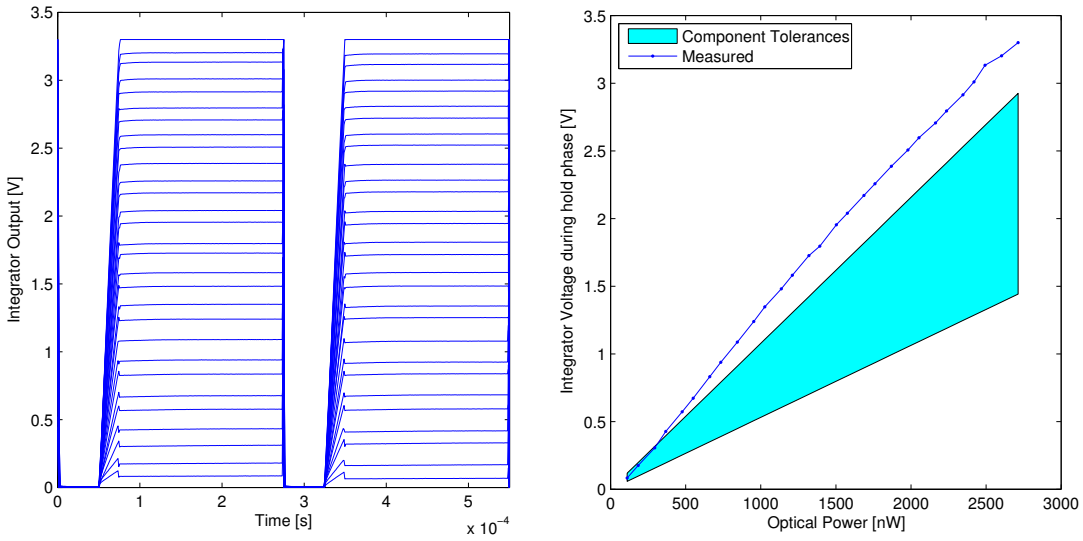
5.2.2 Test Setup

The discrete integrator circuit is laid out on the same PCB as OR1. The discrete photodiode is centred directly below the LED PCB. The Opal Kelly FPGA is used to send the control signals to the IVC102 integrator chip to match Figure 5.5b. The three phases of operation are required to ensure that the voltage across the photodiode is reset, otherwise charge accumulates during the hold period. The MATLAB software written for OR1 can also control the FPGA timing signals. The same 16 bit 2.5MSPS ADC is used as for the OR1. For further details on the OR1 PCB refer to Appendix E.

5.2.3 Light Intensity Measurements

The discrete integrator circuit demonstrated the expected output voltage signal profile with distinct integration, hold and reset phases (Figure 5.6a). When the intensity of the light was varied, the magnitude of the integrator voltage during the hold stage increased linearly (Figure 5.6b). The magnitude of the output voltage was higher than predicted by Eq. 5.1, even when accounting for the tolerance on the integrating capacitor($\pm$20%) and LED intensities ($\pm$15%). This slope would correspond to a capacitance of 6.78pF.

Other possible sources or error could have come from differences in mechanical alignment of the LED between the calibration measurements of Appendix E.2.4 and the integrator measurements. A small difference in the alignment would result in the LED not delivering the same light intensity due to variations in the light spatial distribution. Additional offsets in the slope could be introduced by leakage currents through the PCB which increase with integrator voltage.

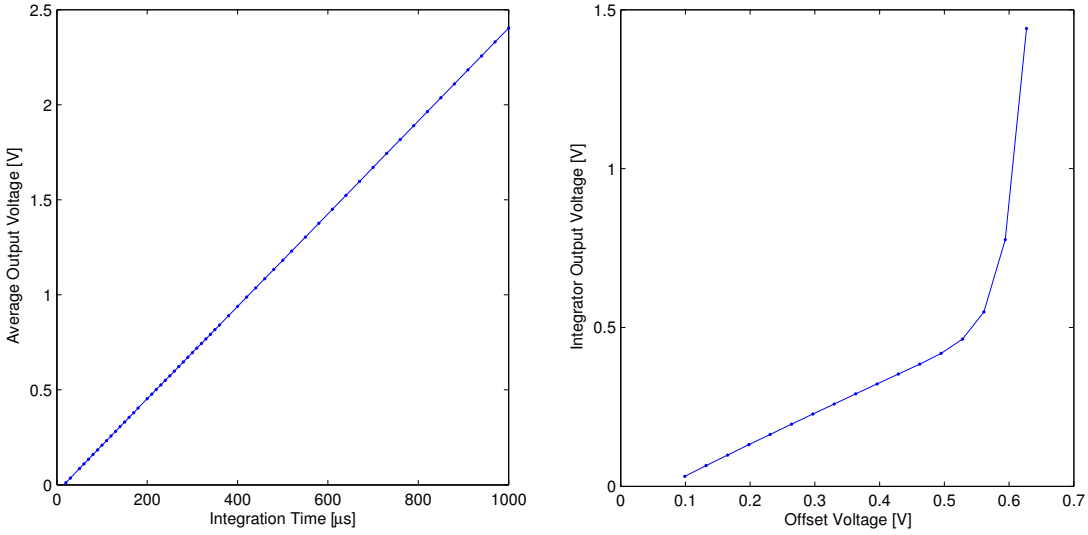


(a) (b)

Figure 5.6: (a) Measured output of the current integrator for different incident light intensities. (b) Line - The measured magnitude of the output voltage during the hold phase. Shaded area - The predicted output region when accounting for capacitor and LED intensity tolerances.

The transimpedance of the CTIA is determined by the capacitor value and the integration time. By varying the integration time a linear increase in the output voltage is measured (Figure 5.7a). The slope is equal to the photodiode current over the capacitor value. The selected integration capacitor is 10pF, predicting an integrated current of 24.3nA, which is in agreement with Figure 5.6b. Other offsets such as from the op-amp or charge injection, are displayed as as the y-intercept of the graph. The y-intercept is measured to be -35.9mV, which is much larger then the specified offsets for the IVC102's

op-amp ($\pm 5mV$). The charge injection from ϕ_1 is specified in the datasheet to contribute -58mV, suggesting that it is the source of the offset voltage.



(a) (b)

Figure 5.7: (a) Measured output of the CTIA for increasing durations of the integration phase. V_{off} was set to ground, $T_h = 200\mu s$, $T_{Reset} = 50\mu s$ (b) Measured output of the CTIA for increasing offset voltages applied to the non-inverting terminal of the CTIA op-amp.

5.2.4 Leakage Currents

When the offset is adjusted, the reset value of the output must track the input. Due to the intrinsic resistance of the photodiode, a DC current is expected to flow proportional to the applied voltage. This allows for the measurement of the shunt resistance of the photodiode. The photodiode is expected to demonstrate a resistance on the order of $100M\Omega$ however lower voltages demonstrate a resistance of $5.14M\Omega$ for voltages less than 0.5V. Above 0.5V the diode appears to break down and a rapid increase in current is measured, which saturates the detector (Figure 5.7b). The lower then expected photodiode resistance could be the result of parasitic resistance across the photodiode. This hypothesis is sug-

gested by initial recordings (not shown) that demonstrated very large currents flowing into the integrator which were later mitigated by cleaning all the solder points with isopropyl alcohol to remove residual flux. The sharp increase in the photodiode current is as of yet unexplained and will need further investigation.

5.2.5 Frequency Response

The frequency response to photodiode currents plays a key role in shaping much of the noise that propagates through the acquisition channel. The transimpedance of the acquisition channel is measured by sinusoidally modulating the light intensity of the LED and measuring the magnitude of the output voltage. To do so, the LED drive transistor is feed a 60mV peak-to-peak sine-wave with a 40mV DC offset by a Agilent 33522A function generator. An integration period of $50\mu s$ is selected to allow for a peak-peak output signal of 2V at low frequencies. The mean of the integrator output is used to calculate the mapping from the function generator voltage to the photodiode current. The photodiode current is calculated to have an amplitude of 200nA at low frequencies. Using this, the output frequency response is predicted to follow Eq. 5.1. The magnitude response is measured as half the peak-to-peak output voltage of the integrator. Due to digital interference a 40mV offset is added to the measurement.

$$V_{int}(f) = I_{PD}(f) \cdot \frac{T_{int}}{C_{int}} \cdot sinc(f \cdot T_{int}) + 40mV. \tag{5.2}$$

The magnitude is plotted against the output frequency in Figure 5.8. Close agreement can be seen between the two plots allowing for the conclusion that Eq. 5.1 accurately predicts the transimpedance of the acquisition channel.

5.2.6 Output Noise

Despite the difference in circuit architecture, the discrete implementation of the acquisition channel demonstrates very similar output noise characteristics. Of the four dominant noise

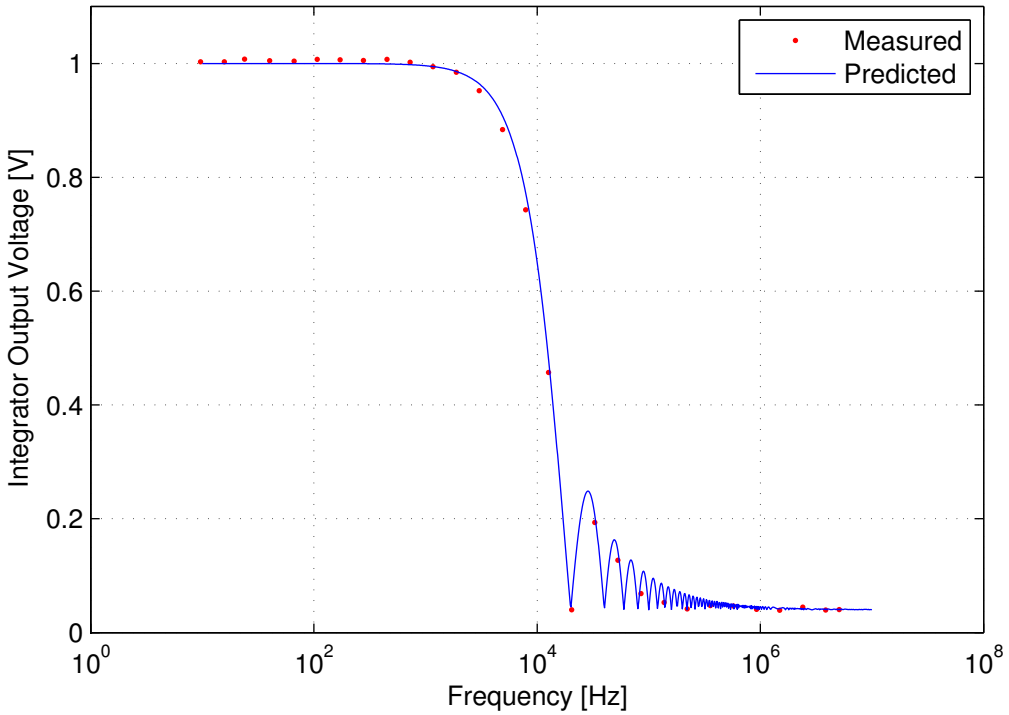


Figure 5.8: Output voltage of the integrator as a function of different optical input frequencies.

sources found in Section 3.3.2, two of them demonstrate the same transfer function; they are: the photodiode shot noise and the CTIA op-amp during the integration phase. The output buffer noise contribution is not present in the the discrete circuit, so its noise contribution is no longer present. The equations describing the CTIA op-amp noise during reset and hold are modified, as a result of the photodiode being disconnected:

$$v_{outv_{n1}H}{}^2 = \frac{T_h}{T_s} \cdot v_{n1}{}^2 \tag{5.3}$$

$$v_{outv_{n1}R}{}^2 = \frac{T_{Reset}}{T_s} \cdot v_{n1}{}^2 \tag{5.4}$$

The PCB also contributes noise to the final output measurement. The exact sources of

this noise is difficult to identify as the PCB contains many possible sources. Characterization of the this noise however demonstrated that it is nearly white with an amplitude of approximately $465\mu V_{RMS}$, depending on the warm-up period of the electronics.

The total noise of the measurement is therefore made up of:

$$V_n{}^2 = v_{outi_nI}{}^2 + v_{outv_{n1}I}{}^2 + v_{outv_{n1}R}{}^2 + v_{outv_{n1}H}{}^2 + v_{outPCB}{}^2 \tag{5.5}$$

$$= \frac{T_{int}}{2\ C_{int}{}^2} \cdot \overline{i_n}^2 + \frac{v_{n1}{}^2}{T_s} \cdot \left(T_{int} \left(1 + \frac{C_{PD}}{C_{int}} \right)^2 + T_h + T_{Reset} \right) + v_{outPCB}{}^2 \tag{5.6}$$

As described by Eq. 3.32, the shot noise of the photodiode is related to the incident light intensity. By increasing the light intensity the output noise should increase. This is tested in Figure 5.9. The light intensity on the photodiode is increased by increasing the current driven through the LED above the photodiode. The integration period is $T_{int} = 10\mu s$, the reset period is $T_{Reset} = 10\mu s$, and the hold period is $T_h = 100\mu s$, for a total period of $T_s = 120\mu s$. The photodiode current is calculated by taking the mean value of the sampled output and dividing by T_{int} and multiplying by C_{int}.

The measured noise when the light intensity is increased is slightly higher than that predicted. The predicted noise is however, based on a calculated value of I_{PD}, which assumes that the values of C_{int} and T_{int} are accurate. The timing is well controlled by the FPGA, however the value of C_{int} could be lower than specified by the datasheet. By using the value of $C_{int} = 6.78pF$ which was found to fit the data in Figure 5.6b, the predicted noise follows the measured noise much more accurately. The predicted values assume that the noise measured when the light is off, is constant while the light intensity increase. The results shown in Figure 5.9 demonstrates good agreement with the noise predicted by the equation.

As described by Eq. 5.6, the total noise is also a function of T_{int}. By increasing T_{int} the contribution from the shot noise will increase and the relative contribution from the CTIA op-amp will be dominated by $v_{outv_{n1}I}$. This is measured by applying a large LED intensity onto the photodiode and measuring the standard deviation of the sampled output for different values of T_{int}. As the total current can be determined by the mean of

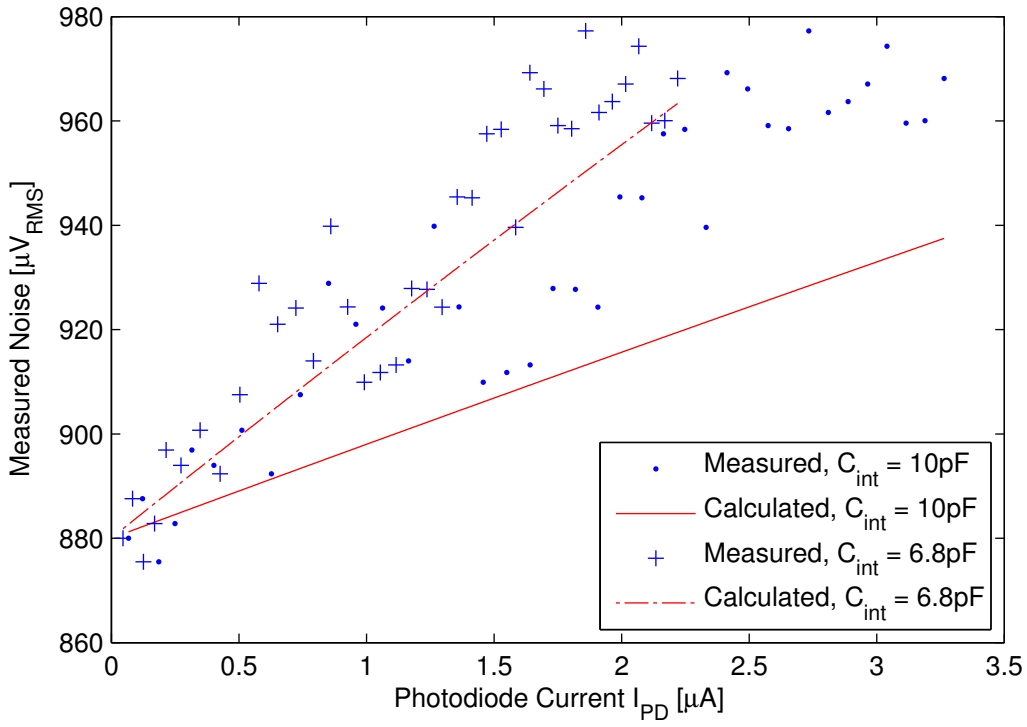


Figure 5.9: The noise as a function of photodiode photo-current. The measured data back calculates the photodiode current based on the value of C_{int} and T_{int}. The values for $C_{int} = 10pF$ and $C_{int} = 6.8pF$ are plotted here.

the measured output the total photodiode current for Figure 5.10 is found to be $2.11\mu A$, taking $C_{int} = 6.8pF$ as determined before. The op-amp noise v_{n1} is taken to be $200\mu V_{RMS}$ as specified by the IVC102 datasheet. To calculate the contribution of the noise generated by the PCB the following equation can be used:

$$v_{outPCB}{}^2 = V_n{}^2|_{T_{int}=0} - v_{n1}{}^2 \tag{5.7}$$

From this the total noise from the PCB is found to be $218\mu V_{RMS}$.

When the values predicted by Eq. 5.6 for a 50% op-amp noise correlation are compared to the measured values of the discrete integrator, good agreement is seen for integration period greater than $2\mu s$. Below $2\mu s$ it is suspected that the circuit is still in transi-

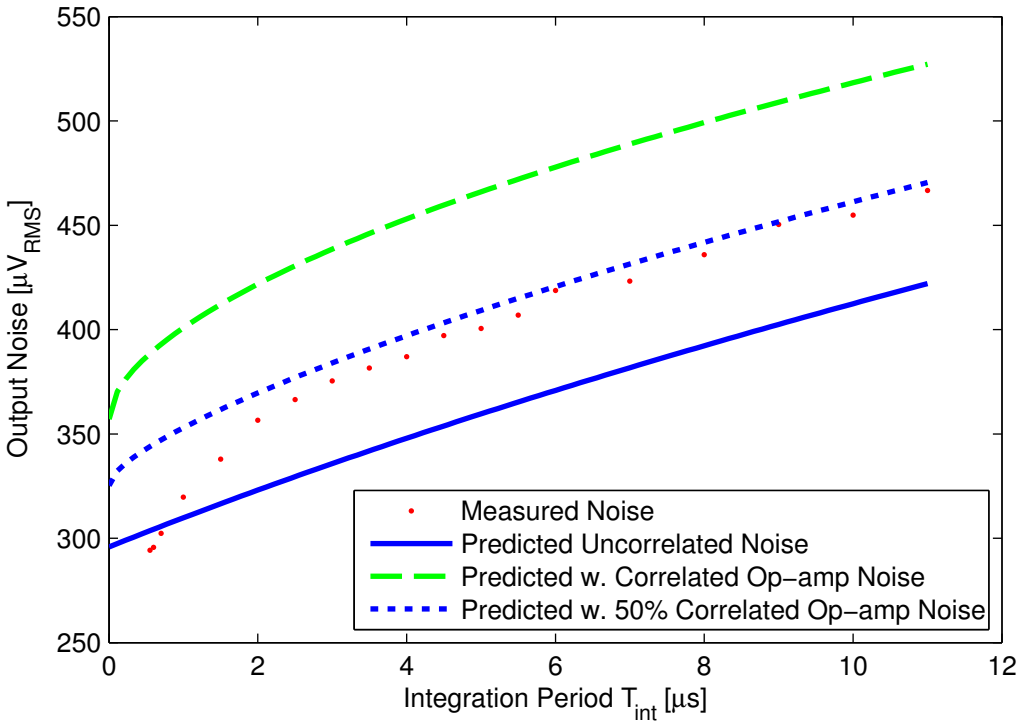


Figure 5.10: Comparison between the total noise predicted and the measured as a function of T_{int}.

tion switching from reset into integrate. This is supported by direct measurement of the waveform which still shows charge injection taking place.

Chapter 6

Discussion and Conclusion

6.1 Discussion of the ASIC Integrator

The physical implementation of the acquisition channel in an ASIC was largely unsuccessful. There were a number of problems which contributed to the failure of this chip including: the op-amp output resistance; the non-functional S/H circuit; the photo-sensitivity of other active components of the circuit.

The output buffer was intended to drive off-chip currents to allow for measurement without compromising the S/H circuit. Simulations of this circuit were performed only with a probe capacitance and not a parasitic resistance. As the output resistance of the op-amp is calculated to be approximately $100M\Omega$, the addition of a probe $R = 1M\Omega$ drops the output resistance and therefore the gain of the op-amp by a factor of 100. When an ADC is connected to the output, the gain is compromised even further, preventing the buffer from operating at all.

The S/H circuit was intended to sample the output of the CTIA and hold it for the output buffer. The measured output profiles of the buffer indicate that after the integration period the voltage on the hold capacitor begins to droop immediately. Simulations demonstrate that a parasitic resistance of $1G\Omega$ is sufficient to compromise the performance

of the S/H circuit. The circuit extracted from the layout was expected to identify this type of error, however as shown in Figure 4.4, these simulations demonstrate proper operation. It is possible that the extraction process was set to ignore parasitics over $1G\Omega$, which would result in this being missed.

The photo-sensitivity of the active components of the circuit was an unexpected result. As the photo-currents generated in the photodiode are on the order of 100nA, the influence of currents generated in the active components of the circuit were not expected to be significant in comparison to the currents in the op-amp. However, as the light intensity increased, the output of the integrator decreased, rendering this circuit useless for optical detection.

6.2 Discussion of the Discrete Integrator

The implementation of the signal acquisition channel using discrete components demonstrated far better performance that the ASIC implementation. Possibly the most important result from the this circuit is the proper demonstration of the CTIA transfer function. Eq. 3.7 demonstrated a close match to the measured results across a wide frequency range.

The discrete implementation however presented several problems intrinsic to discrete electronics. A significant baseline noise generated by the PCB was measured. This baseline noise was on the same order of the noise predicted, and fluctuated in time. This complicated the comparison between the noise modelled in Section 3.3.2 and the measurements. Additionally leakage currents between pins on the ICV102 package resulted in currents bypassing the input switch and integrating current during the hold phase.

The total noise measured by the discrete implementation of the signal acquisition channel however mostly followed the trends predicted. As the light intensity was increased, the shot noise increased as predicted. The noise contributed by the CTIA op-amp however diverged from the predicted trend. A larger noise amplitude was measured then predicted by Eq. 5.6, which is hypothesized to be a result of correlated noise. When a 50% correlation was assumed agreement was seen between the modelled noise and the measured

results; however, further analysis of this is needed to fully characterise this effect. This hypothesis is further supported by the transient noise simulation results presented in Figure 4.13a, which also demonstrate the simulated total noise being higher than expected. This is despite the transfer function from the non-inverting terminal to the output being independently validated in Figure 4.8.

6.2.1 Limit of Detection

To calculate the LOD achieved by the discrete integrator a few assumptions can be made about the signal: (i) the power of the fluorescence signal is described by Eq. 3.2 (ii) the measured output of the integrator is completely made up of stray excitation light, that is, the fluorescence is insignificant in comparison.

Using these assumptions the measured data can be used to back calculate the LOD for the hypothetical LOC device proposed in Section 3. These calculated values are compared to that predicted by Eq. 3.68, for different values of T_{int} in Figure 6.1. The trend of the two lines matches closely, a vertical difference in the values is accounted for by noting that the op-amp noise in the discrete amplifier was better than that predicted for the CMOS. From this it can be determined that the minimum LOD for the discrete implementation of the signal acquisition channel would be $7.2\mu M$.

6.3 Conclusions

This work has performed analysis and measured the noise performance of CTIA-based circuits for FD in LOC applications. Various relationships were derived for improving the LOD for CTIA based FD. Some of these relationships were verified in simulation and again in physical implementation of the proposed signal acquisition channel.

Of the various noise sources identified within the proposed ASIC signal acquisition channel, three of them dominated over the others. They were: the CTIA op-amp noise, the photodiode shot noise, and the output buffer noise. Simulations of the output buffer

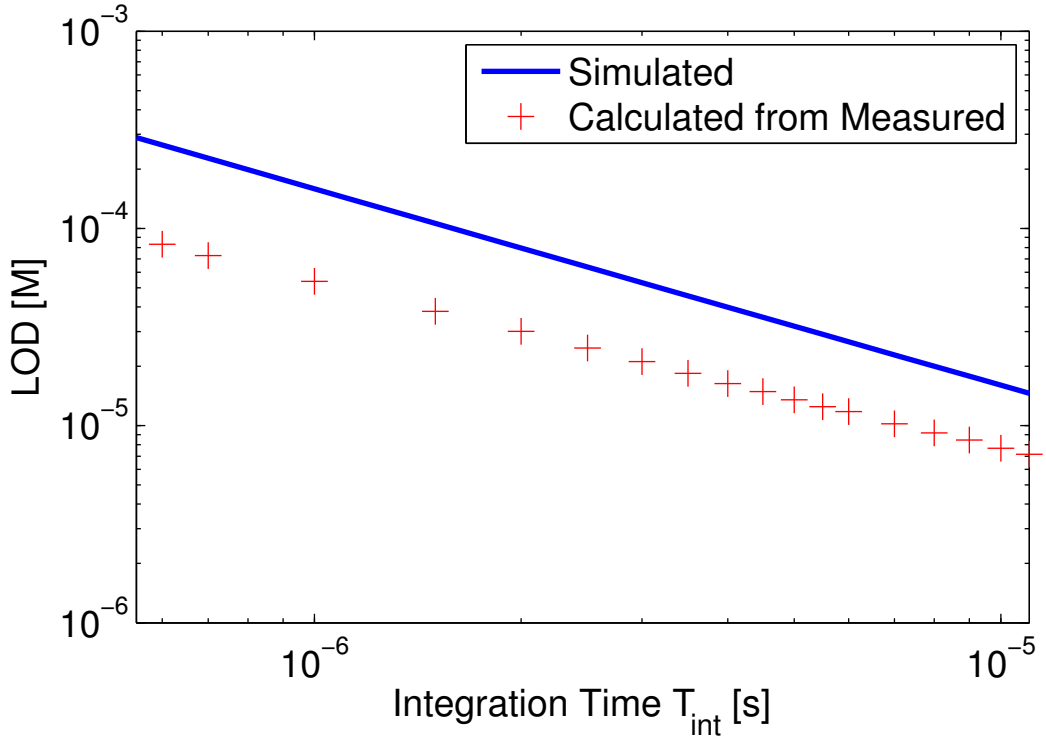


Figure 6.1: Comparison between the predicted LOD performance and that calculated from the measured signal and noise parameters.

noise and the photodiode shot noise were used to validated the transfer functions. The CTIA op-amp noise deviated from the expected profile, as it is hypothesized that the noise is partially correlated between the reset and integrate phase. Further analytical analysis is needed to verify this hypothesis.

The signal acquisition channel was implemented as an ASIC; a modified channel was implemented in discrete components. The ASIC demonstrated various unexpected behaviours which did not present themselves in simulation. A parasitic resistance prevented the S/H circuitry from working and the large output impedance of the FCC op-amp used, prevented the signals from being effectively sent off chip. Additionally the op-amp demonstrated photo-sensitivity which prevented the signal acquisition channel from working as a optical detector. The discrete implementation of the signal acquisition channel demon-

strated the trends predicted by simulation and provided validation of the photodiode shot noise relationship. The discrete implementation demonstrated a SNR which would result in a LOD of $7.2\mu M$ for AF532 fluorophore in the proposed hypothetical LOC FD device.

6.4 Future Directions

There are a number of different directions that this work can be taken. More immediately, improvements to the signal acquisition channel are proposed. In a broader sense, LOC FD is a growing field and various options are available. These topics are discussed in the following sections.

6.4.1 Acquisition Channel

The acquisition channel requires further development before it is ready for integration with the microfluidics. A working chip must first be demonstrated with the capability to drive signals off-chip without the assistance of additional buffers. Additionally, a functional S/H circuit is needed to allow for proper operation of the circuit. Further analysis needs to be done into the photo-sensitivity of the active components of the circuit. The exact mechanism for the optical fluctuations needs to be identified so that it can be resolved. Optically shielding the op-amps and bias-circuitry using a top-metal layer may resolve many of the issues.

There are various other options for the signal acquisition channel that can also be explored. It is not necessary to restrict the acquisition channel to integrator based circuits. Many other groups have started using avalanche photodiodes (APDs) for fluorescence detection applications. These devices effectively have infinite gain making them extremely sensitive. They also double as ADCs because the photons present themselves as spike events which can be easily counted by digital circuitry. The problem with APDs is they require high bias voltages which requires special doping profiles to accommodate, limiting

these devices to high voltage CMOS processes. Additionally if photons arrive faster then the circuit can be clenched, the detector will saturate.

6.4.2 Lab-on-a-Chip Fluorescence Detection

Before a commercially viable LOC FD device is possible there are many engineering challenges that must be overcome. Much of the rudimentary technologies required for LOC FD has already been demonstrated. The integrated optics, the fabrication and the electronics have already been demonstrated in isolation. One major challenge which needs to be overcome is the integration of these many components into a single chip while maintaining a usable interface. Advanced packaging techniques are needed to allow sample loading, optical and electrical interfaces to these LOC devices. This is an area of active research and will likely be seeing significant development in the coming years [63].

Sample preparation has also been identified as an area needing further evaluation. FD is often only the final step of often long and complicated assays. Much work needs to be done to automate and integrate these assays into simple preloaded cartridges. The off chip mixing of reagents is contrary to the model of LOC and reduces the field to only an incremental improvement to the existing centralized lab model of modern healthcare.

More generally, ASIC based FD, has other applications in other fields of biology. Of particular interest is opto-genetics, which enables the fluorescence based recording of neural activity. As it is undesirable to kill the neurological tissue which is being recorded, integrated implantable devices are being developed for this particular application [64]. To achieve this, implementation of the excitation light source is needed. Integration of LED and eventually OLED technology is needed to allow these types of implantable devices.

On chip light sources were discussed in the creation of OR1. Some versions of the chip have already been integrated with LED dies. Further work is needed to characterize and model the new excitation schemes possible with this new integrated architecture.

Appendices

Appendix A

Folded Cascode Op-amp Design

The complete signal acquisition circuit requires two op-amps. The circuit makes use of an NMOS-input, fully-differential folded cascode (FCC) op-amp previously designed by B. Crowley in the AMSP350 process. This design is modified from the original, to provide a single-ended output. Although an FCC op-amp is not ideally suited for this application, due to its relatively high output impedance, it is used to minimize the number of untested components used. All biasing circuitry had also been previously taped out and is reused for this design.

A.1 Gain and Output Impedance

The op-amp schematic is implemented as shown in Figure A.1. Hand calculation of the gain and output impedance can be performed by analysing the half circuit of the op-amp (Figure A.2) [61, 65].

The gain (A_v) of the op-amp is described by [66]:

$$A_v = G_M \; R_{out} \tag{A.1}$$

where R_{out} is the output impedance of the op-amp and G_M is the total transconductance

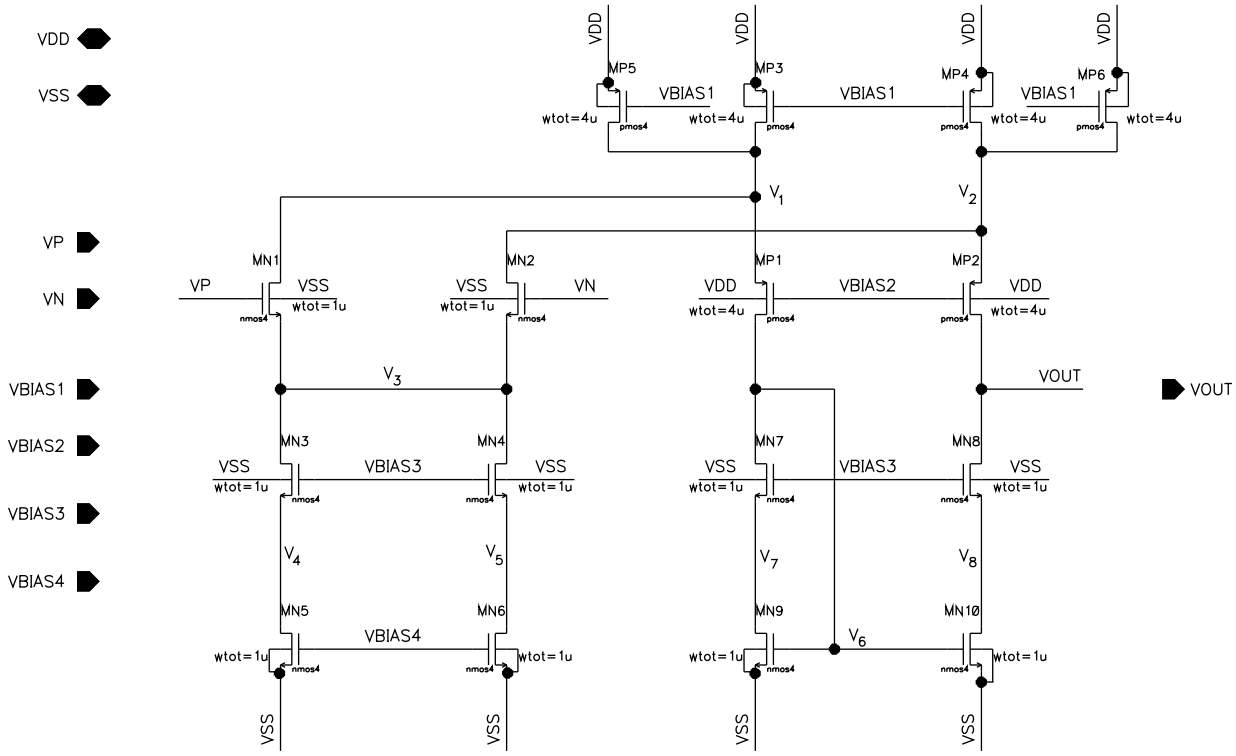


Figure A.1: FCC Op-amp schematic.

of the op-amp. The transconductance of an FCC is simply the transconductance of the input transistor.

$$G_M = g_{m_{N1}} = g_{m_{N2}} \tag{A.2}$$

The output impedance can be calculated by analysing Figure A.2

Hand analysis shows the output resistance is:

$$R_{Out} = (r_{o_{n10}} + r_{o_{n8}} + r_{o_{n8}} \cdot r_{o_{n10}} \cdot g_{m_{n8}}) || (r_{o_{p4}} || r_{o_{p6}} || r_{o_{n2}} + r_{o_{p2}} + r_{o_{p4}} || r_{o_{p6}} || r_{o_{n2}} \cdot r_{o_{p2}} \cdot g_{m_{p2}}) \tag{A.3}$$

$$\approx (r_{o_{n8}} \cdot r_{o_{n10}} \cdot g_{m_{n8}}) || ((\frac{r_{o_{p4}}}{2} || r_{o_{n2}}) \cdot r_{o_{p2}} \cdot g_{m_{p2}}) \tag{A.4}$$

Utilizing a DC simulation of the op-amp, the values of g_m and r_o were extracted (Table A.1) using the bias voltages presented in Table A.2. These values provide an output impedance of $R_{out} = 123.8M\Omega$ and gain of $A_v = 2408V/V$:

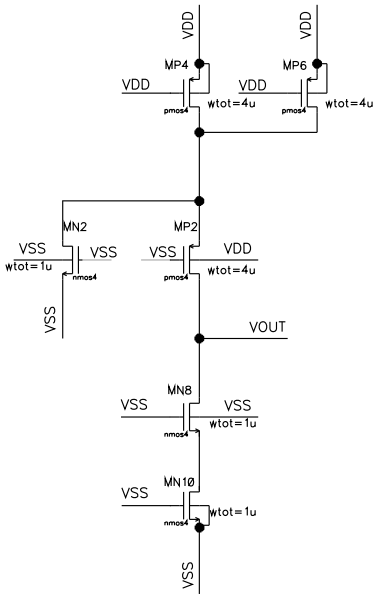


Figure A.2: Folded Cascode half circuit

Transistor	$r_o[M\Omega]$	$g_m[\mu A/V]$
MN1	31.358	19.45
MN2	31.358	19.45
MN3	3.300	18.90
MN4	3.300	18.90
MN5	10.043	18.89
MN6	10.043	18.89
MN7	0.782	18.12
MN8	0.782	18.12
MN9	9.921	18.93
MN10	9.921	18.93
MP1	15.853	23.46
MP2	15.853	23.46
MP3	6.105	22.63
MP4	6.105	22.63
MP5	6.105	22.63
MP6	6.105	22.63

Table A.1: Simulated small signal parameters of FCC op-amp transistors. These were obtained with $V_{CM} = 1.65V$ and bias voltages applied as in Table A.2.

V_{Bias}	$[V]$
V_{Bias1}	2.437
V_{Bias2}	1.986
V_{Bias3}	1.303
V_{Bias4}	0.679

Table A.2: Simulated bias voltages applied to the FCC op-amp.

A.2 Op-amp

The total noise of the op-amp was predicted in hand calculations to contribute 117 μV of output noise when configured in unity feedback with a 2pF load. Much of these hand calculations were based off DC operating points extracted from simulations however these small signal parameters can change depending on the operation of the op-amp. The following subsections will validate the hand calculations against Cadence simulations allowing the hand calculations to be carried forward for use in later parts of the noise analysis of the fluorescence detection integrator.

A.2.1 Rout and Gm

Based on the hand equations (Equation A.1) provided in the design section, the gain of the folded cascode op-amp is highly dependent on the values of g_m and R_{out}. Both of these values depend on the DC operating point of the op-amp. The DC operating points depend on the biasing, the common mode voltage and the output load. Sweeping the DC common mode voltage (Figure A.3) allows us to see how linear the gain will be across the input range. It can be seen that neither R_{out} or g_m provide a good gain for V_{CM} below 0.7 V. This results from the NMOS input stage which isn't in saturation until V_{CM} is large enough to drive the current mirror and the NMOS gate. The total gain for different V_{CM} is shown in Figure A.4.

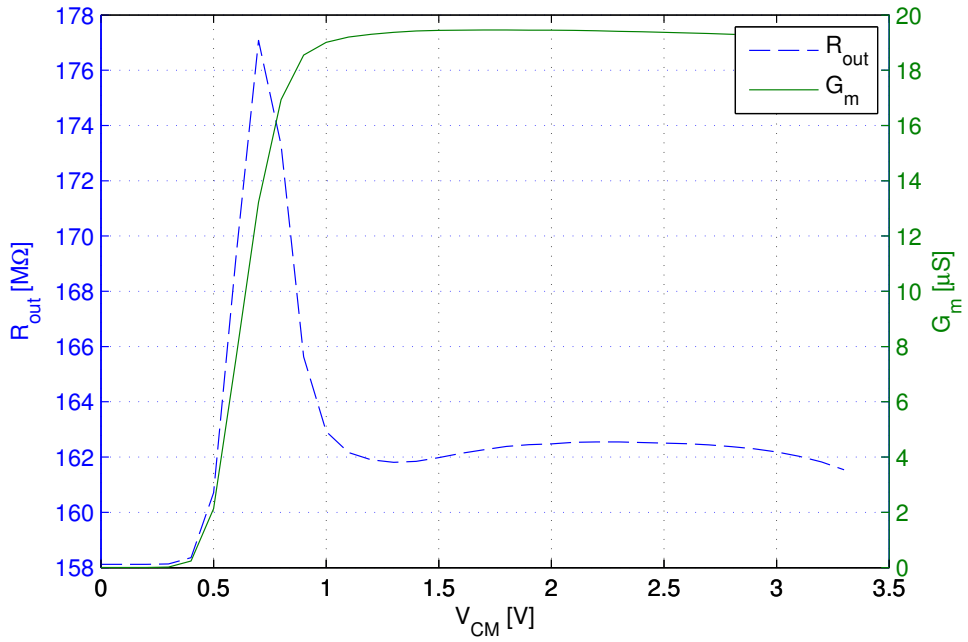


Figure A.3: As the DC operating points change depending on the common mode voltage applied, R_{out} and G_m will change accordingly. This simulation was performed using the specified bias voltages.

A.2.2 Gain and Phase Analysis

Simulation of the gain and phase of the FCC (Figure A.4) provides a gain of 68dB which corresponds to a gain of $2511V/V$ which is reasonably close to the hand calculated value of $2408V/V$.

A.2.3 Gain Under Load

When the FCC op-amp is resistively loaded, the small signal model of the output voltage changes to accomidate. When a resistive load is added to the output it is placed in parallel to R_{out} of the op-amp lowering the effective resistance. The gain has been previously found to be $G_m \cdot R_{out}$, however when accounting for the loading it becomes:

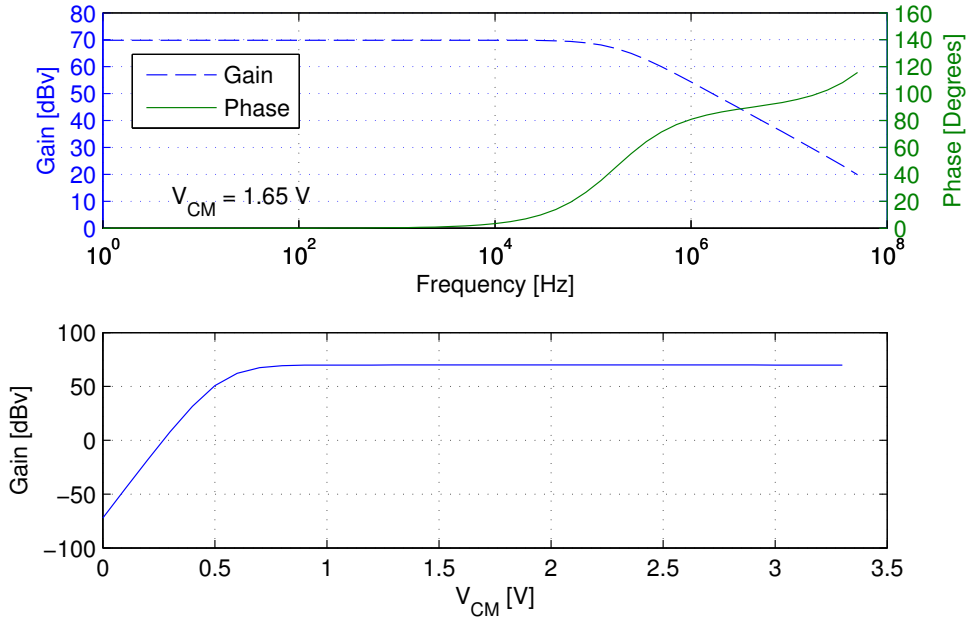


Figure A.4: Top: Gain and Phase of the folded cascode op-amp unloaded. Maximum gain is 69.8 dBv. Bottom: Gain as calculated by multiplying extracted g_m and R_{out} values. Maximum gain is around 70.0 dBv.

$$A_v = G_m \cdot (R_{out}||R_{Load}) \tag{A.5}$$

Thus as the load impedance decreases the gain also decreases (Figure A.5). The load will also effect the DC operating points of the cascoded transistors further effecting the gain. Conventionally this wouldn't dramatically influence the gain as R_{out} is usually smaller than R_{Load} but because of the high output impedance, even negligible loading (i.e. parasitic resistance of the PCB) will dramatically reduce the gain.

A.2.4 Noise Performance

To initially verify the matrix of equations (Section A.3.1) used to solve for the transimpedance for each transistors noise, the AC node voltages were also calculated using

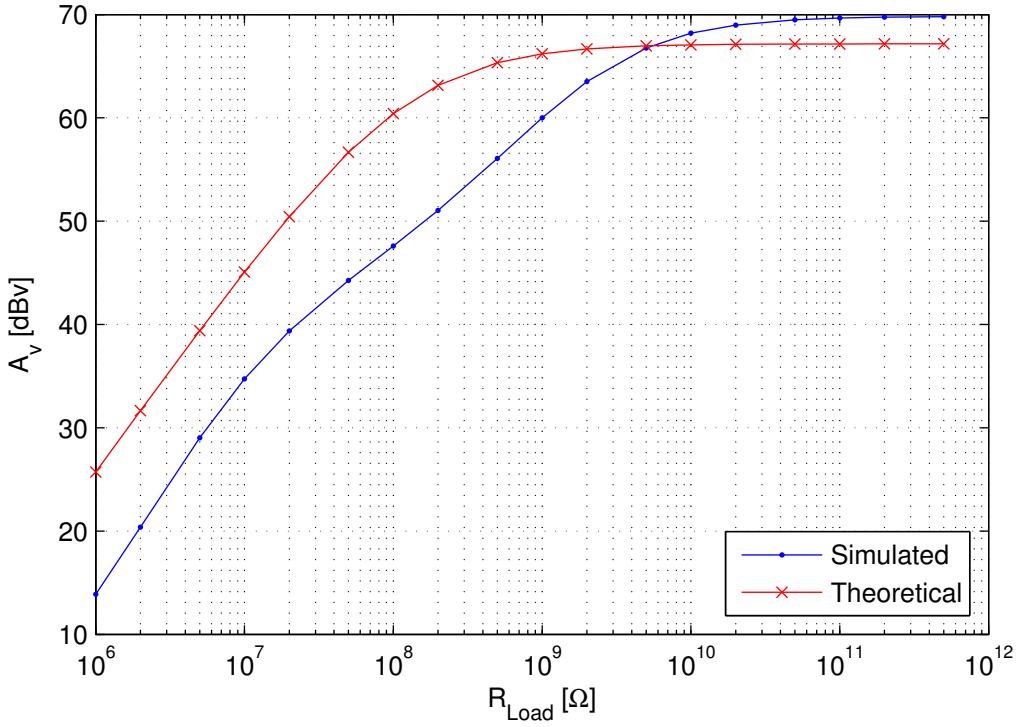


Figure A.5: As the output load is increased the gain at a common mode input voltage of 1.65V increases until it plateaus. In the hand calculated model (Eq. A.5) the gain manages to plateau around $400M\Omega$ however in the simulation the plateau doesn't occur until much higher load impedances around $10G\Omega$.

the DC operating points presented in Table A.1. As can be seen in Table A.3 the equation matrix provides a fairly close approximation to the node voltages predicted by the spectre models.

As shown in Table A.4 the hand calculated noise for each transistor provides a fairly accurate value for the noise contributed. It can be seen that the lower frequency hand calculation is less accurate then the high frequency. It is suspected that this is because in the AMS documentation they provide two sets of equations for flicker noise, which is dominant at lower frequencies. One equation provides all the parameters but is less accurate, the other involves term representing a non-linear expression not given in the documentation. This was also observed in Appendix C.

	AC		DC
Node	Simulated	Hand Calculated	Simulated
V1	335mV	403mV	2.918V
V2	7.15V	7.10V	2.928V
V3	402mV	505mV	778mV
V4	5.09mV	7.92mV	493mV
V5	5.09mV	7.92mV	493mV
V6	504mV	502mV	679mV
V7	372mV	455mV	490mV
V8	166V	167V	490mV
Vout	3105V	2535V	679mV

Table A.3: The low frequency AC node voltages with a $V_{CM} = 1.65V$ as simulated by spectre. The hand calculated node AC node voltages as found as the solution to Equations A.8 to A.16

	Predicted Noise $[\mu V/\sqrt{Hz}]$		Simulated Noise $[\mu V/\sqrt{Hz}]$	
Transistor	@ 1kHz	@ 100kHz	@ 1kHz	@ 100kHz
N1 and N2	429.76	79.37	983.00	110.00
P3/5 and P4/6	273.83	106.32	202.94	110.41
N9 and N10	435.17	80.02	863.20	103.30

Table A.4: Comparison between the output referred noise calculated using the matrix of equations and the spectre simulated results. The simulation was performed without load and a $V_{CM} = 1.65V$. All other transistors were also measured however their contribution to the noise was less than 0.01% of total output noise.

A.2.5 Bias Generator Noise

In the fabricated circuit the op-amp bias will be generated by a bias generator instance. This circuit will have its own noise associated with it. A simulation was performed using this bias generator and was compared against the ideal bias sources. It was found to shift the PSD by less than 3% and will be considered negligible.

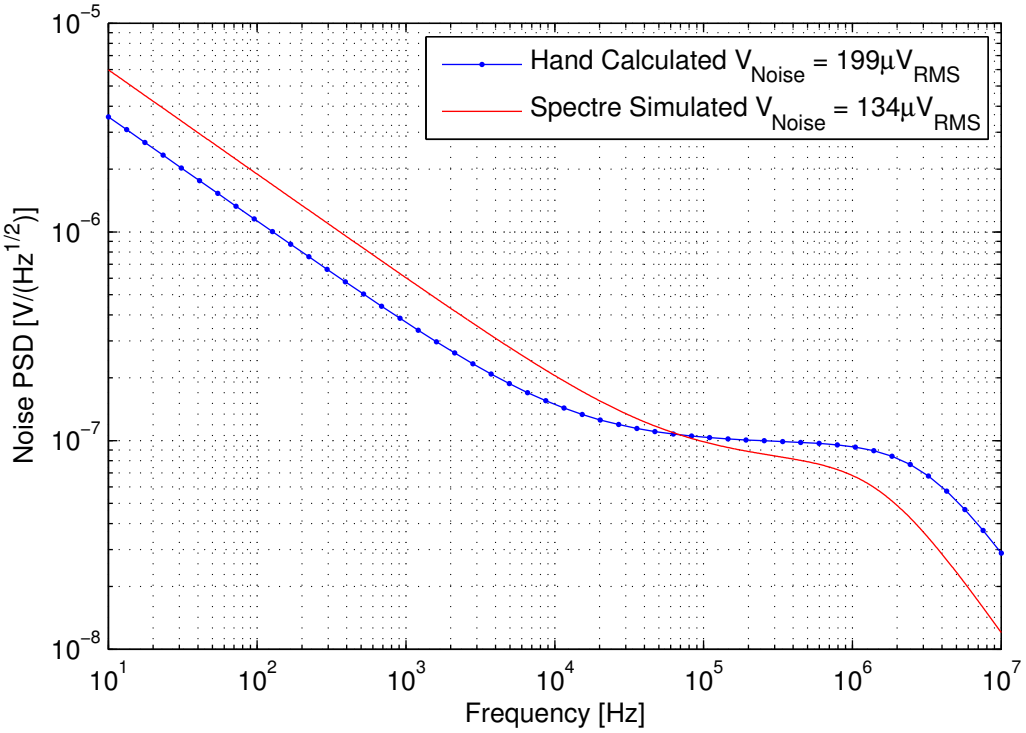


Figure A.6: Comparison between noise calculated using Eq. A.17 (adjusted for unity gain, loaded with a 2pF capacitor) and that produced by SpectreRF.

A.3 Op-Amp Noise

As the noise is of great importance for the operation of this circuit, the noise of the op-amp needs to be characterized. This section provides the noise analysis of the FCC op-amp.

From the AMSP35 process documentation the transistor thermal current noise power spectral density (PSD), measured in $[A^2/Hz]$, is described by [67]:

$$I_n{}^2 = \frac{8}{3} \cdot k \cdot T \cdot (g_m + g_{ds} + g_{mb}) \tag{A.6}$$

where k is the Boltzmann constant, T is the temperature, g_m, g_{ds} and g_{mb} are all transconductance parameters of the transistor. The flicker noise current PSD is similarly described

by:

$$I_n{}^2 = \frac{K_f \cdot I_d{}^{AF}}{C_{ox} \cdot w \cdot l} \cdot \frac{1}{f} \tag{A.7}$$

where K_f and A_f are noise parameters, I_d is the transistor drain current, C_{ox} is the gate oxide capacitance and l and w are the dimensions of the transistor.

By reducing the op-amp into its small-signal model, it is possible to derive the node equations for the entire circuit. By adding the a current noise source to the node equations for each transistor (as shown in Figure A.7) the transimpedance for each source can be found. By summing the PSD from each transistor the total output referred noise voltage can be found. The output noise can be input referred to a noise voltage by dividing by the gain profile of the op-amp. This approach was verified using a simple common source amplifier in Appendix C.

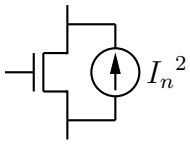


Figure A.7: Transistor noise model

A.3.1 Systems of Equations

The following equations represent the node equations for KCL for the FCC op-amp with no signal applied and no noise sources present. For each noise source a single term would need to be added to either one or two node equations. To reduce the number of equations MP3 was combined with MP5 and MP4 was combined with MP6. This was dealt with numerically but adding their g_m values. The matrix was solved using MATLAB and the output referred noise was taken as the voltage presented at V_{out}. The small signal parameters were taken as those presented in Table A.1.

$$V_1\, g_{p1} - V_3\, g_{n1} + \frac{2\, V_1}{r_{p3}} + \frac{V_1 - V_3}{r_{n1}} + \frac{V_1 - V_6}{r_{p1}} = 0 \tag{A.8}$$

$$V_2\, g_{p2} - V_3\, g_{n2} + \frac{2\,V_2}{r_{p4}} + \frac{V_2 - V_3}{r_{n2}} + \frac{V_2 - V_{out}}{r_{p2}} = 0 \tag{A.9}$$

$$\frac{V_1 - V_3}{r_{n1}} - V_3\, g_{n2} - V_3\, g_{n1} + \frac{V_2 - V_3}{r_{n2}} = \frac{V_3 - V_4}{r_{n3}} - V_5\, g_{n4} - V_4\, g_{n3} + \frac{V_3 - V_5}{r_{n4}} \tag{A.10}$$

$$\frac{V_3 - V_4}{r_{n3}} - V_4\, g_{n3} = \frac{V_4}{r_{n5}} \tag{A.11}$$

$$\frac{V_3 - V_5}{r_{n4}} - V_5\, g_{n4} = \frac{V_5}{r_{n6}} \tag{A.12}$$

$$V_1\, g_{p1} + \frac{V_1 - V_6}{r_{p1}} = \frac{V_6 - V_7}{r_{n7}} - V_7\, g_{n7} \tag{A.13}$$

$$\frac{V_6 - V_7}{r_{n7}} - V_7\, g_{n7} = V_6\, g_{n9} + \frac{V_7}{r_{n9}} \tag{A.14}$$

$$-V_8\, g_{n8} - \frac{V_8 - V_{out}}{r_{n8}} = V_6\, g_{n10} + \frac{V_8}{r_{n10}} \tag{A.15}$$

$$V_2\, g_{p2} + \frac{V_2 - V_{out}}{r_{p2}} = -V_8\, g_{n8} - \frac{V_8 - V_{out}}{r_{n8}} \tag{A.16}$$

A.3.2 Noise Transimpedance

By solving for the transimpedance from the transistor to the output seen by each noise current source, the output-referred noise voltage can be calculated. Examining Table A.5, it can be seen that only six transistors contribute significantly to the output noise. These transistors are also mirrored in each half circuit. By examining the half circuit small signal models it can be seen that MN2, MP4/6 and MN10 (and the mirrored counter parts MN1, MP3/5 and MN9) all see the output impedance of the op-amp providing the largest amplification of the noise. All the other transistors see significantly lower impedances thus making their noise contributions negligible.

This allows for the total output referred noise contributed to be summarized into a reduced equation:

$${V_{N_{out}}}^2 = 2 \cdot {R_{out}}^2 \cdot ({I_{n_{N2}}}^2 + {I_{n_{N10}}}^2 + 2 \cdot {I_{n_{P4}}}^2) \tag{A.17}$$

Transistor	Input Current Noise @ 1kHz $[pA/\sqrt{Hz}]$	Input Current Noise @ 100kHz $[pA/\sqrt{Hz}]$	Transimpedance $[M\Omega]$	Output Referred Noise Voltage @ 1kHz $[\mu V/\sqrt{Hz}]$
N1	3.298	0.609	130.324	429.764
N2	3.298	0.609	130.324	429.764
N3	3.296	0.608	≈ 0	≈ 0
N4	3.296	0.608	≈ 0	≈ 0
N5	3.297	0.613	0.026	0.086
N6	3.297	0.613	0.026	0.086
N7	3.306	0.608	0.684	2.261
N8	3.306	0.608	0.684	2.261
N9	3.307	0.614	131.605	435.166
N10	3.307	0.614	131.658	435.341
P1	1.726	0.584	1.991	3.437
P2	1.726	0.584	1.992	3.439
P3	2.102	0.816	130.298	273.830
P4	2.102	0.816	130.350	273.941

Table A.5: Input noise magnitudes, transimpedance gain and output-referred noise voltage of each transistor in the FCC op-amp

where ${I_{n_{xx}}}^2$ is the sum of the flicker and thermal noise sources. Eq. A.17 is divided by ${A_v}^2$ to input refer the noise PSD. Substituting $A_v = R_{Out} \cdot g_{m_{N2}}$ results in:

$$ {V_{N_{in}}}^2 = \frac{2}{{g_{m_{N2}}}^2} \cdot ({I_{n_{N2}}}^2 + {I_{n_{N10}}}^2 + 2 \cdot {I_{n_{P4}}}^2) \tag{A.18} $$

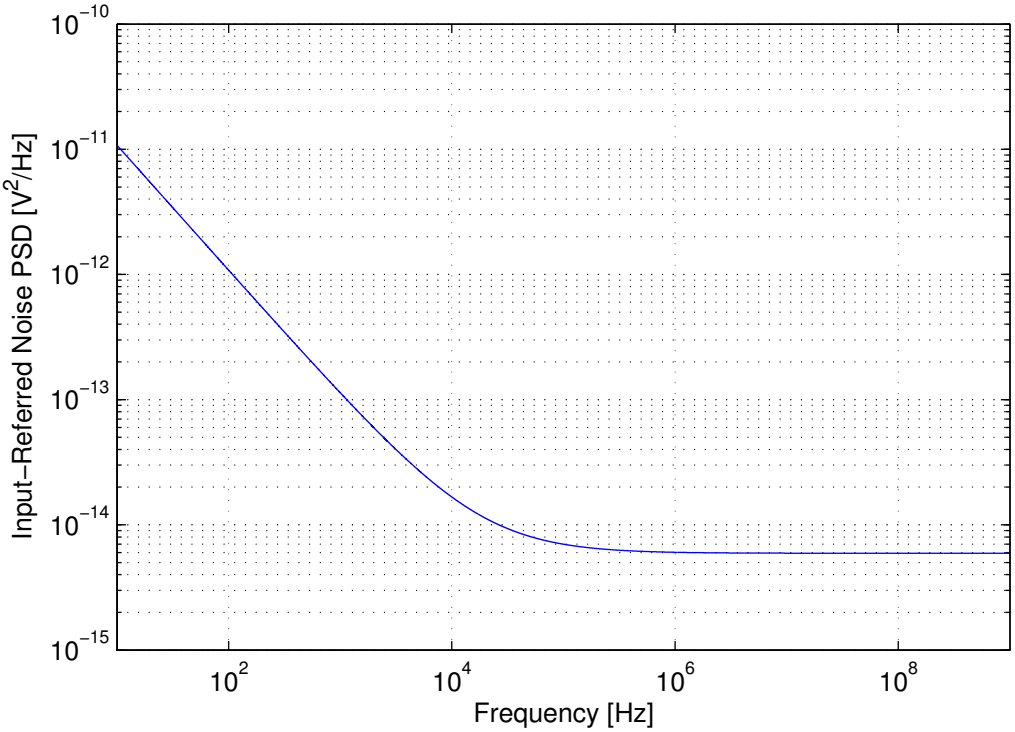


Figure A.8: Calculated input-referred noise voltage PSD of FCC op-amp accounting for both shot and flicker noise.

Appendix B

LED Power Calculations

B.1 LED Power Calculations

To convert from lumens or candelas to watts is not a straight forward calculation. Lumens are mapped to the responsivity of the human eye and thus green LEDs are more lumeniant that blue or red LEDs.

Lumens are roughly the equivalent of total power emitted by a source. Candelas can be though of as an angular power density. As we are operating in three dimensions steradians are used instead of radians.

To get the candela for an LED you simply divide the lumenous intensity by the solid viewing angle of the LED.

$$I_v[cd] = \frac{\Phi_v[lm]}{\Omega[sr]} \tag{B.1}$$

To get the solid angle of an LED in steradians, you apply the following equation, where θ is the viewing angle of the LED.

$$\Omega = 2 * \pi * (1 - cos(\theta/2))[sr] \tag{B.2}$$

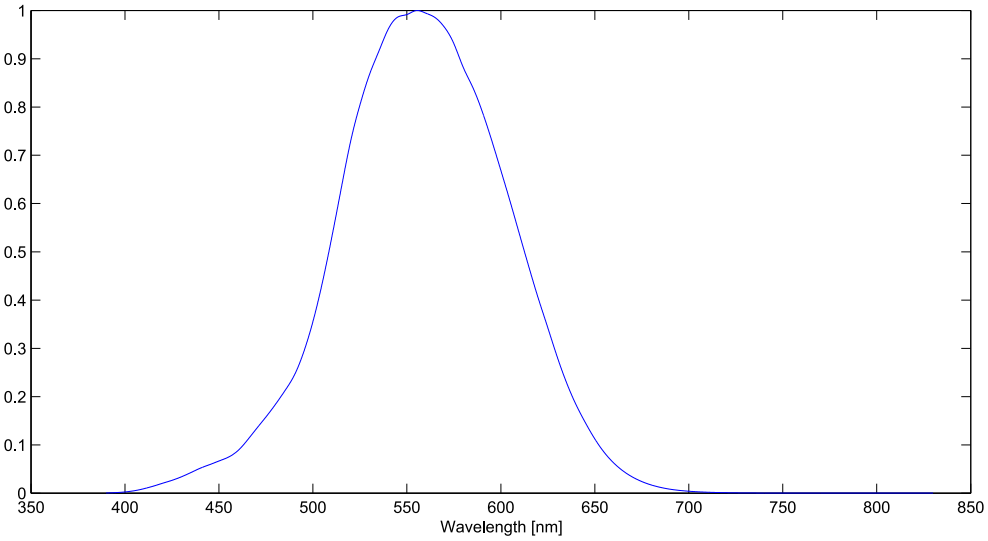


Figure B.1: Luminosity function

To convert between candelas and watts per steradians the luminosity function is used. The function is as follows:

$$I_v[cd] = I_e[w/sr] * 683 * y(\lambda) \tag{B.3}$$

Where $y(\lambda)$ is the function which describes the sensitivity of the human eye. The equation and data was derived by *Sharpe, Stockman, Jagla & Jaegle (2005) 2-deg V*(l) luminous efficiency function.*

B.1.1 Sample Calculations

To verify the calculations we will take an LED datasheet and attempt to reproduce the quoted values. We will use a blue LED from SuperBrightLEDs. The following is the

specified values of the LED:

$$\begin{aligned}
\Phi_v &= 0.5lm \\
\theta &= 30^o \\
I_v &= 2400mcd \\
\lambda &= 470nm \\
P &= 8.58mW
\end{aligned}$$

Can demonstrate the conversion between lumens and millicandelas:

$$\begin{aligned}
\Omega &= 2 * \pi * (1 - cos(\theta/2)) \\
&= 2 * \pi * (1 - cos(30^o/2)) \\
&= 0.214[sr]
\end{aligned}$$

$$\begin{aligned}
I_v &= \frac{\Omega}{\Phi_v} \\
&= 0.5/0.214 \\
&= 2336mcd
\end{aligned}$$

This is within the round off error the specifications.

If we look to convert the lumins to watts, we can use Equation B.3. By cancelling off the steradians from either side we get:

$$
\begin{aligned}
I_v[cd] &= \frac{\Phi_v[lm]}{\Omega[sr]} \\
I_e &= \frac{P[W]}{\Omega[sr]} \\
I_v[cd] &= I_e[W/sr] * 683 * y(\lambda) \\
P &= \Phi_v * \frac{1}{683 * y(\lambda)} \\
P &= 13.7mW
\end{aligned}
$$

It is unclear from the data sheet what values are measured and what values are calculated however this value is close enough to be usable for our purposes.

B.2 LED Power Specifications

In order for an LED to illuminate to the same intensity of a laser, the LED must apply the equivalent of $290\mu W$ onto the channel over an area of the spot size.

Assumptions about the laser:

$$
\begin{aligned}
P_{Laser} &= 290\mu W \\
r_{spot} &= 50\mu m
\end{aligned}
$$

First by converting the power of the laser into the equivalent lumins required from the

LED[1]:

$$\Phi_v = P_{Laser} * 683 * y(\lambda) \tag{B.4}$$
$$= 60mlm \tag{B.5}$$

Now to identify the candelas of the LED we must first find the angle in steradians which the LED would illuminate onto the channel. This becomes a function of height which we will parameterize as h, resulting in:

$$\Omega[sr] = 2 * \pi * (1 - cos(\frac{\theta}{2})) \tag{B.6}$$
$$= 2 * \pi * (1 - \frac{h}{\sqrt{h^2 + r^2}}) \tag{B.7}$$

Now to map to the LED candela rating:

$$I_{v_{LED}}[cd] = \frac{\Phi_v}{\Omega[sr]} \tag{B.8}$$
$$= \frac{\Phi_v}{2 * \pi * (1 - \frac{h}{\sqrt{h^2+r^2}})} \tag{B.9}$$

By assuming that the LED will be within 1mm of the channel, we get and approximate value of the candela rating:

[1]We will assume that the Luminosity Function ($y(\lambda)$) for our LED is approximately 0.3 (around 500nm), which will give us a high estimate our the power requirement

$$
\begin{aligned}
I_{v_{LED}}[cd] &= \frac{\Phi_v}{2 * \pi * (1 - \frac{h}{\sqrt{h^2+r^2}})} \\
&= \frac{60mcd}{2 * \pi * (1 - \frac{1mm}{\sqrt{(1mm)^2+(50\mu m)^2}})} \\
&= 7.6538cd
\end{aligned}
$$

Thus we require for a LED with a wavelength around 500nm to produce a candela rating of 7700mcd. A quick search online has identified multiple sources for such LEDs. However it does appear that such high candela rating does require the larger 5mm diameter LEDs. Brighter LEDs do exist however these tend to require heat sinks and dramatically more current, on the order of 700mA-1A, which is beyond our power budget.

Possible suppliers are:

Vendor	Part #	λ	$I_{v_{LED}}$	Price [$/each]
SuperBrightLEDs	RL5-A7032	507nm	7000mcd	$0.54
Digikey	754-1607-ND	505nm	12000mcd	$0.72
Digikey	516-2275-1-ND	470nm	9600mcd	$1.45

Table B.1: Possible Suppliers of LEDs for Excitation

B.3 OLED Power Calculations

A typical OLED will quote its optical output in terms of candelas per m^2. To convert this into a power intensity the following conversions must take place:

$$
P_{OLED} = \frac{A_{OLED} \cdot \rho_{OLED} \cdot \Omega}{683 \cdot y(\lambda)} = \frac{40000\mu m^2 \cdot 1000[cd/m^2]1.84[sr]}{683 \cdot 1} = 15nW \tag{B.10}
$$

Appendix C

Verification of Approach

To test to ensure my methods are accurate, I designed and compared the hand calculations and simulations of a simple common source amplifier (Figure C.1). The only noise source in this circuit would be the resistor and nmos transistor. The nmos transistor will have two sources of noise: Flicker and Thermal. The Thermal noise at low frequencies is characterized by the following equation taken from the AMS process documentation:

$$I_n{}^2 = \frac{8}{3} \cdot k \cdot T \cdot (g_m + g_{ds} + g_{mb}) \tag{C.1}$$

The flicker noise can be similarly characterized by:

$$I_n{}^2 = \frac{K_f \cdot I_d{}^{AF}}{C_{ox} \cdot w \cdot l} \cdot \frac{1}{f} \tag{C.2}$$

The gain of this amplifier is described by:

$$A_v = g_m * (r_o || R) \tag{C.3}$$

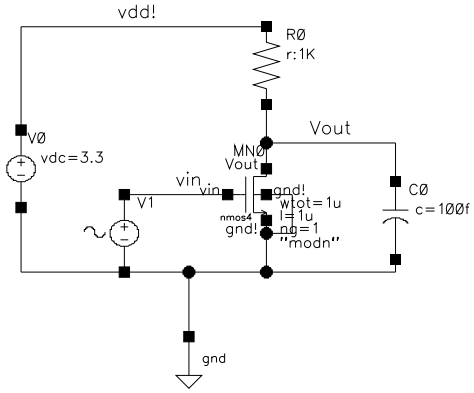


Figure C.1: Common source amplifier circuit to verify hand calculations

Performing a DC analysis, the transistor parameters are:

$$
\begin{aligned}
g_m &= 92.79\mu mho \\
g_{ds} &= 326nmho \\
g_{mb} &= 23\mu mho \\
K_f &= 2.17 \cdot 10^{-26} \\
AF &= 1.507 \\
i_d &= 60.69\mu A \\
l &= 1\mu m \\
k &= 1.38 \cdot 10^{-26} \\
C_{ox} &= 4.54 \cdot 10^{-3} \\
T &= 300^o K
\end{aligned}
$$

The output referred noise generated by the transistor can be described by:

$$V_{n_{Output}} = I_n \ (r_o \ || \ R) \tag{C.4}$$

The input referred noise can be calculated by simply dividing the output referred noise by

	Hand Calculated		Simulated	
Referred Direction	Flicker Noise	Thermal Noise	Flicker Noise	Thermal Noise
Output $[\frac{V^2}{Hz}]$	$2.11 * 10^{-14}$	$1.28 * 10^{-18}$	$5.37 * 10^{-14}$	$1.27 * 10^{-18}$
Input $[\frac{V^2}{Hz}]$	$2.45 * 10^{-12}$	$1.49 * 10^{-16}$	-	-
A_v	$92.8mV/V$		$92.1mV/V$	

Table C.1: Results comparison between the hand calculated values and the simulated values.

the gain of the circuit:

$$V_{n_{Input}} = \frac{V_{n_{Output}}}{A_v} \tag{C.5}$$

Based off the results shown in Table C.1 it appears that the thermal noise hand calculations are very close to the expected output referred noise. The flicker noise however doesn't seem to present the same level of accuracy. In AMS noise parameter documentation, it is mentioned that the flicker noise is calculated using a high order function, not provided by the document. This suggests that the accuracy of the flicker noise hand calculation may vary dramatically from the simulated value. The gain was nearly perfectly predicted by the hand calculations.

Appendix D

Derivation of CTIA Transimpedance Function

The transfer function of the CTIA shown in Figure 3.2, is derived by starting with KCL at the inverting terminal of the op-amp. If we assume that the photodiode can simply be modelled as a capacitor (C_{PD}) in parallel with a current source ($I_{PD}(t)$), the node equation becomes:

$$I_{PD}(t) + C_{PD} \cdot \frac{dV_{PD}}{dt} = C_{int} \cdot \frac{d(V_{int} - V_{PD})}{dt} \tag{D.1}$$

Using circuit linearity, V_{off} can be thought of as a ground. Thus the op-amp gain equation will be:

$$V_{int}(s) = A(s)(0 - V_{PD}(s)) \tag{D.2}$$

The circuit will be in this state from $t_1 = t_0 + k \cdot T_s$ to $t_2 = t_0 + k \cdot T_s + T_{int}$ where $k \in Z$. This allows for the integration to be setup to be:

$$\int_{t1}^{t2} I_{PD}(t)dt + C_{PD} \cdot V_{PD}(t) = C_{int} \cdot (V_{int}(t) - V_{PD}(t)) \tag{D.3}$$

Examining the limits of the integration, this is the equivalent of the indefinite integral of:

$$\int_{t1}^{t2} I_{PD}(t)dt = \int I_{PD}(t) \cdot [u(t-t_1) - u(t-t_2)]dt \tag{D.4}$$

$$= \int I_{PD}(t) \cdot [u(t-(t_0 + k \cdot T_s)) - u(t-(t_0 + k \cdot T_s + T_{int}))]dt \tag{D.5}$$

Using the definition of convolution of:

$$f(t) * g(t) \equiv \int f(\tau) \cdot g(t-\tau) \cdot d\tau \tag{D.6}$$

Eq. D.3 becomes:

$$I_{PD}(t) * [u(t-t_1) - u(t-t_2)] + C_{PD} \cdot V_{PD}(t) = C_{int} \cdot (V_{int}(t) - V_{PD}(t)) \tag{D.7}$$

Taking Eq. D.7 into the frequency domain:

$$\frac{I_{PD}(s)}{s} \cdot \left[e^{-s \cdot t_1} - e^{-s \cdot t_2}\right] = C_{int} \cdot (V_{int}(s) - V_{PD}(s)) - C_{PD} \cdot V_{PD}(s) \tag{D.8}$$

Then by substituting Eq. D.2 into Eq. D.8 and doing some basic manipulation

$$\frac{I_{PD}(s)}{s} \cdot \left[e^{-s \cdot t_1} - e^{-s \cdot t_2}\right] = V_{int}(s) \left(C_{int} + \frac{C_{PD} + C_{int}}{A(s)}\right) \tag{D.9}$$

The subtracted complex exponentials result in a sine:

$$\begin{aligned} e^{-s \cdot t_1} - e^{-s \cdot t_2} &= e^{-s \cdot (t_0 + k \cdot T_s)} - e^{-s \cdot (t_0 + k \cdot T_s + T_{int})} \\ &= e^{-s \cdot (t_0 + k \cdot T_s)}(1 - e^{-s \cdot T_{int}}) \\ &= e^{-s \cdot (t_0 + k \cdot T_s + T_{int}/2)}(e^{s \cdot T_{int}/2} - e^{-s \cdot T_{int}/2}) \end{aligned}$$

Then using Euler's Formula:

$$sin(x) = \frac{e^{jx} - e^{-jx}}{2j} \tag{D.10}$$

the exponentials can be manipulated to be:

$$e^{-s\cdot t_1} - e^{-s\cdot t_2} = e^{-s\cdot(t_0+k\cdot T_s+T_{int}/2)} \cdot \left(2j \cdot sin\left(\frac{s\cdot T_{int}}{2j}\right)\right) \tag{D.11}$$

Placing back into Eq. D.9 we get:

$$\frac{I_{PD}(s)}{s} \cdot e^{-s\cdot(t_0+k\cdot T_s+T_{int}/2)} \cdot \left(2j \cdot sin\left(\frac{s\cdot T_{int}}{2j}\right)\right) = V_{int}(s)\left(C_{int} + \frac{C_{PD}+C_{int}}{A(s)}\right) \tag{D.12}$$

When this is manipulated into the form of a transfer function the equation becomes:

$$\frac{V_{int}(s)}{I_{PD}(s)} = \frac{2j}{s\cdot\left(C_{int}+\frac{C_{PD}+C_{int}}{A(s)}\right)} \cdot e^{-s\cdot(t_0+k\cdot T_s+T_{int}/2)} \cdot sin\left(\frac{s\cdot T_{int}}{2j}\right) \tag{D.13}$$

$$\frac{V_{int}(f)}{I_{PD}(f)} = \frac{2j}{j2\pi f\cdot\left(C_{int}+\frac{C_{PD}+C_{int}}{A(f)}\right)} \cdot e^{-j2\pi f\cdot(t_0+k\cdot T_s+T_{int}/2)} \cdot sin\left(\frac{j2\pi f\cdot T_{int}}{2j}\right) \tag{D.14}$$

$$= \frac{1}{\pi f\cdot\left(C_{int}+\frac{C_{PD}+C_{int}}{A(f)}\right)} \cdot e^{-j2\pi f\cdot(t_0+k\cdot T_s+T_{int}/2)} \cdot sin\left(\pi f\cdot T_{int}\right) \tag{D.15}$$

Then using the definition of a sinc:

$$sinc(x) = \frac{sin(\pi\cdot x)}{\pi\cdot x} \tag{D.16}$$

where $x = f\cdot T_{int}$. Eq. D.15 becomes:

$$\frac{V_{int}(f)}{I_{PD}(f)} = \frac{T_{int}}{C_{int}+\frac{C_{PD}+C_{int}}{A(f)}} \cdot e^{-j2\pi f\cdot(t_0+k\cdot T_s+T_{int}/2)} \cdot sinc\left(f\cdot T_{int}\right) \tag{D.17}$$

When examining Eq. D.17 in order for the signal to be maximized the resulting phase of $V_{int}(f)$ must be zero. By setting $k=0$ and $t_0=0$, the input phase of $I_{PD}(f)$ must be:

$$\phi_{I_{PD}} = \pi f\cdot T_{int} \tag{D.18}$$

When the op-amp gain isn't assumed to be large with infinite bandwidth there is a pole added to the magnitude profile:

$$\frac{V_{int}(f)}{I_{PD}(f)} = \frac{T_{int}}{C_{int} + \frac{C_{PD}+C_{int}}{A(f)}} \cdot sinc\left(f \cdot T_{int}\right) \tag{D.19}$$

When Eq. 3.3 is placed in Eq. D.19 the pole location can be identified:

$$\frac{V_{int}(f)}{I_{PD}(f)} = \frac{T_{int} \cdot A(f)}{C_{int} \cdot A(f) + C_{PD} + C_{int}} \cdot sinc\left(f \cdot T_{int}\right) \tag{D.20}$$

$$= \frac{T_{int} \cdot A_o}{C_{int} \cdot A_o + (C_{PD} + C_{int}) \cdot (1 + \frac{j \cdot f}{f_{3dB}})} \cdot sinc\left(f \cdot T_{int}\right) \tag{D.21}$$

Setting the denominator to zero:

$$0 = C_{int} \cdot A_o \cdot f_{3dB} + (C_{PD} + C_{int}) \cdot (1 + \frac{j \cdot f}{f_{3dB}}) \tag{D.22}$$

$$0 = C_{int} \cdot A_o \cdot f_{3dB} + (C_{PD} + C_{int}) \cdot (f_{3dB} + j \cdot f) \tag{D.23}$$

$$-C_{int} \cdot A_o \cdot f_{3dB} = (C_{PD} + C_{int}) \cdot (f_{3dB} + j \cdot f) \tag{D.24}$$

$$\frac{-C_{int} \cdot A_o \cdot f_{3dB}}{(C_{PD} + C_{int})} = (f_{3dB} + j \cdot f) \tag{D.25}$$

$$\frac{-C_{int} \cdot A_o \cdot f_{3dB}}{(C_{PD} + C_{int})} - f_{3dB} = j \cdot f \tag{D.26}$$

This results in a pole located at approximately:

$$f \approx \frac{C_{int} \cdot A_o \cdot f_{3dB}}{(C_{PD} + C_{int})} \tag{D.27}$$

which is a scaled version of the unity gain frequency of the op-amp located at approximately $f = A_o \cdot f_{3dB}$. As C_{int} and C_{PD} are of roughly the same scale, the unity gain frequency is moved only slightly. As C_{PD} becomes larger then C_{int} however, the corner frequency drops. This may influence the SNR of the system as C_{PD} is coupled with the area of the photodiode and therefore amplitude of the signal.

As is described by Xu and Yuan [68], the 3dB frequency of the sinc function is located at $0.44/T_{int}$. Assuming that:

$$\frac{0.44}{T_{int}} \ll \frac{C_{int} \cdot A_o \cdot f_{3dB}}{(C_{PD} + C_{int})} \tag{D.28}$$

the higher order pole does not significantly influence the result. Thus, $A(f)$ can be assumed to be large for all frequencies.

To look strictly at the magnitude response the phase modifying term can be dropped. By doing so Eq. D.17 comes back to the common form of integrator equation:

$$\left\| \frac{V_{int}(f)}{I_{PD}(f)} \right\| = \left\| \frac{T_{int}}{C_{int}} \cdot sinc\left(f \cdot T_{int}\right) \right\| \tag{D.29}$$

Appendix E

OR1 PCB Datasheet

E.1 PCB Design

A Printed Circuit Board (PCB) was designed for the purpose of testing and verification of the OR1 chip. The control signalling and USB interface was provided through an Opal Kelly XEM6010-LX45 FPGA board which attached to the bottom of the OR1 Board.

E.2 PCB Calibration

E.2.1 Measuring ADC SNR

To measure the SNR of the ADC the standard practice is to apply a sine wave and measure the take the FFT of the recorded signal. The sine wave needs to be of a frequency such that its frequency is a integer multiple of the bin frequency of the recording. Additionally, the number of samples needs to be a value of 2^n, where n is a positive integer. [69]

$$F_{Bin} = \frac{F_s}{N_{Samples}} \tag{E.1}$$

$$F_{Sine} = N_{Prime} F_{Bin} \tag{E.2}$$

E.2.2 ADC Quantization Noise

To test the ADC influence of the ADC quantization noise a recording was first made using the DAC generating a 23.84 Hz sine wave which was recorded by the AD7985 16-bit ADC. The ADC recorded 32768 samples at a frequency of 13.7kHz. This provided a coherent recording of the sine wave.

The SNR of this recording was measured by first measuring the total power of the signal in the frequency domain and then removing the 23.84 Hz tone by setting the point in the spectrum to equal the data point prior to it (i.e. in MATLAB data(2,58) = data(2,57)) and remeasuring the power. From this the SNDR can be calculated as follows:

$$SNDR = 10\ log_{10}\left(\frac{P_{sine}}{P_{SineRemoved}}\right) \tag{E.3}$$

The SNDR was measured for the data points with increasing level of quantization. This was implemented by setting the lower significant bits to 0 and then recalculating the SNDR for an increasing number of bits. The this produced a profile seen in Figure E.1.

The quantization noise of a sine wave is well characterized and is known to have the power of:

$$\sigma^2 = \left(\frac{V_{Max}}{2^{N_{ADC}}}\right)^2 \frac{1}{12} \tag{E.4}$$

When the quantization noise is increased, at some point it becomes the dominant noise source and the other noise in the system becomes insignificant. This will occur at the point where the SNDR drops 3dB below the maximum SNDR. The recording used to generate

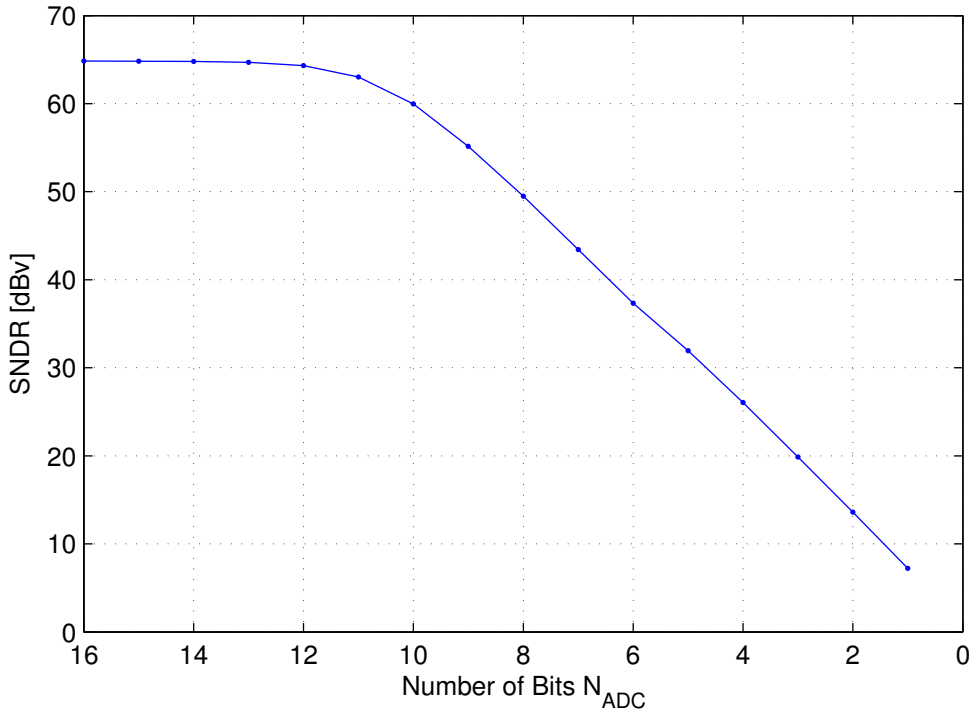


Figure E.1: SNR vs Quantized ADC values

Figure E.1 demonstrates this point at $N_{ADC} = 11$. This means that the other noise in measurement is approximately:

$$\sigma^2 = \frac{3.3^2}{2^{2*11}\ 12} = 2.16 * 10^{-7} V^2 \tag{E.5}$$

$$\sigma = 465 \mu V_{RMS} \tag{E.6}$$

E.2.3 DAC Quantization Noise

Similar to the ADC Quantization noise, the DAC introduces quantization noise by only being able to generate discrete voltage levels. By manipulating the level of quantization there will be a point at which the quantization noise becomes dominant over the other noise in the measurement. At the point where the SNR drops by 3dB the quantization noise is equal to the other noise in the system. Using the noise measured in Section E.2.2 the theoretical SNR profile can be plotted Figure E.2.

A 16-bit AD5060 DAC was used to generate the sine wave. The FPGA sequentially shifted the DAC values over SPI providing a sine wave frequency of 23.84Hz. To adjust the quantization noise level, the DAC values were logically "and'd" with a quantization register forcing specific bits of the DAC levels to 0. The level of quantization was sequentially dropped from 16 bits down to 1 bit. The signal level was measured as the standard deviation of the raw signal.

The theoretical SNR profile matched fairly closely to the measured values. The discrepancy for bits 16 to 12 suggests that introduced noise is somewhat higher than $465 \mu V$. The 3dB occurred around 10-bits providing an estimated total noise of:

$$\sigma^2 = \frac{3.3^2}{2^{2*10}\ 12} = 8.65 * 10^{-7} V^2 \tag{E.7}$$

$$\sigma = 930 \mu V_{RMS} \tag{E.8}$$

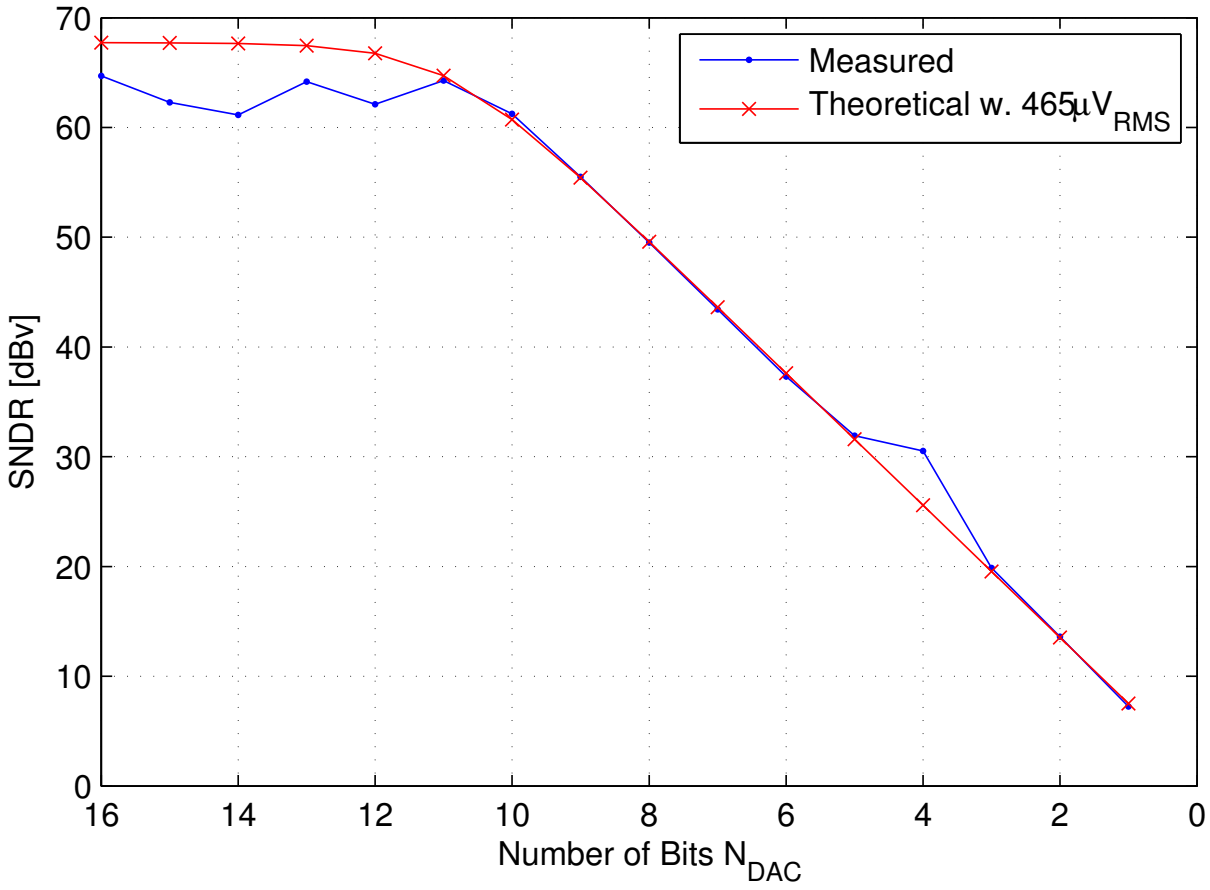


Figure E.2: SNR as a function of the quantization of the DAC output signals.

E.2.4 Optical Characterization

To properly test the circuits design in the previous section, an known optical light source needs to be used. To do this a green LED (Kingbright APTL3216ZGC) is driven by a NPN (2N3904) transistor connected to a low noise DAC (Analog Devices AD5450). The driving circuit was selected for its low noise from an Analog Devices Application Note [70]. This circuit is implemented on a separate PCB from the OR1 and discrete integrator such that it can be mounted directly above the OR1 and discrete photodiode.

To verify the LED intensities a photodiode (Edmunds Optics PD-NT53 372) of known area and responsivity is used. The photodiode active area is circular having a total area of $3.2mm^2$. The responsivity at 500nm is 0.3 A/W.

LED Intensity

The Kingbright LED is specified to have a intensity of 1.1cd at 25mA and a viewing angle of 70^o. The LED PCB is mounted approximately 25.4mm above the discrete photodiode which will be used to calibrate the intensity. As the photodiode is known to have a radius of 1mm the viewing angle of the photodiode with respect to the LED is described by:

$$\theta = tan^{-1}\left(\frac{r_{PD}}{h}\right) \tag{E.9}$$

To covert this viewing angle into the steradians the following transformation can be applied:

$$\Omega = 2\pi(1 - cos\theta) \tag{E.10}$$

Finally to convert from candelas to watts the following conversion can be applied:

$$I_{Watts} = \frac{I_{cd} \cdot \Omega}{638 \cdot 0.8} \tag{E.11}$$

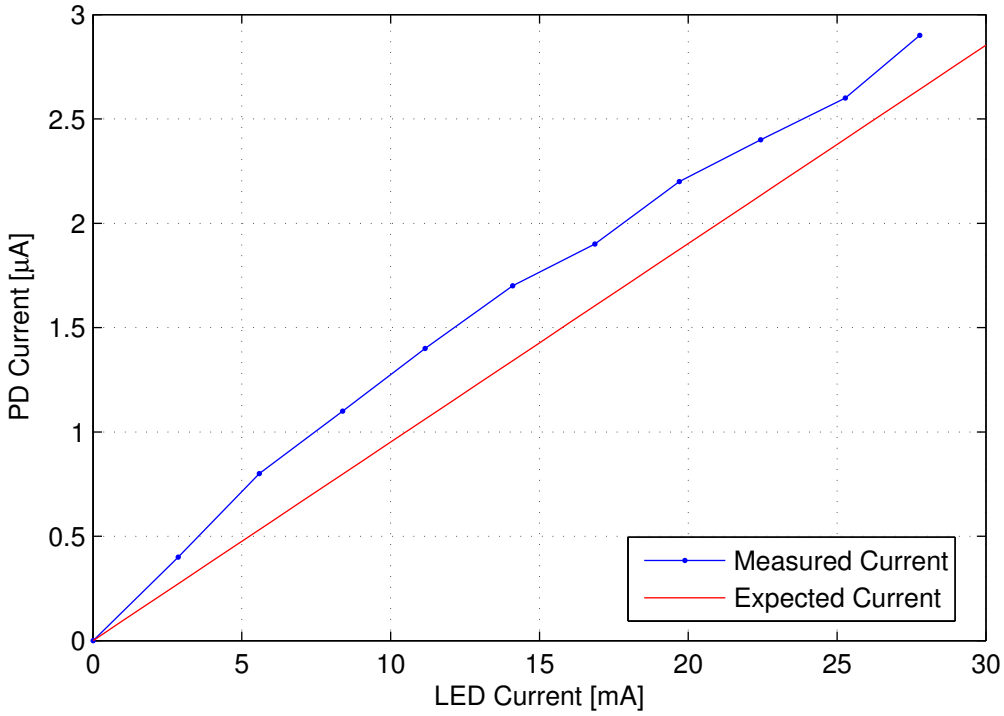


Figure E.3: Relationship between photodiode current and the LED drive current.

Giving an approximate light intensity of $I_{Watts} = 7.9\mu W$ which would result in a photodiode current of $2.38\mu A$ for an LED driven at 25mA.

This light intensity is a linear function of the current driven through the LED. To validate the LED intensity and the photodiode responsivity, the LED drive was swept and the photodiode current was measured using an Agilent U3606A DMM (Figure E.3). The linear relationship as a function of LED current was observed. A systematic error was observed which can be explained by error in the LED height, horizontal alignment and true intensity[1]. Additional quantization error is introduced by the DMM as the measurement was limited by the two least significant figures of the display.

This means that we'd expect an output intensity of $2.47mW/m^2$ at 25mA. This is $0.0986W/(A \cdot m^2)$

[1]The LED datasheet specifies the intensity to be correct within 15%

LED Stability

The DAC at max counts output 617 mV. The specified noise value of the drive circuit is $2.42\mu V_{RMS}$ [70]. This gives us an expected SNR of 108 dB. This is sufficiently stable that it is an insignificant source of noise for the photodiode.

E.3 FPGA Memory Map

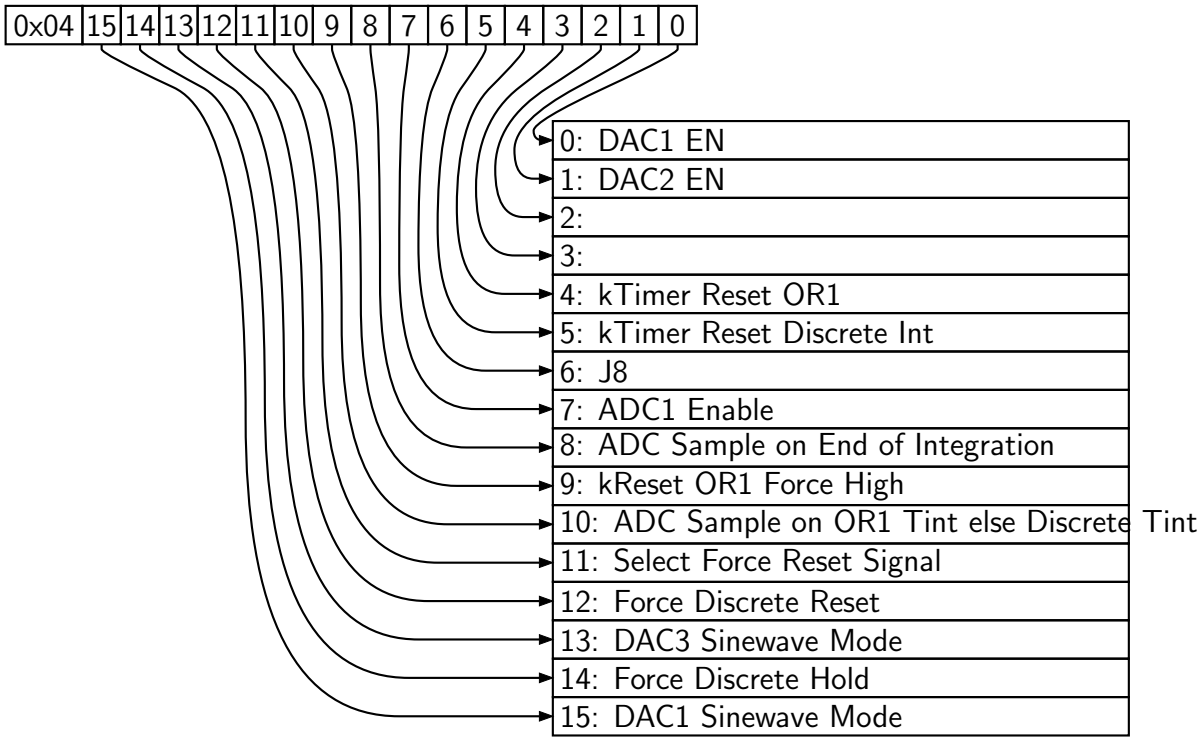


Figure E.4: Memory map of OR1 control register.

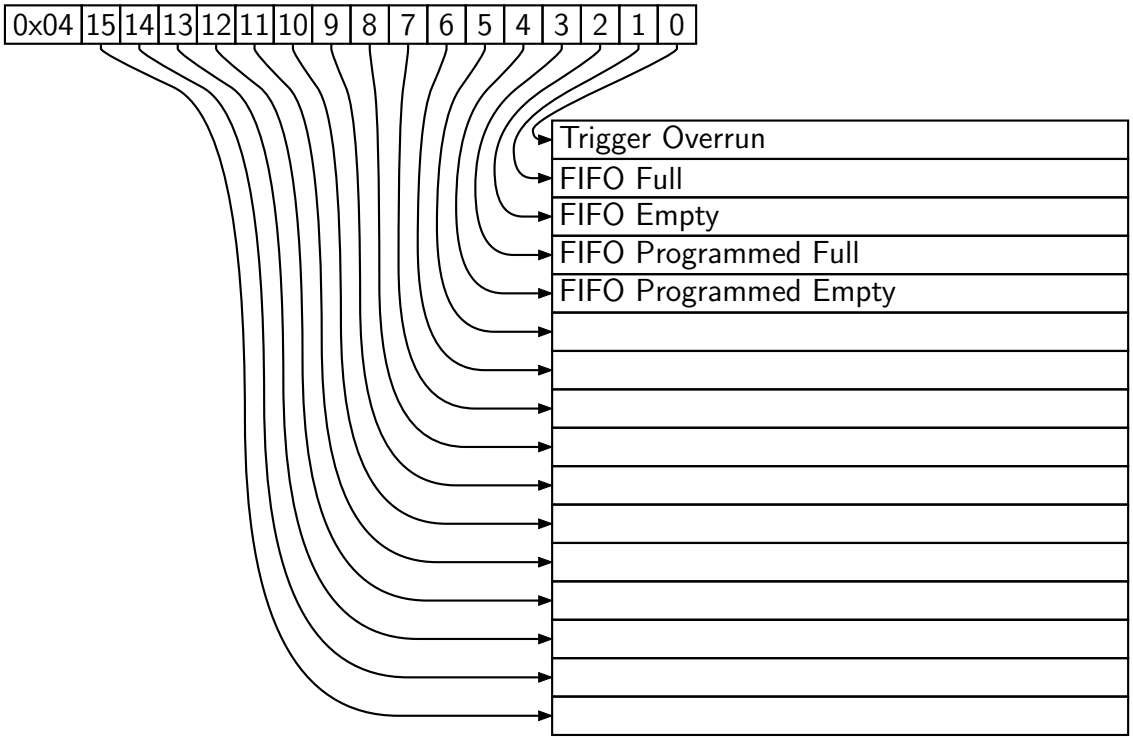


Figure E.5: Register map of OR1 Status register

Appendix F

Light Collection Efficiency Calculation

Integration of a photodiode into a microfluidic chip is thought to increase the sensitivity of the optical detection of fluorescence. The idea is that as proximity of the photodiode increases, no collection optics will be required to direct the light onto the photodiode.

F.1 Derivation

The nature of an isotropic light source dictates that the power emitted from the source will be distributed over the total area of a sphere with the point source at the centre. Beginning with the total surface area of a sphere:

$$SA = 4\pi r^2 \tag{F.1}$$

This can be used to identify the total intensity of light on the surface of the sphere:

$$I = \frac{P_{total}}{SA} = \frac{P_{total}}{4\pi r^2} \tag{F.2}$$

We can now integrate the intensity over the surface of a photodiode to identify the total power collected by the photodiode. If we assume a circular photodiode with a radius w, at a distance h from the point source, the intensity can be easily integrated over the surface area of the photodiode (Figure 2.3a).

This produces the following integration:

$$P_{collected} = \int_{\pi-A}^{\pi}\int_{0}^{2\pi} Ir^2 sin(\phi)d\theta d\phi \tag{F.3}$$

$$= \frac{P_{total}}{4\pi}\int_{\pi-A}^{\pi}\int_{0}^{2\pi} sin(\phi)d\theta d\phi \tag{F.4}$$

$$= \frac{P_{total}2\pi}{4\pi}\int_{\pi-A}^{\pi} sin(\phi)d\phi \tag{F.5}$$

$$\frac{P_{total}}{2}(-cos(\pi) + cos(\pi - A)) \tag{F.6}$$

$$\frac{P_{total}}{2}(1 + cos(A)) \tag{F.7}$$

From geometry (Figure 2.3a) it can be seen that:

$$cos(A) = \frac{h}{\sqrt{h^2 + r^2}} \tag{F.8}$$

When this is substituted in:

$$P_{collected} = \frac{P_{total}}{2}\left(1 - \frac{h}{\sqrt{h^2 + r^2}}\right) \tag{F.9}$$

The light collection efficiency is by definition:

$$LCE \equiv \frac{P_{collected}}{P_{total}} \tag{F.10}$$

Therefore for a circular photodiode:

$$LCE = \frac{1}{2}\left(1 - \frac{h}{\sqrt{h^2 + r^2}}\right) \tag{F.11}$$

F.2 Analysis

This analysis gives a unique perspective on how geometry interplays with the light collection of isotropic light sources. By plotting the LCE logarithmically with the height of the isotropic light source, a strong argument can be gained for the advantages of integration.

Figure 3 - LCE of 150?m diameter photodiode When the channel distance to the photodiode is approximately the same order of magnitude in size as the distance to the channel, there is a rapid increase in the light collection efficiency. This shows an interesting number for our current TTK optics of a LCE of 4%. Alternatively, this same calculation can be used for sizing of a photodiode for a given process. Current estimates from DALSA provide a separation distance of $20\mu m$. This means that for a LCE of 40% requires a photodiode with a $200\mu m$ diameter.

F.3 Conclusion

Basic geometric analysis has provided a means to size a photodiode based on the distance from the channel. A rule of thumb is to provide a photodiode which is an order of magnitude larger than the separation distance. This will provide a large LCE without sacrificing too much surface area of the wafer.

Appendix G

CTIA Reset Interference

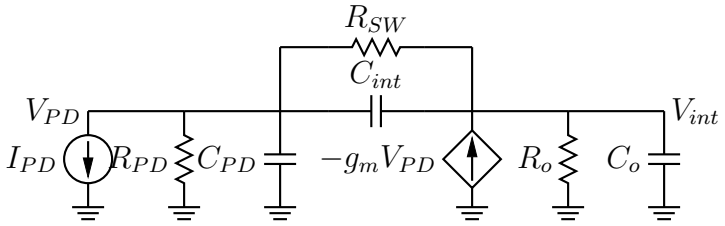


Figure G.1: Small signal model of the integrator during the reset phase of operation. R_o and C_o represent that output impedance of the op-amp. R_{SW} is the switch impedance of the transmission gate. R_{PD} and C_{PD} models the impedance of the photodiode. I_{PD} is the signal input from the photodiode.

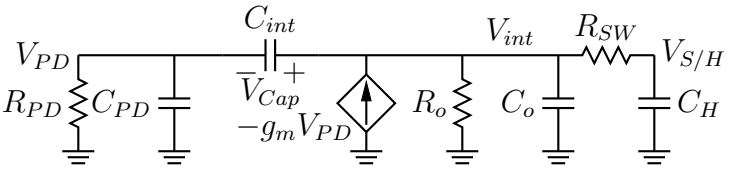


Figure G.2: Small signal model of the integrator during the integration phase of operation. The parameters remain the same as in Figure G.1 with the addition of C_H which is the capacitor the integrator output is sampled onto. The output buffer isn't shown here.

Reset Phase

First finding the value of the voltage sampled onto C_{int}. The KCL node equations are:

$$I_{PD}(f) + \frac{V_{PD}(f)}{Z_{PD}} = \frac{V_{Cap}(f)}{Z_{SW}} \tag{G.1}$$

$$\frac{V_{Cap}(f)}{Z_{SW}} + \frac{V_{Cap}(f) + V_{PD}(f)}{Z_o} = -g_m \cdot V_{PD}(f) \tag{G.2}$$

Where:

$$Z_o = R_o || \frac{1}{sC_o} \tag{G.3}$$

$$Z_{SW} = R_{SW} || \frac{1}{sC_{int}} \tag{G.4}$$

$$Z_{PD} = R_{PD} || \frac{1}{sC_{PD}} \tag{G.5}$$

$$V_{Cap}(f) = V_{int} - V_{PD}(f) \tag{G.6}$$

By manipulating (G.2), $V_{PD}(f)$ can be isolated:

$$V_{PD}(f) = -V_{Cap}(f) \left(\frac{\frac{1}{Z_{SW}} + \frac{1}{Z_o}}{g_m + \frac{1}{Z_o}} \right) \tag{G.7}$$

Placing (G.7) into (G.1) results in:

$$\frac{V_{Cap}(f)}{Z_{SW}} = I_{PD}(f) - \frac{V_{Cap}(f)}{Z_{PD}} \left(\frac{\frac{1}{Z_{SW}} + \frac{1}{Z_o}}{g_m + \frac{1}{Z_o}} \right) \tag{G.8}$$

which can be manipulated into:

$$\frac{V_{Cap}(f)}{Z_{SW}} + \frac{V_{Cap}(f)}{Z_{PD}} \left(\frac{\frac{1}{Z_{SW}} + \frac{1}{Z_o}}{g_m + \frac{1}{Z_o}} \right) = I_{PD}(f) \tag{G.9}$$

$$\frac{V_{Cap}(f)}{I_{PD}(f)} = \frac{Z_{SW} \cdot Z_{PD} \cdot (g_m \cdot Z_o \cdot +1)}{Z_o \cdot Z_{PD} \cdot g_m + Z_o + Z_{PD} + Z_{SW}} \tag{G.10}$$

Assuming the photodiode is of large impedance:

$$\frac{V_{Cap}(f)}{I_{PD}(f)} = \lim_{Z_{PD} \to \infty} \frac{Z_{SW} \cdot Z_{PD} \cdot (g_m \cdot Z_o \cdot +1)}{Z_o \cdot Z_{PD} \cdot g_m + Z_o + Z_{PD} + Z_{SW}} \tag{G.11}$$

$$\frac{V_{Cap}(f)}{I_{PD}(f)} = \lim_{Z_{PD} \to \infty} \frac{Z_{SW} \cdot (g_m \cdot Z_o \cdot +1)}{Z_o \cdot g_m + 1 + \frac{Z_o + Z_{SW}}{Z_{PD}}} \tag{G.12}$$

$$\frac{V_{Cap}(f)}{I_{PD}(f)} = Z_{SW} \tag{G.13}$$

which is the standard transimpedance amplifier equation.

Integration Phase

At the beginning of the integrate stage the voltage across the capacitor described by (G.10), is sampled and held for the duration of the integration period. Describing this in time domain is the equivalent of multiplying by a train of dirac functions and convolving with a rect function:

$$V'_{Cap}(t) = \sum_{k=-\infty}^{\infty} V_{Cap}(t) \cdot \delta(t - (t_0 + k \cdot T_s)) * rect\left(\frac{t}{T_{int}}\right) \tag{G.14}$$

For consistency, the prior notation will be used where $t1 = t_0 + k \cdot T_s$. Taking (G.14) into frequency domain:

$$V'_{Cap}(f) = \frac{T_{int} \cdot e^{-j2\pi f t_o}}{T_s} \cdot sinc(T_{int} f) \sum_{k=-\infty}^{\infty} V_{Cap}\left(f - \frac{k}{T_s}\right) \tag{G.15}$$

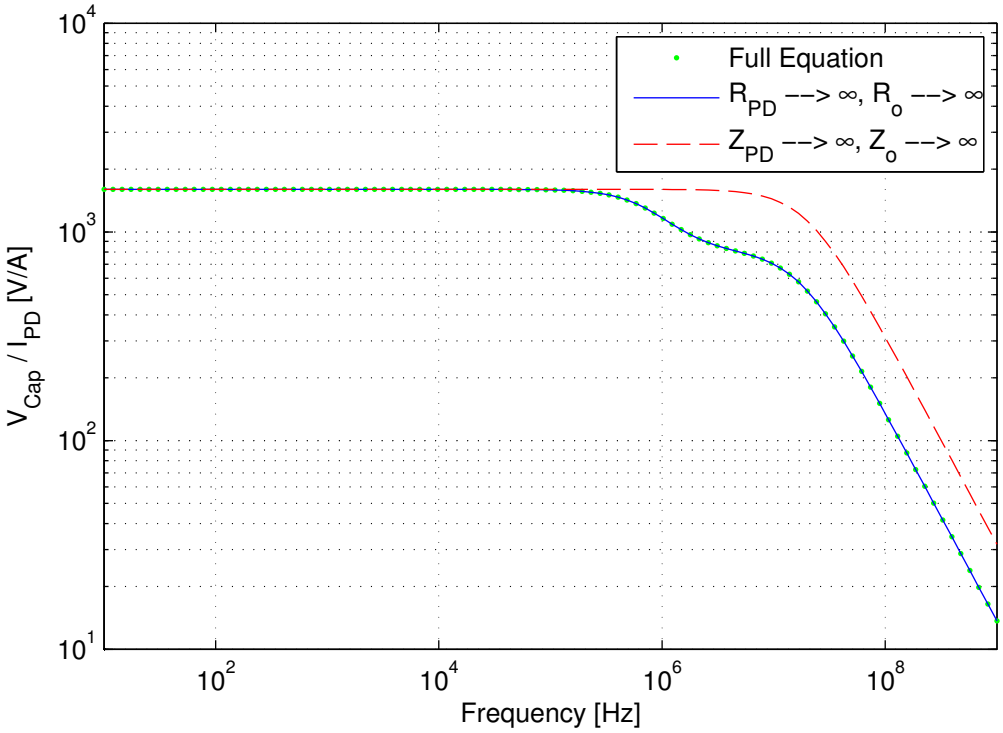


Figure G.3: Plot of various approximations of (G.10)

To refer this to the output, the transfer function from $V'_{Cap}(f)$ to $V_{out}(f)$ needs to be found. To do this it can be noted that the voltage dependent current sources output current can be described by:

$$i(s) = g_m \cdot (V'_{cap}(s) - V_{int}(s)) \tag{G.16}$$

If it's assumed that V_{PD} is driven to ground, the impedance that this current is driven through is described by:

$$Z_{eq} = \frac{R_o}{(1 + s(C_o + C_{int})R_o)(1 + sC_H R_{SW})(2 + s(C_o + C_{int})R_o + sC_h R_{SW})} \tag{G.17}$$

As a result:

$$V_{int}(s) = i(s) \cdot Z_{eq} \tag{G.18}$$

Manipulated, this becomes:

$$V_{int}(s) = g_m Z_{eq}(V'_{cap}(s) - V_{int}(s)) \tag{G.19}$$

$$= V_{cap}\frac{Z_{eq}g_m}{1 + Z_{eq}g_m} \tag{G.20}$$

As $V_{S/H}$ is a voltage divider of V_{int}, it can be found to be:

$$V_{S/H}(s) = \frac{V_{int}(s)}{1 + sR_{SW}C_H} \tag{G.21}$$

Which becomes:

$$V_{S/H}(s) = V'_{cap}(s)\frac{Z_{eq}g_m}{1 + Z_{eq}g_m} \cdot \frac{1}{1 + sR_{SW}C_H} \tag{G.22}$$

Meaning the final output is:

$$V_{S/H}(s) = \frac{Z_{eq}g_m}{1 + Z_{eq}g_m} \cdot \frac{1}{1 + sR_{SW}C_H}\frac{T_{int}}{T_s} \cdot sinc(T_{int}f) \sum_{k=-\infty}^{\infty} V_{Cap}\left(f - \frac{k}{T_s}\right) \tag{G.23}$$

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