Numerical Modeling of Flexible ZnO Thin-Film Transistors Using COMSOL Multiphysics

by

Chunyan Nan

A thesis
presented to the University of Waterloo
in fulfillment of the
thesis requirement for the degree of
Master of Applied Science
in
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2013

© Chunyan Nan 2013

AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

Increasing attention has been directed towards the development of optically transparent and mechanically flexible thin film transistors (TFTs) and associated circuits based on the transition metal oxides. These flexible see-through structures offer reduced weight, potential low-cost fabrication, and high performance compared to commonly used hydrogenated amorphous silicon (a-Si:H) in applications for large-area electronics and displays. As these emerging technologies evolve towards commercialization, a thorough investigation of the impacts of the thermo-mechanical stress and strain and their effects on the electrical and mechanical stability of the flexible microelectronic devices have become increasingly necessary. However, not much progress has been reported in this area, and the numerical modeling of the flexible transistors with the Finite Element Method (FEM) would provide unique insight to the design and operation of the flexible TFTs. In this thesis, numerical models of flexible TFTs are built up by COMSOL Multiphysics and compared with analytical models to reach the best agreement between the experimental measurements and the numerical analyses. These simulations provide additional insight into the local stress induced strain within the device due to both intrinsic and applied stress. It was shown that the thermal and mechanical impacts on the TFT performance can be reduced by placing the vital active layer of the flexible device near the neutral mechanical plane or by proper designing the device structure and processing conditions based on the data derived from the numerical models. The mathematical analysis and numerical simulation will be used to improve the electrical and mechanical performance and the reliability of the transistors for flexible applications.

Acknowledgements

I would like to express my sincere gratitude to my supervisor, Professor William Wong, for his guidance and support throughout my graduate studies. I am honored to have Professor Bo Cui and Professor Hany Aziz as my thesis readers.

I would also like to take this opportunity to acknowledge the following organizations for funding my research: Waterloo Institute for Nanotechnology (WIN), Toyota Motor Manufacturing Canada (TMMC), and University of Waterloo.

I am also very grateful to Professor Derek O. Northwood and Professor Randy Bowers for their continuous encouragement and support throughout my studies in Canada.

I wish to thank my dear friends, Xuan, Hai, Umar, Michael, Bright, and Scott, who were always there for me. Special thanks go to all my friends who accompanied me all the way and shared all the happy moments together.

Finally, I would like to show my appreciation to the University of Waterloo for its friendly environment and resourceful research facilities during my research.

Dedication

This thesis is dedicated to my beloved parents, whose endless love, encouragement, and moral support have been steadfast throughout my life and educational journey.

Also, this thesis is dedicated to my dearest grandmother, who loves me most and always praying for my success and happiness in my life.

Finally, this thesis is dedicated to my lovely brother, Rong. Thank you for being so wonderful, supportive, and for always inspiring me to be brave enough to overcome the difficulties and challenges. Since 'life is either a daring adventure or nothing', never be afraid to try something new.

Table of Contents

Author's Declaration ii
Abstract iii
Acknowledgements iv
Dedication v
Table of Contents vi
List of Figures viii
List of Tables x
Chapter 1 Introduction 1
1.1 Flexible Thin-Film Transistors 1
1.2 Motivation for Flexible ZnO TFTs 2
1.3 Thesis Objectives 3
1.4 Thesis Organization 4
Chapter 2 Background 6
2.1 Zinc Oxide Thin-Film Transistors 6
2.1.1 Properties of Zinc Oxide 6
2.1.2 TFT Structure 7
2.1.3 Fabrication Procedure 9
2.1.4 Characteristics of Accumulation-Mode TFTs 10
2.2 Flexible Thin-Film Transistors 14
2.2.1 Hydrogenated Amorphous Silicon (a-Si: H) Based TFTs 14
2.2.2 Amorphous Indium–Gallium–Zinc Oxide (a-IGZO) Based TFTs 15
2.2.3 Zinc Oxide Based TFTs 15
Chapter 3 Experimental 18
3.1 Characterization of Thin Films 18
3.1.1 Scanning Electron Microscopy 18
3.1.2 Atomic Force Microscopy 19
3.1.3 Stress Gauge Measurement 21
3.1.4 X-Ray Diffraction 23
3.2 Bending Test of TFTs 26
Chapter 4 Modeling of Flexible ZnO TFTs 28
4.1 Analytical Model 28

4.1.1 Strain and Stress Analysis of a Single Thin-Film on Thick Substrate 28
4.1.1.1 Origin of intrinsic stresses during thin-film growth 28
4.1.1.2 Fundamental formulas for stress and strain in thin films 29
4.1.1.3 Built-in strain and built-in stress 32
4.1.1.4 Stress/strain distribution as a result of applied bending moment 32
4.1.2 Strain and Stress Analysis of Thin-Film Multilayers on Thick Substrate 35
4.1.2.1 Formulation of stress and strain models for multiple thin films on compliant substrates 35
4.1.2.2 Stress/strain simulation due to applied mechanical bending of thin films on various platforms 37
4.2 Numerical Model 38
4.2.1 Two-Dimensional Model of Thin Film Deposited on Thick Substrate 38
4.2.1.1 Assumptions and boundary conditions used in numerical models 38
4.2.1.2 Comparison of results for finite element analysis models with analytical model 38
4.2.1.3 Stress/strain simulation due to applied mechanical bending 41
4.2.2 Two-Dimensional Model of TFT devices 43
4.2.2.1 Stress/strain simulation of ZnO TFT on flexible platforms by mechanical bending 43
4.2.2.2 Proposed designs to minimize stress induced strain within the active TFT layer under bending 48
4.2.2.3 Simulation of flexible TFT structures using different inorganic and organic materials 50
4.2.3 Numerical Simulation of Complex TFT Devices 60
4.2.3.1 Simulation of flexible double gate TFT 60
Chapter 5 Conclusions 65
References 68

List of Figures

Fig. 2.1 Schematic of ZnO crystal structures: (a) cubic rocksalt (*B*1), (b) cubic zinc blende (*B*3), and (c) hexagonal wurtzite (*B*4). The shaded gray and black spheres represent Zn and O atoms, respectively [11].. 6

Fig. 2.2 Four general TFT configurations, including: (a) staggered top-gate, (b) staggered bottom-gate, (c) coplanar top-gate, and (d) coplanar bottom-gate [13]. 8

Fig. 2.3 Energy band diagram of n-type semiconductor based TFT. (a) equilibrium, (b) V_{GS} <0 V, and (c) V_{GS} >0 V [23, 24]... 10

Fig. 2.4 Relation of drain-source current versus voltage 11

Fig. 2.5 band diagrams of ZnO:N channel/Al_2O_3 gate insulator/Ti gate indicating the piezoelectricity mechanism occurred in flexible TFTs in response to external stresses, (a) compressive stress, and (b) tensile stress [41].. 17

Fig. 3.1 SEM images of the ZnO thin film deposited on silicon substrate (Magnification: 125.27 K×) 19

Fig. 3.2 AFM image of a nanocrystalline ZnO film deposited using RF-sputtering method. 21

Fig. 3.3 Schematic of thin-film stress measurement [52]. 22

Fig. 3.4 (a) Geometric arrangement of a high resolution X-ray diffractometer (PANalytical X'pert Pro MRD system), and (b) schematics of some primary operation parameters [53]................................ 23

Fig. 3.5 Diffraction geometry of GIXRD for thin film analysis, it shows X-ray incident and diffraction directions [54] 24

Fig. 3.6 GIXRD analysis of ZnO thin film by varying two-theta from 30° to 60°. 25

Fig. 3.7 Photograph of a bending tester with a loaded carrier substrate and an attached flexible TFT [61]. The bending radius is about 19 mm. 27

Fig. 4.1 Schematic of film-substrate combination under residual stresses. (a) tensile stresses in the film; (b) compressive stresses in the film. 30

Fig. 4.2 Schematic of thin film-substrate couple after temperature change....................................... 31

Fig. 4.3 Elastic bending of beam under applied end moment. 33

Fig. 4.4 Schematic of a n-layer stack. 35

Fig. 4.5 Curve fitting using 4th degree polynomial by Matlab. 40

Fig. 4.6 Strain tensor-x (Scale factor: 50). 42

Fig. 4.7 Contour plot of stress tensor-x (Scale factor: 1). 42

Fig. 4.8 Curve fitting using 4th degree polynomial by Matlab. 43

Fig. 4.9 Schematic of ZnO TFT structure. 44
Fig. 4.10 Strain tensor-x of film-substrate stack by applying bending moment of 1E-5 N ·m 45
Fig. 4.11 Stress tensor-x of film-substrate stack by applying bending moment of 1E-5 N ·m. 46
Fig. 4.12 Stress tensor-x distribution in the magnified top surface area. 46
Fig. 4.13 Curve fitting using 4th degree polynomial by Matlab. 48
Fig. 4.14 Schematic of ZnO layer near the neutral plane by adjusting the thickness of the encapsulating layer. 49
Fig. 4.15 Location of ZnO film near neutral plane by varying the thickness of the encapsulating layer 50
Fig. 4.16 Schematic of TFT structure: (a) a-IGZO TFT; (b) pentacene organic TFT. 51
Fig. 4.17 Strain tensor-x in a-IGZO TFT device due to applied bending moment of 1E-5 N ·m. 52
Fig. 4.18 Strain tensor-x in pentacene organic TFT due to applied bending moment of 1E-5 N ·m 52
Fig. 4.19 Stress tensor-x in a-IGZO TFT device due to applied bending moment of 1E-5 N ·m. 53
Fig. 4.20 Stress tensor-x in pentacene organic TFT device due to applied bending moment of 1E-5 N ·m. 54
Fig. 4.21 Comparison of strain tensor-x in each layer of different TFT structures 55
Fig. 4.22 Comparison of stress tensor-x in each layer of different TFT structures 56
Fig. 4.23 Schematic of a-Si TFT structure. 57
Fig. 4.24 Strain tensor-x in a-Si TFT device 58
Fig. 4.25 Stress tensor-x of a-Si TFT 58
Fig. 4.26 Average stress tensor-x in the various active layers and maximum stress tensor-x in different TFT structures. 59
Fig. 4.27 Schematic of a dual gate TFT structure 61
Fig. 4.28 Strain tensor-x by applying bending moment of 1E-5 N ·m. 61
Fig. 4.29 Stress tensor-x by applying bending moment of 1E-5 N ·m. 62
Fig. 4.30 Average values of Strain Tensor-x in TFT multilayer. 63
Fig. 4.31 Average values of Stress Tensor-x in TFT multilayer. 63

List of Tables

Table 2.1 Electrical Properties of competing n-type thin film technologies [12] 7
Table 4.1 Material properties used in the numerical study 39
Table 4.2 Material properties used in the numerical model of ZnO TFT. 44
Table 4.3 Average stress and strain tensor-x of different TFT layers. 47
Table 4.4 Material properties used in modeling organic and inorganic TFTs 51
Table 4.5 Average stress and strain tensor-x of different TFT layers. 54
Table 4.6 Material properties used in the numerical model of a-Si TFT 57
Table 4.7 Average stress and strain tensor-x over each layer of a-Si TFT 59
Table 4.8 Material properties of a dual gate TFT device. 60
Table 4.9 Average values of stress and strain tensor-x of the double gate TFT 62

Chapter 1 Introduction

Flexible electronics is a rapidly developing technology for assembling electronic circuits, integrating electronic devices with novel flexible substrates. It involves multidisciplinary research, from materials selection, process design and manufacturing of thin layers of organic and inorganic semiconductors, dielectrics and other functional layers and devices, to the implementation of complete electronic systems on flexible substrates. This technology has the potential for tremendous impact on the electronics industry for applications in flat-panel displays, images sensors, and energy generation (flexible solar cells) and storage (flexible batteries). Multiple factors contribute to the increasing interest in the field of flexible electronics, primarily driven by the need for light weight, mechanical flexibility, and reduced size to provide enhanced portability. In addition, large area applications potentially are able to reduce fabrication costs with roll-to-roll sheet fed processing in comparison to rigid substrate counterparts.

In order to achieve the integration between materials, device, and systems technologies for the application of large-area flexible electronics and optoelectronics, special attention is required in the development of all the components that will make up the device and the associated circuits. The components include the semiconductor, dielectric, metals, and processes used to fabricate the device structures. In order to fully optimize the device performance, the constraints of the flexible substrate on these electronic materials must be fully understood. Incompatibilities with flexible platforms and the transition metal oxides are complex and properties such as the thermal resistance, thermal expansion coefficient, mechanical stiffness, thermo-mechanical behavior, electrical behavior under induced mechanical strain, and process integration present a variety of challenges to understand and model the behavior of this emerging flexible electronics technology [1, 2].

1.1 Flexible Thin-Film Transistors

The thin-film transistor (TFT) and its potential utility can be traced back to the 1930s when the invention of the TFT was patented and the basic principle is known today as the metal-semiconductor field-effect transistor (MESFET). Later on, insulating materials (such as aluminum oxide) was introduced between the semiconductor (copper sulfide) and the field-effect electrode (aluminum), forming the so-called metal-insulator-semiconductor field-effect transistor (MISFET) [3]. In 1962, RCA laboratories reported the fabrication of a TFT using thin films of polycrystalline Cadmium Sulfide (CdS) as the semiconductor material. Since the mid-1980s, silicon-based TFTs have become

the most important devices for active-matrix liquid crystal displays (AMLCDs). In the past ten years, amorphous silicon (a-Si:H) TFTs have successfully dominated the large-area LCD product market. Meanwhile, research and development activities on polycrystalline silicon (poly-Si) TFTs are steadily increasing [4, 5]. More recently, a new generation of oxide semiconductors are being studied and applied as the active material to the TFT device, particularly the zinc oxide (ZnO) and InGaZnO (IGZO) thin films.

The primary study of the flexibility of TFTs starts in 1994, when a-Si:H TFT circuits were fabricated on flexible polyimide substrates and subsequently formed on flexible stainless steel in 1996. In 1997, polycrystalline silicon (poly-Si) TFTs were made on plastic substrates using laser-annealing method. Thereafter, extensive research has been carried out on the flexible electronics and remarkable progress has been achieved in the utilization of flexible displays on either steel or plastic foil substrates [6, 7].

1.2 Motivation for Flexible ZnO TFTs

Currently, transparent electronics are one of the most advanced topics for a wide range of device applications, including invisible electronic circuitry, next generation displays, and optoelectronic devices. The key components of the transparent electronics are transparent conductive oxides (TCOs). TCOs are a special class of materials which possesses both high visual transparency due to their large band gap energy and high electrical conductivity. One of the most commonly used TCOs is ZnO, and the birth of transparent electronics is normally associated with the reports on ZnO TFTs presented in 2001-2003 [8, 9].

Because the ZnO is transparent in the visible region of the spectra, it is less light sensitive. Besides, the primary advantage of transistors using ZnO as active channel layer is the high electron channel mobility and the corresponding higher drive current and faster operating speeds. Another predominant advantage is that ZnO can be deposited at or near room temperature with high-quality polycrystalline structure, which is compatible with the use of flexible substrate under lower processing temperature. InGaZnO (IGZO) is currently emerging as the preferred semiconductor for high performance and transparent large-area electronics. The advantage of IGZO material is its amorphous state compared to polycrystalline ZnO. The disorder in the IGZO system is comparable to a-Si:H thin films, providing excellent electrical uniformity over large areas compared to polycrystalline materials while possessing higher field-effect mobilities compared to a-Si:H.

1.3 Thesis Objectives

The main objective of this thesis is to investigate the mechanical flexibility of thin-film transistors and model and simulate the stress induced strains due to intrinsic and applied stress using numerical computation for TFT structures. The investigation begins with simple models of thin films on rigid substrates and extends to patterned TFT structures on flexible platforms with applied bending stress. These models are analyzed to optimize the device structure design and extend the model towards more complicated and flexible electronics applications. To achieve this goal, the thesis is divided into the following categories:

1. Analytical model

1) Single thin-film layer on rigid/flexible substrate

  a) Basic formulation to model thin-film stress
  b) Induced intrinsic stress during thin-film growth
  c) Properties that affect thin-film strain
  d) Stress/strain simulation for applied mechanical bending of thin films on flexible substrates

2) Multiple thin-film layers deposited on rigid/flexible substrate

  a) Basic considerations for simulation of multiple thin-film stresses on compliant substrates
  b) Formulation of models used to determine stress and strain in the multilayer stack
  c) Stress and strain resulting from mismatch in thermal expansion coefficient of multiple films
  d) Stress/strain simulation due to applied mechanical bending of thin films on various platforms

2. Numerical model

1) Two-dimensional simulation of single film deposited on flexible substrates

  a) Assumptions and boundary conditions used in numerical models
  b) Modeling and analysis of thin-film built-in strain on flexible substrates
  c) Comparison of results for finite element analysis models with analytical models
  d) Stress/strain simulation due to applied mechanical bending of an isolated beam

2) Two-dimensional simulation of thin-film transistors

a) Stress/strain simulation of flexible ZnO TFT due to applied mechanical bending

b) Analysis of the radius curvature of the TFT structure under bending and the position of neutral axis

c) Proposed designs to minimize stress and strain within active TFT layers under bending

3. Generalize the numerical model for simulations of complicated devices

a) Simulating the mechanical properties of complex TFT structures

i. Different semiconducting materials, include a-IGZO TFT, pentacene organic TFT, and a-Si TFT

ii. Simulation of complex TFT structures, e.g. double-gate TFT

iii. Comparison of stress and strain distribution for various TFT structures under bending

1.4 Thesis Organization

In the present thesis, flexible thin-film transistors especially transparent and flexible ZnO based thin-film transistors are studied. A brief review of the development of thin-film transistors and the increasing attention on the fabrication of flexible ZnO TFTs and IGZO based TFTs are discussed in Chapter 1.

In Chapter 2, the basic physics of ZnO material include crystal structure and electrical properties are reviewed. Besides, the TFT device structure, operating principle, and the electrical properties such as the current-voltage relationship, field-effect mobility, threshold voltage, and subthreshold slope are illustrated. Furthermore, the recent research progress in the flexibility study of the most commonly used TFTs are summarized, including hydrogenated amorphous Silicon (a-Si:H) TFTs, amorphous Indium–Gallium–Zinc Oxide (a-IGZO) TFTs, and Zinc Oxide (ZnO) TFTs. The variations of the electrical properties as a result of the mechanical strain are mainly discussed.Chapter 3 is primarily focused on the experimental characterization of the deposited materials and the mechanical bending test. The commonly used methodologies of SEM, AFM, XRD, and strain gauge are reviewed and the results of experimental measurements are analyzed. Moreover, the mechanical bending tests using flexible substrate with TFTs attached are presented.

The major emphasis of this thesis is the numerical modeling of flexible TFT structures using FEM method, as presented in Chapter 4. Numerical models are first used to simulate the stress and strain distribution in thin films and multiple layers on top of rigid and flexible substrates. The thermal strain due to thermal mismatch, the built-in strain as a result of the thin-film deposition, and the interaction among multiple deposited layers are considered. Furthermore, by applying a pair of opposite mechanical bending to both ends of the TFT structures, the analytical solution of stress/strain distribution and bending curvature of multi-layer structure on flexible substrate are summarized. Then, numerical modeling of the stress and strain distribution in multi-layer structure and TFT devices are performed. The flexibility of the TFTs is simulated in two-dimensional systems by applying external bending moment to their boundary. Those numerical simulations are compared with the analytical models to verify and improve the numerical model for simulation of complex devices. In particular, the numerical model is used to minimize the strain in TFTs subjected to mechanical bending by placing the vital functional layer near the neutral mechanical plane in terms of designing the device structure and layer thicknesses. An extension of the numerical model is to simulate the mechanical properties of TFTs with different materials and complex structures.

Finally, Chapter 5 concludes this thesis and proposes recommendations for further research. Based on the numerical models of TFTs, further study may focus on investigating the correlations between the mechanical and electrical properties of complex TFTs, striving toward modeling more complicated electronic devices with accurate and reliable simulation results.

Chapter 2 Background

2.1 Zinc Oxide Thin-Film Transistors

The fabrication of TFTs at low temperature on flexible substrates (e.g. plastic or thin glass), is a primary technique used in the realization of flexible electronics. Nowadays, thin-film transistors (TFTs) using wide bandgap oxide semiconductors have attracted much attention for applications in flexible electronic devices. In particular, ZnO has emerged as one of the most promising semiconducting materials, due to its optical and electrical properties, high chemical and mechanical stability, and greatest potential to grow high-quality crystals at low temperature. Moreover, ZnO is recognized as an ecological and economical semiconductor, which cost less than the currently used transparent conductive oxide materials, such as ITO and SnO_2 [10].

2.1.1 Properties of Zinc Oxide

Zinc oxide is a wide bandgap (Eg ~ 3.3 eV) compound semiconductor of the II-VI semiconductor group. The Zn-O bond possesses very strong ionic character which lies on the borderline between covalent and ionic compound. It has a large exciton binding energy of 60 meV. Generally, ZnO crystallizes in three main types, wurtzite (B4), zinc blende (B3), and rocksalt (B1), the schematic of which are shown in Fig. 2.1. Among those, the most stable phase of ZnO at ambient condition is wurtzite. The rocksalt structure (similar to NaCl) can be obtained at relatively high pressures, and the zinc-blende structure can grow on top of cubic substrates [11].

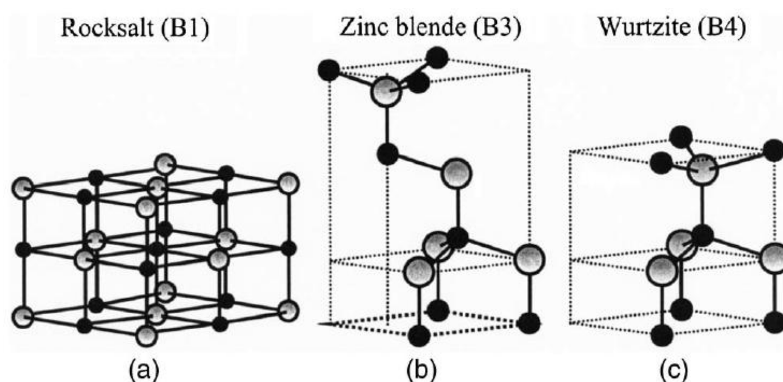

Fig. 2.1 Schematic of ZnO crystal structures: (a) cubic rocksalt (*B*1), (b) cubic zinc blende (*B*3), and (c) hexagonal wurtzite (*B*4). The shaded gray and black spheres represent Zn and O atoms, respectively [11].

Zinc oxide is typically an n-type semiconductor, due to the inherent nature of forming oxygen deficient films. Although experimental work indicates the feasibility of p-type doping of ZnO material, the prospect for achieving p-type doping in ZnO is quite difficult compared with n-type doping, due to the carrier compensation by native defects such as zinc interstitial and oxygen vacancies. It is known that poly-crystalline ZnO is inherently n-type. Compared with other n-type semiconductors, ZnO has predominant advantages. A list of the electrical properties of the competing n-type thin films is summarized in Table 2.1. The mobility of ZnO thin film can be achieved as high as 110 $cm^2/(V \cdot s)$. Furthermore, ZnO thin film retains its bulk wide bandgap and transparent qualities at deposition temperature up to 250 ˚C, which makes it extremely attractive for high performance large area electronics under various temperature conditions.

Table 2.1 Electrical Properties of competing n-type thin film technologies [12].

Figure of merit	**High Performance a-Si TFT**	**Organic TFT**	**a-IGZO**	**Zinc Tin Oxide (ZTO)**	**ZnO**
μ ($cm^2/(V \cdot s)$)	1.5	0.02	14	43	110
I_D^{on}/I_D^{off}	~10^8	~10^6	>10^8	10^7	10^{12}
I_D^{off} (pA)	0.1	1	0.1	1	0.01
V_{TH} (V)	2	~0.7	2.3	1.4	2
S (mV/dec)	300	170	200	180	100

2.1.2 TFT Structure

A typical TFT is made up of five different components: gate, source and drain, semiconductor, and gate insulator. The gate is separated from the semiconductor by a gate insulating layer. The source and drain islands are in contact with the semiconductor. Due to the different layouts of the functional layer, the structure of TFT devices can be classified into four groups, including staggered TFT, inverted staggered TFT, coplanar TFT, and inverted coplanar TFT. A staggered TFT has the gate and source/drain electrodes on the opposite sides of the semiconductor, whereas a coplanar TFT has the gate and source/drain electrodes on the same side of the semiconductor. In addition, when the gate is

placed at the bottom of the TFT, it is called inverted TFT. The schematic of various TFT structures are shown below.

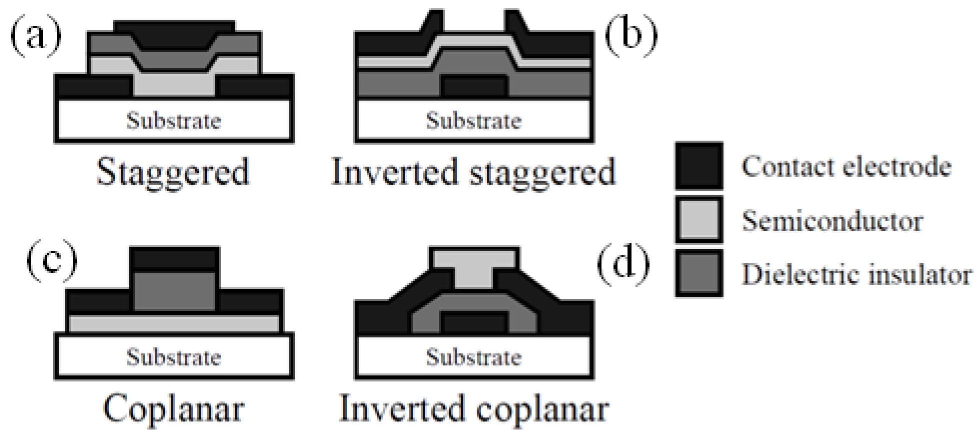

Fig. 2.2 Four general TFT configurations, including: (a) staggered top-gate, (b) staggered bottom-gate, (c) coplanar top-gate, and (d) coplanar bottom-gate [13].

Generally, a transistor can be thought as a three-terminal switch, which has two inputs (drain and gate) and one output (source). When the transistor is at 'on' state, electrons will flow from the source port to the drain port like water flowing to a sink drain, and the drain as an input is usually biased at some static bias values. In the bottom gate configuration, the drain is located on the top of the semiconductor separated from the source by a length called the gate length (L_G). On the other hand, the gate as the second input is used to influence the semiconductor, controlling whether electrons can flow from the source to the drain or not, just like a gate in a damn which determines the water flow.

The semiconductor connecting the drain and the source is the key material in the operation of TFTs. It can be used either as an insulator or a conductor. When it serves as a low-resistance material, it will conduct an electrical signal from the drain to the source. In this case, the transistor is considered 'on'. When the semiconductor has low conductivity, then the transistor is 'off'. Another vital layer of TFTs is the gate dielectric, which is an insulating material that physically separates the gate electrode from the semiconductor. It not only prevents electrons from flowing out of the semiconductor, but also allows the electric field from the gate electrode to affect the properties of the semiconductor by changing from an insulator to a conductor or vice versa, thus determining the 'on' or 'off ' state of the switch.

2.1.3 Fabrication Procedure

Several thin film fabrication approaches have been used for the deposition of the metal oxide films, such as RF/DC sputtering [14, 15], pulsed laser deposition (PLD) [16, 17], ion beam deposition [18], and chemical vapor deposition (CVD). Among these techniques, the most commonly used method is RF sputtering, which is attractive due to the formation of uniform films on various substrates, and its application for large-area manufacturing over a wide temperature range. Pulsed-laser deposition (PLD) has recently become an important technique for producing transparent conductive films as well as undoped films for TFT applications. The main advantage of PLD is that it provides a controlled growth process ideal for fabricating oxide thin films. The ion beam deposition process uses ion beam that generated from the ion source to bombard on a source target surface to evaporate the source, which deposits onto a substrate surface to form thin films.

Chemical vapor deposition introduces gases into the deposition chamber to react and form desired films. Compared to other processes using line-of-sight techniques that are difficult to coat high aspect ratio and shadowed structures uniformly, the CVD method has high conformality, whereas the high temperature required for the reaction process limits its application. Atomic layer deposition (ALD) [19] is a modified form of CVD which enables the growth of highly uniform and conformal films with thickness at the atomic level. Besides, it provides an accurate control of the incorporation of extrinsic dopants, and has been considered as a promising method for the deposition of doped ZnO films. Plasma enhanced chemical vapor deposition (PECVD) [20] is a method using highly ionized gases to provide the energy needed for the chemical reactions. It allows the film deposition to occur at lower substrate temperatures than those using solely thermal CVD methods to generate thermal energy.

A general fabrication process flow of a coplanar ZnO TFT on flexible substrate is as follows [21, 22]: 1) cleaning of the substrate surface; 2) a thick buffer layer is directly deposited on the flexible substrate; 3) a ZnO film is formed by various techniques described above and patterned by photolithography to work as semiconducting active layer; 4) source and drain electrode layer is formed on top of the ZnO film by deposition and subject to a subsequent lift-off patterning; 5) dielectric layer is deposited as gate insulator; 6) a gate electrode layer is deposited to achieve desired gate length. In order to improve the device performance, thermal annealing is usually carried out after the formation of the active layer and/or after the fabrication of the entire TFT device.

2.1.4 Characteristics of Accumulation-mode TFTs

To turn on a n-type semiconductor based TFT in accumulation mode, a positive charge is applied to the gate to form a positive electric field, therefore attracts electrons in the semiconductor. The electrons will be collected near the semiconductor and the gate dielectric interface, and be available to conduct the electrical signal between the source and the drain. This is regarded as the 'on' state of the TFT. Conversely, a negative electric field will repel electrons away from the semiconductor and the gate dielectric interface; as a result, there will be no carriers for any electrical signal to transfer between the source and the drain, which is called 'off' state.

1) Energy Band Diagram

The energy band diagrams of an n-type semiconductor based TFT at various bias conditions are shown in Fig. 2.3 (a) - (c).

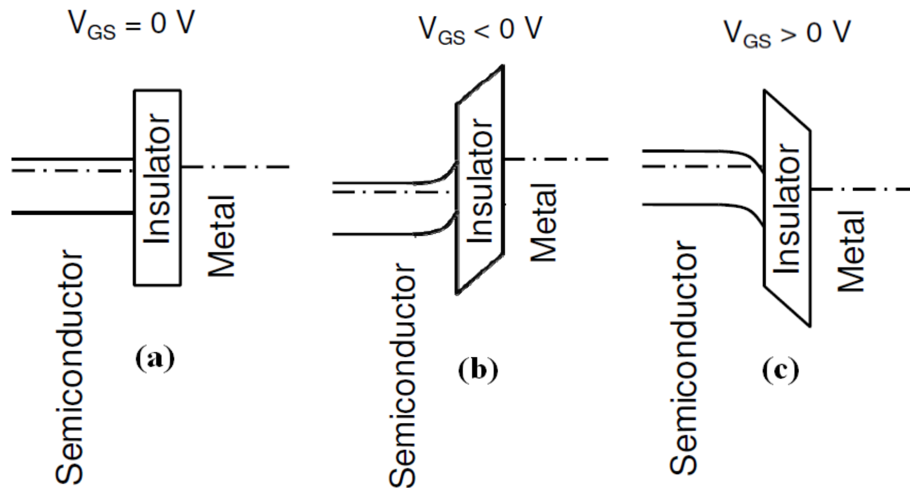

Fig. 2.3 Energy band diagram of n-type semiconductor based TFT. (a) Equilibrium, (b) $V_{GS} < 0$ V, and (c) $V_{GS} > 0$ V [23, 24].

In Fig. 2.3(a), when no potential is applied to the source, drain, and the gate terminals, the device is at equilibrium. When the gate is negatively biased, as shown in Fig. 2.3(b), the applied negative bias repels mobile electrons from the semiconductor, leading to a depletion region near the insulator-semiconductor interface. Accordingly, the conductance of the region is reduced due to the reduced number of mobile electrons in the semiconductor. When the gate is positively biased in Fig. 2.3(c),

the applied positive bias attracts mobile electrons, forming an accumulation region of electrons near the insulator-semiconductor interface; as a result, the conductance of the semiconductor is increased.

2) Current-Voltage Relationship

For the case that the gate is positively biased and under accumulation mode, as shown in the above Fig. 2.3(c), the semiconductor is initially acts as a resistor, the drain-source current (I_{DS}) increases linearly with the applied drain-source voltage (V_{DS}). With further increasing the V_{DS}, the accumulation near the drain starts to decrease and eventually begins to deplete. The voltage at which the semiconductor region near the drain is fully depleted of carriers is denoted the pinch-off voltage. Therefore, application of V_{DS} greater than the pinch-off voltage results in the saturation characteristics of the drain current, whereas the drain current becomes almost constant, as shown in Fig. 2.4.

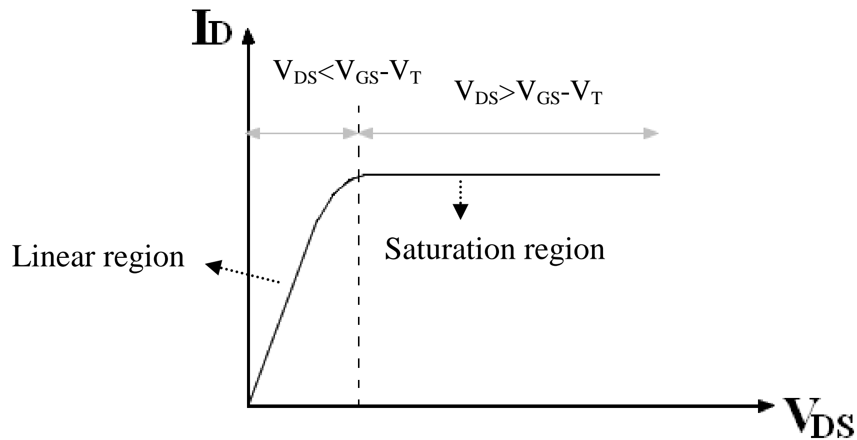

Fig. 2.4 Relation of drain-source current versus voltage.

For n-channel TFT, the ideal current-voltage relation in the linear region is shown below [25].

$$I_D = \frac{W\mu C_{OX}}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \quad \text{(Eq. 2.1)}$$

where W is the width of the channel region (between the source/drain electrodes), L is the length of the channel, μ is the mobility in the semiconductor, C_{ox} is the gate insulator capacitance, V_{DS} is the drain-source voltage, V_T is the threshold voltage, and V_{GS} is the gate-source voltage. The above equation is valid for $V_{GS} \geq V_T$, and for $0 \leq V_{DS} \leq V_{DS}$ (sat).

In the saturation region, the relation is

$$I_D = \frac{W\mu C_{OX}}{2L}(V_{GS} - V_T)^2 \quad \text{(Eq. 2.2)}$$

The above formula is valid for $V_{DS} \geq V_{DS}$ (sat), where $V_{DS}(sat) = V_{GS}-V_T$

3) Threshold Voltage

Threshold voltage (V_T) is defined as the applied gate voltage at which the channel of mobile carriers begins to form and thus the TFT devices begin to switch from 'off' to 'on'. The importance of V_T is that it helps to determine the necessary supply voltage for circuit operation. When $V_{GS} < V_T$, the drain current is zero. With the V_{GS} becomes larger than the V_T, channel charge density increases, increasing the channel conductance.

The value of threshold voltage is commonly extracted from the following two methods [12]. The first method extracts V_T from the transfer curve of a TFT in the linear region of operation when a small V_{DS} is applied. In this case, Eq. 2.1 is simplified to:

$$I_D = \frac{W\mu C_{OX}}{L}[(V_{GS} - V_T)V_{DS}] \quad \text{(Eq. 2.3)}$$

The threshold voltage is the gate voltage at which the tangent to the I_D vs. V_{GS} curve at the point of maximum transconductance intersects the x-axis.

Another method is to extract threshold voltage from the transfer curve of TFT in the saturation region of operation, where V_T is the intercept in the x-axis by best fitting the on-state data of the $\sqrt{I_D}$ vs. V_{GS} curve.

4) Mobility

Mobility (μ) is a material property that is used to describe the drift velocity of electrons or holes to the applied electric field across a material. The most widely used term for mobility is field-effect mobility (μ_{FE}), which represents the mobility of carriers under the influence of the device structure in field-effect transistors. By plotting the square root of drain current as a function of the gate voltage, the value of μ_{FE} can be extracted from the slope (m_{sat}) of the curve using the following equation [26]:

$$\mu = \mu_{sat} = m_{sat}^2 \cdot \frac{2L}{W} \cdot \frac{1}{C_{ox}} \quad \text{(Eq. 2.4)}$$

The value of μ_{FE} can also be extracted from the slope (m_{lin}) of the linear region of the drain current against V_{GS} curve when a small drain-source bias V_{DS} is applied, which is given by

$$\mu = \mu_{lin} = m_{lin} \cdot \frac{L}{W} \cdot \frac{1}{C_{ox}} \qquad \text{(Eq. 2.5)}$$

The field-effect mobility extracted from the saturated region may result in conservative values than those extracted from the linear region of the I_D-V_{GS} curve, since the latter is limited for a condition of very small V_{DS} and large V_{GS}.

It should be noted that, the mobility may be influenced by several factors, such as energy, interface charge density, process conditions, and dielectric material selection, etc. [23, 27].

5) Subthreshold Swing

Subthreshold swing (S) is a performance criterion used to evaluate the efficiency of a device in terms of the transition from the off-state to the on-state. It is estimated using a semi-log plot of the transfer characteristics taken at high V_{DS} ($V_{DS} \geq V_{DS}$ (sat), where V_{DS} (sat) = V_{GS}-V_T). Subthreshold swing is defined as the inverse of the slope of $\log_{10}(I_D)$ versus V_{GS} in the subthreshold region of the operation of a transfer curve.

$$S = [\frac{\delta \log_{10}(I_D)}{\delta V_{GS}}]^{-1} \qquad \text{(Eq. 2.6)}$$

A smaller value of subthreshold swing is desired because it indicates the device is more efficient in transitioning from off-state to on-state [25, 27].

It is known that the subthreshold current depends exponentially on the gate voltage, and is strongly dependent on temperature. Suppose a finite depletion layer with capacitance C_D in series with the geometric capacitance C_{ox} of the gate oxide, the relation is given by [28]:

$$S = \left(\frac{kT}{e}\right) \ln 10 \times \left(1 + \frac{C_D}{C_{ox}}\right) \qquad \text{(Eq. 2.7)}$$

At room temperature, a typical value of the subthreshold swing is between 70 and 100 mV/decade. It is generally known that, the increment of the subthreshold swing is attributed primarily to the interface traps.

2.2 Flexible Thin-Film Transistors

Due to the significant application of bendable TFTs in flexible electronics such as flexible displays, many investigations have focused on the flexibility study of TFTs, especially the hydrogenated amorphous Silicon (a-Si:H) based TFTs. A brief discussion of the research findings and the progress that has been made is summarized below.

2.2.1 Hydrogenated Amorphous Silicon (a-Si: H) Based TFTs

Several papers presented the a-Si: H TFTs fabricated on polyimide foil under uniaxial compressive or tensile strain (1% compressive strain to ~ 0.3% tensile strain) [29, 30]. It shows that the field-effect mobility increases with uniaxial tensile strain (up to the failure strain), and decreases with uniaxial compressive strain. The possible reason is that compressive strain broadens both the valence and conduction band tails of the a-Si:H channel material, and thus reduces the effective electron mobility. Similar findings are reported in [31], the field-effect mobility increases with tensile strain, which correlates with a decreasing width of the conduction band tail in a-Si:H. Furthermore, the threshold voltage increases with increasing mechanical strain due to the defect generation. A recent publication by M. H. Lee et al. [32] claims that the formation of trapped states by way of mechanical strain dominates the characteristics of hydrogenated amorphous silicon (a-Si:H) TFTs. During a mechanical strain, the trap states are redistributed into a Gaussian distribution rather than the ordinary exponential distribution, resulting in unstable electrical characteristics, such as variation in threshold voltage, subthreshold swing, and the mobility of carriers due to mechanical strain.

A study of the failure resistance of a-Si TFTs on polyimide foil shows that, the amorphous layers of the TFT fail by periodic cracks at a tensile strain of ~0.5%, while under compression, the TFTs do not fail when strained by up to 2% [33]. The difference is due to the fact that, the tensile driving force is sufficient to overcome the resistance to crack formation, however, the compressive failure mechanism of delamination is not activated due to the large delamination length required between transistor layers and polymer substrate. Moreover, by replacing the brittle, silicon nitride barrier layer and the gate insulator in a-Si:H TFTs on polyimide foil with a resilient hybrid of silicon dioxide and silicone polymer, the transistor structures can withstand up to 5% tensile strain and 2.5% compressive strain [34].

2.2.2 Amorphous Indium–Gallium–Zinc Oxide (a-IGZO) Based TFTs

Recently, plenty of research has been carried out for the fabrication of a-IGZO based TFTs in flexible electronic applications, such as flexible thermal and pressure sensors. Among various transparent amorphous oxide semiconductors (TAOSs), a-IGZO has attracted considerable attention because of its relatively high electron mobility and good chemical stability. Moreover, a-IGZO layer can be formed at a low temperature with good large-area uniformity and good electrical stability [35-36].

Refer to N. Münzenrieder et al. [37], a-IGZO TFTs are fabricated on flexible substrates and their electrical behavior are measured under tensile and compressive strains with bending radii decreased to less than 10 mm. A comparison of the bending tests performed with and without illumination shows that, the mobility and threshold voltage are changed under illumination condition, whereas the performance of TFT kept stable in the dark after the applied mechanical strain. A decrease in the V_T after tensile bending is due to an increase in the interatomic distance that cause an effective decrease in the energy level splitting (ΔE) of the bonding and antibonding orbitals between the atoms in the semiconductor material. This results in a decrease in the effective mass (m^*) of the charge carriers (due to $m^* \sim \Delta E$) according to $k \cdot p$ method; consequently, the mobility ($\mu \sim 1/m^*$) increases. The tensile bending results in the increase in the channel conductivity and a negative shift of the threshold voltage.

Besides the repeatable resistance to tensile or compressive strain of the TFT devices, a stretchable and stable connection between the individual TFT structures is also important. The mechanical characteristics of a stretchable a-IGZO based inverter are investigated by B.-J. Kim et al. [38]. A FEM numerical model is used to improve the mechanical stability by optimizing the device structure and evaluating the stress and strain distribution near the SiO_2 bridge.

2.2.3 Zinc Oxide Based TFTs

Due to the great potential for high-performance and low-cost electronics, TFTs using ZnO as the active channel layer is particularly attractive for the application of highly flexible structures. Several research groups have investigated the mechanical flexibility of ZnO TFTs and circuits by mechanical bending to a specific radius [39-41].

M. S. Oh et al. showed a complementary inverter using n-channel sputtered ZnO and p-channel pentacene channels on a polyethersulfone flexible substrate under a bending condition of 56 mm

radius of curvature [39]. It pointed out that the interface defects affect the electrical properties of the inverter. During the deposition of ZnO on AlO_x dielectric layer by RF sputtering, the energetic Zn and O particles may damage the dielectric surface, which is vulnerable to be charged by ZnO channel electrons during the operation of TFTs subjected to a positive gate voltage bias.

Due to the advantages of low deposition temperatures and high electron mobilities, both ZnO and a-IGZO are regarded as alternative materials to replace the a-Si:H active layer in flexible TFTs. As presented in [40], TFTs using both ZnO and IGZO semiconducting layers are fabricated on polyimide substrates and exposed to tensile bending radii down to 10 mm. For IGZO based TFTs, the mobility, threshold voltages, and the subthreshold slope are stable over the entire bending range. However, for ZnO TFTs, the electrical properties are strongly degraded. As the bending radius reduces from 35 mm to 10 mm, a decreasing mobility, and increasing threshold voltage and subthreshold slope are observed, which may be due to the formation of microcracks in the ZnO film.

A recent report by J.-M. Kim et al. [41] investigated the fabricated Atomic Layer Deposition (ALD) nitrogen doped ZnO based TFTs on Polyethylene Naphthalate (PEN) substrates and studied the change in device properties with respect to the amount of substrate bending. It shows the value of V_T is systematically decreased from compressive strain to tensile strain, with the normalized V_T varying in the range of $\pm 5\%$. Meanwhile, the values of saturation mobility increased from compressive strain to tensile strain with respect to normalized saturation mobility varied from -2% to 2%.

There are several factors that might be responsible for the variation of device properties regarding to the mechanical bending, such as the piezoresistive effect in the semiconductor [41]; changes in the band structure of the semiconductor [37]; electrons are trapped at the interface of the dielectric and semiconductor; or the change of grain size (e.g. the mobility generally increase with grain size because the grain boundaries are associated with scattering and trapping sites) [42].

ZnO is a well-known piezoelectric material which has the highest piezoelectric tensor among the tetrahedrally bonded semiconductors. When a piezoelectric material is strained, an electrical polarization is generated; likewise, it is strained when an electric field is applied to it. Deflection of a ZnO thin film creates in a relative displacement of Zn^{2+} cations with respect to O^{2-} anions in the wurzite structure, resulting in a strong piezoelectric potential field inside the channel area [41, 43].

A schematic of the piezoelectric effect on the band diagram of ZnO:N channel/Al_2O_3 gate insulator/Ti is shown in Fig. 2.5 (a) and (b). The possible mechanism of the modulations on the electrical transport behavior in flexible TFTs with respect to substrate bending is described below.

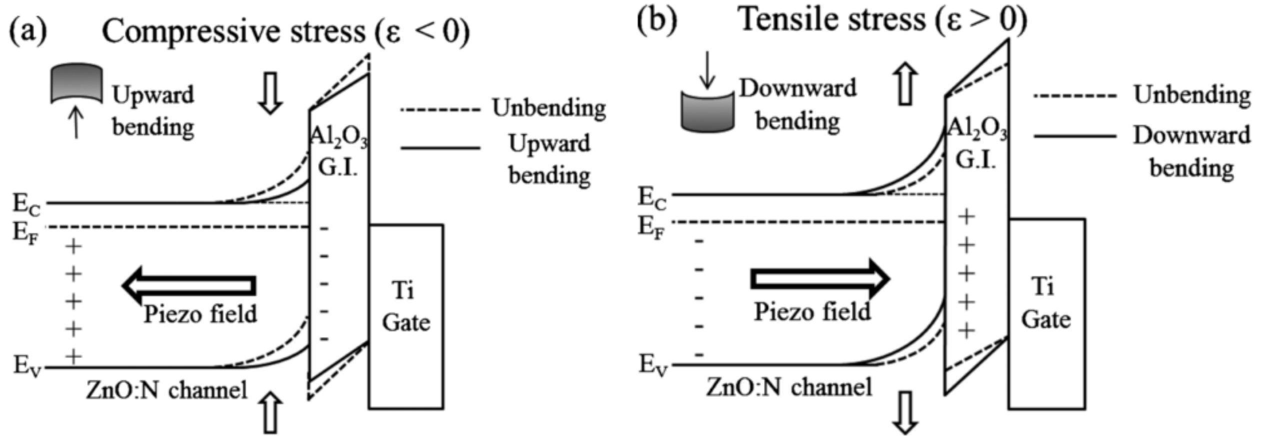

Fig. 2.5 band diagrams of ZnO:N channel/Al_2O_3 gate insulator/Ti gate indicating the piezoelectricity mechanism occurred in flexible TFTs in response to external stresses, (a) compressive stress, and (b) tensile stress [41].

In Fig. 2.5(a), when the TFT is under compressive stress, a negative piezoelectric field is produced in the semiconductor, which helps to reduce the ZnO:N channel surface potential barrier. Consequently, a negative shift of V_T is observed since less gate voltage is needed to reach the channel accumulation layer for the formation of an electrical channel. Oppositely, a positive piezoelectric field is generated at the ZnO channel/gate insulator interface when the device is bent downwards, as shown in Fig. 2.5(b). As a result, the potential barrier increases, leading to a positive shift of V_T.

A recently published paper by K. T. Eun et al. [44] illustrated the fabrication of flexible ZnO TFTs by transfer printing process. It focused on the formation and growth of cracking in the SiO_2 bridges when the bending radius goes down to 11 mm. The bridges are used to connect individual TFT devices which are more susceptible for stress concentration due to the device layout and structure. Stress analysis after mechanical bending is also performed by the finite element method (FEM). The numerical simulation shows stress concentration at the edge of the SiO_2 bridge layer, which can be compensated by optimizing the bridge structure through the FEM model to prevent failure of the TFT devices.

Chapter 3 Experimental

3.1 Characterization of Thin Films

With the explosive growth of thin-film utilization in flexible microelectronics, it becomes significant to understand the intrinsic nature of films. Various technologies are used for measuring and analyzing internal structure, surface morphology, film composition, and internal stress and strain for thin-film applications, include X-ray diffraction, electron microscopy, and mechanical testing.

3.1.1 Scanning Electron Microscopy

The scanning electron microscope (SEM) is the most important electro-optical instrument that provides highly resolved surface images for the investigation of bulk specimens, and is considered as a relatively rapid, inexpensive, and non-destructive surface analytical technique.

The fundamental principle of SEM is that, it uses a focused beam of high-energy electrons to generate a variety of signals from the solid specimens. The signals that derive from the interactions reveal the material information, such as the external morphology (texture), chemical composition, and crystalline structure and orientation. In detail, electrons are first accelerated with significant kinetic energy through a voltage difference (usually about 0.1 keV to 50 keV) between cathode and anode. The incident electrons are then decelerated in the solid sample, and the kinetic energy is dissipated as a variety of signals. The types of signals produced in SEM include Secondary Electrons (SE), Backscattered Electrons (BSE), characteristic X-rays, photons, specimen current and transmitted electrons. Among those signals, secondary electrons and backscattered electrons are commonly used for imaging samples. By convention, electrons with exit energies larger than 50 eV are called backscattered electrons, and those with energies less than 50 eV are classified as secondary electrons. The secondary electrons are used to present the morphology and topography of samples, while the backscattered electrons are most useful for displaying compositional in multiphase samples [45, 46].

This study uses secondary electrons to present the surface morphology of ZnO thin films deposited on silicon substrate using AJA sputtering system, and the SEM images are shown in Fig. 3.1. The ZnO film is deposited using a ZnO target with deposition power of 100 W, deposition pressure of 5 mTorr, deposition gas argon (Ar) and oxygen (O_2) ratio of 12: 1. In order to improve the film quality, ZnO films are first deposited as buffer layer at 220 ˚C, the deposition temperature is then reduced

to room temperature for the subsequent film deposition. Fig. 3.1 shows the SEM micrographs of a nanocrystalline ZnO layer having rounded fine particles with dimensions range around 33 nm. The film thickness is 370 nm, measured by a Dektak Profilometer.

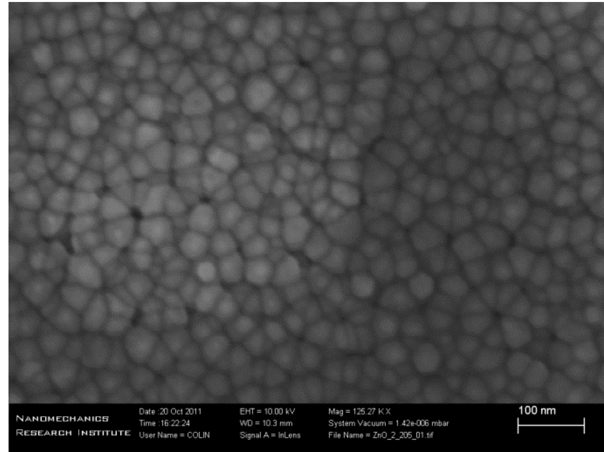

Fig. 3.1 SEM images of the ZnO thin film deposited on silicon substrate (Magnification: 125.27 K×).

3.1.2 Atomic Force Microscopy

Atomic Force Microscopy (AFM) is a high resolution imaging technique to see the shape of a surface in three-dimensional detail by measuring the surface height down to the nanometer scale using a sharp solid force probe. AFM offers unique perspective for the study of surface morphology of various materials, no matter if it is hard or soft, synthetic or natural, irrespective of opaqueness or conductivity, which is beyond the limits of conventional optical microscopic methods. Commercially available AFM tips with a tip radius of curvature on the order of nanometers, integrated with force sensing cantilevers, are microfabricated from silicon and silicon nitride by lithographic and anisotropic etching techniques. Either the force probe may move over a stationary sample or the sample can move under the fixed probe. With the tip of the cantilever approaches the surface of a sample, the force between the tip and sample surface results in the vertical deflection of the cantilever [47].

Based on the nature of the interactions between the scanning tip and the sample surface, AFM scanning can be classified into three modes: contact mode, noncontact mode, and tapping mode. In contact mode, the scanning tip makes a direct contact with the sample surface throughout the scanning period to obtain the topographic features of the surface based on the degree of cantilever

reflection. It provides high scan speeds, but the combination of lateral forces and high normal forces may damage soft samples due to scraping between the tip and the sample.

In noncontact mode, both the tip-sample separation and the oscillation amplitude are in the order of 1-10 nm, thus the tip does not contact the sample surface. Because no forces are exerted on the sample surface, it helps to reduce the surface damage associated with the contact mode. However, the noncontact mode has limited applications, and is usually suitable for scanning extremely hydrophobic samples in order to avoid getting stuck when contacting the adsorbed fluid layer.

In tapping mode, the scanning tip is literally bouncing up and down as it travels across the sample surface, while maintaining the vertical movement of the cantilever at constant oscillation amplitude throughout the scanning period. The oscillation amplitude of the probe tip is much larger than that of the noncontact mode, often in the range of 20-200 nm. Tapping mode is regarded as the most useful scanning mode for almost all the applications due to its less destructive effects on both the sample surfaces and the tips, whereas the disadvantage is the slightly slower scan speed than the contact mode [48, 49].

Based on the use of AFM under tapping mode, the three-dimensional surface morphology of the same ZnO film as described in the SEM image is shown in Fig. 3.2. Roughness measurements are performed over the selected 1μm × 1μm region of the film surface. The AFM analysis shows a relatively smooth surface with a root mean square (RMS) roughness of 3.6 nm. The Z scale is 30nm. The ZnO layer shows textured with a preferential c-axis orientation in accordance with the strongly predominant (0 02) reflection of the wurtzite ZnO phase. The average size of grains observed in the AFM mage was measured to be about 39 nm, which is close to the results obtained from the SEM image as shown in Fig. 3.1.

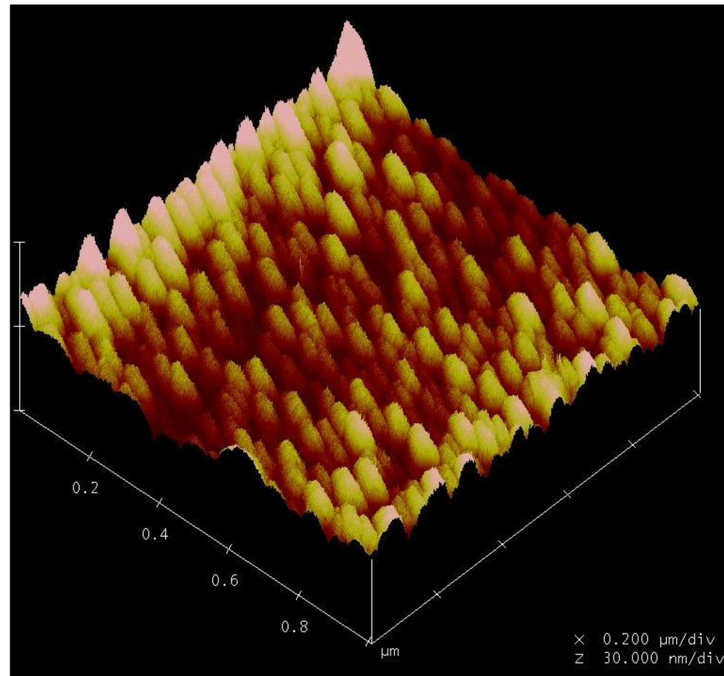

Fig. 3.2 AFM image of a nanocrystalline ZnO film deposited using RF-sputtering method.

3.1.3 Stress Gauge Measurement

When a thin film is deposited to a silicon wafer, it may lead to a certain amount of bow to the wafer. The accurate measurement of this bow contributes to the computation of the stress in the thin film. The Ionic Systems' stress gauge provides a quick, repeatable, and nondestructive way to measure film stress on production wafers. It measures the deflection in a substrate by means of reflected light using a fiber-optic bundle which contains both transmitters and receivers of light. The intensity of returning light indicates the distance from the end of the bundle to the back of the wafer. For comparison purposes, distance readings are recorded before and after thin-film deposition on the wafer, so the difference in the readings is the total deflection caused by the thin-film deposition. The stress in the film is then determined by substituting the total deflection into a simplified Stoney formula [50, 51]:

$$\text{Stress} = \frac{4d}{D^2} \cdot \frac{E_s}{3(1-v)} \cdot \frac{T_s^2}{T_f} \qquad \text{(Eq. 3.1)}$$

where E_s is Young's modulus for the substrate, v is the Poisson's ratio for the substrate, D represents the substrate support diameter, T_s and T_f are the thicknesses of the substrate and the film, respectively.

A schematic of the thin-film stress measurement using Ionic Systems' stress gauge is shown in Fig. 3.3. If a bare wafer has bowed away from the light sensor after film deposition, the coating is under compressive stress. Likewise, when the wafer bows towards the light sensor with a decreasing of the gap between the wafer and the probe, it is under tensile stress.

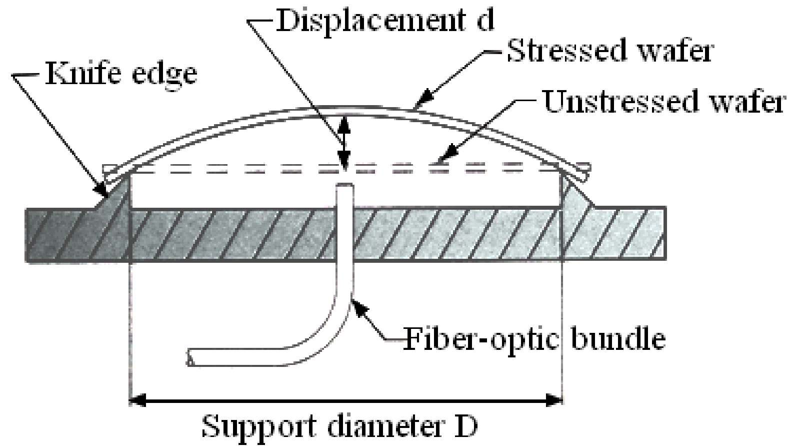

Fig. 3.3 Schematic of thin-film stress measurement [52].

The samples used for stress gauge measurement are ZnO films which deposited on silicon wafers using deposition power of 80 W, 100 W, and 120 W, respectively. Other deposition parameters are kept constant, including pressure of 5 mTorr, Ar:O_2 ratio of 12:1, room temperature deposition, deposition time of 25 minutes. The Young's modulus of silicon is 130 GPa, the substrate is 3-inch silicon wafer with thickness of 0.4mm. The Poisson's ratio is 0.28. The thickness of the films deposited under 80 W, 100 W, and 120 W are 35.5 nm, 49 nm, and 71 nm, respectively. Inserting these data into Eq. 5, the corresponding film stresses are -33 MPa, -52 MPa, and 19 MPa, separately. The experimental results indicate that the parameters used during the thin film deposition process, such as power and deposition temperature, has non-negligible influence on the residual stress in the film. It is also feasible to optimize the combination of deposition parameters for a multilayer structure in such a way that the compressive stresses and tensile stresses generated in each layer by different parameters are compensated, so that the total stresses in the thin film stack could be significantly reduced.

3.1.4 X-Ray Diffraction

X-Ray Diffraction (XRD) is a non-destructive technique for determining the crystalline structure of solid materials. When analyzing thin films with thickness varies in the rage of 1 - 1000 nm, the conventional θ - 2θ scanning method generally produces a weak signal from the film and an intense signal from the substrate. An effective method to avoid intense signal from the substrate and to collect stronger signal from the thin film is to perform Grazing Incidence X-ray Diffraction (GIXRD) analysis. It involves a scan with a fixed grazing angle of incidence, which is generally chosen to be slightly above the critical angle for total reflection of the film material. A schematic of the setup and operation of the X-ray diffractometer is shown in Fig. 3.4 (a). The diffractometer has an incident angle of ω, a scattering angle of 2θ, a rotation about the film surface normal of φ, and an inclination perpendicular to the scattering plane of Ψ, as shown in Fig. 3.4 (b).

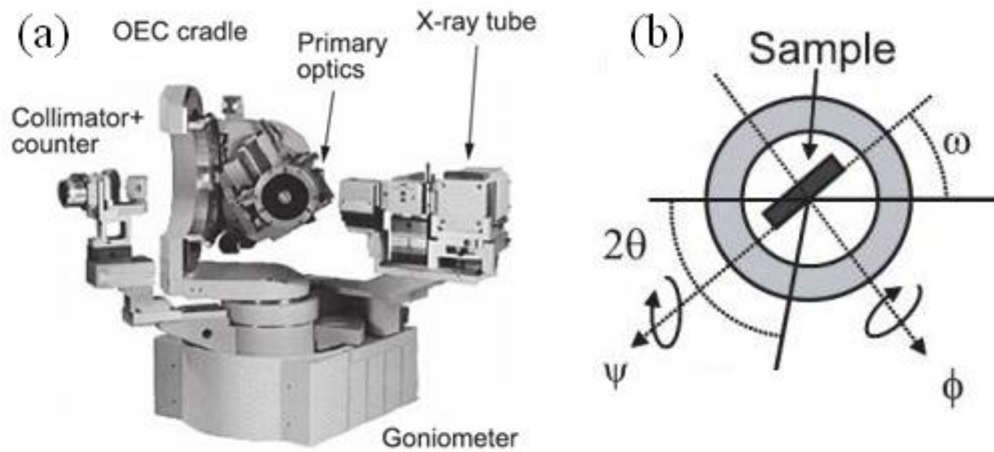

Fig. 3.4 (a) Geometric arrangement of a high resolution X-ray diffractometer (PANalytical X'pert Pro MRD system), and (b) schematics of some primary operation parameters [53].

A schematic of the X-ray incident and diffraction directions of GIXRD is shown in Fig. 3.5. In the coordinate system of the thin-film specimen, S_1 represents the sample surface. L_3 is the normal of diffraction planes (hkl) for which spacing is measured. L_1 and L_2 are the two orthogonal axes lying on the (hkl) plane. The angle between the sample surface and the diffracting plane is α. The incident X-ray beam making a grazing angle ω with respect to the specimen surface and the grazing angle is kept constant during the rotation of the sample. The incident wave will generate the diffracted wave with atomic planes in the film when conditions satisfy Bragg's Law ($n\lambda = 2d \sin \theta$). The main advantages

of GIXRD is that it provides information on the structure of very thin surface layer, especially for the study of thin films deposited on substrate whereas the substrate might affect the diffraction data in standard XRD, such as polymers, glass, or crystalline Si [54, 55].

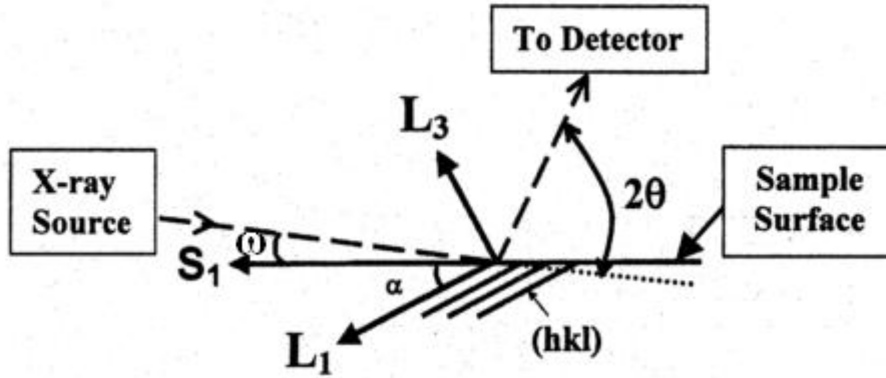

Fig. 3.5 Diffraction geometry of GIXRD for thin film analysis, it shows X-ray incident and diffraction directions [54].

In the present study, GIXRD analysis of a thin film of ZnO is performed with the PANalytical X'pert Pro MRD (Materials Research Diffractometer) system. The X-ray diffractometer is equipped with a Cu tube, with a generator setting of 45 kV and 35 mA. The grazing incident angle (ω) is fixed at 0.3°. Patterns were collected from 30 ° to 60 ° of 2θ using a step size of 0.03° and a count time of 2s per step. The ZnO sample is deposited at 220 ℃, using deposition power of 100 W, pressure of 5 mTorr, and gas ratio Ar:O_2 of 12:2. The film thickness is 280 nm. The results of the GIXRD scan are shown in Fig. 3.6.

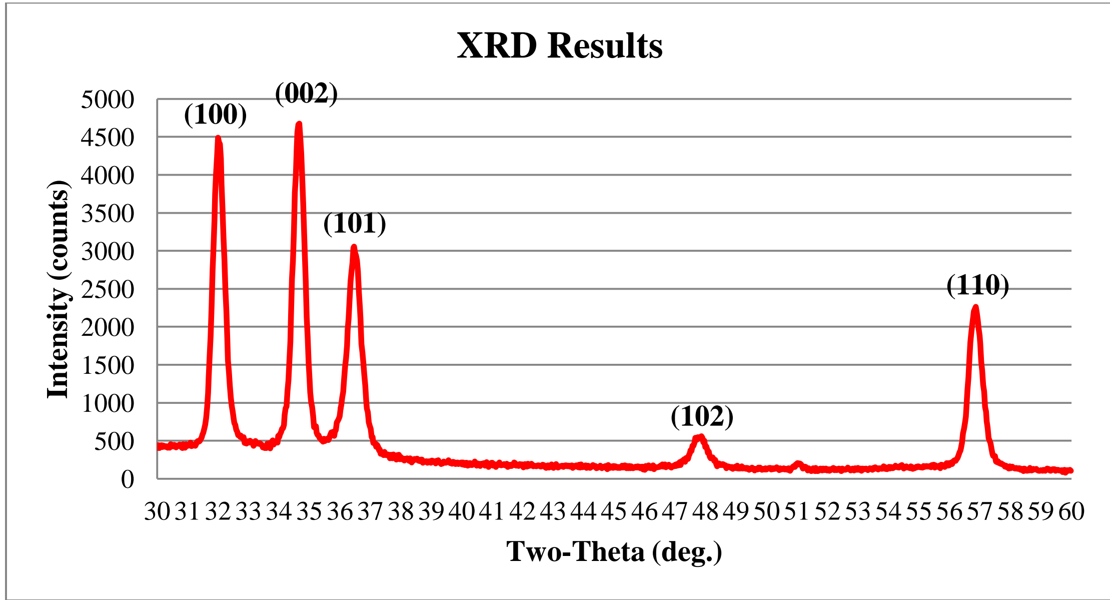

Fig. 3.6 GIXRD analysis of ZnO thin film by varying two-theta from 30 °to 60 °.

In the pattern, the first three peaks with highest intensity represent the (hkl) planes of (100), (002), and (101), respectively. Because the structure of ZnO is hexagonal, the applicable plane spacing equation is [56]:

$$\frac{1}{d^2} = \frac{4}{3}\left(\frac{h^2+hk+k^2}{a^2}\right) + \frac{l^2}{c^2} \qquad \text{(Eq. 3.2)}$$

Combining Bragg's law ($\lambda = 2d \sin \theta$), the lattice parameters of the ZnO film is derived from the position of the (002) diffraction peak. When the wavelength λ is 1.5418 Å, the calculated plane spacing d is 2.5898 Å, and the lattice constant c of ZnO film is 5.1796 Å. The lattice constant can be further utilized to evaluate the average uniform strain, e_{zz}, in the lattice along the c-axis [57]:

$$e_{zz} = \frac{c-c_0}{c_0} \qquad \text{(Eq. 3.3)}$$

where c_o refers to the lattice constant c of ZnO bulk, which is 5.2066 Å.

The biaxial film stress is related to the calculated c-axis strain by the relation:

$$\sigma = \frac{2C_{13}^2 - C_{33}(C_{11}+C_{12})}{2C_{13}} e_{zz} \qquad \text{(Eq. 3.4)}$$

where C_{ij} are elastic stiffness constants. For polycrystalline ZnO, the values are: C_{11}=209.7 GPa, C_{12}=121.1 GPa, C_{13}= 105.1 GPa, C_{33}=210.9 GPa [58]. The biaxial stress for the as-grown ZnO films is derived from Eq. 3.3 and 3.4, which is -1.17 GPa. Compared with the stress gauge measurements of ZnO film deposited at room temperature with compressive stress of 52 MPa, the XRD results indicates that, a much larger residual stress is generated in the ZnO deposited at 220 ℃ due to the significant decrease in temperature from as high as 220 ℃ to room temperature. Post annealing is usually performed after the film deposition to relieve the residual stress in the film, and previous findings has indicates an effective relaxation of the residual compressive stress after rapid thermal annealing. As shown by Y.-C. Lee et al. [59], the residual stress in ZnO film can be decreased from -0.8 GPa to 0.2 GPa after annealing at 800 ℃ for 1 minute .

Assuming a homogeneous strain exists in the ZnO films, the average grain size of the film can be estimated from the full-width at half- maximum (FWHM) of (002) peak by Scherrer relation [60]:

$$\tau = \frac{K\lambda}{\beta\cos\theta} \qquad \text{(Eq. 3.5)}$$

where τ is the mean grain size, K is the shape factor (typically equals to 0.9), λ is the X-ray wavelength, β is the line broadening at half the maximum intensity (FWHM) in radians and θ is the Bragg angle. The average grain size of the ZnO film calculated from Eq. 3.5 is 17 nm. It satisfies the restriction of the Scherrer equation that it is limited to nanoscale particles and not applicable to grains larger than about 0.1 μm. In addition, it shows that the average size of grains measured from the XRD method is smaller than the SEM and AFM measurements. Actually, the Scherrer formula provides a lower bound of the particle size due to the fact that a variety of factors (e.g. dislocations, grain boundaries) can contribute to the width of a diffraction peak besides the instrumental effects and crystalline size. As a result, the crystalline size can be larger than the predicted value by the Scherrer formula.

3.2 Bending Test of TFTs

In order to study the flexibility of thin-film transistors, specific bending testers are designed to perform the mechanical bending of flexible devices. A schematic of a bending tester under operation is shown below.

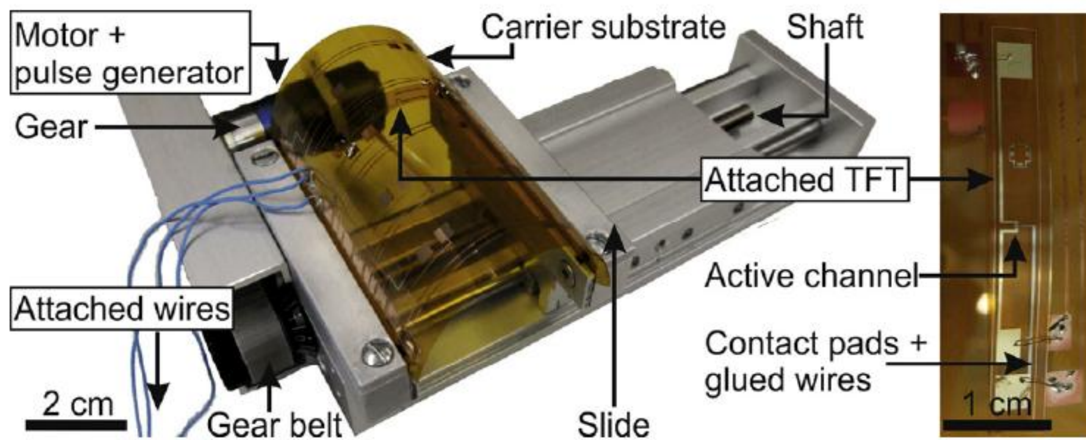

Fig. 3.7 Photograph of a bending tester with a loaded carrier substrate and an attached flexible TFT [61]. The bending radius is about 19 mm.

A flexible foil substrate with TFTs attached is loaded on the bending tester by clamping the edge of the foil with two metal plates. One plate is fixed on the machine, while the other plate can be moved by rotating a shaft screwed through it, where one complete rotation of the shaft corresponds to a horizontal movement of 1 mm. The bending of the TFTs on the flexible substrate is performed by varying the horizontal distance between the two plates, and the resulting bending stress and strain, as well as the bending radius are analyzed. The mechanical bending of flexible TFTs described above can be simulated using FEM, and the details of the numerical modeling are discussed in Chapter 4.

Chapter 4 Modeling of Flexible ZnO TFTs

Finite element method (FEM) is used to accurately model products and processes by determining structural integrity, performance and reliability, as well as predicting structural failures. In the present study, the states of stress and strain in the deposited thin films of TFT devices and their distribution after mechanical bending are simulated using finite element analysis. COMSOL Multiphysics is used for the numerical simulation. Moreover, in order to improve the numerical approximation, the theoretical models of stress and strain relations in multilayer thin films are summarized and used as a framework of the numerical model for achieving consistent simulation results of mechanical properties in multilayer thin film stacks and TFT devices.

4.1 Analytical Model

Analytical models are mathematical formulas that can be expressed as analytic functions to describe changes in a system. With the increasing interest in the application of flexible electronics, it is of importance to investigate the states of stress and strain in flexible thin-film transistors resulting from the deposition process and external mechanical deformation. Firstly, simulation of a single thin film deposited on a thick substrate is presented, then the model is extended for a multilayer structure, and finally the developed models are used for the simulation of TFT devices.

4.1.1 Strain and Stress Analysis of a Single Thin-Film on Thick Substrate

4.1.1.1 Origin of intrinsic stresses during thin-film growth

Thin-film materials play an important role in a variety of technological applications including microelectronic devices, photonic and magnetic devices, and surface coatings. However, due to the use of various fabrication and post-processing processes and different intrinsic material properties involved, stress and strain commonly exist in thin films as a result of constraints imposed by their substrates. The originated stresses may possibly be related to the following factors [62]:

i. Different thermal expansion coefficients of film and substrate

ii. Differences in lattice spacing, interatomic spacing or crystal size

iii. Incorporation of atoms such as residual gases or chemical reactions

iv. Voids, dislocations

v. Recrystallization processes

vi. Phase transformations

When a thin film and a substrate has different thermal expansion coefficients, the temperature changes during film deposition and post processing will produce stress and strain, which are called thermal stress and thermal strain. Furthermore, because the atoms of the substrate have specific atomic size and arrangement, if the atomic spacing of the film is not corresponding to those of the substrate, it will result in stresses in the film-substrate combination. The stresses resulting from the internal structure of a material during its deposition is generally regarded as intrinsic stresses, which are less clearly understood than the thermal stress and will be discussed in the following numerical simulation.

4.1.1.2 Fundamental formulas for stress and strain in thin films

In the present study, thin films are deposited on substrate using Physical Vapor Deposition (PVD). During the PVD processes, thin films are deposited on substrates at elevated temperatures. Then the film/substrate composite is cooled to room temperature, during which they contract by different amounts owing to different thermal expansion coefficients. The film is subsequently strained elastically to match the substrate and remain attached, causing the substrate and film combination to bend. For the numerical simulation, suppose each layer of thin film is linear elastic material and the film/substrate system is subject to very small deformation during temperature change. The resulting thermal stresses presented by Hooke's law is

$$\sigma_{th} = E\,\alpha\,(T - T_0) \qquad \text{(Eq. 4.1)}$$

where α is the coefficient of linear thermal expansion which is constant along the temperature change, E is the Young's modulus, T_0 and T are the initial and final temperatures. The Young’s modulus is assumed to be constant during the temperature variation.

It is known that, when the film and the substrate are bonded together and cannot slide relative to each other, mismatch forces arise at the interface to maintain the bonding states [62], as shown in Fig. 4.1.

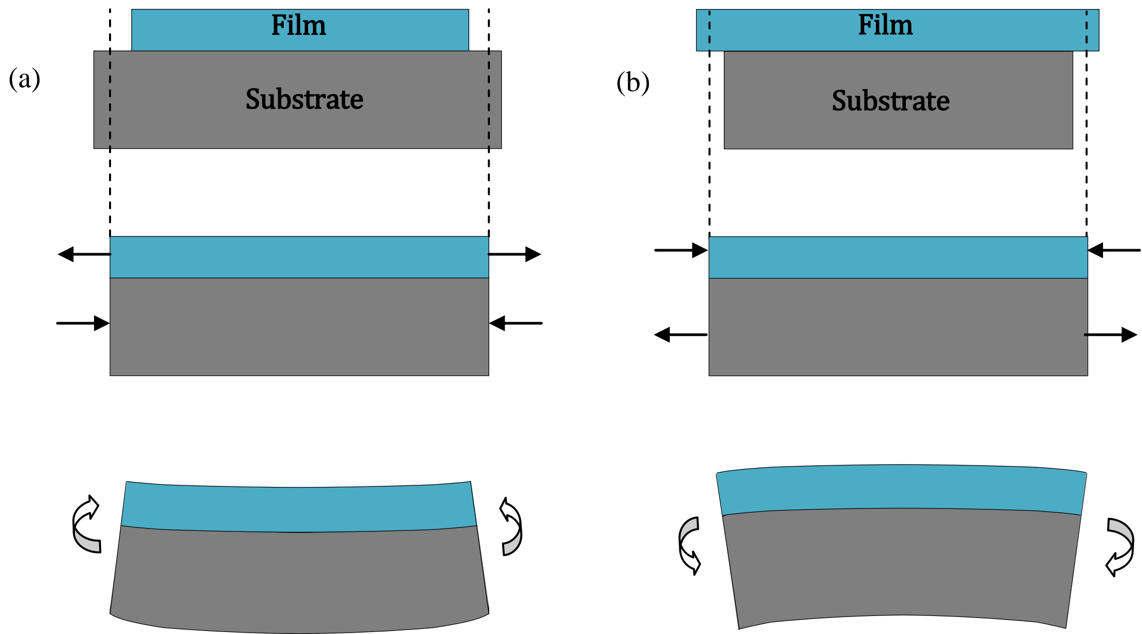

Fig. 4.1 Schematic of film-substrate combination under residual stresses. (a) Tensile stresses in the film; (b) compressive stresses in the film.

In Fig.1 (a), when the growing film initially shrinks relative to the substrate, the film is stretched and the substrate is contracted to keep the same length. To keep force balance, the tensile force developed in the film are balanced by the compressive force in the substrate as

$$F_f = F_s \tag{Eq. 4.2}$$

where F_f and F_s are inducing forces in the film and substrate, respectively.

The film/substrate combination is not in mechanical equilibrium because of the uncompensated end moments. Thus, if the substrate is compliant and unconstrained from moving, it will elastically bend to counteract the unbalanced moments. As a result, the substrate with films containing internal tensile stresses bends concavely upward. Similarly, the substrate with compressively stressed films bends convexly outward, as shown in Fig. 1(b). When the tensile stresses become extensively large, it can cause film fracture, whereas extremely large compressive stresses may result in film buckling and partial loss of adhesion to the substrate, which are not discussed in this study.

A film-substrate combination subjected to a temperature differential ΔT and bend convexly upward is shown in Fig. 4.2.

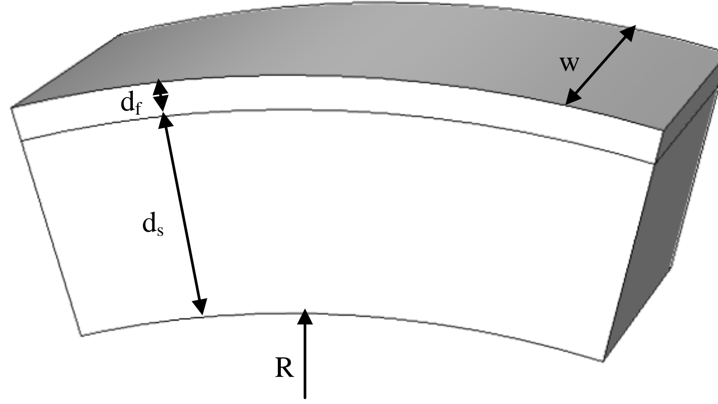

Fig. 4.2 Schematic of thin film-substrate couple after temperature change.

The strains in the film and the substrate are

$$\varepsilon_f = \alpha_f \Delta T + \frac{F_f(1-v_f)}{E_f d_f w} \quad \text{(Eq. 4.3)}$$

$$\varepsilon_s = \alpha_s \Delta T - \frac{F_f(1-v_s)}{E_s d_s w} \quad \text{(Eq. 4.4)}$$

where E is the Young's modulus, d is the layer thickness, w is in plane width, v is the Poisson's ratio, the subscript s and f refer to substrate and film, respectively. The first term on the right hand side of the formula refers to thermal strain, and the second term represents the elastic strain. In order to account for biaxial stress conditions, the Young's modulus E is generally replaced by E/(1-v), which are called biaxial modulus.

The strain compatibility requires that

$$\varepsilon_f = \varepsilon_s \quad \text{(Eq. 4.5)}$$

By inserting Eq. 4.3 and Eq. 4.4 into Eq. 4.5, the mismatch force is

$$F_f = \frac{w(\alpha_s - \alpha_f)\Delta T}{\left(\frac{1-v_f}{d_f E_f}\right) + \left(\frac{1-v_s}{d_s E_s}\right)} \quad \text{(Eq. 4.6)}$$

Suppose the force act uniformly over the film cross section (d_f w) giving rise to the film stress, if $d_s E_s/(1-v_s) \gg d_f E_f/(1-v_f)$, the thermal stress in the film is

$$\sigma_f(T) = \frac{F_f}{d_f w} = \frac{(\alpha_s - \alpha_f)\,\Delta T\, E_f}{1 - v_f} \qquad \text{(Eq. 4.7)}$$

It should be noted that, the numerical model is built based on the assumption that the stress distribution is uniform throughout the same isotropic material, and the calculated stress is the average value over the cross-section, other effects such as boundary restraints or stress concentration are ignored.

4.1.1.3 Built-in strain and built-in stress

As it is discussed before, there are several factors corresponding to the formation of intrinsic stress and strain in thin films. The strain arises from atom deposition in out-of-equilibrium positions during film growth is considered as built-in strain. When the built-in strain is considered, the total strain in the film becomes

$$\varepsilon_f = \alpha_f \Delta T + \varepsilon_{bi} + \frac{F_f(1 - v_f)}{E_f d_f w} \qquad \text{(Eq. 4.8)}$$

It is evident that the strain in the film is mainly composed of thermal strain, built-in strain and elastic strain.

The relationship between built-in strain and built-in stress is [63]

$$\varepsilon_{bi} = -\frac{\sigma_{bi}}{E_f^*} \cdot \left(1 + \frac{E_f^*\, d_f}{E_s^*\, d_s}\right) \qquad \text{(Eq. 4.9)}$$

where $E_f^* = E_f/(1 - v_f)$, and $E_s^* = E_s/(1 - v_s)$

The strain in thin films can be induced by the change of deposition temperature, deposition rate and pressure in the deposition chamber, incorporation of impurities during film growth, different grain structure, fabrication process defects, etc. Generally, both stress and strain are not uniformly distributed across the film-substrate combination. In this study, the built-in stress is an average value extracted from the stress gauge measurements for a given film/substrate couple.

4.1.1.4 Stress/strain distribution as a result of applied bending moment

Suppose an isolated beam possesses a longitudinal plane of symmetry, and is subjected to a pair of bending moments M [62, 64], as shown in Fig. 4.3. For reasons of symmetry only the right half of the beam is presented.

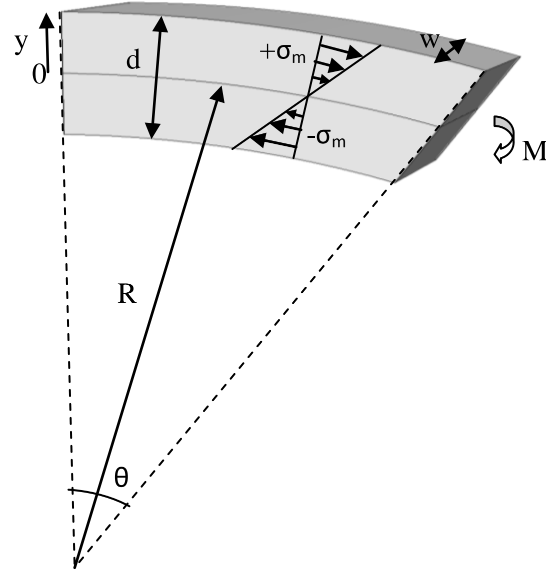

Fig. 4.3 Elastic bending of beam under applied end moment.

After uniform bending, the beam is curved forming an arc with radius R and subtended angle θ. Consider a fiber of distance y above the neutral axis which is unstrained, due to the strain is the linear variation of a dimension relatively to an initial value, the strain in the bending direction is linear in y, namely:

$$\varepsilon = \frac{(R+y)\theta - R\theta}{R\theta} = \frac{y}{R} \qquad \text{(Eq. 4.10)}$$

It shows that, the deformation of the beam fibers is proportional to their distance from the neutral axis. Accordingly, the stress distribution varies linearly across the section from maximum tension ($+\sigma_m$) to zero at the neutral axis and to maximum compression ($-\sigma_m$). According to Hooke's law, the maximum and minimum stresses of the beam are

$$\sigma_m = E\left(\frac{\left(R \pm {}^{d}/_{2}\right) - R\,\theta}{R\,\theta}\right) = \pm\,\frac{E\,d}{2\,R} \qquad \text{(Eq. 4.11)}$$

Corresponding to the stress distribution is the bending moment across the beam section:

$$M = 2\int_0^{d/2} \sigma_m w\left(\frac{2y}{d}\right)\, y\, dy = \frac{\sigma_m d^2 w}{6} = \frac{E\, d^3 w}{12\, R} \qquad \text{(Eq. 4.12)}$$

By extension of this result to a thin film deposited on substrate structure, we have

$$M_f = E_f d_f^3 \frac{w}{12R} \quad \text{(Eq. 4.13)}$$

$$M_s = E_s d_s^3 \frac{w}{12R} \quad \text{(Eq. 4.14)}$$

The loading condition for a pure bending of the beam requires that the clockwise and counterclockwise moments are compensated, a condition expressed by

$$\left(\frac{d_f+d_s}{2}\right) F_f = \frac{w}{12R} \left(\left(\frac{E_f}{1-v_f}\right) d_f^3 + \left(\frac{E_s}{1-v_s}\right) d_s^3\right) \quad \text{(Eq. 4.15)}$$

where the E is replaced by E/(1-v) to account for biaxial stress distribution rather than uniaxial stress.

In the case that the thickness of the substrate is much larger than the film, the film stress σ_f is, to a good approximation, given by

$$\sigma_f = \frac{F_f}{d_f\, w} = \frac{E_s d_s^2}{6R(1-v_s)\, d_f} \quad \text{(Eq. 4.16)}$$

which is the Stoney formula. If the radius of curvature of the film-substrate combination can be measured or calculated, then the stress in the film can be determined accordingly. It should be noted that the stress calculated by Stoney method is an average value by integrating the stress over the cross-section of the beam.

By Eq. 4.7 and Eq. 4.16, we have

$$\frac{1}{R} = \frac{6E_f\,(1-v_s)d_f}{E_s\,(1-v_f)d_s^2}\,(\alpha_s - \alpha_f)\Delta T \quad \text{(Eq. 4.17)}$$

This modification of Stoney equation represents the extent of bowing because different thermal expansion effects cause the stress.

The distance between neutral axis and the bottom surface of the substrate is

$$\eta = \frac{E_s d_s^2 + E_f d_f (2d_s + d_f)}{2(E_s d_s + E_f d_f)} \quad \text{(Eq. 4.18)}$$

where d_s and d_f are substrate thickness and film thickness, respectively; E_s and E_f are Young's modulus of the substrate and the film, respectively.

4.1.2 Strain and Stress Analysis of Thin-Film Multilayers on Thick Substrate

4.1.2.1 Formulation of stress and strain models for multiple thin films on compliant substrates

Suppose a multilayer structure is composed of n-1 continuous thin films deposited on a thick substrate with different mechanical properties, as shown in Fig.4.4. The substrate thickness d_s is greater than the total thickness of all the films ($d_s \gg \sum_{i=2}^{n} d_i$). The height coordinate of the stack is

$$h_n = \sum_{i=1}^{n} d_i \quad \text{(Eq. 4.19)}$$

Because of the layer's different properties and all the layers are confined at each interface, elastic strains will form to accommodate these differences, giving rise to internal stresses and moments in each layer, causing the structure to experience bending and planar relaxation until the whole structure is in equilibrium, thus no resultant edge forces or applied moments are remained.

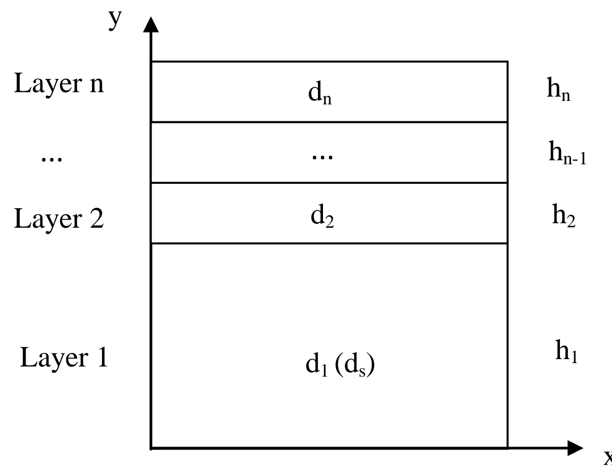

Fig. 4.4 Schematic of a n-layer stack.

According to Newton's third law of motion, when the layers are bonded together, the reaction forces resulting from the adjacent layer will act as applied forces in the layer i, which will balance each other out to the point of zero net force, lead to

$$\sum_{i=1}^{n} F_i = 0 \quad \text{(Eq. 4.20)}$$

To keep equilibrium, bending occurs to balance out the bending moments caused by the reaction forces, and the total moment must be null, that is

$$\sum_{i=1}^{n} M_i = 0 \quad \text{(Eq. 4.21)}$$

The bending relatively to the bending axis is caused by the total internal moments which appear in each layer, and are symmetrical to the bending moments formed by the applied forces in that layer.

The total curvature is the sum of the individual films contributions due to the moments being additive, it therefore indicates that each film independently interacts with the substrate without taking account of the adjacent films or the stacking sequence of films in the composite structure.

The stress in the i-th film is [65]

$$\sigma_{fi} = \frac{E_s d_s^2}{6R_i(1-v_s)\, d_{fi}} \quad \text{(Eq. 4.22)}$$

And the total stress in the n stacked films is

$$\sigma_{fi} = \frac{E_s d_s^2}{6(1-v_s)} \cdot \frac{1}{\sum_{i=2}^{n} d_{fi}} \cdot \sum_{i=2}^{n} \frac{1}{R_i} \quad \text{(Eq. 4.23)}$$

where R_i and d_{fi} are the radius of curvature and thickness of the i-th film, respectively.

The strain equation of a single film on substrate can be extended to any number of layers. The strain in the i-th film with respect to the free-standing film at the same temperature can be expressed as

$$\varepsilon_{fi} = \frac{\sum_{i=2}^{n} E_s^* d_s[\left(T-T_d^i\right)(\alpha_s-\alpha_i)+\varepsilon_{bi}^i]}{E_s^* d_s+\sum_{i=2}^{n} E_{fi}^* d_{fi}} \quad \text{(Eq. 4.24)}$$

Similarly, the strain in the substrate coated with multiple films with respect to the uncoated substrate at the same temperature is

$$\varepsilon_s = \frac{\sum_{i=2}^{n} E_{fi}^* d_{fi}[\left(T_d^i-T\right)(\alpha_s-\alpha_i)+\varepsilon_{bi}^i]}{E_s^* d_s+\sum_{i=2}^{n} E_{fi}^* d_{fi}} \quad \text{(Eq.4.25)}$$

where $E_i^* = E_i/(1-v_i)$, T_d^i is the deposition temperature of the i-th layer, E_{fi} and ε_{bi}^i are Young's modulus and built-in strain of the i-th film, αs and α_i are the thermal expansion coefficient of the substrate and the i-th layer, respectively.

The above theories and formulas for a film-substrate combination can be extended to any number of layers. For a three-layer structure using the same deposition temperature, the strain of the substrate at room temperature with respect to uncoated substrate is [63]

$$\varepsilon_s(Tr) = \frac{E_{f1}^* d_{f1}[(T_d - T_r)(\alpha_s - \alpha_{f1}) + \varepsilon_{bi1}] + E_{f2}^* d_{f2}[(T_d - T_r)(\alpha_s - \alpha_{f2}) + \varepsilon_{bi2}]}{E_s^* d_s + E_{f1}^* d_{f1} + E_{f2}^* d_{f2}} \quad \text{(Eq. 4.26)}$$

where f_1 and f_2 denote the first and second films, respectively. The above equation is valid no matter the two films are deposited on each side of the substrate or on the same side of the substrate.

For a three layer structure with Young's modulus of E_1, E_2, and E_3, and thickness of d_1, d_2, and d_3, if the Poisson ratio v is the same for all the three layers, the radius of curvature R of the relaxed three-layer structure at room temperature is given by [63]

$$R = \frac{d_1}{6(1+v)} \cdot \frac{(1 - \frac{E_2 d_2^2}{E_1 d_1^2} - \frac{E_2 d_2^2}{E_1 d_1^2})^2 + 4\frac{E_2 d_2}{E_1 d_1}(1 + \frac{d_2}{d_1})^2 + \frac{4E_3 d_3}{E_1 d_1}[\left(1 + \frac{d_3}{d_1}\right)^2 + \frac{3d_2}{d_1}\left(1 + \frac{d_2}{d_1} + \frac{d_3}{d_1}\right) + \frac{E_2 d_2}{E_1 d_1}\left(\frac{d_2^2}{d_1^2} + \frac{d_2 d_3}{d_1^2} + \frac{d_3^2}{d_1^2}\right)]}{\left(1 + \frac{d_2}{d_1}\right)\left[\frac{E_2 d_2}{E_1 d_1}(e_2 - e_1) + \frac{E_3 d_3}{E_1 d_1}(e_3 - e_1)\right] + \frac{E_3 d_3}{E_1 d_1}\left(\frac{d_2}{d_1} + \frac{d_3}{d_1}\right)[(e_3 - e_1) + \frac{E_2 d_2}{E_1 d_1}(e_3 - e_2)]} \quad \text{(Eq. 4.27)}$$

4.1.2.2 Stress/strain simulation due to applied mechanical bending of thin films on various platforms

When a pure bending moment if applied to a stack of films, under equilibrium conditions, the following conditions are satisfied [66]:

$$\sum_{i=1}^{n} F_i = \sum_{i=1}^{n} \int_{h_{i-1}}^{h_i} \sigma_i dy = 0 \quad \text{(Eq. 4.28)}$$

$$\sum_{i=1}^{n} M_i = \sum_{i=1}^{n} \int_{h_{i-1}}^{h_i} y\sigma_i dy = M_{app} \quad \text{(Eq. 4.29)}$$

Define the height of the mid-plane of each layer i as

$$h_{mi} = \frac{h_i + h_{i-1}}{2} = h_i - \frac{d_i}{2} \quad \text{(Eq. 4.30)}$$

The bending axis is

$$h_b = \frac{\sum_{i=1}^{n} E_i d_i h_{mi}}{\sum_{i=1}^{n} E_i d_i} \quad \text{(Eq. 4.31)}$$

where h_b is the position of the bending axis, where the resultant force due to bending is null. E_i is elastic modulus, d_i is the thickness of the i-th layer, $E_i\, d_i$ is the bending stiffness of the layer i.

For a stack of (n-1) thin films on thick substrate, the location of the bending axis is dominated by the location of the substrate mid-plane. The classical approximation for the bending axis is:

$$h_b^{class} = \frac{d_s}{2}\left(1 + \sum_{i=2}^{n} \frac{E_i d_i}{E_s d_s}\right) \quad \text{(Eq. 4.32)}$$

The above equation indicates that the position of the bending axis shifts from the substrate centerline, towards the interface between the thick substrate and thin films, by a small quantity of $\sum_{i=2}^{n} \frac{E_i d_i}{E_s d_s}$. When biaxial system is considered, the elastic modulus E in the above equation is replaced by E/(1-v).

4.2 Numerical Model

4.2.1 Two-Dimensional Model of Thin Film Deposited on Thick Substrate

4.2.1.1 Assumptions and boundary conditions used in numerical models

The plane strain model is commonly used in the numerical simulation, which assumes that the strain components along the propagation direction z are negligible compared to the strain in the x and y directions. In other words, it supposes that all out-of-plane strain components of the total strain ε_z, ε_{yz}, and ε_{xz} are zero. Loads in the x and y directions are allowed. The loads are assumed to be constant throughout the thickness of the material, but the thickness can vary with x and y.

For a thin film-substrate combination, the boundary condition applied is that, the lower-left corner of the substrate is fixed in both x and y direction, and the lower-right corner of the substrate is fixed in the y direction. This prevents rigid-body movements but has less effect on the stress distribution. The other boundaries are free to move. Besides, the interface of the film and the substrate are continuous so that the displacement of each layer will affect the other layers since they are in contact with each other.

4.2.1.2 Comparison of results for finite element analysis models with analytical model

Suppose a thin Al film is deposited on a silicon substrate, then the film-substrate couple is cooled from deposition temperature (T_d) to room temperature (T_r). The properties of the materials are given in Table 4.1.

Table 4.1 Material properties used in the numerical study.

Material	E [GPa]	v	α[˚C^{-1}]	Thickness [m]	Diameter [m]	T_d[˚C]	T_r[˚C]
Al film	70 [67]	0.33	23e-6	1E-7	1E-5	50	20
Si wafer	181[68]	0.28	3e-6	5E-6	1E-5	50	20

Based on the analytical model, the mismatch strain in Al film respect to substrate at room temperature:

$\varepsilon_m = (\alpha_s - \alpha_f)\,\Delta T = 6e\text{-}4$

According to Eq. 4.6, the mismatch force in the film-substrate system is $F_f = 6E\text{-}5$ N

So the stress in the film is $\sigma_f = \frac{F_f}{d_f\, w} = 60$ MPa

According to Eq.4.3, the film strain is -1E-4

The curvature of the film-substrate combination is

$\frac{1}{R} = \frac{6E_f\,(1-v_s)d_f}{E_s\,(1-v_f)d_s^2}\,(\alpha_s - \alpha_f)\Delta T = 5.98\ m^{-1}$

So the radius of curvature is 0.16 m

Based on the numerical model:

The thermal strain in the film $\varepsilon_{th\text{-}f} = -6.9e\text{-}4$

The thermal strain in the substrate $\varepsilon_{th\text{-}s} = -9e\text{-}5$

So the thermal mismatch strain is $\Delta\varepsilon_{th} = (\varepsilon_{th\text{-}s} - \varepsilon_{th\text{-}f}) = 6e\text{-}4$

It is known that the strain tensor of the film $\varepsilon_x = \frac{\partial u}{\partial x}$ and $\varepsilon_y = \frac{\partial v}{\partial y}$

where u and v are displacements in horizontal and vertical direction, respectively.

The strain tensor calculated by Comsol is $\varepsilon_x = -1.8E-4$

The stress tensor-x is [69]

$$\sigma_x = \frac{E}{(1+v)(1-2v)}\left[(1-v)\varepsilon_x + v\varepsilon_y\right] - \frac{\alpha E \Delta T}{1-2v} \qquad \text{(Eq. 4.33)}$$

The stress tensor-x component in the film calculated by Comsol is $\sigma_x = 60$ MPa

The bending profile of the film-substrate couple is simulated using Comsol, then the displacement data are plotted and fitted with a 4th degree polynomial curve by MATLAB. The formula for the radius calculation is shown below [70].

$$\text{Radius of curvature} = \frac{[1+(\frac{dy}{dx})^2]^{3/2}}{|\frac{d^2y}{dx^2}|} \quad \text{(Eq. 4.34)}$$

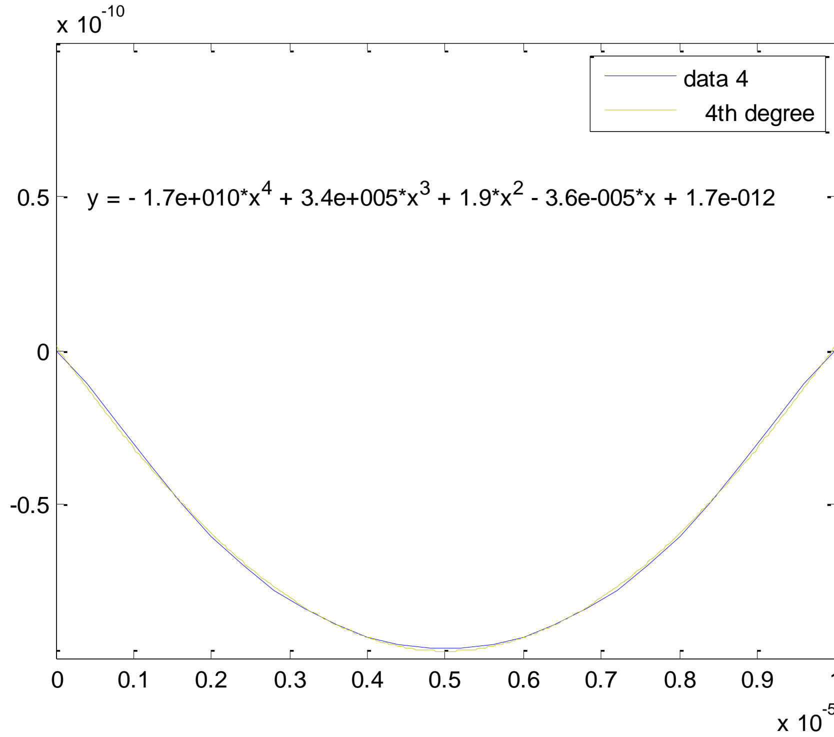

Fig. 4.5 Curve fitting using 4th degree polynomial by Matlab.

The radius of curvature of the film/substrate composition calculated from the mid-plane by Matlab and Comsol is R=0.11 m

It shows that the simulation results by Comsol is consistent with the numerical model, the small deviation is due to the different elasticity matrix are used. In Comsol, the elasticity matrix used for isotropic material is

$$[D] = \frac{E}{(1+v)(1-2v)} \begin{bmatrix} 1-v & v & 0 \\ v & 1-v & 0 \\ 0 & 0 & 0.5-v \end{bmatrix} \quad \text{(Eq. 4.35)}$$

Besides, the boundary condition involved can also affect the strain and stress states by restraining the boundary of the substrate during deformation, whereas for analytical model, the assumption is under ideal conditions that the film-substrate system is held flat during film deposition and free to bend upon cooling without applying external forces.

4.2.1.3 Stress/strain simulation due to applied mechanical bending

Consider an isolated beam is subjected to a pair of opposite bending moment of 1E-3 N ·m over the left and right ends of the TFT structure. Suppose the beam with Young's modulus E=181GPa, thickness d=5E-6m, in-plane width w=1m.The initial values of stress and strain in the TFT structure is negligible.

According to Eq. 4.12, radius of curvature of the beam after bending is

$R = \frac{E\, d^3 w}{12\, M} = 1.9E\text{-}3$ m

The maximum stress calculated from the numerical equation is

$$\sigma_m = \pm \frac{E\, d}{2\, R} = 2.4E + 8 \text{ Pa } = 240 \text{ MPa}$$

The stress and strain distribution simulated by Comsol is shown in Fig. 4.6 and 4.7. Fig. 4.6 shows the beam bends convexly upward compared to the original position which is shown as the black outline. The neutral axis is located at the geometrical central of the structure. Above the axis the beam is under tensile, and below the axis it is under compression. In Fig. 4.7, it shows the contour plot of stress tensor-x distribution throughout the beam. Different from the analytical model which shows the average values of stresses at ideal condition, the two dimensional simulation by Comsol indicates the variation trend of stress throughout the beam. It also shows the region of stress concentration due to the abrupt change in geometrical shape at the free edge of the beam. Since the stress/strain distributions in the flexible TFTs may affect the performance and stability of the devices, the numerical simulations can provide more practical predictions than the analytical solutions.

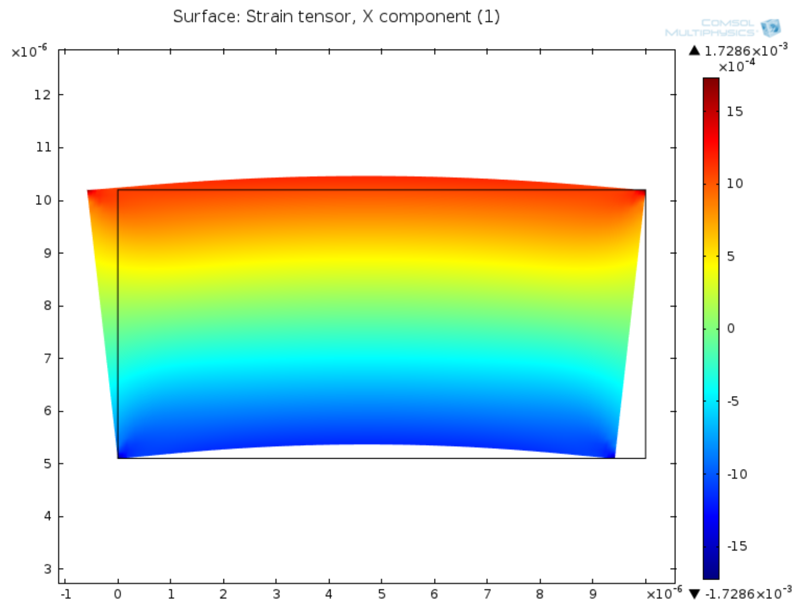

Fig. 4.6 Strain tensor-x (Scale factor: 50).

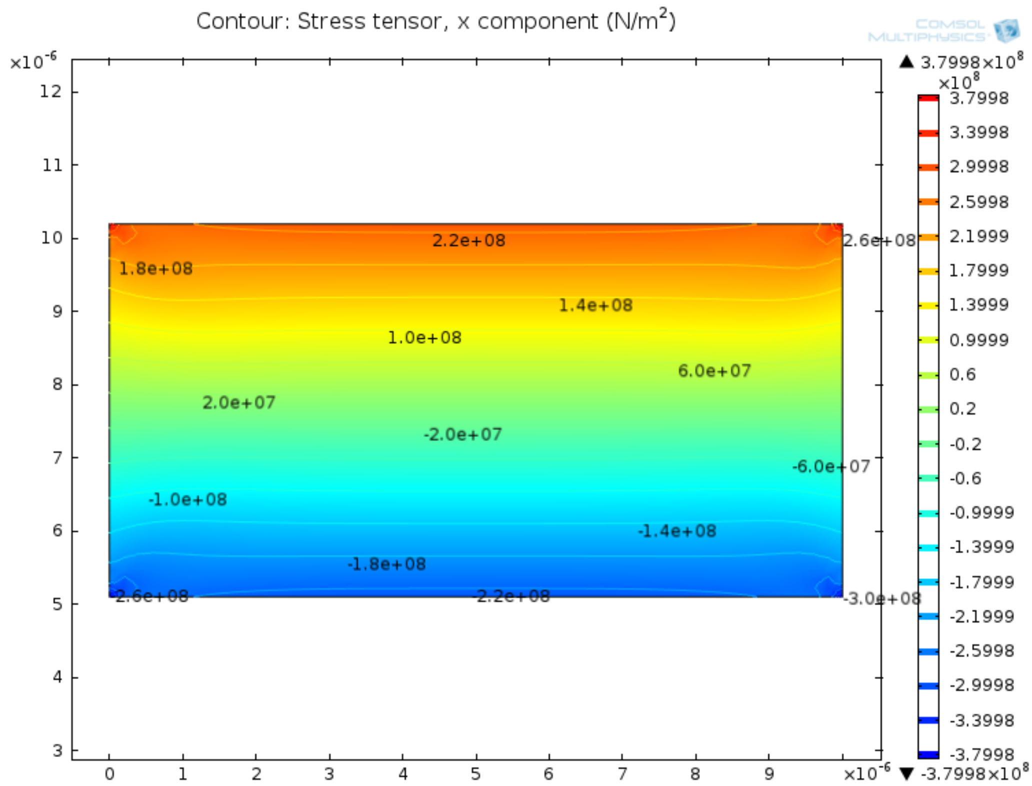

Fig. 4.7 Contour plot of stress tensor-x (Scale factor: 1).

The distance between neutral axis and the bottom surface of the substrate is

$\eta = \frac{E_s d_s^2 + E_f d_f(2d_s + d_f)}{2(E_s d_s + E_f d_f)}$ =2.52E-06 m

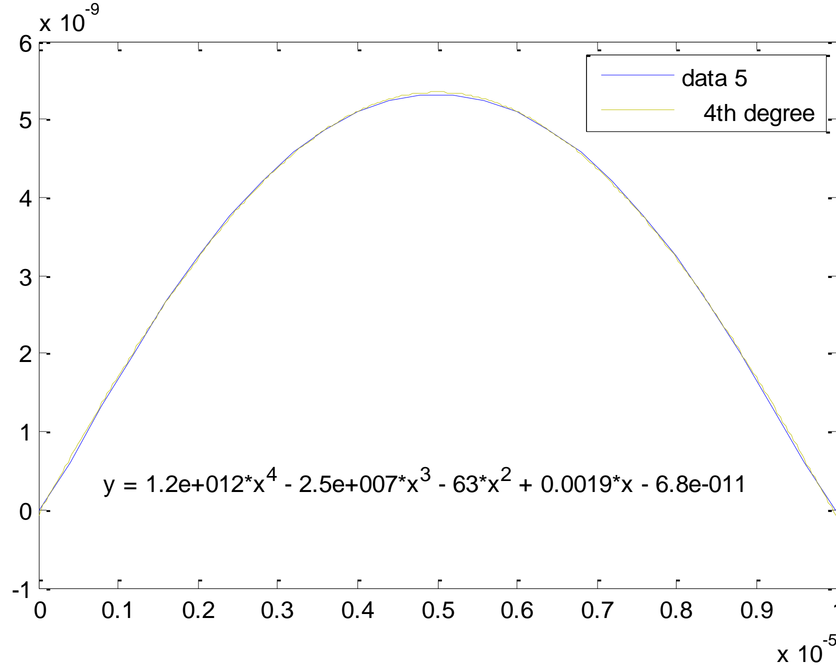

Fig. 4.8 Curve fitting using 4th degree polynomial by Matlab.

Fig. 4.8 shows the vertical displacement of the TFT measured at neutral plane. By curve fitting, the radius of curvature calculated from the neutral plane using Matlab and Comsol is R= 1.9E-3 m. In comparison with the analytical equations, it shows that the simulation results done by Comsol are consistent with the numerical model. It thus indicates that, the numerical model as well as the setting of boundary conditions can be extended for the simulation of stress and strain in multiple layer structures.

4.2.2 Two-Dimensional Model of TFT Devices

4.2.2.1 Stress/strain simulation of ZnO TFT on flexible platforms by mechanical bending

A two-dimensional ZnO TFT structure is simulated using Comsol, wherein the z-component of the strain was assumed to be zero. The material and geometrical structure of the TFT model is shown in Fig. 4.9. The source/drain and gate electrode are ITO, and the semiconducting layer is ZnO. The

insulating layer is SiO_2, which is used as a buffer layer to prevent moisture and solvents permeating into the film, meanwhile maintaining adhesion to the upper layers of the TFT. The channel length (L) is 0.7 μm. The material properties are given in Table 4.2.

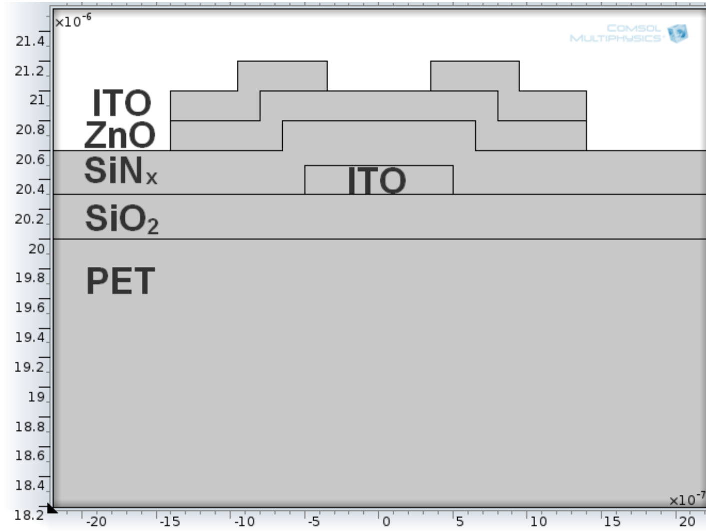

Fig. 4.9 Schematic of ZnO TFT structure.

Table 4.2 Material properties used in the numerical model of ZnO TFT.

Material	E [GPa]	v	Density [g/cm^3]	Thickness [μm]
ITO	116 [38]	0.35	7.1	0.2
ZnO	137 [71]	0.36	5.6	0.2
SiN_x	250 [72]	0.23	3.1	0.3
SiO_2	70 [38]	0.17	2.2	0.3
PET	5 [73]	0.4	1.4	10

Now, a pair of opposite bending moment of M=1E-5 N·m is applied on both ends of the TFT at constant temperature, then the distribution of strain tensor-x in the multilayer structure is simulated by Comsol, as shown in Fig. 4.10. Suppose the initial stress and strain in the TFT structure before external bending is negligible.

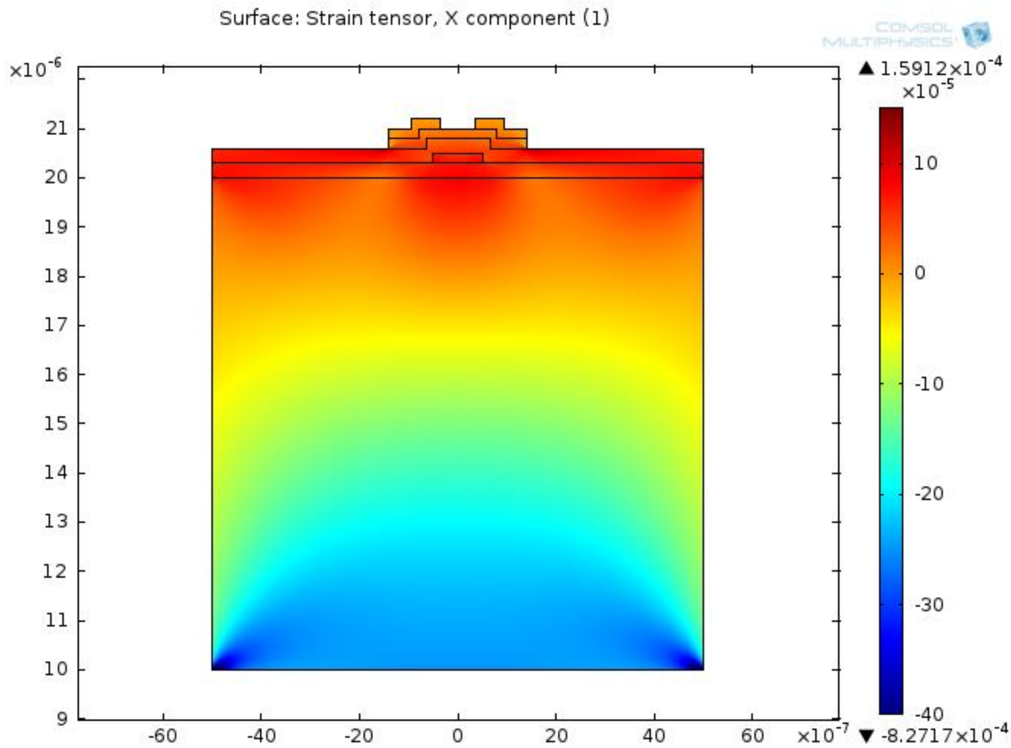

Fig. 4.10 Strain tensor-x of film-substrate stack by applying bending moment of 1E-5 N ·m.

It shows the top surface of the stack is under tensile strain, whereas the bottom substrate is under compressive strain. Due to the applied bending moments, the multilayer stack tends to bend convexly upward. As compared with the mechanical bending of isolated beam shown in Fig. 4.6, the strain is less uniformly distribution throughout the structure due to the patterned TFT layers on top of the substrate. A larger range of compressive strain is shown at the lower left and right corners of the PET substrate because of the boundary constraint.

Simulations showing the distributions of stress tensor-x in the TFT structure as well as a magnified channel region are shown in Figs.4.11 and 4.12, respectively. Because the bending moments are applied to the stack of PET substrate and the above insulating layers of SiO_2 and SiN_x, the only constraint for the ZnO active layer and the ITO source and drain islands is these layers are bonded together at the interface, so these regions are subjected to less tensile stresses than other layers during mechanical bending. In addition, in order to maintain the compatible displacement in the interface of the perfectly bonded SiN_x layer and the ZnO/ITO multilayer, stress concentration is observed at the top surface of the SiN_x beneath the sharp edges of the source and drain islands.

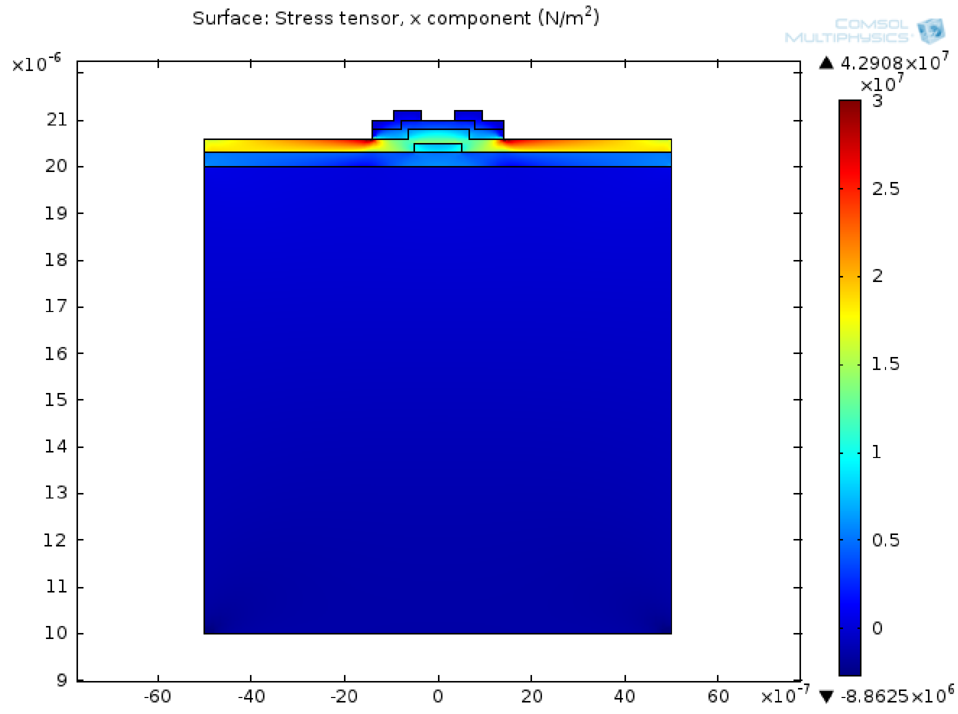

Fig. 4.11 Stress tensor-x of film-substrate stack by applying bending moment of 1E-5 N m.

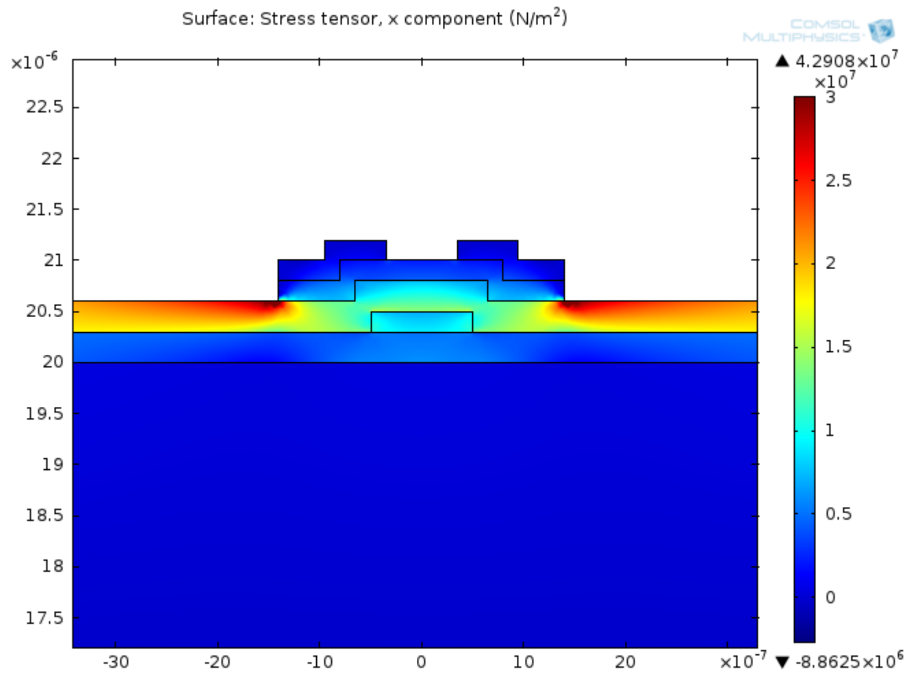

Fig. 4.12 Stress tensor-x distribution in the magnified top surface area.

The average stress tensor-x and strain tensor-x for each TFT layer are calculated by Comsol and summarized in Table 4.3. It shows the trend of variation from tensile stress in the top layers of TFT to compressive stress in the substrate.

Table 4.3 Average stress and strain tensor-x of different TFT layers.

Material	**ITO(S/D)**	**ZnO**	**SiN_x**	**ITO(G)**	**SiO_2**	**PET**
Strain	6.41E-06	2.75E-05	6.69E-05	6.73E-05	6.02E-05	-1.05E-04
Stress [Pa]	8.70E+05	4.37E+06	1.77E+07	8.72E+06	4.34E+06	-7.20E+05

As the height of the mid-plane of each layer is

$$h_{mi} = \frac{h_i + h_{i-1}}{2} = h_i - \frac{d_i}{2} \quad \text{(Eq. 4.30)}$$

If the thick PET substrate is uniformly coated with SiO_2 and SiN_x layers with the same thickness of 300 nm, the neutral axis calculated from the above equation is

$$h_b = \frac{\sum_{i=1}^{n} E_i d_i h_{mi}}{\sum_{i=1}^{n} E_i d_i} = 7.8 \text{ E-6 m}$$

The neutral axis can be distinguished from the color legend in Fig. 4.10. As shown in Fig. 4.13, it shows the vertical displacement of the TFT at the neutral axis. Using curve fitting method, the radius of curvature calculated from the neutral axis by the use of Comsol and Matlab is R=3.33E-2 m.

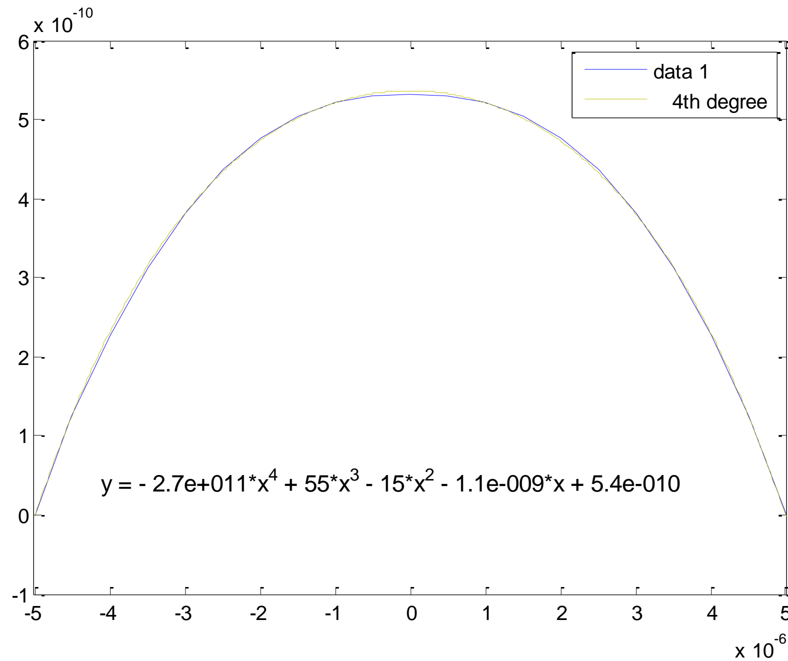

Fig. 4.13 Curve fitting using 4th degree polynomial by Matlab.

4.2.2.2 Proposed designs to minimize stress induced strain within the active TFT layer under bending

In order to improve the flexibility of electronic devices, the active functional layers can be placed near the neutral mechanical plane, where the strain is zero [74, 75]. For ZnO TFTs, because the active ZnO layer is the most sensitive and fragile among other layers as well as being a semiconductor, it can be placed near the neutral plane to be protected against the applied strain. This can be realized by varying the thickness of encapsulating layers such as epoxy coating or changing the thickness of buffer layer, e.g. SiO_x. In the present simulation, a thick epoxy encapsulating layer is deposited on top of the ZnO TFT, as shown in Fig. 4.14. Suppose the Young's modulus and Poisson's ratio of the epoxy layer is 3.1 GPa [76] and 0.3, respectively.

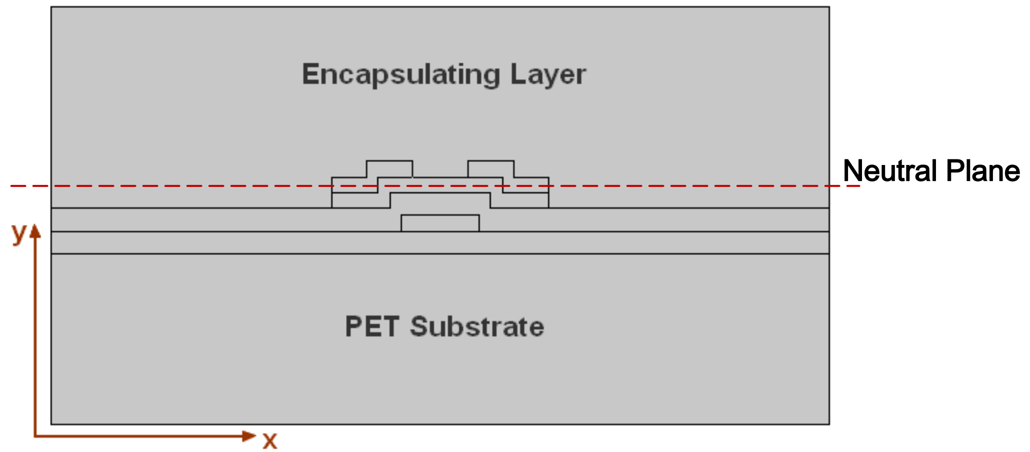

Fig. 4.14 Schematic of ZnO layer near the neutral plane by adjusting the thickness of the encapsulating layer.

In the case that the ZnO layer is placed at the neutral plane, according to the neutral axis equation, the position of neutral axis should be

$$h_b = \frac{\sum_{i=1}^{n} E_i d_i h_{mi}}{\sum_{i=1}^{n} E_i d_i} = 10.9 \text{ E-6 m}$$

Calculated from the above equation, the thickness of the encapsulating layer would be around 15.4E-6 m. Thus, a thick encapsulating layer with thickness of 15.4E-6 m is coated on top of the ZnO TFT device to locate the ZnO layer near the neutral axis. The resulting strain distribution in the TFT is shown in Fig. 4.15. The ZnO layer is now located near the neutral plane after the coating of the encapsulating layer with thickness of 15.4 E-6 m on the top of the TFT structure.

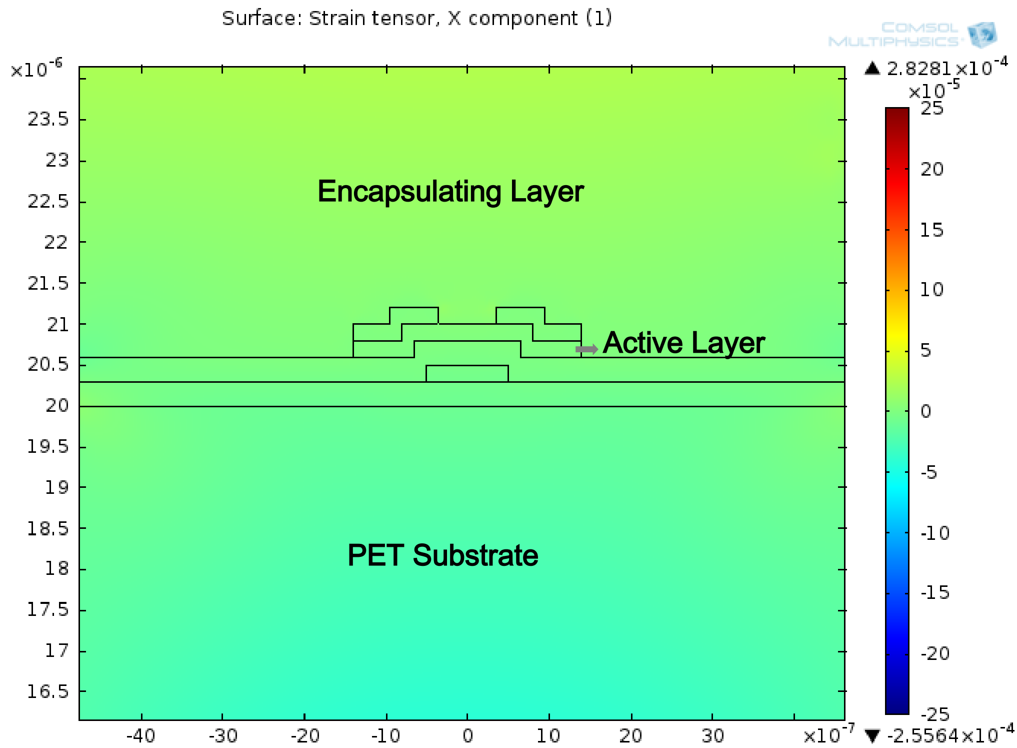

Fig. 4.15 Location of ZnO film near neutral plane by varying the thickness of the encapsulating layer.

4.2.2.3 Simulation of flexible TFT structures using different inorganic and organic materials

(a) a-IGZO TFT and pentacene organic TFT

An extension of the numerical model of ZnO TFT is to simulate different inorganic or organic TFTs. The numerical model is used to simulate a-IGZO TFT and organic TFT by replacing the ZnO layer with a-IGZO and pentacene, respectively. In order to compare the differences resulting from the use of different active layers, the other TFT materials and structures, as well as the bending conditions are kept constant. The TFT structures are shown in Figs. 4.16 (a) and (b), respectively. The material properties of a-IGZO and pentacene are given in Table 4.4.

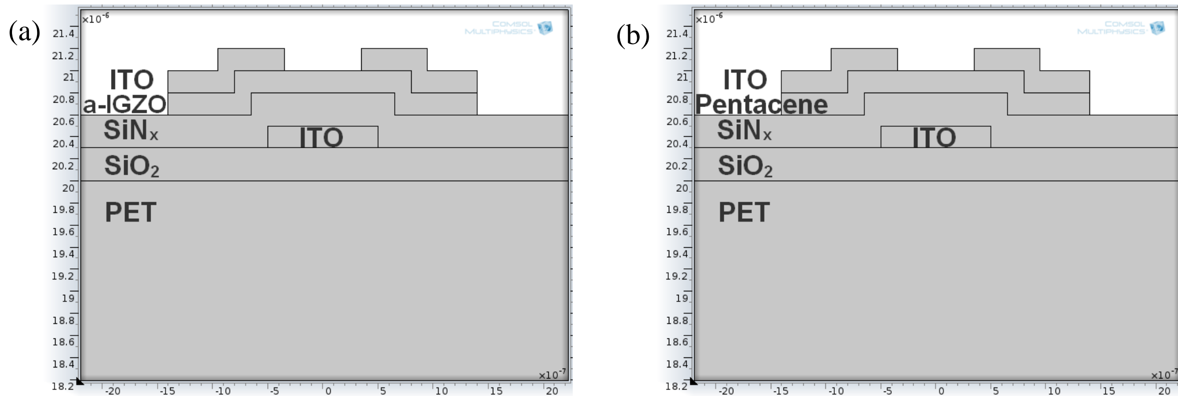

Fig. 4.16 Schematic of TFT structure: (a) a-IGZO TFT; (b) pentacene organic TFT.

Table 4.4 Material properties used in modeling organic and inorganic TFTs.

Material	E [GPa]	v	Density [g/cm^3]	Thickness [μm]
a-IGZO	137[38]	0.36	6.27 [77]	0.2
Pentacene	15[78]	0.4	1.36 [79]	0.2

By applying the opposite bending moment of M= 1E-5 N ·m, the distribution of stress and strain in the a-IGZO TFT multilayer TFT structure is similar to those in the ZnO TFT due to the use of similar material properties (e.g. same film thickness and Young's modulus). In comparison, the organic TFT shows different levels of stress and strain because there is a significant difference in the value of Young's modulus. A comparison of the strain distribution in the a-IGZO TFT and the organic TFT are shown in Figs. 4.17 and 4.18.

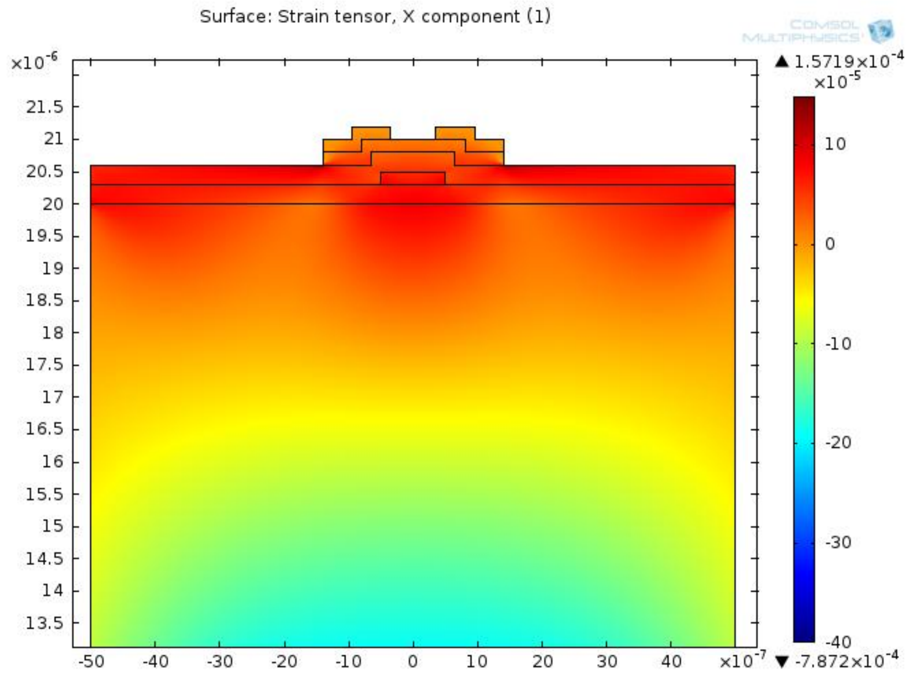

Fig. 4.17 Strain tensor-x in a-IGZO TFT device due to applied bending moment of 1E-5 N ·m.

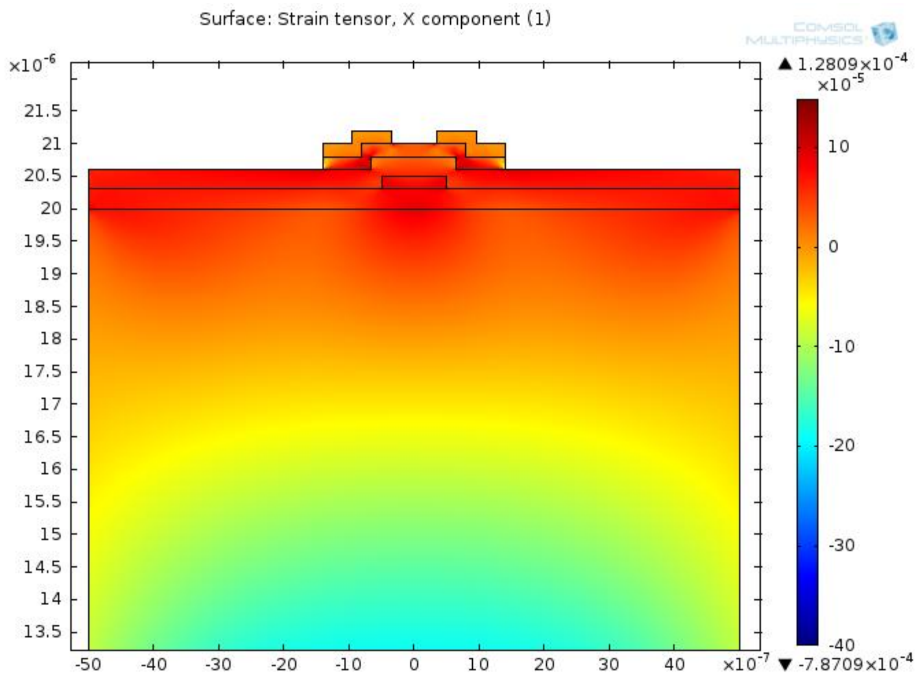

Fig. 4.18 Strain tensor-x in pentacene organic TFT due to applied bending moment of 1E-5 N ·m.

Similar to the ZnO TFT model, above the neutral axis, the TFT is under tensile strain, and below the neutral axis, the TFT is under compressive strain. Moreover, it shows the pentacene TFT is subjected to larger strains in the pentacene layer. This is because the pentacene material has smaller values of stiffness (Young's modulus times thickness) than ZnO and a-IGZO, thus is vulnerable to deform during mechanical bending. The stress distribution in a-IGZO TFT and organic TFT are shown in Figs. 4.19 and 4.20. The stress concentration is reduced in the organic TFT because a relatively lower level of stress is required to maintain the compatibility of the insulating layer with the compliant pentacene layer.

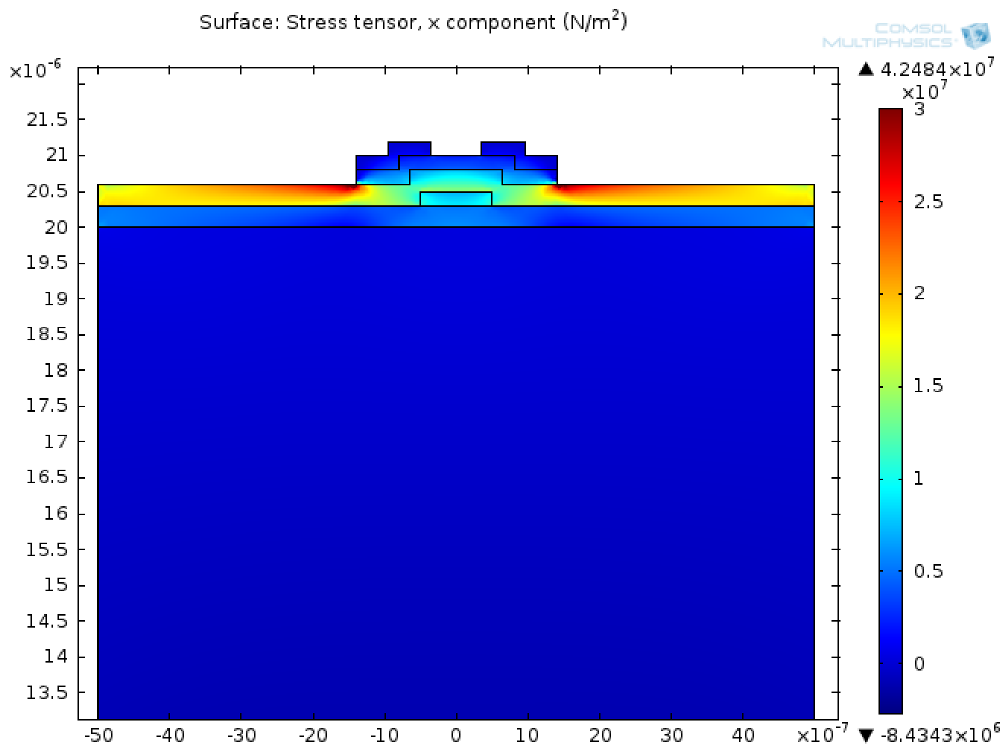

Fig. 4.19 Stress tensor-x in a-IGZO TFT device due to applied bending moment of 1E-5 N m.

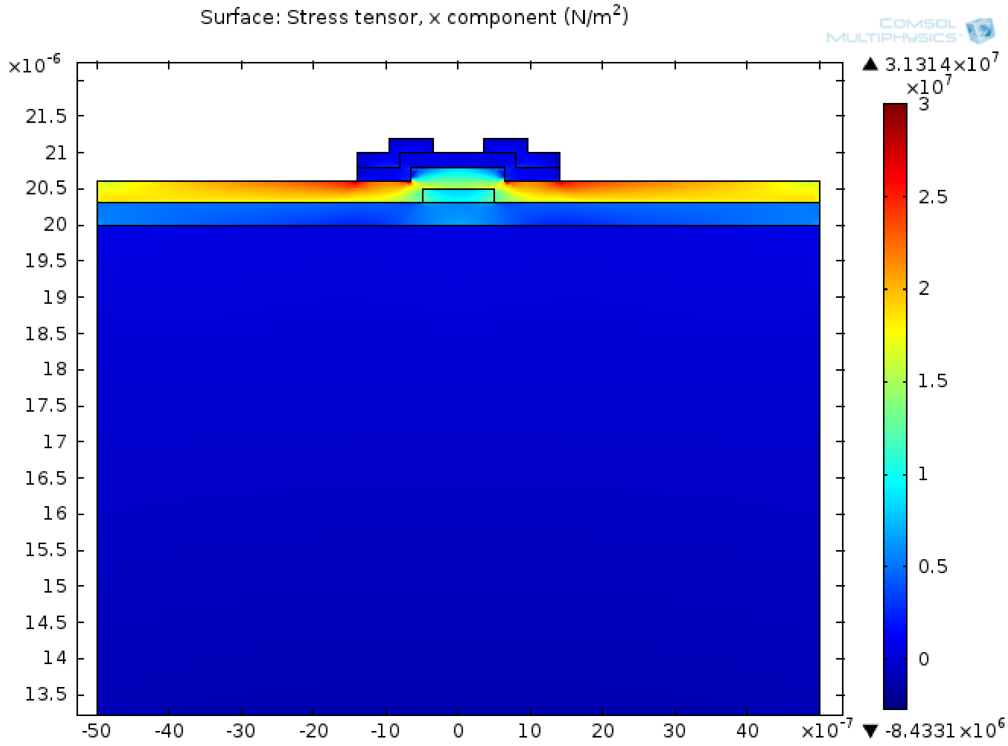

Fig. 4.20 Stress tensor-x in pentacene organic TFT device due to applied bending moment of 1E-5 N·m.

The average values of stress and strain in each layer of different inorganic and organic TFT structures are summarized in Table 4.5. Comparisons of these results are plotted in Fig. 4.21 and 4.22.

Table 4.5 Average stress and strain tensor-x of different TFT layers.

TFTs	Material	ITO(S/D)	Active layer	SiN_x	ITO(G)	SiO_2	PET
ZnO	**Strain**	6.41E-06	2.75E-05	6.69E-05	6.73E-05	6.02E-05	-1.05E-04
	Stress [Pa]	8.70E+05	4.37E+06	1.77E+07	8.72E+06	4.34E+06	-7.20E+05
a-IGZO	**Strain**	6.41E-06	2.75E-05	6.69E-05	6.73E-05	6.02E-05	-1.05E-04
	Stress [Pa]	8.70E+05	4.37E+06	1.77E+07	8.72E+06	4.34E+06	-7.20E+05
Pentacene	**Strain**	5.21E-06	4.57E-05	6.84E-05	7.74E-05	6.24E-05	-1.05E-04
	Stress [Pa]	6.97E+05	8.56E+05	1.81E+07	9.92E+06	4.50E+06	-7.17E+05

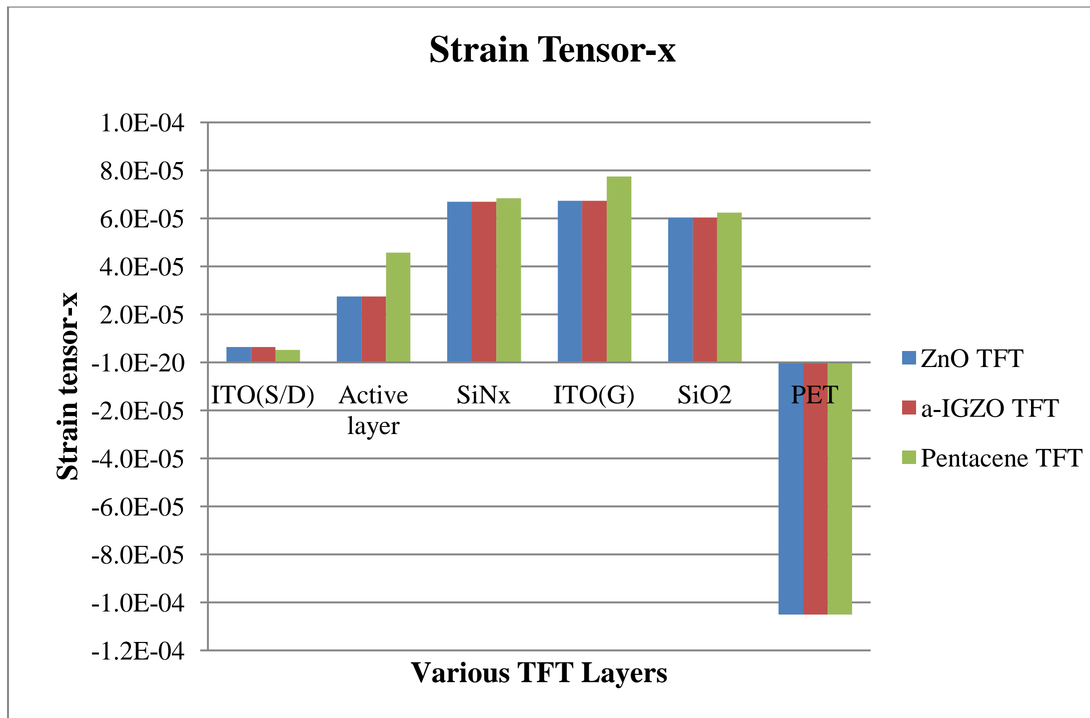

Fig. 4.21 Comparison of strain tensor-x in each layer of different TFT structures.

It is shown in Fig. 4.21 that the pentacene layer is subjected to relatively larger strain than the ZnO and a-IGZO active layers. The pentacene organic layer with a small Young's modulus is compliant and easily to deform as a result of the external mechanical bending. Due to the bonding at the interface of multiple layers, the insulating layers of SiN_x and SiO_2, as well as the ITO gate in pentacene organic TFT undergo relatively larger tensile strain than the same material in the ZnO TFT and a-IGZO TFT. Because of the constrained boundary of the PET substrate and its thickness, the strain in PET substrates is uniform among different TFTs. In Fig. 4.22, it shows the flexible pentacene layer is subjected to less levels of stress, compared to the ZnO and a-IGZO layers which have larger Young's modulus. A relatively small tensile stress is found in the ITO source/drain islands, and a relatively small compressive stress is shown in the thick PET substrate.

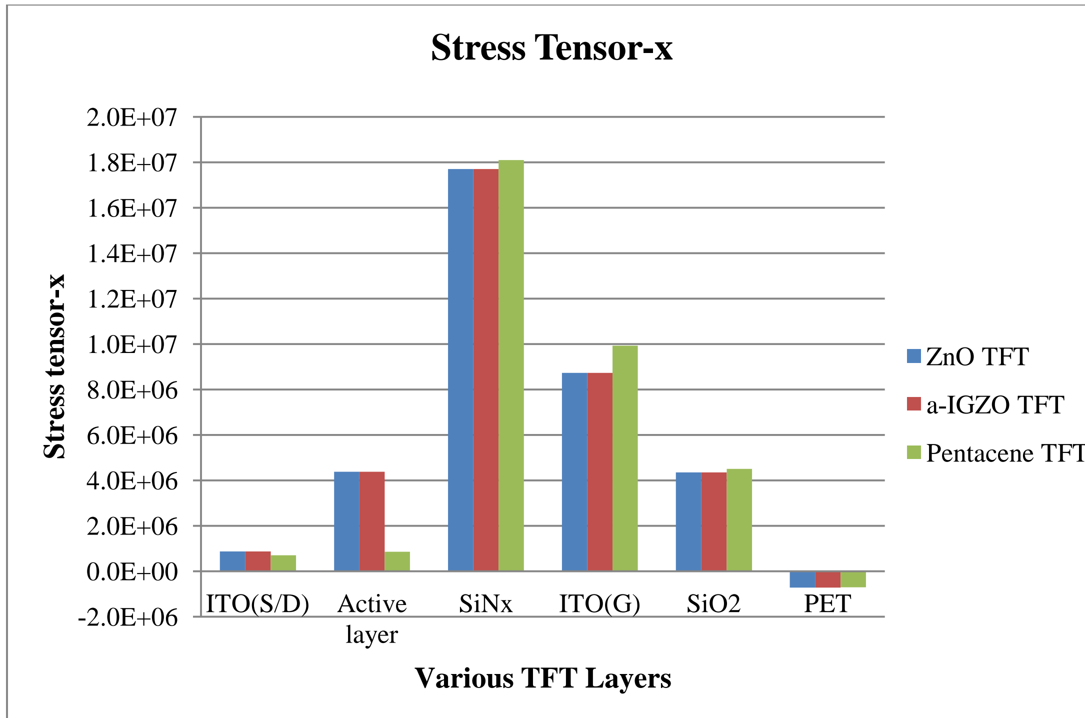

Fig. 4.22 Comparison of stress tensor-x in each layer of different TFT structures.

Similar to the ZnO TFT model, the resulting strain and stress in the semiconducting layer during mechanical bending can be reduced by adjusting the thickness of other TFT layers, such as changing the thickness of the encapsulating layer or the buffer layer. As a result, the active layer is placed near the neutral mechanical plane of the structure, thereby enabling improved bendability and stability of the TFT device.

(b) a-Si:H TFT

In order to simulate the mechanical bending of a-Si:H TFT, the above numerical model is modified by replacing the active layer with a-Si:H layer and an additional n+ a-Si:H layer with 50 nm thickness between the a-Si layer and the source and drain islands. The a-Si TFT structure is shown in Fig. 4.23. The material properties of a-Si and n-type a-Si are listed in Table 4.6.

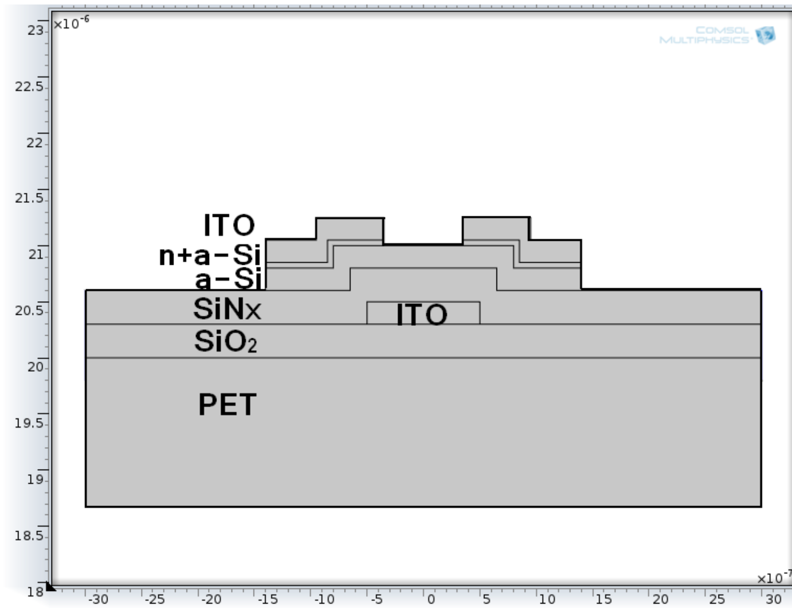

Fig. 4.23 Schematic of a-Si TFT structure.

Table 4.6 Material properties used in the numerical model of a-Si TFT.

Material	E [GPa]	v	Density [g/cm^3]	Thickness [μm]
a-Si	150 [80]	0.22	2.0	0.2
n-type a-Si	147 [81]	0.22	2.0	0.05

When a pair of bending moment of 1E-5 N·m is applied on both ends of the TFT structure, the distribution of strain and stress tensor-x are shown in Figs. 4.24 and 4.25. The average stress and strain tensor-x are summarized in Table 4.7.

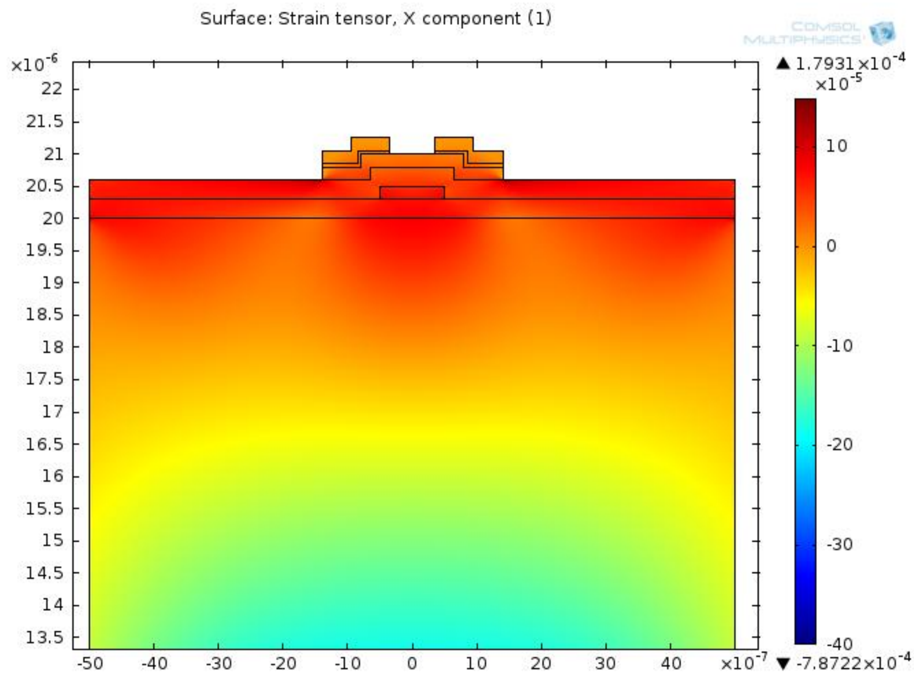

Fig. 4.24 Strain tensor-x in a-Si TFT device.

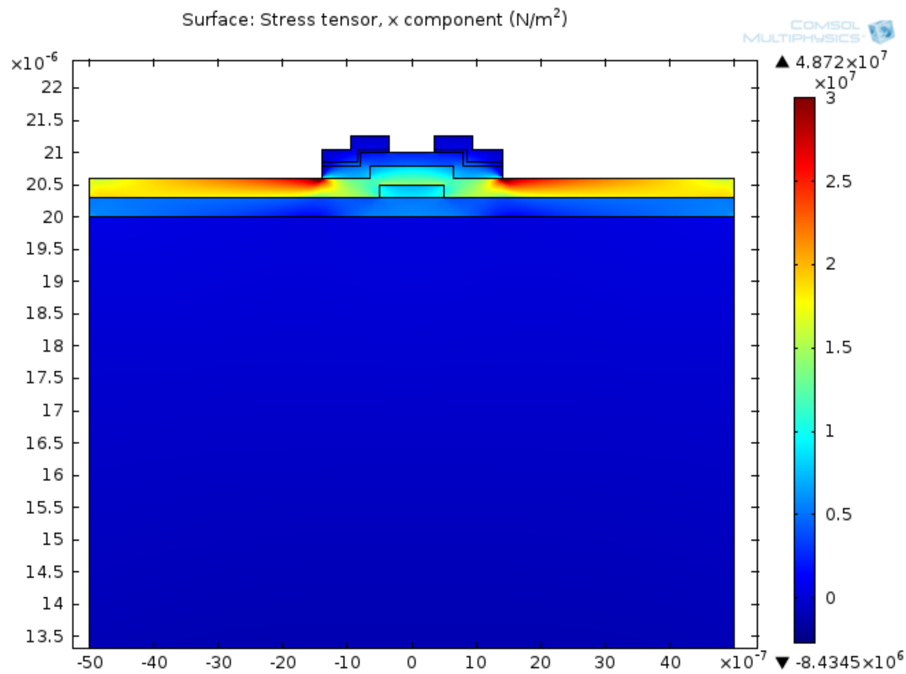

Fig. 4.25 Stress tensor-x of a-Si TFT.

Table 4.7 Average stress and strain tensor-x over each layer of a-Si TFT.

TFTs	Material	ITO(S/D)	n+ a-Si	Active layer	SiN_x	ITO(G)	SiO_2	PET
a-Si	Strain	3.35E-06	1.29E-05	2.75E-05	6.69E-05	6.69E-05	6.01E-05	-1.05E-04
	Stress [Pa]	4.62E+05	1.99E+06	4.33E+06	1.77E+07	8.69E+06	4.33E+06	-7.20E+05

Similar to the ZnO-TFT and IGZO-TFT, large stress concentration is generated at the top surface of SiN_x near the semiconducting layer of a-Si TFT. As we discussed before, the normal stresses σ_x is increased in the above region to maintain compatibility of multiple layers during mechanical bending. Compare with the stress distribution in pentacene organic TFT, much larger stresses are generated in the stress concentration region due to the relatively harder a-Si layer with a larger Young's modulus. The maximum values of stress in the stress concentration region of different TFTs and the average values of stress tensor-x in the various active layers are plotted in Fig. 4.26.

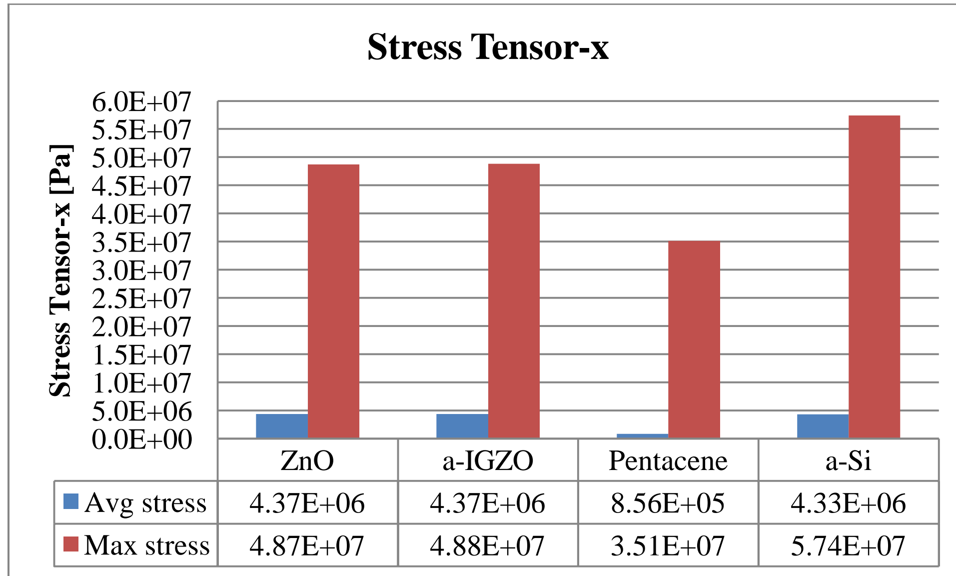

Fig. 4.26 Average stress tensor-x in the various active layers and maximum stress tensor-x in different TFT structures.

As shown in Fig. 4.26, the average of the stresses generated in the pentacene layer is smaller than other semiconducting layers due to its compatible properties in terms of having a smaller Young's modulus. Likewise, the maximum value of stress in the stress concentration region of the pentacene

TFT is the smallest among all these devices. Compared with the ZnO-TFT and IGZO-TFT, the maximum stress in a-Si TFT is 5.74E+07 Pa, which is 8.6 MPa larger than ZnO and IGZO based TFTs due to the relatively harder a-Si material with a larger Young's modulus. Since the yield strength of SiN_x is 14 GPa [67], all of above TFT structures remain intact and stable during the mechanical bending as the maximum stresses in the SiN_x layers are far below the limit. The other TFT layers are also under normal condition as the stresses resulting from bending are several orders smaller than their yield strength, thus these TFT devices can withstand greater levels of mechanical bending without breaking.

4.2.3 Numerical Simulation of Complex TFT Devices

4.2.3.1 Simulation of flexible double gate TFT

Nowadays, double gate TFTs have attract more attention because the double gate configuration facilitates device scaling to ultra-small dimensions and provides more drain current [82]. A simulation of a double gate TFT is made by Comsol Multiphysics based on the numerical model of a-IGZO TFT. On top of the bottom gate TFT structure, a SiO_2 insulating layer and an additional gate electrode is formed. The top and bottom gate material used in this model is Chromium (Cr), and the source and drain electrodes are Aluminum (Al) since Cr and molybdenum are commonly used gate materials while Al is commonly used for source and drain electrode [83]. All the other materials and structures are kept the same as in the a-IGZO TFT. The properties of these materials are listed in Table 4.8, and the schematic structure of the dual gate TFT is shown in Fig. 4.27.

Table 4.8 Material properties of a dual gate TFT device.

Material	E [GPa]	v	Density [g/cm^3]	Thickness [μm]
Cr	279 [84]	0.21[85]	7.2	0.2
Al	70	0.33	2.7 [77]	0.2
SiO_2(top)	70	0.17	2.2	0.4

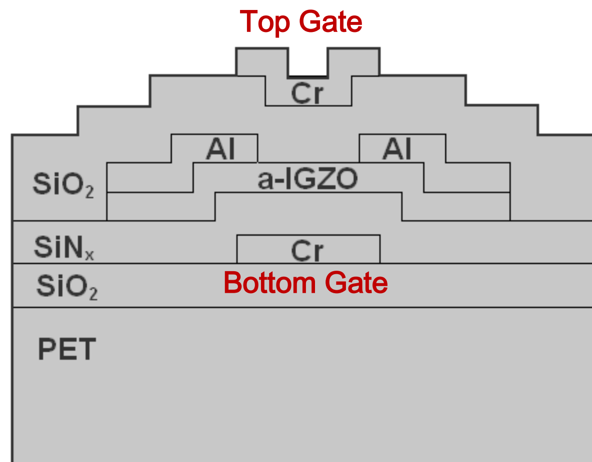

Fig. 4.27 Schematic of a dual gate TFT structure.

When a pair of bending moment of M =1E-5 N m is applied to the left and right boundaries of the TFT structure, the strain and stress distribution are shown below.

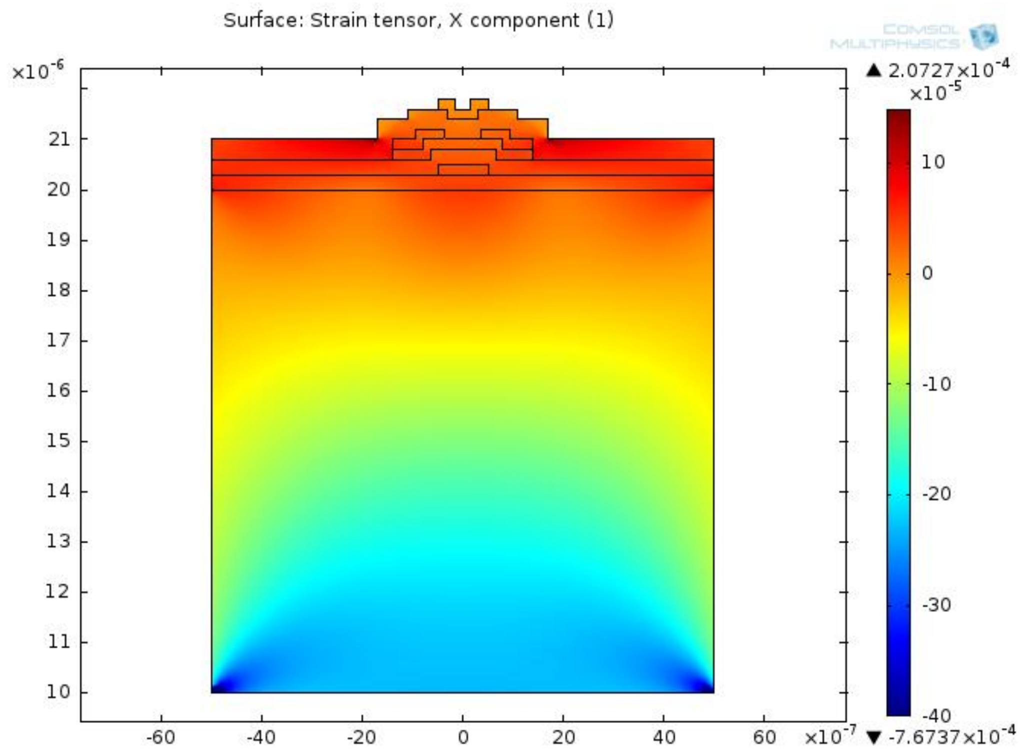

Fig. 4.28 Strain tensor-x by applying bending moment of 1E-5 N m.

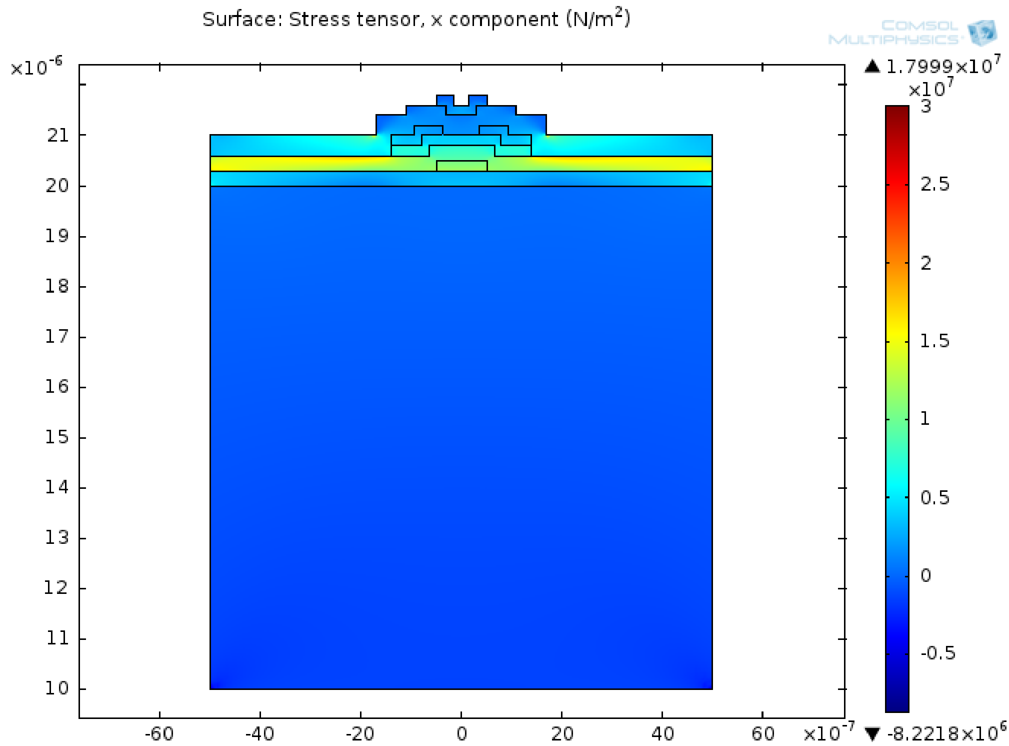

Fig. 4.29 Stress tensor-x by applying bending moment of 1E-5 N m.

Fig. 4.28 shows the dual gate TFT tends to bend convexly upward as a result of the external bending, thus the top region of the TFT stack is under tensile strain, whereas the bottom region of the thick substrate is under compressive strain. In Fig. 4.29, stress concentration is generated in the region with sharp change of boundary. Moreover, the SiN_x layer and the bottom-gate of Cr are subjected to relatively larger stresses due to their larger Young's modulus values. In comparison, much less stress and strain occur in the unconstrained top gate of Cr. The average stress and strain values are listed in Table 4.9. A comparison of the stress and strain data is shown in Figs. 4.30 and 4.31.

Table 4.9 Average values of stress and strain tensor-x of the double gate TFT.

Material	**Cr**	**SiO_2(top)**	**Al(S/D)**	**a-IGZO**	**SiN_x**	**Cr(G)**	**SiO_2**	**PET**
Strain	3.92E-06	5.38E-05	3.74E-05	3.58E-05	5.01E-05	3.84E-05	4.25E-05	-1.06E-04
Stress [Pa]	1.14E+06	3.90E+06	2.91E+06	5.53E+06	1.32E+07	1.11E+07	3.05E+06	-7.39E+05

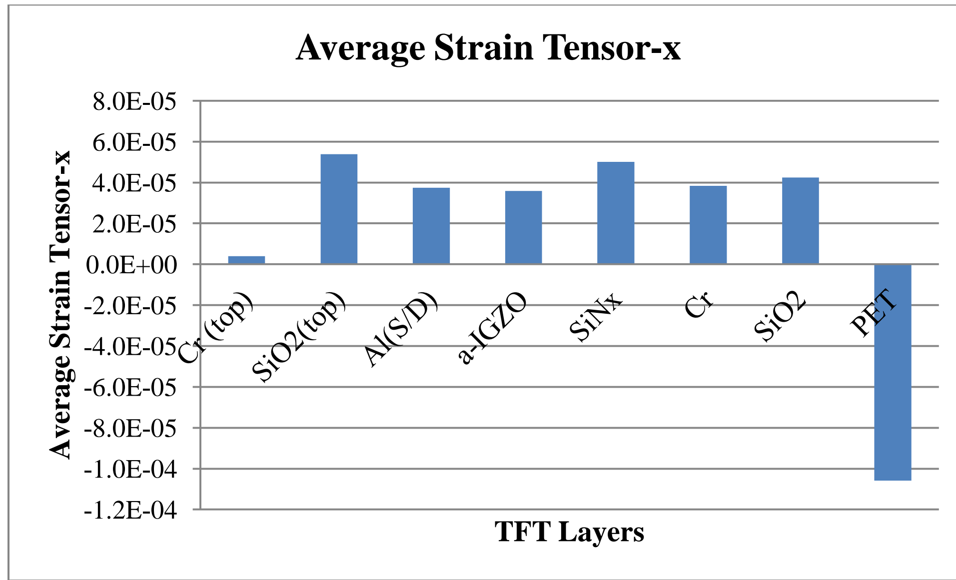

Fig. 4.30 Average values of Strain Tensor-x in TFT multilayer.

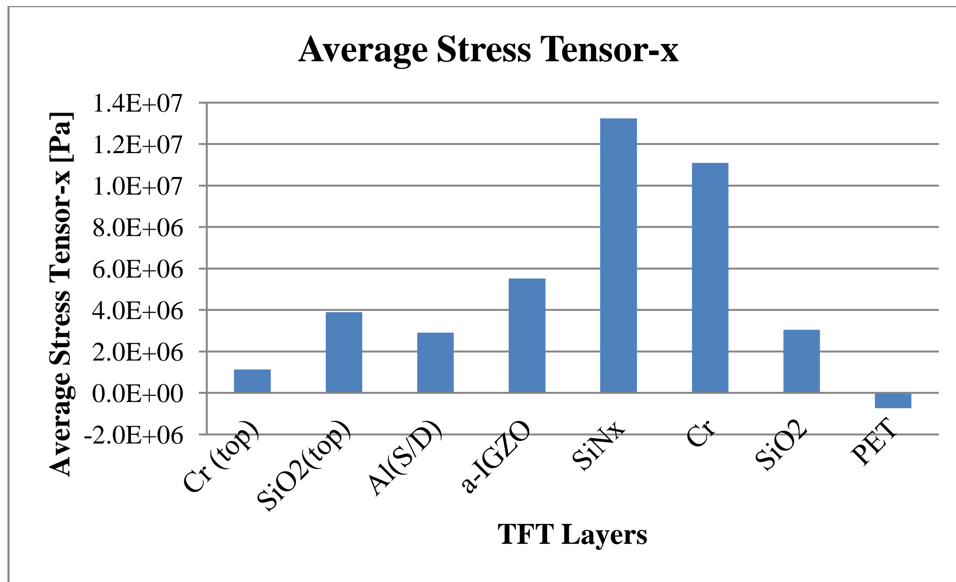

Fig. 4.31 Average values of Stress Tensor-x in TFT multilayer.

In Fig. 4.30, all the layers show tensile strain except the substrate which generates compressive strain during mechanical bending. The top Cr gate shows the smallest tensile strain than the other layers. The a-IGZO layer shows an average strain of 3.58E-05, and an average stress of 5.53E+06 Pa. In order to reduce the stress and strain in the active layer, the a-IGZO layer can be placed near the

neutral plane of the TFT structure by varying the thickness of other layers, as presented in the simulation of ZnO based TFTs. Besides, the harder SiN_x and Cr bottom gate which have larger Young's modulus show relatively larger stresses than other layers, as shown in Fig. 4.31. However, compare to the yield strength of SiN_x material, the resulting stress is much lower than the yield limit, thus the double gate TFT shows great flexibility during mechanical bending.

Chapter 5 Conclusions

Recently, flexible electronics has attracted increasing attention due to the advantages of mechanical flexibility of building electronic systems on flexible and light-weight substrates. Since the thin-film transistors are the essential components of flexible electronics, the primary focus of the present study is to investigate the mechanical flexibility of thin-film transistors.

Both analytical and numerical models are studied to determine the states of stress and strain in thin films deposited on flexible substrates resulting from film deposition process as well as applied mechanical bending. Starting with a basic model of single thin film deposited on a thick substrate, the analytical models have been extended to analyze the average stress and strain of multilayer stack resulting from the temperature change and external bending. The radius of curvature as well as the position of neutral axis is analyzed based on the analytical formulas. On the other hand, numerical models of thin films deposited on flexible substrate have been built by Comsol Multiphysics to simulate the distribution of stress and strain in the multiple films-substrate combination. It shows that the simulation results presented by Comsol are consistent with the analytical models.

Based upon the basic model of film-substrate system, several complex numerical models have been built up for simulating the stress and strain in different inorganic TFT structures (ZnO, a-IGZO, and a-Si based TFTs) and organic TFT (pentacene TFT). Compared with the analytical models, the numerical models not only show the stress and strain distribution in two-dimensional patterned TFT structures, but also provide efficient prediction of the system by studying variables, such as minimizing high stress and strain fields of important active layers by locating these layers near the neutral plane of the TFT structure. Furthermore, these models can be used to analyze and optimize the mechanical properties of more complicated and flexible electronics devices by varying structures, materials, and other thermal or mechanical parameters.

Recommendations for Future Work

Besides the simulation of mechanical properties of flexible TFTs, it is also feasible to combine the numerical models with the characterization of their electrical properties. One interesting topic for further studies is to explore the correlation between the electrical properties and the mechanical properties of TFTs based on the numerical models, which may include:

(1) Characterization of piezoelectric effects of piezoelectric materials due to mechanical

deformation

Take ZnO as an example. It is known that, ZnO has piezoelectric properties that the mechanical energy can convert to electrical energy, and vice versa [86]. Based up on this phenomenon, when the ZnO based device is strained, the generation of electrical polarization can be characterized, the reverse is also true. A brief simulation of the piezoelectric effects is described below. A model of multilayer cantilever beam with piezoelectric interlayer is built up using piezoelectric device module. After defining material properties and boundary conditions, input the electrical potential and mashing the structure. Then compute the module and analyze the displacement of the beam as a result of the piezoelectric effects. Similarly, a value of displacement of the beam can be defined and then calculate the electrical potential within the piezoelectric device. So it is desirable to correlate the mechanical properties of piezoelectric devices with the electrical properties.

(2) Simulation of the change of electrical properties due to mechanical deformation

The previous research shows the behavior of electrical characteristics of a-Si:H thin-film transistors are affected by mechanical strain because the mechanical deformation dominates the re-distribution of trap states in the bandgap [87]. As a result of the applied mechanical strain, the disordered bonds in a-Si may cause a redistribution of trap states, resulting in unstable electrical characteristics, leading to a shift of threshold voltage and the mobility of carriers. The previous research findings have indicated the potential use of numerical model to simulate the shift of threshold voltage due to the effects of doping in transistors using Comsol [88]. Based on this numerical model, it is feasible to simulate the shift of threshold voltage due to the mechanical deformation of flexible TFT devices for future work. Since the shift of threshold voltage is related to charge trapping, it is possible to present the link between the mechanical properties and the electrical properties of flexible TFTs.

In summary, it is feasible to combine the numerical models with experimental results to simulate both the mechanical and electrical properties of TFT devices. Compared with the analytical models, the numerical models are competent in predicting consistent and reliable results for the study of mechanical properties of flexible TFT devices. It is straightforward to design complex TFT devices and simulate the mechanical and electrical performance with numerical models. A comprehensive experimental study of mechanical bending test of TFTs and characterization of their electrical properties can be carried out to verify the simulation results. Furthermore, it is beneficial to build the numerical models to simulate both the electrical and mechanical properties which provide an efficient

guidance on the development and fabrication of novel TFTs and more complicated electronic devices.

References

[1] I-C. Cheng and S. Wagner, "Overview of Flexible Electronics Technology", in "Flexible electronics: materials and applications", ed. W. S. Wong and A. Salleo, Springer, pp. 2-16, 2009.

[2] N. D. Sankir, "Flexible electronics: materials and device fabrication", PhD thesis, Virginia Polytechnic Institute and State University, pp. 1-14, 2005.

[3] R. Shrivastava, "Fundamentals of electronic devices", Krishna Prakashan Media, pp. 173-175, 2009.

[4] P. K. Weimer, "TFT – new thin-film transistor" , Proceedings of the Institute of Radio Engineers, vol. 50, pp. 1462-1469, 1962.

[5] A. T. Voutsas and M. K. Hatalis, "Technology of polysilicon thin-film transistors", in "Thin-film transistors", ed. C. R. Kagan and P. Andry, Marcel Dekker Incorporated, pp. 149-168, 2003.

[6] S. D. Theiss and S. Wagner, "Amorphous silicon thin-film transistors on steel foil substrates", IEEE Electron Device Letters, vol. 17, pp. 578–580, 1996.

[7] N. D. Yang, G. Harkin, R. M. Bunn, D. J. McCulloch, R. W. Wilks, and A. G. Knapp, "Novel fingerprint scanning arrays using polysilicon TFT's on glass and polymer substrates", IEEE Electron Device Letters, vol. 18, no. 1, pp.19-20, 1997.

[8] R. L. Hoffman, B. J. Norris, and J. F. Wager, "ZnO-based transparent thin-film transistors", Applied Physics Letters, vol. 82, issue 5, pp. 733-735, 2003.

[9] E. Fortunato, P. Barquinha, A. Pimentel, A. Gonçalves, A. Marques, L. Pereira, and R. Martins, "Zinc oxide thin-film transistors", in "Zinc oxide – a material for micro- and optoelectronic applications", ed. N. H. Nickel and E. Terukov, vol. 194, Springer, pp. 225-237, 2005.

[10] Ü. Özgür, H. Daniel, and M. Hadis, "ZnO devices and applications: a review of current status and future prospects", Proceedings of the IEEE, vol. 98, no. 7, pp. 1255-1268, 2010.

[11] Ü. Özgür, Y. I. Alivov, C. Liu, A. Teke, M. A. Reshchikov, S. Doğan, V. Avrutin, S. J. Cho and H. Morkoç, "A comprehensive review of ZnO materials and devices", Journal of Applied Physics, vol. 98, pp. 041301, 2005.

[12] J. J. Siddiqui, "Investigation of electrical instabilities and interface charge in zinc oxide thin-film transistors with high-k dielectrics", PhD thesis, University of Michigan, pp. 2-22, 73-78, 2012.

[13] M. J. Chow, "Impact of mechanical stress on the electrical stability of flexible a-Si TFTs", M.A.Sc. thesis, University of Waterloo, pp. 11, 2011.

[14] E. Fortunato, P. Barquinha, A. Pimentel, A. Gonçalves, A. Marques, L. Pereira, and R. Martins, "Recent advances in ZnO transparent thin film transistors", Thin Solid Films, vol. 487, pp. 205–211, 2005.

[15] L. J. Meng and M. P. dos Santos, "Direct current reactive magnetron sputtered zinc oxide thin films the effect of the sputtering pressure," Thin Solid Films, vol. 250, pp. 26, 1994.

[16] T. Higaki, T. Tachibana, Y. Kimura, T. Maemoto, S. Sasa and M. Inoue, “Flexible zinc oxide thin-film transistors using oxide buffer layers on polyethylene napthalate substrates”, 2011 International Meeting for Future of Electron Devices, pp. 92-93, 2011.

[17] Z. L. Wang, Y. Liu, and Z. Zhang, “Handbook of nanophase and nanostructured materials: synthesis”, vol. 1, Tsinghua University Press, pp. 204-213, 2003.

[18] J. George, “Preparation of thin films”, CRC Press, pp. 79-88, 1992.

[19] A. Londergan, “Atomic layer deposition applications 4”, vol. 16, Issue 4 of ECS transactions, The Electrochemical Society, pp. 151-156, 2008.

[20] J. D. Plummer, “Silicon VLSI technology: fundamentals, practice, and modeling”, Pearson Education, pp. 510-529, 2009.

[21] S. E. Takalloo and E. A. Soleimani, “Grain size dependence characteristic of nanocrystalline ZnO-channel thin film transistors”, ESC Transactions, vol. 28, issue 21, pp.1-8, 2010.

[22] M. L. Wu, K. C. Liu, S. H. Hsiao and J. J. Huang, “High-operating current high-mobility thin film transistors using room-temperature sputtering GZO/ZnO as the channel”, ESC Transactions, vol. 16, issue 12, pp. 75-80, 2008.

[23] S. M. Sze and K. K. Ng, “Physics of semiconductor devices”, Third Edition, John Wiley & Sons, pp. 195-199, 293-320, 2006.

[24] D. Hong, “Fabrication and characterization of thin-film transistor materials and devices”, Oregon State University, pp. 39-59, 2008.

[25] D. A. Neamen, “Semiconductor physics and devices: basic principles”, Third Edition, McGraw-Hill, pp. 450-490, 2003.

[26] Constance Rost-Bietsch, “Ambipolar and light emitting organic field effect transistors”, Cuvillier Verlag, pp. 16-19, 2005.

[27] H. Czichos, T. Saiato, L. Smith, “Springer handbook of materials measurement methods”, Springer, pp. 458-460, 2006.

[28] M. J. O’Connell, “Carbon nanotubes: properties and applications”, CRC Press, pp. 90-99, 2006.

[29] H. Gleskova, S. Wagner, W. Soboyejo and Z. Suo, “Electrical response of amorphous silicon thin-film transistors under mechanical strain”, Journal of Applied Physics, vol. 92, no. 10, pp. 6224-6229, 2002.

[30] H. Gleskova, P. I. Hsu, Z. Xi, J. C. Sturm, Z. Suo, and S. Wagner, “Field-effect mobility of amorphous silicon thin-film transistors under strain”, Journal of Non-Crystalline Solids, vol. 338–340 pp. 732–735, 2004.

[31] J. J. Huang and C. N. Chen, “Effect of electrical and mechanical stresses of low temperature a-Si:H thin film transistors fabricated on polyimide and glass substrates”, Thin Solid Films, vol. 529, pp. 454-458, 2013.

[32] M. H. Lee, B. F. Hsieh, and S. T. Chang, "Electrical properties correlated with redistributed deep states in a-Si:H thin-film transistors on flexible substrates undergoing mechanical bending", Thin Solid Films, vol. 528, pp. 82–85, 2013.

[33] H. Gleskova, S. Wagner, and Z. Suo, "Failure resistance of amorphous silicon transistors under extreme in-plane strain", Applied Physics Letters, vol. 75, no. 19, pp. 3011-3013, 1999.

[34] L. Han , K. Song, P. Mandlik, and S. Wagner, "Ultraflexible amorphous silicon transistors made with a resilient insulator", Applied Physics Letters, vol. 96, issue 4, pp. 042111(1-3), 2010.

[35] I.-J. Park, C.-Y. Jeong, I.-T. Cho, J.-H. Lee, E-S. Cho, S. J. Kwon, B. Kim,W.-S. Cheong, S.-H. Song and H.-I. Kwon, "Fabrication of amorphous InGaZnO thin-film transistor-driven flexible thermal and pressure sensors", Semiconductor Science and Technology, vol. 27, issue 10, pp. 105019 (6 pages), 2012.

[36] J. K. Jeong, "The status and perspectives of metal oxide thin-film transistors for active matrix flexible displays", Semiconductor Science and Technology, vol. 26, issue 3, pp. 034008 (10 pages), 2011.

[37] N. Münzenrieder, K. H. Cherenack, and G. Tröster, "The effects of mechanical bending and illumination on the performance of flexible IGZO TFTs", IEEE Transactions on Electron Devices, vol. 58, no. 7, pp. 2041-2048, 2011.

[38] B.-J. Kim, K.-Y. Park, J.-H. Ahn, and Y.-J. Kim, "Numerical design of SiO_2 bridges in stretchable thin film transistors", Japanese Journal of Applied Physics, vol. 51, issue 1, pp. 01AG10-1 (3 pages), 2012.

[39] M. S. Oh, W. Choi, K. Lee, D. K. Hwang, and S. Im, "Flexible high gain complementary inverter using n-ZnO and p-pentacene channels on polyethersulfone substrate", Applied Physics Letters, vol. 93, pp. 033510 (3 pages), 2008.

[40] K. H. Cherenack, N. S. Münzenrieder, and G. Tröster, "Impact of mechanical bending on ZnO and IGZO thin-film transistors", IEEE Electron Device Letters, vol. 31, no. 11, pp. 1254-1256, 2010.

[41] J.-M. Kim, T. Nam, S. J. Lim, Y. G. Seol, N.-E. Lee, D. Kim, and H. Kim, "Atomic layer deposition ZnO:N flexible thin film transistors and the effects of bending on device properties", Applied Physics Letters, vol. 98, issue 14, pp. 142113 (3 pages), 2011.

[42] Y. Sun and J. A. Rogers, "Inorganic semiconductors for flexible electronics", Advanced Material, vol.19, pp. 1897-1916, 2007.

[43] H. Morkoc and Ü. Özgür, "Zinc oxide - fundamentals, materials and device technology", Wiley-VCH, pp. 440-450, 2009.

[44] K. T. Eun, W. J. Hwang, B. K. Sharma, J. H. Ahn, Y. K. Lee, and S. H. Choa, "Mechanical flexibility of zinc oxide thin-film transistors prepared by transfer printing method", Modern Physics Letters B, vol. 26, no. 12, pp.1250077 (10 pages), 2012.

[45] L. Reimer, "Scanning electron microscopy: physics of image formation and microanalysis", Springer, pp. 1-12, 1998.

[46] X. C. Tong, “Advanced materials for thermal management of electronic packaging”, Springer, pp. 109-110, 2011.

[47] B. Bhushan, “Springer handbook of nanotechnology”, Springer, pp. 637-649, 2007.

[48] N. Xi and K. Lai, “Nano optoelectronic sensors and devices: nanophotonics from design to manufacturing”, Micro and Nano Technologies Series, pp. 51-64, 2011.

[49] K. Nogi, M. Hosokawa, M. Naito, and T. Yokoyama, “Nanoparticle technology handbook”, Elsevier, pp. 280-284, 2012.

[50] L. I. Maissel and R. Glang, “Handbook of thin-film technology”, Mcgraw Hill Inc., pp. 12-23, 1970.

[51] X. Feng, Y. Huang, and A. J. Rosakis, “On the stoney formula for a thin film/substrate system with nonuniform substrate thickness”, Transactions of the ASME, vol. 74, pp. 1276-1281, 2007.

[52] Operating manual of ionic stress gauge, Manual Version 1.04, Ionic Systems.

[53] R. Waser, U. Böttger, and S. Tiedke, “Polar oxides”, John Wiley & Sons, pp. 122-130, 2006.

[54] C.-H. Ma, J.-H. Huang, and H. Chen, “Residual stress measurement in textured thin film by grazing-incidence X-ray diffraction”, Thin Solid Films, vol. 418, pp. 73–78, 2002.

[55] [online, accessed June 10 2013] S. Stepanov, “Grazing-incidence X-ray diffraction”, PDF, Illinois Institute of Technology, 1997. Available from: http://tinyurl.com/3po5j.

[56] C. Suryanarayana, and M. G. Norton, “X-ray diffraction: a practical approach”, Springer, pp. 125-136, 1998.

[57] R. Hong, J. Huang, H. He, Z. Fan, and J. Shao, “Influence of different post-treatments on the structureand optical properties of zinc oxide thin films”, Applied Surface Science, vol. 242, pp. 346–352, 2005.

[58] [online, accessed Jan.20 2013] “Physical Properties for ZnO” – Springer Materials, The Landolt-Börnstein Database, Available from: http://www.springer.com/librarians/e-content/springermaterials?SGWID=0-171102-0-0-0.

[59] Y.-C. Lee, S.-Y. Hu, W. Water, K.-K. Tiong, Z.-C. Feng, Y.-T. Chen, J.-C. Huang, J.-W. Lee, C.-C. Huang, J.-L. Shen, and M.-H. Cheng, “Rapid thermal annealing effects on the structural and optical properties of ZnO films deposited on Si substrates”, Journal of Luminescence, vol. 129, pp. 148–152, 2009.

[60] C. Koch, A. Ovid’ko, S. Seal, and S. Veprek, “Structural nanocrystalline materials: fundamentals and applications”, Cambridge University Press, pp. 93-96, 2007.

[61] N.S. Münzenrieder, K.H. Cherenack, and G. Tröster, “Testing of flexible InGaZnO-based thin-film transistors under mechanical strain”, The European Physical Journal-Applied Physics, vol. 55, pp. 23904 (5 pages), 2011.

[62] M. Ohring, “The materials science of thin films”, Academic Press, pp. 413-431, 1992.

[63] H. Gleskova, I-C. Cheng, S. Wagner, and Z. Suo, “Mechanical theory of the film-on-substrate-foil structure: curvature and overlay alignment in amorphous silicon thin-film devices fabricated on free-standing foil substrates”, in “Flexible electronics-materials and applications”, ed. W. S. Wong and A. Salleo, Springer, pp. 29-50, 2009.

[64] K. Malinauskas, V. Ostasevicius and R. Dauksevicius, “Impact of thermal stresses on micro-fabricated devices used for optical applications”, Springer, pp. 245-249, 2012.

[65] J. Laconte, D. Flandre, J.-P. Raskin, “Micromachined thin-film sensors for SOI-CMOS co-integration”, pp. 47-61, 2006.

[66] A. N. V. da Silva, “Analytical modeling of the stress-strain distribution in a multilayer structure with applied bending”, M.A.Sc. thesis, Universidade Técnica de Lisboa, pp. 7-48, 2010.

[67] W. N. Sharpe, “Springer handbook of experimental solid mechanics”, Springer, pp. 206-208, 2008.

[68] Y.-L. Shen, “Constrained deformation of materials: devices, heterogeneous structures and thermo-mechanical modeling”, Springer, pp. 245-246, 2010.

[69] D.-X. Xu, “Polarization control in silicon photonic waveguide components using cladding stress engineering”, in “Topics in applied physics: silicon photonics II-components and integration”, ed. D. J. Lockwood and L. Pavesi, vol. 119, pp. 31-70, 2011.

[70] G. Birkhoff and R. E. Lynch, “Numerical solution of elliptic problems”, SIAM E-Books, vol. 6 of SIAM Studies in Applied Mathematics, SIAM, pp. 14-20, 1984.

[71] D.-K. Lee, K. Park, J.-H. Ahn, N.-E. Lee, and Y.-J. Kim, “A numerical study on the mechanical characteristics of zinc oxide-based transparent thin film transistors”, Journal of Nanoscience and Nanotechnology, vol. 11, no. 7, pp. 5870-5875, 2011.

[72] N. Lobontiu, E. Garcia, “Mechanics of microelectromechanical systems”, Springer, 2005, pp. 363-365.

[73] B. Bhushan, “Mechanics and reliability of flexible magnetic media”, Springer, 2000, pp. 303-304.

[74] K. Park, D.-K. Lee, B.-S. Kim, H. Jeon, N.-E. Lee, D. Whang, H.-J. Lee, Y. J. Kim, and J.-H. Ahn, “Stretchable, transparent zinc oxide thin film transistors”, Advanced Functional Materials, vol. 20, pp. 3577–3582, 2010.

[75] L. Han, K. Song, P. Mandlik, and S. Wagner, “Ultraflexible amorphous silicon transistors made with a resilient insulator”, Applied Physics Letters, vol. 96, pp. 042111 (3 pages), 2010.

[76] Y. H. An and R. A. Draughn, “Mechanical testing of bone and the bone-implant interface”, CRC Press, pp. 297-300, 2010.

[77] A. Kiani, D. G. Hasko, W. I. Milne, and A. J. Flewitt, “Analysis of amorphous indium-gallium-zinc-oxide thin-film transistor contact metal using Pilling-Bedworth theory and a variable capacitance diode model”, Applied Physics Letters, vol. 102, pp. 152102 (5 pages), 2013.

[78] S.-W. Hahm, H.-S. Hwang, D. Kim, and D.-Y. Khang, "Buckling-based measurements of mechanical moduli of thin films", Electronic Materials Letters, vol. 5, no. 4, pp. 157-168, 2009.

[79] Z. Bao and J. Locklin, "Organic field-effect transistors", CRC Press, pp. 271-272, 2007.

[80] F. Jansen, M. A. Machonkln, N. Palmleri, and D. Kuhmar, "Thermal expansion and elastic properties of plasma-deposited amorphous silicon and sincon oxide films", Applied Physics Letters, vol. 50, pp. 1059-1061, 1987.

[81] J. Gaspar, V. Chu, and J. P. Conde, "Electrostatic microresonators from doped hydrogenated amorphous and nanocrystalline silicon thin films", Journal of Microelectromechanical Systems, vol. 14, issue 5, pp. 1082-1088, 2005.

[82] G. Baek, A. Kuo, J. Kanicki, K. Abe and H. Kumomi, "Electrical properties and stability of dual-gate coplanar homojunction amorphous indium-gallium-zinc-oxide thin-film transistor", IEEE Transactions on Electron Devices, vol. 58, issue 12, pp: 4344-4353, 2011.

[83] J. G. Korvink and O. Paul, "MEMS: a practical guide to design, analysis and applications", William Andrew, pp. 296-298, 2005.

[84] J. Guertin, J. A. Jacobs, and C. P. Avakian, "Chromium (VI) handbook", CRC Press, pp. 25-28, 2004.

[85] R. A. Patil, "Complete stress analysis for two dimensional inclusion problem using complex variables", ProQuest, pp. 39-41, 2007.

[86] C. Jagadish and S. J. Pearton, "Zinc oxide bulk, thin films and nanostructures: processing, properties, and applications", Elsevier, pp. 443-452, 2011.

[87] M. H. Lee, B.-F. Hsieh, and S.T. Chang, "Electrical properties correlated with redistributed deep states in a-Si:H thin-film transistors on flexible substrates undergoing mechanical bending", Thin Solid Films, vol. 528, pp. 82-85, 2013.

[88] R. Yan, D. Lynch, T. Cayron, D. Lederer, A. Afzalian, C.-W. Lee, and J. P. Colinge, "3D simulation of doping fluctuation effects in trigate FETs", Proceedings of the COMSOL Users Conference, Grenoble, France, 2007.