High Efficiency Two-Stage GaN Power Amplifier with Improved Linearity

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

The trade-off between linearity and efficiency is the key limiting factor to wideband power amplifier design. Current wireless research focuses much of its effort on building power amplifiers with the two aforementioned criteria going hand in hand to build an optimal design.

This thesis investigates the sources of nonlinearity associated with GaN high electron mobility transistors (HEMT), and their subsequent effects on the linearity metrics of the power amplifier. The investigation began with an analysis of the sources of nonlinearity, and then a design-based approach to mitigate those sources of nonlinearity was developed. This design approach was compared with existing trends in power amplifier design. The device technology used in the design was CREE GaN HEMT (45W and 6W).

In this report, a systematic approach to designing a two stage power amplifier is discussed, and analyzed for design of linear and highly efficient power amplifiers for base stations. The designed power amplifier consists of two stages: a driver stage and a power stage. The driver stage aimed to linearize the power stage by using circuit analysis and transistor properties along with providing the necessary gain. The power stage was built to complement the driver stage and to achieve high efficiency for the power amplifier. An inter-stage matching network placed between the two stages allowed for the required matching of impedances; transmission lines in the bias feed controlled the harmonic impedances for optimal performance without disrupting performance at fundamental frequencies. This approach effectively improved, and maintained, high efficiency over 200MHz of bandwidth.

The design approach was simulated and fabricated in order to test the feasibility of linear power amplifier operation with the use of digital pre-distortion (DPD). The fabricated prototype achieved about 70% peak efficiency over the bandwidth and maintained linearity above 40dBc adjacent channel leakage ratio (ACLR) and below 3% error vector magnitude (EVM). The measurement results indicated that the need for DPD was eliminated when the power amplifier was operating in back-off at the center frequency (800MHz). This thesis compares the prototyped design with existing multistage designs which use linear drivers. The report provides conclusions derive from measurement results and bandwidth limitations faced throughout the course of the design. Lastly, potential research directions, which may allow researchers to overcome the limitations of this design, are discussed.

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Table of Contents

List of Figures

List of Tables

Chapter 1
Introduction

The evolution of wireless networks has been dictated by a rise in the complexity of communication signals. In order to meet the needs of broadband mobile technology, advanced modulation techniques have been devised such that spectral efficiency is maximized. This has led to communication signals with high peak to average power ratios and, therefore, greater sensitivity to sources of distortions and higher radio system power consumption. This has put a lot of strain on the power hungry power amplifiers. Although one of the dominant sources of nonlinearity, modern power amplifiers are expected to operate linearly and efficiently when processing modern communication signals. To meet these two inconsistent challenges for base station networks, power amplifier designers focus on maximizing efficiency at the power stage; placing little emphasis on the linearity. The resulting distortion, exhibited by the highly efficient power stage, is compensated for by using linearization techniques such as digital pre-distortion (DPD) [1]. This approach is successful to an extent, since the power overhead associated with DPD implementation is negligible when compared with the targeted output power (~50W). However, due to an increase in the density of mobile users and data requirements, wireless networks call for the deployment of large numbers of small cell base stations with output power in the range of 0.25W-5W [2]. Hence, pre-distortion techniques are no longer viable as the DPD power overhead cannot be neglected any longer. Therefore, there is a need to implement a design approach that minimizes the nonlinearity of power amplifiers while maintaining their high power efficiency.

The base station power amplifier design space is mainly dominated by LDMOS and GaN HEMT transistors. Both of these technologies have advantages as well as disadvantages. GaN HEMT transistors have higher power density, higher breakdown and larger bandwidth as compared with LDMOS technology, which makes them more appealing [3]. Choosing GaN over LDMOS technology can result in smaller design sizes for the same output power. However, the drawbacks of GaN transistors, such as soft gain compression, compromise their linearity. Another significant difference between GaN and LDMOS technologies is the nonlinear capacitance. LDMOS has a nonlinear output capacitance; on the other hand, GaN has a nonlinear input capacitance. The distortion caused by the two capacitances is very different and cannot be mitigated in the same manner.

Traditionally, the design of power amplifiers has mainly focuses on the main power stage and the gain requirement has been met by adding linear gain elements (drivers) before the amplifier. These driving stages are made linear in order to maintain the overall linearity of the power amplifier [1]. However, in GaN HEMT transistors, the overall linearity is dictated by the power stage, the linearity of which is quite poor, even at power back-off. By using a nonlinear driving stage, with the opposite nonlinearity of the power stage, a linear amplifier system can be achieved. By appropriately biasing the driving stage and designing the matching networks, a more linear power amplifier can be built.

In this thesis, the nonlinearities associated with GaN HEMT transistors are studied and their mitigation is discussed. The focus of the report is to utilize the required driving stage as a pre-distorter for the main power stage in order to build a linear power amplifier. In addition, the report aims to provide design methods that improve the power amplifier linearity without the use of DPD.

The outline of this thesis begins with a review of transistor models, classical high power amplifier design, power amplifier classes of operation; and an analysis of linearity performance metrics in Chapter 2. Chapter 2 also includes a literature review of recent breakthroughs in augmenting the linearity performance of power amplifiers and their influence on this thesis. In Chapter 3, the design analysis of a two stage power amplifier is outlined and a systematic design approach is presented. Next, the final prototype design and simulation results are presented in Chapter 4, along with measurement results of a fully fabricated power amplifier. A detailed comparison of the proposed design, with popularly used power amplifiers which use linear drivers, is also presented. Lastly, conclusions and recommendations for future work are discussed in Chapter 5.

Chapter 2
Background – High Power Amplifiers

This Chapter of thesis introduces a general transistor model and then narrows down to the specifics of GaN HEMT technology. Next, various classes of operation are discussed and the right class is selected for the design of the two stage power amplifier. In addition, to the basics of a transistor, the sources of nonlinearity associated with GaN HEMT are discussed along with their effects on linearity performance discussed in the Sections 2.3 and 2.4. The Chapter will conclude with a literature review of design solutions which have been implemented in order to improve the linearity of power amplifiers.

2.1 Transistor Technology

Base station power amplifier design is mainly dominated by FET/HEMT technologies. In this section we will discuss the how a FET works and build on its ideal nature by exploring the various non-idealities. An ideal FET can be viewed as an ideal current (I_{DS}) source controlled by an input voltage (V_{GS}) as shown in Figure 2-1.

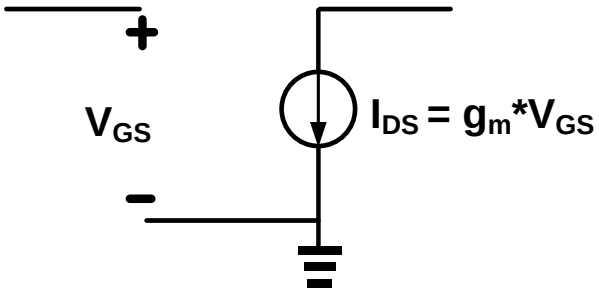


Figure 2-1: Ideal FET model

The ideal linear relationship is given by the transconductance of the FET, g_m. As there are no capacitors present in this ideal model, there is no feedback and the input impedance is infinite.

The operation of the above FET structure is defined by the DC-IV curves shown in Figure 2.2 below. Even though these curves lack many sources of distortion, they still contain a number of

sources of nonlinearity (i.e. the knee region, cut-off and saturation). These sources of distortion are quite significant to the design of power amplifiers and will be studied during the course of this thesis.

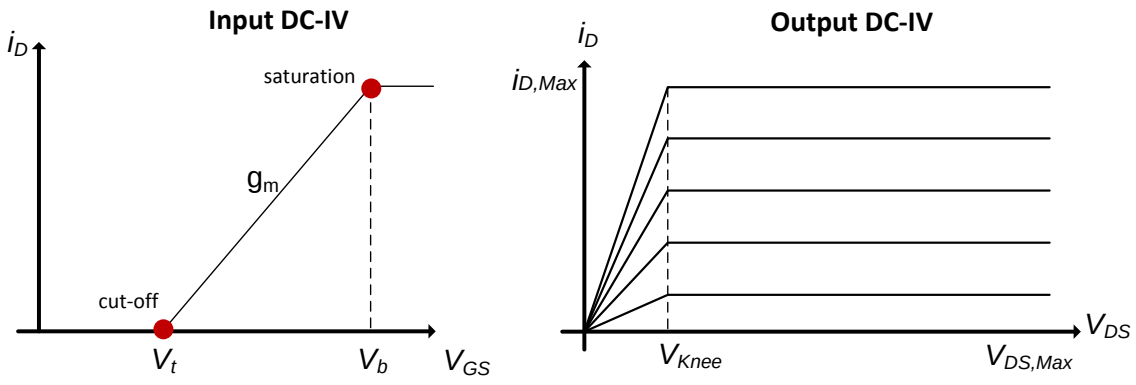


Figure 2-2: DC-IV curves of an ideal transistor

In addition to the sources of distortion discussed above, a transistor has other non-idealities. Figure 2-3 represents an equivalent circuit model of a non-ideal transistor. The current source I_{DS} is a nonlinear function of V_{GS}. Hence, the linear curve shown in Figure 2-2 is no longer valid. In addition, the capacitors C_{gs}, C_{ds} and C_{gd} are also nonlinear functions of V_{GS} as well as V_{DS}. Both the non-ideal current source, and capacitors, affect the linearity of the power amplifier and distort the input and output waveforms. These sources of nonlinearity will be visited in detail during the course of this chapter.

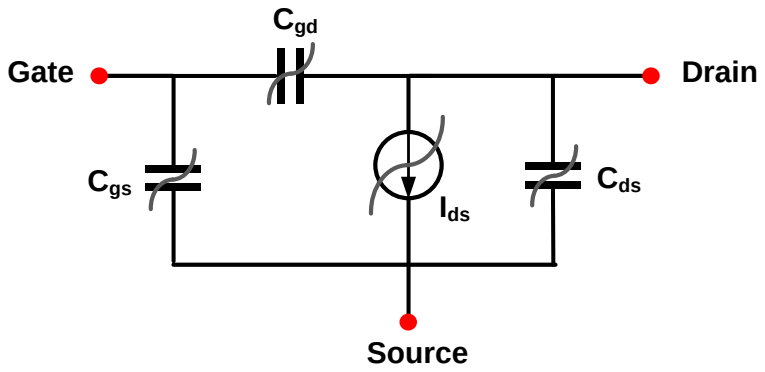


Figure 2-3: Intrinsic transistor model [4]

The RF transistors used by designers are typically either packaged or bare die. Since bare die transistors require more complex assembly, to ease the design process, researchers use packaged

transistor structures. These structures tend to have pre-matching circuits within them that help the designer match the transistor over a specific range of frequencies. However, they add complexity to the device model. In order to completely understand the transistor model used by designers to build power amplifiers, the parasitic inductance and capacitance need to be extracted. The figure below shows the complete transistor model including the package parasitics, as seen by the designer.

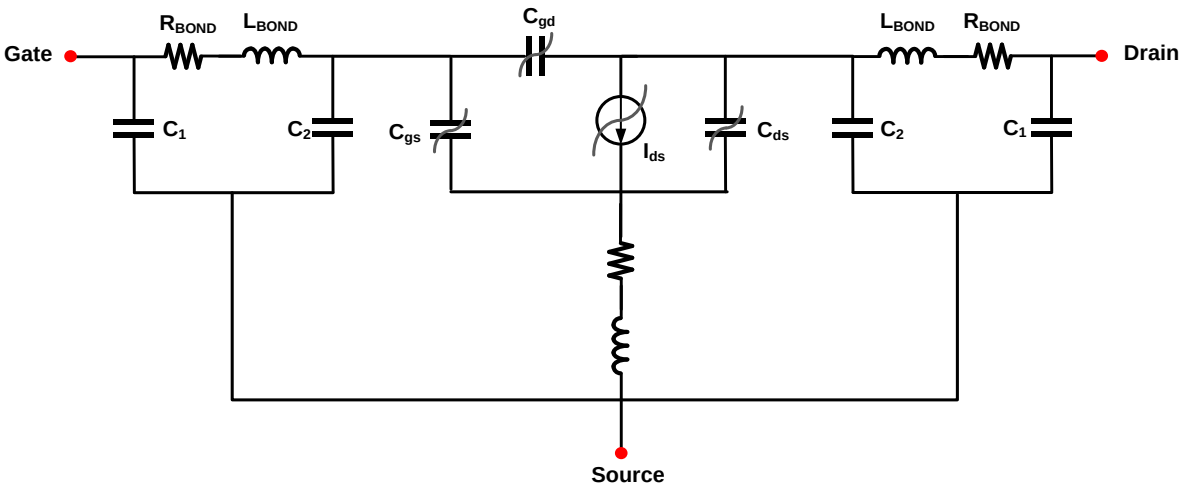


Figure 2-4: Approximate generic package model of a HEMT transistor [4]

This model is more complex and has resistive losses than the ideal model introduced in the beginning of the Chapter. These losses cannot be removed and will result in loss of gain. However, the parasitic inductive and capacitive elements can be merged into the matching networks of the amplifier while designing it.

A typical transistor topology has been discussed above; however, before designing a power amplifier, there is a need to narrow down the specific parasitics, topology and non-linearities. The two main technologies in the field of base station power amplifier design are LDMOS and GaN HEMT.

The main advantage of LDMOS is that the devices are linear when used in back-off and easily linearizable through DPD [5]. This is the main disadvantage of GaN transistors as they have a slow compressing gain [6]. However, there are many advantages of GaN transistors over LDMOS transistors such as higher tolerance to breakdown, resistance to high temperatures, larger bandgap and

higher power density just to name a few [7]. Table 2.1 below summarizes the pros and cons of comparable LDMOS and GaN devices.

Table 2-1: Comparison of LDMOS and GaN HEMT technology [7]

	Silicon LDMOS	GaN HEMT
epi	homogeneous silicon	heterogeneous, GaN
bandgap	1.1 eV	3.4 eV
electron velocity:	-	-
saturated	1 x 10^5 m/s	1.5 x 10^5 m/s
peak	1 x 10^5 m/s	2.7 x 10^5 m/s
breakdown field	25V/µm	300V/µm
typ BVds	75 V	175 V
processing	standard CMOS	bespoke fab
mask count	22	13
max frequency	3.8 GHz	>12 GHz
max temperature	225 °C	250 °C
Johnson's FoM	1	324

Hence, due to the various advantages of GaN HEMT transistor, namely the power density and higher breakdown, it is the choice of technology for the study and design of highly efficient and linear power amplifiers. First, the various non-linearities associated with GaN will be studied following which a design strategy will be develop to build the two stage amplifier.

The next section outlines various classes of operation in order to select the most fitting bias for the two stage design.

2.2 Classes of Operation

The choice of class of operation of a transistor is determined by its application and the performance required. The classical modes of operation of power amplifiers as discussed in this chapter are Class A, B, AB and C. In addition, the advanced concept of class J will also be introduced. The metrics of

comparison for power amplifier design are gain, output power, efficiency, and linearity. The following equations bring the performance metrics together and help with evaluating the classes of operation.

$$\text{Gain} = \frac{P_{out}}{P_{in}} \quad 2\text{-}1$$

$$DE = \frac{P_{out}}{P_{dc}} \quad 2\text{-}2$$

Here, DE is the drain efficiency, P_{out} is the output power of the power amplifier, P_{in} is the input power and P_{dc} is the DC power consumed by the power amplifier.

2.2.1 Class A

Class A amplifiers are commonly known as linear amplifiers. In a Class A amplifier the transistor is biased at the mid-point between the saturation and cutoff regions. It will operate in linear mode with half of the voltage swing on either side of the midpoint [8].

In a Class A amplifier, the voltage swing at the output of the transistor goes from 0 to $2V_{DD}$ where V_{DC} is the voltage biasing point as seen from the DC-IV characteristics. Similarly, the current goes from 0 to I_{max} where $I_{max} = 2I_{DD}$ in a class A, I_{DD} being the current biasing point. The load line shown in Figure 2-5 (blue dotted) is the inverse of the voltage versus the current at any instantaneous value [8]. For a class A power amplifier, the maximum output power is delivered when the load impedance is set to its optimum value, Ropt, given by the following equation:

$$\text{Ropt} = \frac{V_{DD}}{I_{max}/2} = \frac{V_{DD}}{I_{DD}} \quad 2\text{-}3$$

The maximum efficiency of a class A amplifier can be calculated as,

$$DE_{max} = \frac{P_{out}}{P_{dc}} = \frac{0.5V_{DD}^2/R_{opt}}{I_{DD}V_{DD}} = 50\%. \quad 2\text{-}4$$

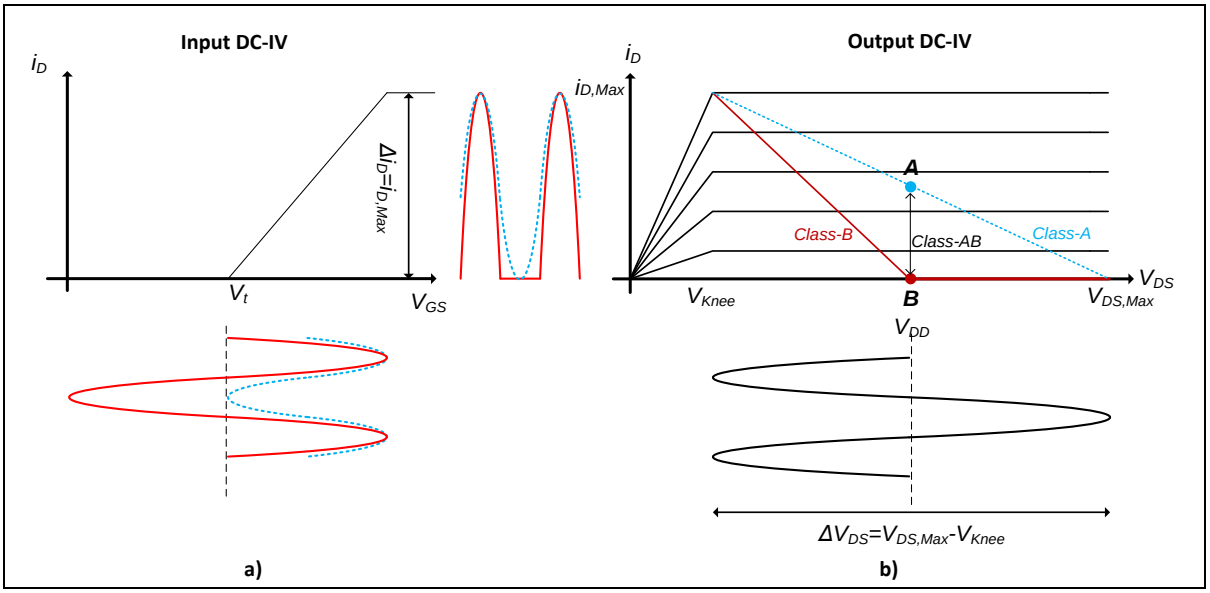


Figure 2-5: DC-IV curves and Drain and Gate Waveforms a) IDS vs. VGS, b) IDS vs. VDS

2.2.2 Reduced Conduction Angle Modes (Class AB, B, C)

In order to improve peak, as well as back-off, drain efficiency the reduced conduction angle modes of operation are employed. To increase drain efficiency as per Equation 2-2, the DC power can be reduced by lowering the biasing current. This results in a sacrifice of part of the gain. The lower conduction angle is the result of the transistor being turned off for part of the time (i.e. below the threshold voltage). The output voltage waveform is unaffected and remains 0 to $2V_{DD}$. Note that all the harmonics at the drain are assumed to be short circuit (i.e. drain voltage contains only fundamental and no harmonics). Class A has a conduction angle of 2π. Class B has a conduction angle of π since its biasing point is at 0A DC current. The output current wave-form is a rectified half sine wave as seen from Figure 2-5. Similarly, Class AB has a conduction angle between that of Class A and B, i.e. 2π to π and Class C has a conduction angle lower than that of Class B (i.e. below π) [8].

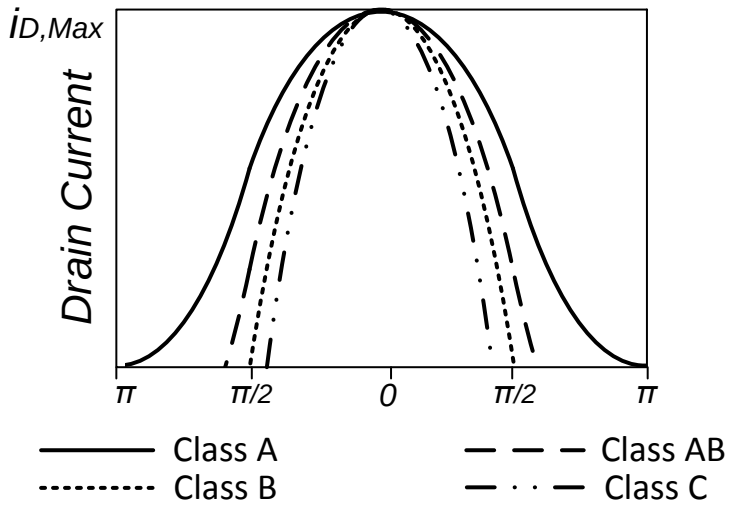


Figure 2-6: Drain Current conduction angles for different classes of operation

The gate biasing voltage can be lowered or increased (upto Class A) in order to vary the class of operation. Figure 2-6 above shows the current waveform under varying biasing points and their respective classes of operation.

The current wave-form of a transistor, at different classes of operation, can be expressed as [8],

$$\mathrm{I}(\theta) = \frac{\mathrm{I_{max}}}{1-\cos(\alpha/2)}.(\cos\theta - \cos(\alpha/2)) \qquad 2\text{-}5$$

Here α is the conduction angle of the current waveform and θ spans from –α/2 to α/2. The DC and fundamental current as a function of conduction angle can be expressed as below [8].

$$\mathrm{I_{dc}} = \frac{1}{2\pi}.\int_{-\alpha/2}^{\alpha/2} \frac{\mathrm{I_{max}}}{1-\cos(\alpha/2)}.(\cos\theta - \cos(\alpha/2))\mathrm{d}\theta \qquad 2\text{-}6$$

$$\mathrm{I_n} = \frac{1}{\pi}.\int_{-\alpha/2}^{\alpha/2} \frac{\mathrm{I_{max}}}{1-\cos(\alpha/2)}.(\cos\theta - \cos(\alpha/2)).\cos\mathrm{n}\theta\mathrm{d}\theta \qquad 2\text{-}7$$

Using the above equations, values of conduction angles and Equation 2.2, the maximum efficiency of class B is 78.5% and for a class A PA, the efficiency is 50%. Hence, the efficiency of a Class AB

PA will fall between that of Class A and B. This will result in a tradeoff of linearity, efficiency and gain.

The Class C PA is biased lower than pinch off voltage and the conduction angle is lower than π. This helps to improve drain efficiency to be higher than 78.5%. The drawback of this class of operation is that the gain is 3dB lower than Class A and the transistor is subjected to more nonlinearity issues.

2.2.3 Class B/J/J* Modes

A Class J/J* power amplifier is similar to a Class B amplifier in that the input is biased at the same point. The current wave-form remains a rectified sine wave. However, in contrast to Class B operation, the fundamental load impedance has a reactive component to it and the second harmonic frequencies are not shorted but have a reactive component termination. This allows the power amplifier in Class J/J* to maintain the same efficiency as Class B (78.5%), but allows for a larger design space. The following equations show the impedance termination of a Class J amplifier [9].

$$Z_{f0} = R_{opt} + j.\alpha.R_{opt} \quad (-1 < \alpha < 1) \tag{2-8}$$

$$Z_{2f0} = 0 - j.\alpha.\frac{3\pi}{8}R_{opt} \quad (-1 < \alpha < 1) \tag{2-9}$$

Here α is a unit less variable that varies from -1 to 1.

In a Class J design, not unlike a Class B design, the higher odd harmonics are ignored as their influence on the design is not significant. In the above Equations (2-8 and 2-9), when α is 0, the Class B operation is reproduced. If α is positive, then Class J mode is achieved and if it is negative, Class J* mode is produced.

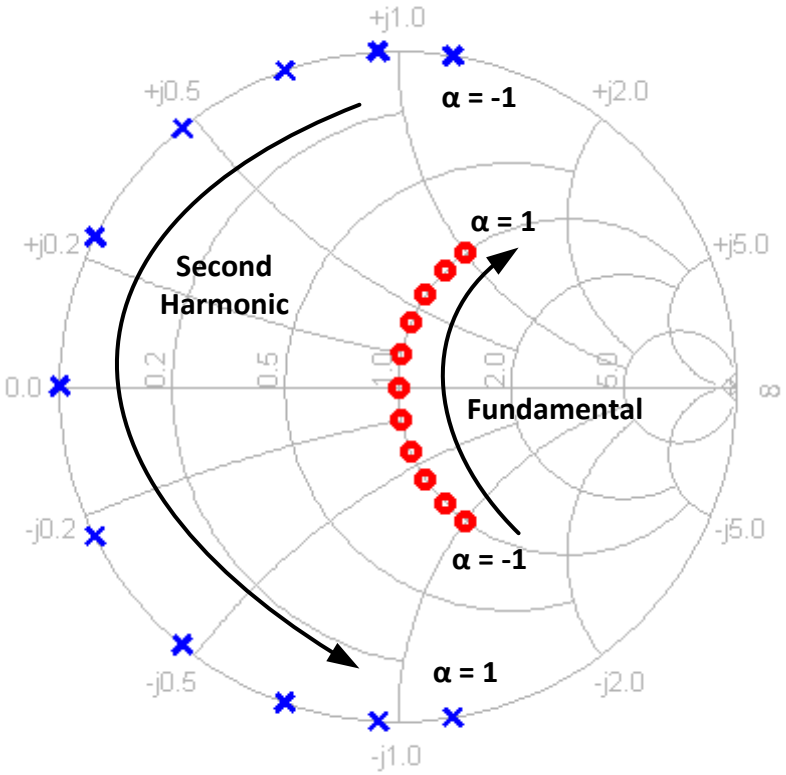


Figure 2-7: Class B/J/J* fundamental and second harmonic design space

The Smith Chart in Figure 2-7 represents the previously discussed design spaces and helps with understanding the impact on each design. Through further analysis [10], it has been concluded that the design space for a Class B/J power amplifier would be larger than that of its counterpart, a Class B amplifier. In turn, the bandwidth of the amplifier is also improved if the harmonic impedances are chosen appropriately [9]. Another advantage to Class J/J* classes of operation is that they allow for the fundamental wave-form to be shaped appropriately such that maximum efficiency can be achieved. This is done through terminating the second harmonic impedance and choosing the right fundamental impedance. The variation in fundamental current with Class B, J and J* is shown in Figure 2-8.

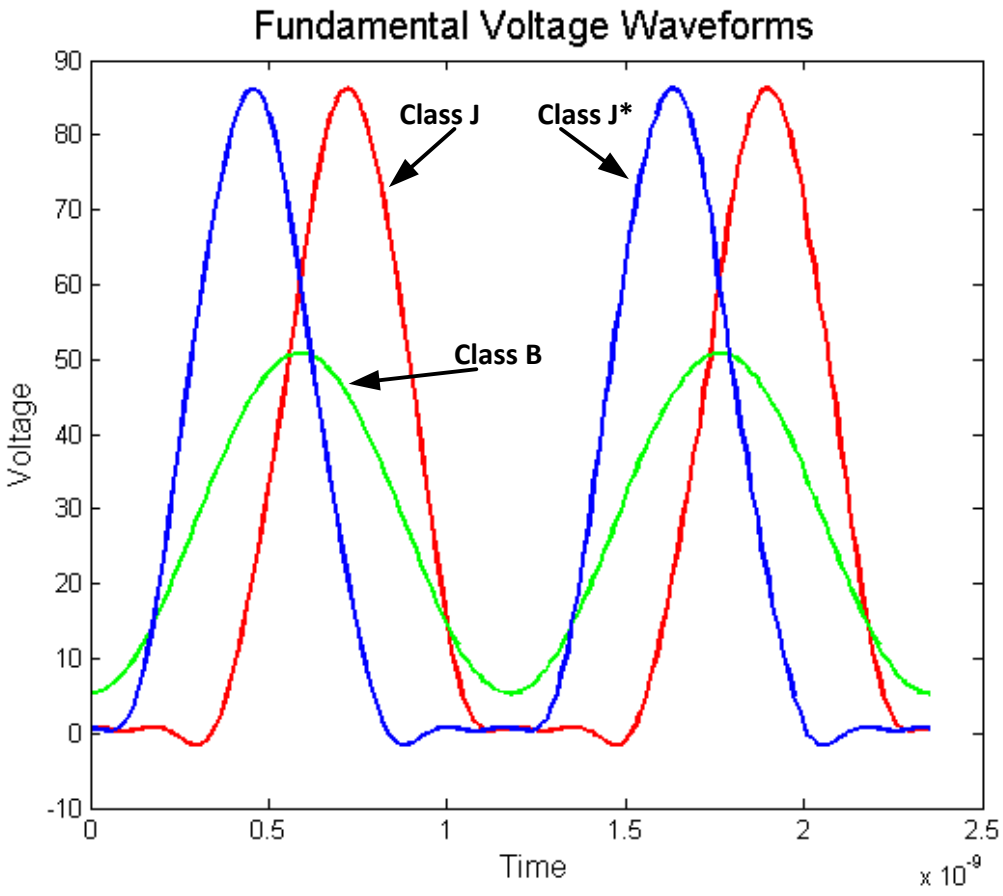


Figure 2-8: Fundamental Voltage Waveforms for Class B/J/J* operation

Being inspired by the class J operation modes, the two stage power amplifier will be designed keeping in mind that the fundamental impedance can be matched with the complex impedance. This will help to increase the design space and provide more control over the harmonics. In addition, the second harmonic impedance can be tuned in order to desensitize the power amplifier to changes in its value that arises from either errors in fabrication or errors with the actual transistor impedance.

2.3 Sources of Nonlinearity in GaN HEMT transistors

It has been found that GaN has a number of sources of nonlinearity [6] [11]. This thesis will only be discussing the most dominant sources of nonlinearity, i.e. nonlinear input capacitance,

transconductance and knee region. These sources of nonlinearity have a significant effect on the performance of the power amplifiers as discussed in the next few sections.

2.3.1 Nonlinear Input Capacitance

Due to the physics of GaN HEMT transistors, the performance of the power amplifier will be affected by the capacitors (C_{gs}, C_{gd} and C_{ds}). The drain to source capacitor is not very nonlinear in GaN HEMT devices and hence does not affect the performance as much. On the other hand, the input capacitance in a GaN HEMT device has a nonlinear characteristic versus the input voltage V_{gs} [11]. The input capacitance includes the nonlinear input C_{gs} as well as the Miller capacitance of the nonlinear C_{gd}. The nonlinear input capacitance distorts the input signal, creating harmonic distortions that in turn affect the AM/AM and AM/PM and, as a result the ACPR and EVM of the amplifier. This effect has shown to hinder the linearizability of the amplifier as shown in [11]. The Figure 2-9 is a simple circuit approximation of the input of the transistor.

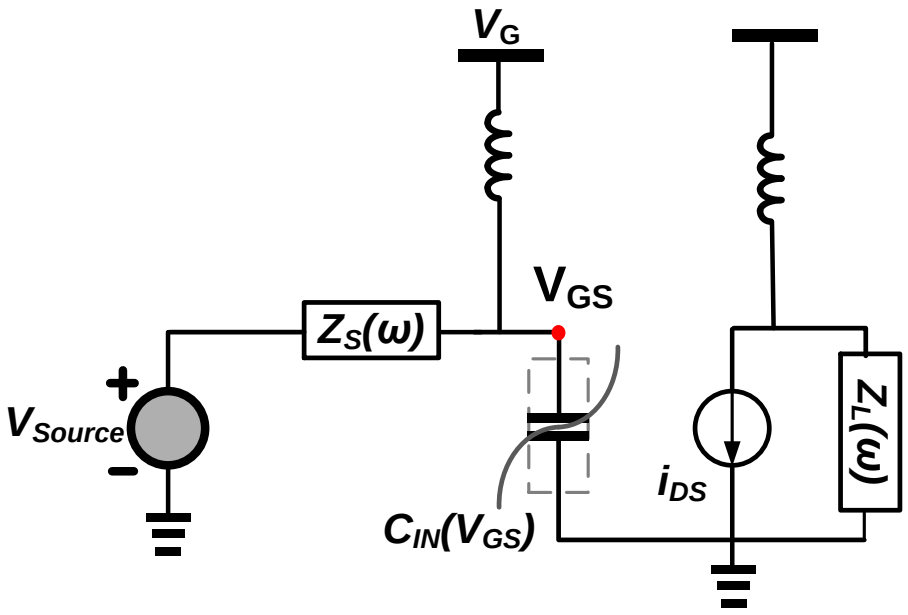


Figure 2-9: Simple equivalent circuit of GaN HEMT device

To understand the effects of the nonlinear input capacitance on the input signal, the following derivation has been devised [12]. The input capacitor of a GaN HEMT transistor can be approximated as a nonlinear function of the applied input voltage as shown via Equation 2-10; C_A and C_B are constants

$$C_{in} = C_A + C_B.tanh(V_{gs} - V_t) \quad 2\text{-}10$$

The Taylor expansion of the above nonlinearity has been truncated and it has been assumed that the input capacitor only contributes up to the second order of nonlinearity. It has been assumed that V_t is very small, almost negligible.

$$C_{in} = C_0 + C_1.V_{gs} + C_2.V_{gs}^2 \quad 2\text{-}11$$

The input voltage is a real sinusoidal signal with only a fundamental component. Z(ω0) is the source impedance of the power amplifier and is selected such that all other harmonics except the fundamental are shorted at V_{GS}. The equations below are time-domain representations of the input voltage and drain current. Here, V_S is the magnitude of the fundamental input voltage.

$$V_{in} = V_S.\cos(\omega_0 t) \quad 2\text{-}12$$

$$i(t) = C_{in}\frac{dV_{gs}}{dt} \quad 2\text{-}13$$

The voltages and currents below are shown in phasor form and up to the third order of nonlinearity.

$$V_{in}(\omega) = [0\ V_S\ 0\ 0] \quad 2\text{-}14$$

$$V_{gs}(\omega) = [V_0\ V_1 e^{j\theta_1}\ V_2 e^{j\theta_2}\ V_3 e^{j\theta_3}] \quad 2\text{-}15$$

$$I(\omega) = [0\ I_1 e^{j\alpha_1}\ I_2 e^{j\alpha_2}\ I_2 e^{j\alpha_2}] \quad 2\text{-}16$$

The variables α and θ represent the phase shift of the various frequency components of i(t) and $v_{GS}(t)$ from the input voltage $v_{in}(t)$. The following sets of equation denote the time domain counterparts of the above equations.

$$v_{in}(t) = Re[V_S e^{j\omega_0 t}] \quad 2\text{-}17$$

$$v_{gs}(t) = Re[V_0 + V_1 e^{j\omega_0 t + j\theta_1} + V_2 e^{2j\omega_0 t + j\theta_2} + V_3 e^{3j\omega_0 t + j\theta_3}] \quad 2\text{-}18$$

$$i(t) = Re[I_1 e^{j\omega_0 t + j\alpha_1} + I_2 e^{2j\omega_0 t + j\alpha_2} + I_2 e^{3j\omega_0 t + j\alpha_2}] \quad 2\text{-}19$$

In phasor form, the input current is related to the input voltage as follows, where $Z_S(\omega_0)$ is the source impedance.

$$I(\omega) = \frac{V_{in}(\omega) - V_{gs}(\omega)}{Z_S(\omega)} \quad 2\text{-}20$$

Using Equation 2-13, expansion of Cin can be included.

$$i(t) = C_0.\frac{dV_{gs}}{dt} + C_1.V_{gs}.\frac{dV_{gs}}{dt} + C_2.V_{gs}^2.\frac{dV_{gs}}{dt} \quad 2\text{-}21$$

After applying Equation 2-18 to 2-21. Since all harmonics have been short circuited by $Z_S(\omega_0)$ at V_{GS} (red point), V_{gs} only remains with the fundamental and DC components.

$$i(t) = C_0.[\omega_0 V_1 \sin(\omega_0 t + \theta_1)] + C_1.[V_0 + V_1\cos(\omega_0 t + \theta_1)].[\omega_0 V_1 \sin(\omega_0 t + \theta_1)] + C_2.[V_0 + V_1\cos(\omega_0 t + \theta_1)]^2.[\omega_0 V_1 \sin(\omega_0 t + \theta_1)] \quad 2\text{-}22$$

All of the fundamental terms are gathered in the equation below.

$$i(t) = C_0.\omega_0 V_1 \sin(\omega_0 t + \theta_1) + C_1.\omega_0 V_0 V_1 \sin(\omega_0 t + \theta_1) + C_2.[\omega_0 V_0^2 V_1 \sin(\omega_0 t + \theta_1) + 0.25\omega_0 V_1^3 \sin(\omega_0 t + \theta_1)] + (\dots)\sin(2\omega_0 t + \theta_1) + \cdots \quad 2\text{-}23$$

The above equation is transformed to its phasor form in order to equate it to Equation 2-20. Here, $Y_S(\omega_0) = 1/Z_S(\omega_0)$

$$\left(V_{in}(\omega_0) - V_{gs}(\omega_0)\right)Y_S(\omega_0) = C_0.j\omega_0 V_1 e^{j\theta_1} + C_1.j\omega_0 V_0 V_1 e^{j\theta_1} + C_2[j\omega_0 V_0^2 V_1 e^{j\theta_1} + 0.25j\omega_0 V_1^3 e^{j\theta_1}] \quad 2\text{-}24$$

$$\left(V_{in}(\omega_0) - V_1(\omega_0)\right)Y_S(\omega_0) = C_0.j\omega_0 V_1 e^{j\theta_1} + C_1.j\omega_0 V_0 V_1 e^{j\theta_1} + C_2[j\omega_0 V_0^2 V_1 e^{j\theta_1} + 0.25j\omega_0 V_1^3 e^{j\theta_1}] \quad 2\text{-}25$$

Hence,

$$V_{in}(\omega_0)Y_S(\omega_0) = (C_0.j\omega_0 e^{j\theta_1} + C_1.j\omega_0 V_0 e^{j\theta_1} + C_2.\left[j\omega_0 V_0^2 e^{j\theta_1} + 0.25j\omega_0 V_1^2 e^{j\theta_1}\right] + Y_S(\omega_0))V_1(\omega_0) \quad 2\text{-}26$$

$$V_1(\omega_0)e^{j\theta_1} = \frac{V_{in}(\omega_0)Y_S(\omega_0)}{\left(C_0.j\omega_0 + C_1.j\omega_0 V_0 + C_2.[j\omega_0 V_0^2 + 0.75j\omega_0 V_1^2] + Y(\omega_0)\right)} \quad 2\text{-}27$$

We can decompose $Y_S(\omega_0)$ into its real and imaginary part and find the magnitude and phase of the input voltage.

$$V_1 = V_S.\sqrt{\frac{G_S^2(\omega_0) + B_S^2(\omega_0)}{\left(C_0.\omega_0 + C_1.\omega_0 V_0 + C_2.[\omega_0 V_0^2 + 0.25\omega_0 V_1^2] + B_S(\omega_0)\right)^2 + G_S^2(\omega_0)}} \quad 2\text{-}28$$

$$\theta_1 = \tan^{-1}\left(\frac{B_S(\omega_0)}{G_S(\omega_0)}\right) - \tan^{-1}\left(\frac{\left(C_0.\omega_0 + C_1.\omega_0 V_0 + C_2.[\omega_0 V_0^2 + 0.25\omega_0 V_1^2] + B_S(\omega_0)\right)}{G(\omega_0)}\right) \quad 2\text{-}29$$

As seen from the above equations, the magnitude of the input voltage at C_{in} is a function of the input source voltage (V_S) as well as its own magnitude. Similarly, the phase of the voltage on C_{in} is a function of its magnitude. This nonlinear relationship of phase and magnitude will be discussed later in this chapter to understand the influence on various performance metrics.

2.3.2 Transconductance

The transconductance of GaN HEMT devices has a very slow turn on region in addition to a nonlinear curve. The input DC-IV of a GaN 45W transistor is shown in Figure 2-10 [11].

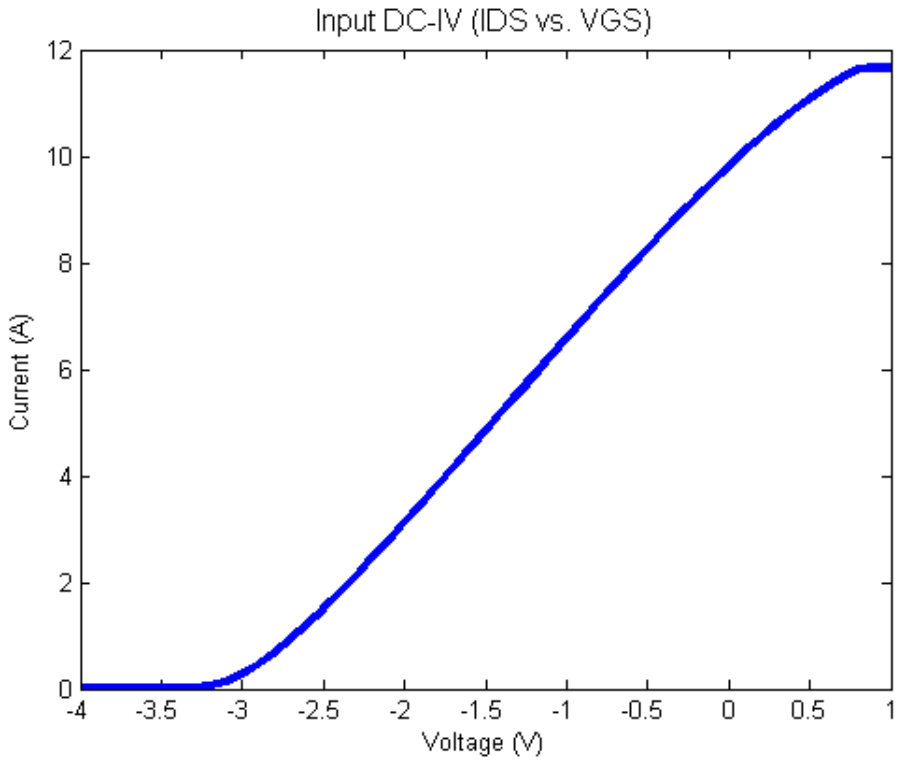


Figure 2-10: Simulated input DC-IV curve (IDS vs. VGS)

The relationship between the DC biasing current and the gate biasing current is a nonlinear function in GaN HEMT transistors as seen from Figure 2-10. This relationship defines the small

signal transconductance gm. Similarly, the large signal fundamental transconductance is defined as follows.

$$Gm(\omega) = \frac{\partial I_{DS}(\omega)}{\partial V_{GS}(\omega)} \qquad 2\text{-}30$$

This fundamental G_m nonlinearity varies versus the gate biasing voltage resulting in a different nonlinear function versus input power. In order to see the actual effect of transconductance nonlinearity on the power amplifier performance, the fundamental transconductance G_m is simulated at different biasing voltages (V_{gs}) in Figure 2-11. As seen from these curves, we have a wide range of biasing points that allow for compression and expansion nonlinearity at higher power. This provides freedom in the design of the power amplifier as a choice of biasing point could help improve the gain linearity of the power amplifier.

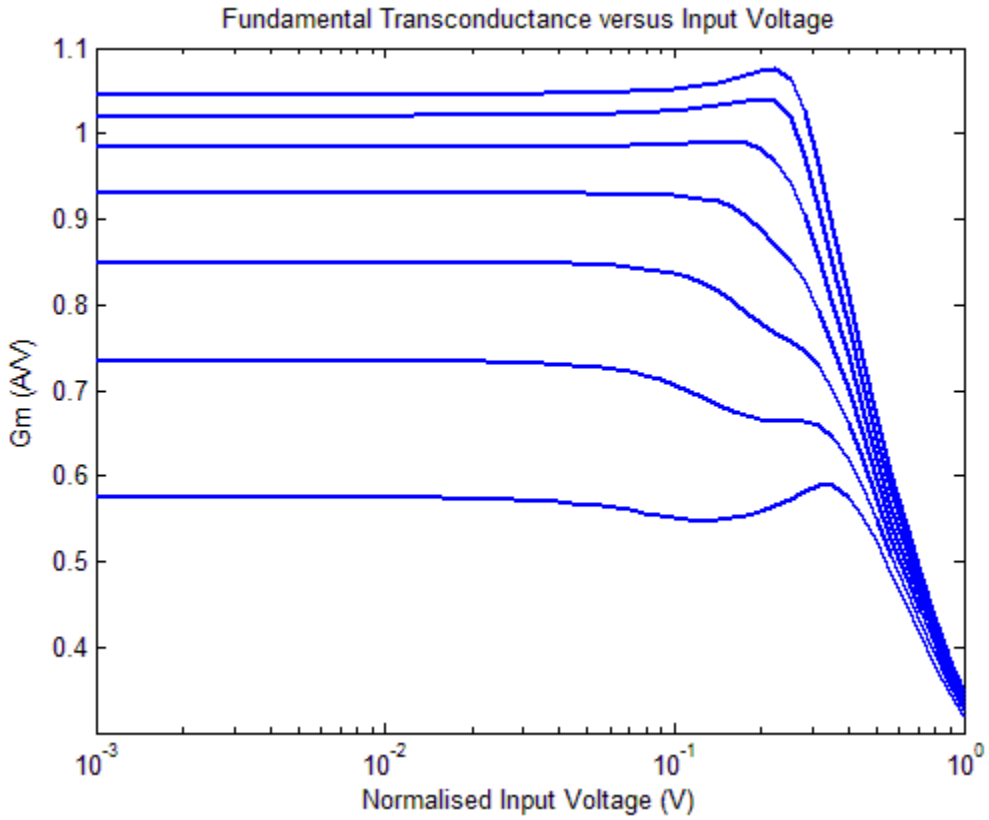


Figure 2-11: Simulated fundamental transconductance (Gm) vs. input voltage (Vsource) at different biasing points

The effect of input voltage and biasing voltage on the fundamental transconductance G_m can be shown by the analysis below. Figure 2-9 is a simple circuit approximation of the input of the transistor. The Taylor expansion of the i_{DS} versus v_{GS} nonlinearity has been truncated and it has been assumed that it only contributes to odd orders of nonlinearity.

$$i_{DS}(t) = gm_1.V_{gs}(t) + gm_3.V_{gs}^3(t) \quad 2\text{-}31$$

It has been assumed that all harmonics at V_{GS} are shorted and only the fundamental component is present along with DC. $Z_S(\omega_0)$ is the source impedance of the power amplifier which shorts out all harmonics except the fundamental.

The voltages and currents below are shown in phasor form, up to the third order of nonlinearity. Here, V_S is the fundamental input voltage and V_1 to V_3 are the first to third harmonics of V_{GS}

$$V_{in}(\omega) = [0\ V_S\ 0\ 0] \quad 2\text{-}32$$

$$V_{gs}(\omega) = [V_0\ V_1 e^{j\theta_1}\ V_2 e^{j\theta_2}\ V_3 e^{j\theta_3}] \quad 2\text{-}33$$

$$I_{DS}(\omega) = [0\ I_1 e^{j\alpha_1}\ I_2 e^{j\alpha_2}\ I_2 e^{j\alpha_2}] \quad 2\text{-}34$$

The following sets of equation denote the time domain counterparts of the above equations. The variables α and θ represent the phase shift of the various frequency components of i(t) and $v_{GS}(t)$ from the input voltage $v_{in}(t)$.

$$v_{gs}(t) = Re[V_0 + V_1 e^{j\omega_0 t + j\theta_1} + V_2 e^{2j\omega_0 t + j\theta_2} + V_3 e^{3j\omega_0 t + j\theta_3}] \quad 2\text{-}35$$

$$i_{DS}(t) = Re[I_1 e^{j\omega_0 t + j\alpha_1} + I_2 e^{2j\omega_0 t + j\alpha_2} + I_2 e^{3j\omega_0 t + j\alpha_2}] \quad 2\text{-}36$$

$$i_{DS}(t) = gm_1.[V_0 + V_1\cos(\omega_0 t + \theta_1)] + gm_3.[V_0 + V_1\cos(\omega_0 t + \theta_1)]^3 \quad 2\text{-}37$$

$$\begin{aligned} i_{DS}(t) = {} & gm_1.[V_0 + V_1\cos(\omega_0 t + \theta_1) + gm_3.[V_0^3 \\ & + V_1^3\left(\frac{\cos 3(\omega_0 t + \theta_1) + 3\cos(\omega_0 t + \theta_1)}{4}\right) + 3V_0^2 V_1\cos(\omega_0 t + \theta_1) \\ & + 3V_0 V_1^2\left(\frac{1 + \cos 2(\omega_0 t + \theta_1)}{2}\right)] \end{aligned} \quad 2\text{-}38$$

A relationship is formed between the fundamental current and voltage, and is done by:

$$I_{DS}(\omega_0) = gm_1 V_1 e^{j\emptyset_1} + gm_3\left[0.75.V_1^3 e^{j\emptyset_1} + 3V_0^2 V_1 e^{j\emptyset_1}\right].e^{j\omega_0 t} \quad 2\text{-}39$$

$$Gm(\omega_0) = \frac{I_{DS}(\omega_0)}{V_{GS}(\omega_0)} = gm_1 + gm_3[0.75.V_1^2 + 3V_0^2] \quad \text{2-40}$$

As seen from the above equation, it is obvious that the fundamental transconductance is a nonlinear function of both the gate biasing voltage (V_0) as well as the magnitude of input power (V_1).

2.3.3 Knee Region

Another source of nonlinearity, present in almost all transistors, is the knee region. Figure 2-12 shows the DC-IV curves of a 45W GaN HEMT device. When the voltage waveform, as shown in Figure 2-7 enters the knee region (triode region of the transistor), the current waveform gets distorted. This results in the addition of harmonics to the ideal voltage and current waveforms. This distortion is present in all classes of operation when the signal, at high power, enters the knee region of the transistor.

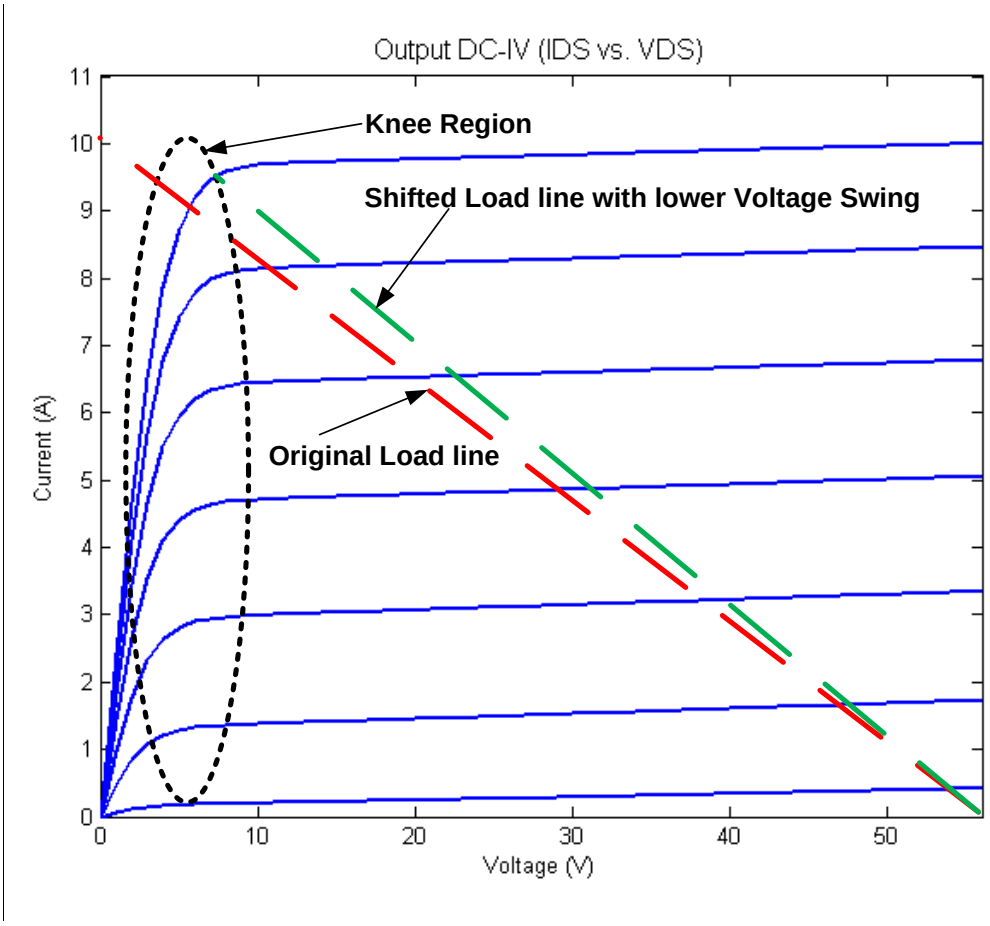


Figure 2-12: Simulated output DC-IV curve (IDS vs. VDS)

As seen from Figure 2-11, the different transconductance curves enter the knee region at around 0.3V of input power regardless of the biasing point of the transistor. There is a very quick and noticeable gain compression once the large signal enters the knee region. In order to reduce the amount of distortion caused, the Ropt as per Equation 2-3 can be reduced, by reducing the voltage swing. This will in turn sacrifice the efficiency by a few percent.

2.4 Effects of Nonlinearity on the Performance of Power Amplifiers

In this section of the chapter, the linearity metrics, AM/AM and AM/PM, are introduced and discussed. This section will also evaluate the effects of the sources of nonlinearities discussed earlier, on AM/AM and AM/PM.

2.4.1 AM/AM

This figure of merit describes the relationship between output and input powers at the fundamental frequency. AM/AM helps evaluate the measure of expansion or compression introduced by transistor nonlinearity. The knee region as discussed in Section 2.3.3 is the cause of the steep compression drop close to the end of the AM/AM curve. This nonlinearity is seen in all classes of operation and in ideal transistors.

Typically, that would be the only nonlinearity in an AM/AM curve. However, before the knee region, GaN HEMT transistors are subjected to quite significant slow gain compression due to the transconductance nonlinearity. From Section 2.3.2, it has be shown that the fundamental transconductance (G_m) nonlinearity can be given by,

$$Gm(\omega_0) = gm_1 + gm_3[0.75.V_1^2 + 3V_0^2] \quad \text{2-41}$$

The fundamental transconductance is a nonlinear function of both fundamental (V_1) and DC (V_0) voltage at V_{GS}. This results in the gain of the power amplifier to compress and expand at different biasing points, as shown by the Gm curves in Figure 2-11 [6]. This in turn degrades the linearizability of these devices and the DPD requirement is still maintained at back-off power levels.

In addition to transconductance and knee region, nonlinear input capacitance also contributes to AM/AM nonlinearity. As discussed in Section 2.3.1, the impact of nonlinear capacitance is decomposed into the magnitude of fundamental V_{gs} as shown by equation below.

$$V_1 = V_S.\sqrt{\frac{G_S^2(\omega_0) + B_S^2(\omega_0)}{\left(C_0.\omega_0 + C_1.\omega_0 V_0 + C_2.[\omega_0 V_0^2 + 0.25\omega_0 V_1^2] + B_S(\omega_0)\right)^2 + G_S^2(\omega_0)}} \quad 2\text{-}42$$

The above equation clearly shows that the voltage V_{GS} is a nonlinear function of input voltage V_S and its own value. This results in a complicated relationship between V_{gs} and the nonlinear input capacitance which is not a straight forward resolve. The harmonics produced due to this nonlinearity, further distort the gate signal which further compresses AM/AM. However, the effect of nonlinear input capacitance can be minimized through some circuit methods including proper termination of harmonics at the input of the transistor.

2.4.2 AM/PM

This figure of merit describes the nonlinearity associated with the phase of the output signal with respect to the input power. It is a good measure of the static nonlinearity as well as the memory effects induced in the power amplifier. The main cause of AM/PM in GaN HEMT transistors is the vector addition of the fundamental power with the harmonics when they are produced by the distortion generated by the transistor. The variation in AM/PM, as well as its shape versus frequency, influence the overall linearity performance measure; represented by ACPR and EVM along with the spread of the spectrum (memory effects) when subjected to modulated signals [11].

The nonlinearity that causes AM/PM targeted in this design is the nonlinear input capacitance which adds significant phase distortion. The variation of input capacitance with the gate voltage causes the phase to change nonlinearly with the input voltage. The harmonics produced due to the nonlinearity, also add to this effect. The analysis shown in Section 2.3.1 explains the effect of the nonlinear input capacitance on AM/PM through the derivation of the following equation.

$$\theta_1 = \tan^{-1}\left(\frac{B_S(\omega_0)}{G_S(\omega_0)}\right) - \tan^{-1}\left(\frac{(C_0.\omega_0 + C_1.\omega_0 V_0 + C_2.[\omega_0 V_0^2 + 0.25\omega_0 V_1^2] + B_S(\omega_0))}{G_S(\omega_0)}\right) \quad 2\text{-}43$$

In order to decrease the phase nonlinearity and keep the phase value to minimum, $B_S(\omega_0)$ needs to be capacitive, i.e. $B_S(\omega_0)$ is positive. This results in the maximum reduction of phase variation contributed by C_{in} to AM/PM [11].

However, this results in the loss of gain as per equation 2-28 as it is required that $B_S(\omega_0)$ be negative (inductive) in order to maximize gain. Ultimately, the choice of input impedance ($Z_S(\omega_0)$) is going to be based on a tradeoff between gain and phase nonlinearity.

2.5 Literature

In order to begin the design, it was clear that a transistor type needed to be chosen. LDMOS transistors dominate base station power amplifiers due to their lower costs. However, with the emerging advantages of GaN HEMT, both industrial as well as academic research have been focusing on developing GaN HEMT transistor based power amplifiers. The work presented in [13] compares similar LDMOS and GaN die transistors. From the data presented, it was evident that GaN transistors dominate in terms of efficiency, higher breakdown voltage and gain. These advantages are mainly dictated by the fact that GaN HEMT technology has a higher bandgap. Another pro for the GaN technology is that it has a higher power density which allows for the design to be smaller in size. The broader bandwidth of GaN HEMT, along with better efficiencies allows for the development of better power amplifiers for future applications [3].

Two major issues with GaN HEMT transistors are the nonlinear input capacitance and slowly compressing transconductance [6]. Many approaches have been proposed in the literature to deal with the above two issues.

The design presented in [14] utilizes a nonlinear feedback loop to linearize the power amplifier. The feedback loop consists of two capacitors and transistors as shown in Figure 2-13.

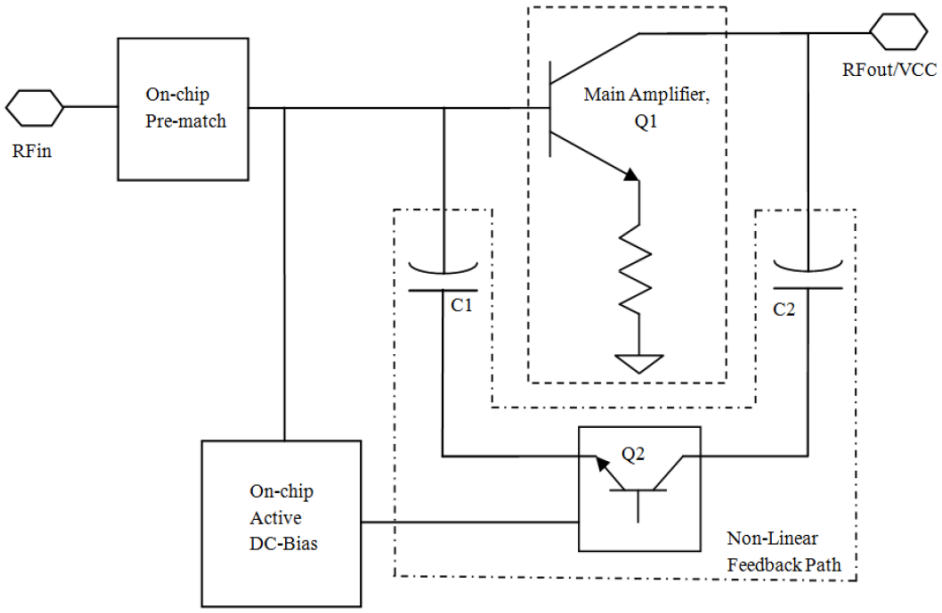


Figure 2-13: Main amplifier with nonlinear feedback [14]

The values of the capacitor and transistor biasing point were adjusted such that the intermodulation distortion (IMD) of the main output amplifier was suppressed. However, this was done at one output level and one frequency. Hence, the ability to design this amplifier for a wider bandwidth would be difficult. In addition, EVM requirements were not discussed, which is a significant linearity metric in power amplifier design.

The work presented in papers [15] and [16] is based on tuning the biasing point of the driver and output power stage in order to cancel the gain nonlinearity and achieve better linearity. However, the biasing points of a power amplifier change its design parasitics and impedances; varying them on bench would result in possible loss of efficiency and gain.

The work presented in [17] uses two transistors with different sizes in parallel to cancel out the IMD produced at the output of the power amplifier. This approach is used to linearize the compression nonlinearity produced by the transconductance by offsetting the gain biases of the two transistors, as shown in Figure 2-14.

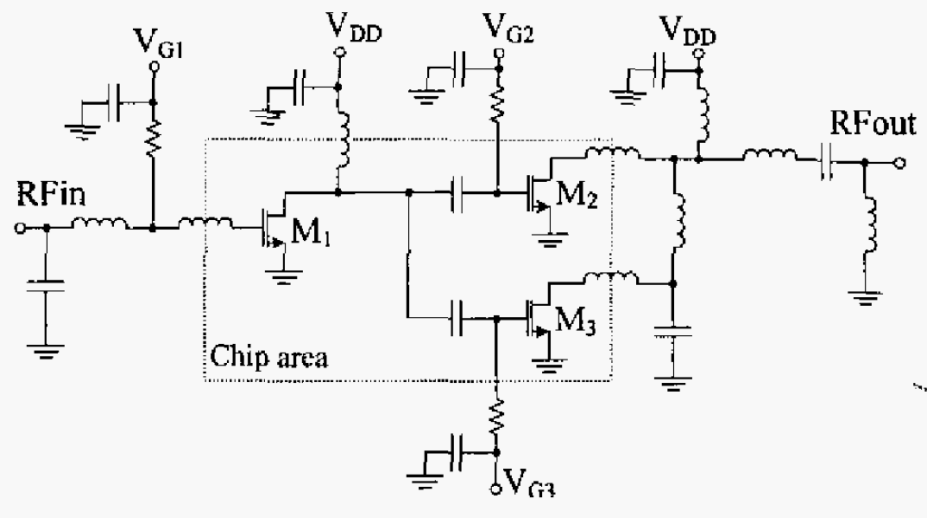


Figure 2-14: Parallel path IMD cancellation technique [17]

Another similar design that analyses the possibility of reducing the gain nonlinearity is presented in [18]. In this work, compression of the output stage was cancelled out by the expansion generated by the driver stage. This was done by providing an anti-phase IMD produced by the driver stage for the output stage. This results in almost no power in the 3rd order sidebands.

The papers discussed abovewere able to minimize the gain nonlinearity. However, other key nonlinearity elements were missing. There is a potential for linearity improvement if the phase nonlinearity associated with each design were to be studied and compensated. Secondly, signal bandwidth discussed was 5MHz, which will not be enough in the next few years as the density of wireless users is rising and wireless standards are demanding higher data rates. Thirdly, there is a possibility that fifth order IMD components may still be present and distort the AM/AM curve. Hence, this technique might work for a small bandwidth of 5MHz WCDMA one carrier signal but not a multicarrier WCDMA signal for a base station as the linearity and bandwidth requirements are more stringent.

Another methodology implemented to improve the linearity of a power amplifier is to eliminate the variation of the input capacitance with respect to the input voltage. One method to minimize this nonlinearity is to provide the input with a mirror opposite nonlinear capacitance. Such a design has been presented in [19].

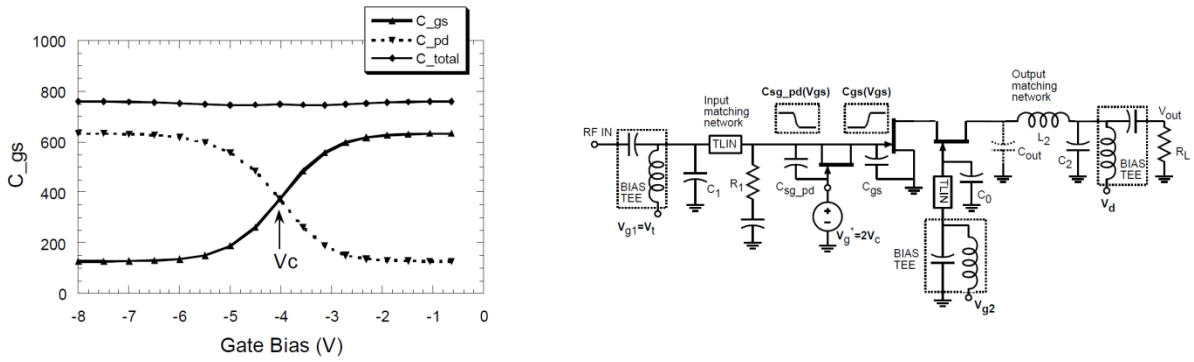


Figure 2-15: a) Capacitance with and without pre-linearization b) Pre-linearization circuit [19]

This method of linearization resulted in a flat input capacitance response with respect to input voltage. As a result, AM/PM distortion was reduced to achieve better ACPR and EVM. As seen from the IMD measurements, there was not significant improvement in IMD at higher power levels. This could be due to the fact that certain sources of distortion were missing from this analysis such as nonlinear transconductance. This solution would also suffer from significant heating due to the presence of two transistors in close proximity with significant biasing currents. In addition, this method of linearization would result in high input capacitance over all power levels which could cause a significant loss of gain in the power amplifier.

Chapter 3
Design Analysis of Power and Driver Stages

This chapter discusses the design methodology and design analysis of the two stage amplifier. The procedure of using the driver stage of the amplifier to pre-distort the signal will be and investigated and a crude design will be completed at the end of this section.

3.1 Problem statement

The GaN amplifiers used nowadays achieve 20% efficiency and almost always require DPD at all power levels. The additional power used by DPD lowers the efficiency further at back-off power levels. The need for DPD arises due to the fact that ACLR and EVM are not able to meet the specifications of the mask. Due to the slow compression in GaN HEMT designs, DPD is always needed. The figure below shows two cases of EVM and ACLR; one requiring DPD at all times and the other requiring DPD at higher powers.

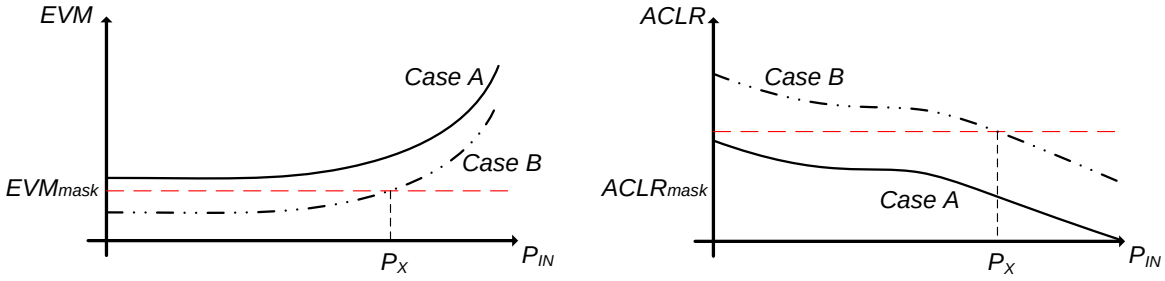


Figure 3-1: Targeted EVM and ACLR performance of two stage power amplifier design

As it can be seen above, the need for DPD is eliminated at powers above P_X as the mask requirements are satisfied by case B. Hence, the aim of this thesis is to move away from the case B design (most power amplifiers today) and build a case B design.

This thesis attempted to design a linear amplifier by using a two stage amplifier design and leveraging the driver that was used to boost gain. The driver worked as a nonlinear pre-distorter to linearize the two stage design.

Before beginning the analysis of the two stage power amplifier, two transistors needed to be selected. The power stage was selected to be 45W transistor. The driver stage was selected to provide just enough input power. Since the smallest available transistor was 6W, it was used as the driver. The design structure shown in Figure 3-2 below helps with the analysis of the two stage power amplifier.

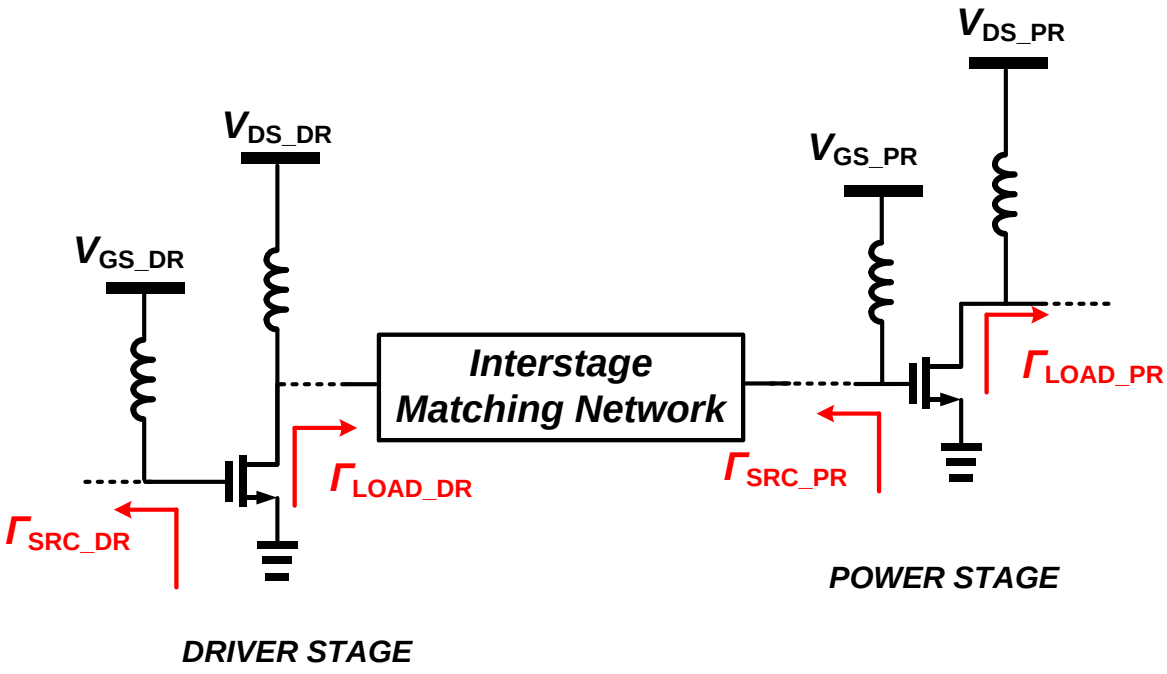


Figure 3-2: Two stage power amplifier design methodology

3.2 Biasing Points

The two main linearity metrics studied in section 2.4 are AM/AM and AM/PM. Both of these metrics are a function of a number of parameters mainly the biasing points, the reflection load and source coefficients, and harmonic termination. In order to build a linear power amplifier, the AM/AM of the power stage needs to be linear with no soft compression. This can be done by pre-distorting it with the driver stage AM/AM as shown through Figure 3-3 below.

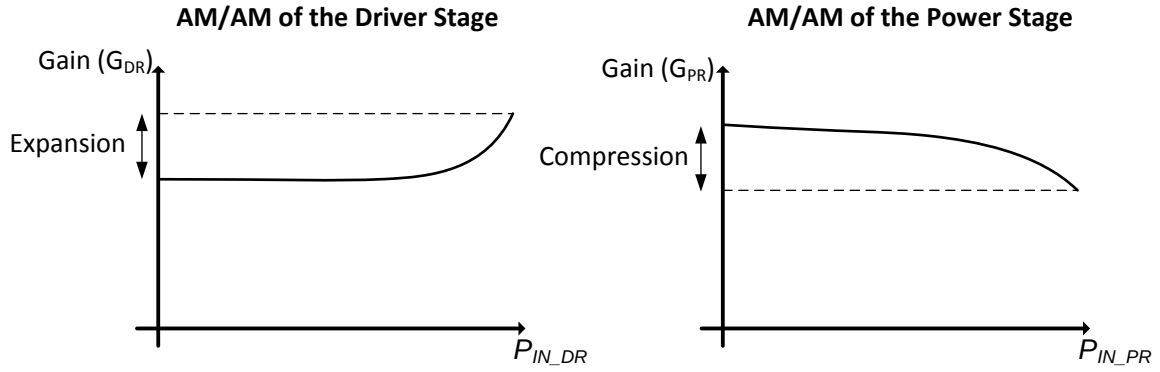


Figure 3-3: Pre-distortion using driver to linearize power stage

The AM/AM of the driver and power stage are a function of a few parameters as shown by equations below.

$$G_{DR} = f(V_{GS\_DR}, V_{DS\_DR}, \Gamma_{SRC\_DR}, \Gamma_{LOAD\_DR}) \quad 3\text{-}1$$

$$G_{PR} = g(V_{GS\_PR}, V_{DS\_PR}, \Gamma_{SRC\_PR}, \Gamma_{LOAD\_PR}) \quad 3\text{-}2$$

Here, V_{GS} is the gate biasing point, V_{DS} is the drain biasing point and Γ_{SRC} and Γ_{LOAD} are source and load reflection coefficients respectively. The most dominant nonlinearity in the AM/AM curve is the Gm nonlinearity as discussed in section 2.3.2. Hence, the major control parameter above is the biasing point V_{GS}. Hence, the less dominant control parameters can be used to fine tune the design once a course design is achieved.

3.2.1 Power Stage

The first step towards designing the two stage power amplifier was to select a suitable bias point for the power stage. The Gm curves as shown in Figure 2-11 show various gain profiles at different biasing points. In order to have a flat AM/AM, the biasing point with the most constant Gm was selected. The selected biasing point was at Class AB at a drain biasing current of 400mA.

In order to choose the appropriate biasing point for the drain voltage of the power stage, 28V was selected as it is the recommended value for transistors used in this design [20]. This also ensured that an output power of 45W was achievable by selecting the appropriate fundamental impedance whilst achieving maximum possible efficiencies.

The following is the AM/AM curve of the power stage that was used to select appropriate biasing point of the driver stage.

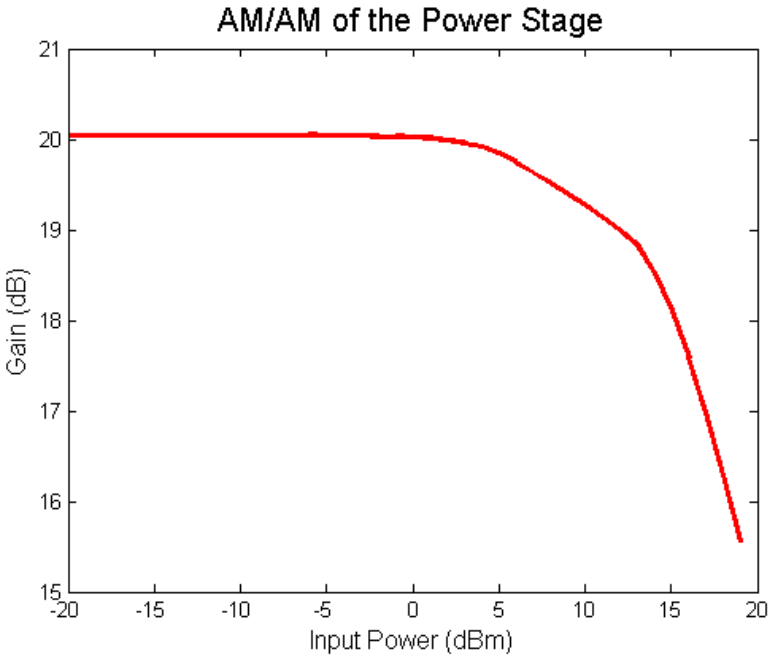


Figure 3-4: AM/AM of power stage at 850MHz

3.2.2 Driver Stage

In order to design the nonlinear driver stage, the AM/AM curves of the power stage shown in Figure 3-4 were used. The driver biasing point is picked such that it provided the same amount of expansion as there was compression in the power stage. The Figure 3-5 below represents the AM/AM of the driver at the chosen biasing point. As seen from figure below, the driver is able to linearize the power stage up to 15dBm of input power. Here, the knee region was not linearized as both the driver and power stages eventually enter the knee region and it cannot be completely eliminated.

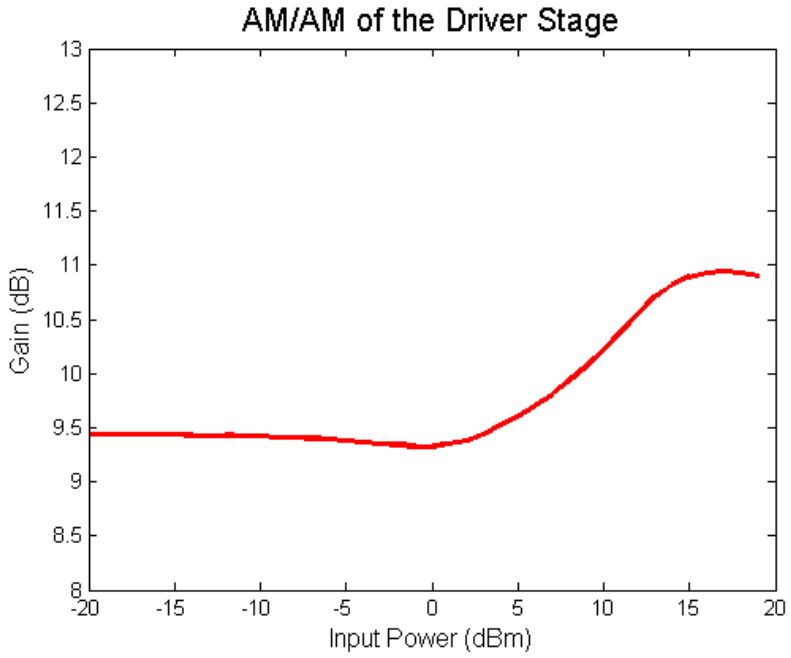


Figure 3-5: AM/AM of the nonlinear driver stage at 850MHz

In the first step of picking the drain biasing point of the driver, it was set to the suggested value of 28V to get maximum output swing and maximum efficiency. However, the two stage efficiency will be affected following the equation below.

$$\eta_{total} = \frac{P_{out}}{P_{dc}} = \frac{P_{out}}{V_{DS\_DR} * I_{DS\_DR} + V_{DS\_PR} * I_{DS\_PR}} \quad 3\text{-}3$$

Here, V_{DS} and I_{DS} are the voltage and current biasing points at the drain. In order to maintain the two stage efficiency as close to the power stage as possible, the drain of the driver was down biased to 15V. This reduced the contribution of the driver's efficiency to the two stage amplifier's overall efficiency.

For the comparison of the linear and nonlinear drivers, the biasing point of the linear driver has to be chosen such that the driver operated in class A operation mode. Hence, the driver is up-biased to 150mA.

A summary of the biasing points of each stage are shown in the table below. These results are from the first iteration of design and were adjusted when the two stages of the power amplifier were put together.

Table 3-1: Biasing points of the two stage power amplifier

Biasing Points	$V_{DS}\ (V)$	$I_{DS}\ (mA)$
Power Stage	28	150
Nonlinear Driver Stage	15	25
Linear Driver Stage	15	150

3.3 Fundamental Impedance and Harmonic Termination

In order to finely control the AM/AM and AM/PM of the two stage amplifier, the fundamental load and source impedances are chosen keeping in mind a good performance overall. The main consideration to be kept in mind is to reduce the amount of total AM/PM by using the driver AM/PM to cancel out the AM/PM produced by the power stage using the load and source impedances (Γ_{SRC} and Γ_{LOAD}).

The AM/PM can be controlled with load and source matching as well as harmonic matching. As shown below, the equations represent the AM/PM as a function of the above parameters. The major contributors to controlling AM/PM are source matching (Γ_{SRC}) and harmonic impedance termination ($\theta(2\omega_0)$).

$$\Phi_{DR} = f(V_{GS\_DR}, \Gamma_{SRC\_DR}, \Gamma_{LOAD\_DR}, \theta_{DR}(2\omega_0)) \quad 3\text{-}4$$

$$\Phi_{PR} = f(V_{GS\_PR}, \Gamma_{SRC\_PR}, \Gamma_{LOAD\_PR}, \theta_{PR}(2\omega_0)) \quad 3\text{-}5$$

The first step to the impedance selection was selecting the load impedance of power and driver stages. Being inspired by the class J methodology, the optimum load impedance is selected such that the reactive component of the load impedance allows the freedom to tune harmonic impedance for better efficiency and linearity and have a larger design space. Hence, the reactive impedance of the load impedance is chosen to be inductive (class J).

The optimum fundamental source impedance of power stage is first chosen to reduce the AM/PM produced. The power stage AM/PM is chosen such that the effect of the input capacitance is minimized, which is the main contributor to the AM/PM nonlinearity, as seen from section 2.4.2. In

order to make the nonlinear input capacitance variation less significant, the source matching can be chosen to be capacitive. From Equation 2-29, it is evident that a capacitive source matching reduces the nonlinearity contribution of input capacitance to the AM/PM. This results in partial sacrifice of gain as shown from Equation 2-28, which will be boosted by the additional gain contribution of the driver stage. The AM/PM of the power stage is shown in figure below.

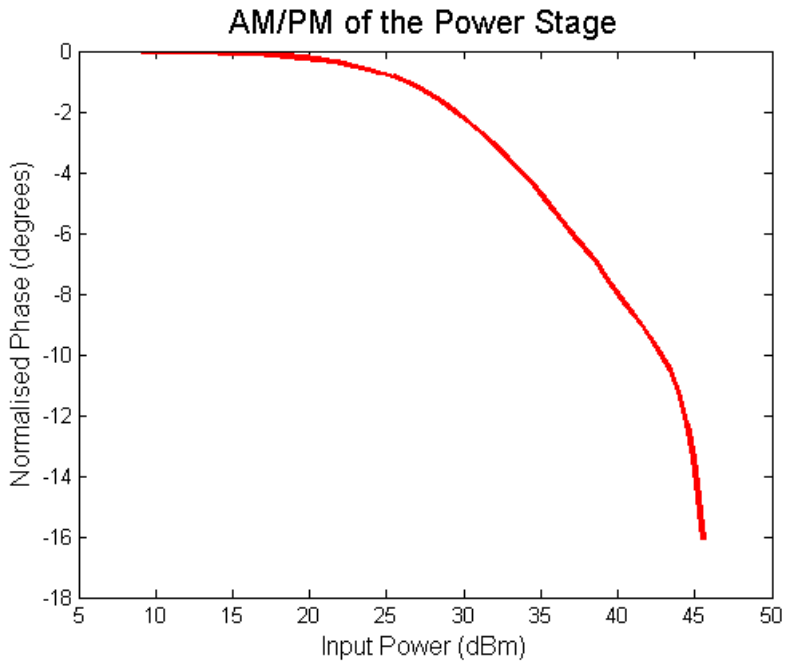


Figure 3-6: AM/PM of power stage at 850MHz

Once the fundamental source impedance of the power stage is selected, the driver stage impedances can be selected in a similar manner to achieve an AM/PM curve that will compensate for the above power stage AM/PM. This is done by selecting the appropriate input matching of the driver stage. The driver stage AM/PM is shown below.

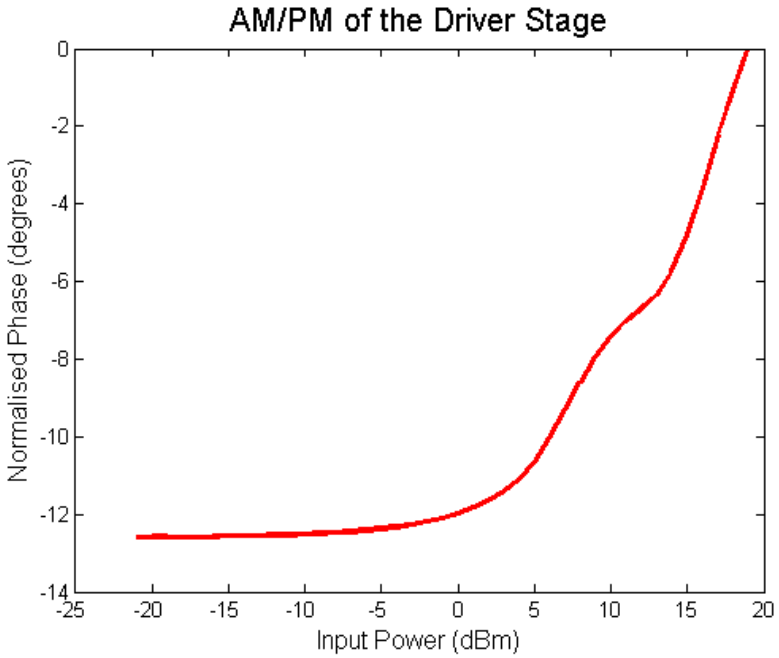


Figure 3-7: AM/PM of the nonlinear driver stage at 850MHz

Hence, the AM/PM of the driver compensated for the AM/PM of the power stage resulting in a flatter overall AM/PM curve of the two stage amplifier. The nonlinear driver and the linear driver both had similar fundamental impedance terminations and hence, were designed to be the same.

The harmonic impedances are used to fine tune the AM/PM once the source and load fundamental impedances are chosen. The harmonic impedance is imaginary and the angle of termination is varied in order to tune the performance. The two criteria limiting the second harmonic termination are the characteristic impedance and length of the bias feed, and their effect on fundamental and second harmonic bandwidth. The impedance of the bias feed transmission line can be given by equation 3-6 [21].

$$Z_{BIAS} = Z_O \tan \beta l \qquad 3\text{-}6$$

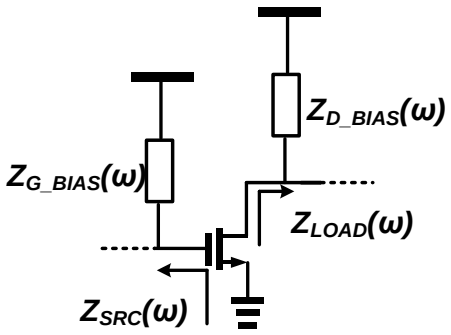


Figure 3-8: schematic structure of a power amplifier

As seen from Figure 3-8 above, the optimum impedance termination of the transistor is impacted by bias feed impedance. For the design of bias feed, the fundamental impedance should be very high close to being open such that the all power is transferred to the load. The second harmonic should be terminated to almost a short such that no power is transferred to the load. If the design was a class B or class AB, the bias feed length can be made $\lambda/4$ (90°) which in turn makes the second harmonic length $\lambda/2$ (180°) and an open and short are achieved at fundamental and second harmonic respectively.

However, as it can be seen from the Figure 3-9 below, in order to keep the efficiency of the power amplifier high, the short and open solution is not feasible as the frequency of the design declines when the angle of second harmonic termination is chosen to be 180°.

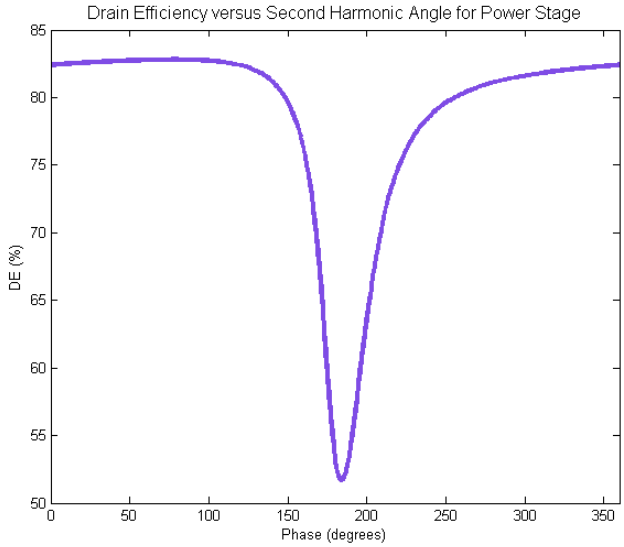


Figure 3-9: Drain Efficiency vs. second harmonic phase of power stage

In order to select the appropriate harmonic termination, the region of phase is selected from Figure 3-9 to be not too sensitive and maintains good efficiency.

The second step is to select the characteristic impedance. As stated above, the fundamental impedance has to be high and second harmonic impedance has to be low. That is, the characteristic impedance Z_0 from Equation 3-6 needs to be high for better fundamental bandwidth performance, but has to be low for better harmonic termination bandwidth. Hence, a tradeoff has been made in this design and Z_0 is tuned such that both harmonic and fundamental terminations are satisfied over a small bandwidth. The following table summarizes the initial values of fundamental impedances and harmonic terminations for the power and driver stages.

The summary of load and source impedances and harmonic terminations are shown below.

Table 3-2: Impedance summary of the two stage design at 850MHz

	Load Impedance	Source Impedance	$Z_O(2\omega_0)$ (Gate)	Electrical Length (Gate)	$Z_O(2\omega_0)$ (Drain)	Electrical Length (Drain)
Power Stage	8+j5 Ω	5.5-j2 Ω	34 Ω	150°	50 Ω	120°
Driver Stage	46+j15 Ω	20-j24 Ω	50 Ω	20°	34 Ω	200°

This chapter has summarized the design methodology and the procedure followed in order to build the power and driver stages. The theory used in this chapter will be used in the following chapter to build the complete design of the two stage power amplifier.

Chapter 4
Design of the Two Stage Power Amplifier

The analyses of the power and driver stages were completed in the previous chapter and will be used to complete the design of the two stage power amplifier in this chapter. The schematic of the two stage power amplifier is shown in Figure 4-1below.

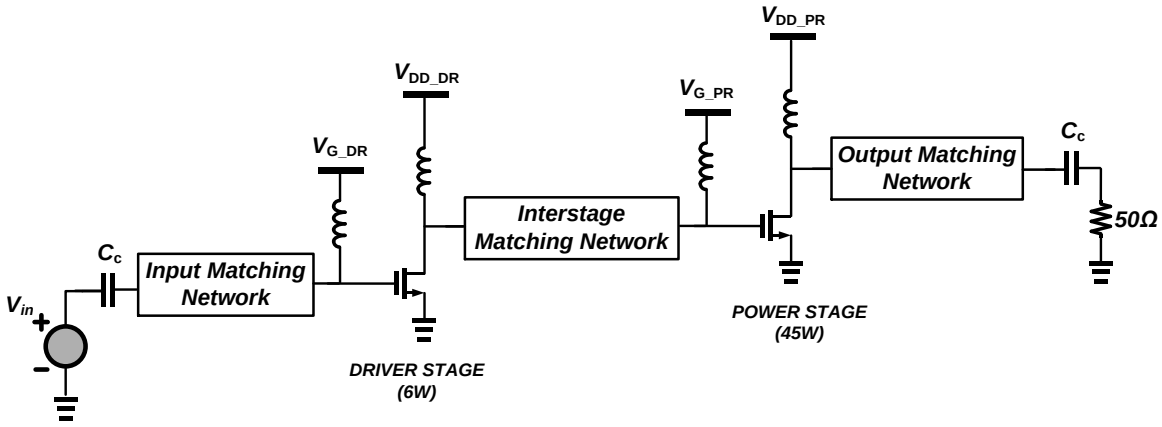


Figure 4-1: Schematic of two stage power amplifier

After selecting the biasing points and impedance terminations in chapter 3, the power and driver stages are connected using an inter-stage matching network in order to complete the two stage design. The analysis done in the previous chapter was using ideal transmission lines and load tuners and will need to be tuned to incorporate the non-idealities such as transmission line losses, the harmonics injected from the driver stage into the power stage and impedance mismatches to name a few.

4.1 Matching Network Design

4.1.1 Inter-stage Matching Network Design

After designing the driver and power stages separately using tuners and ideal matching components, the two stages were connected together through an inter-stage matching network. The

figure below shows the inter-stage matching structure and reflection coefficients used to build the final structure.

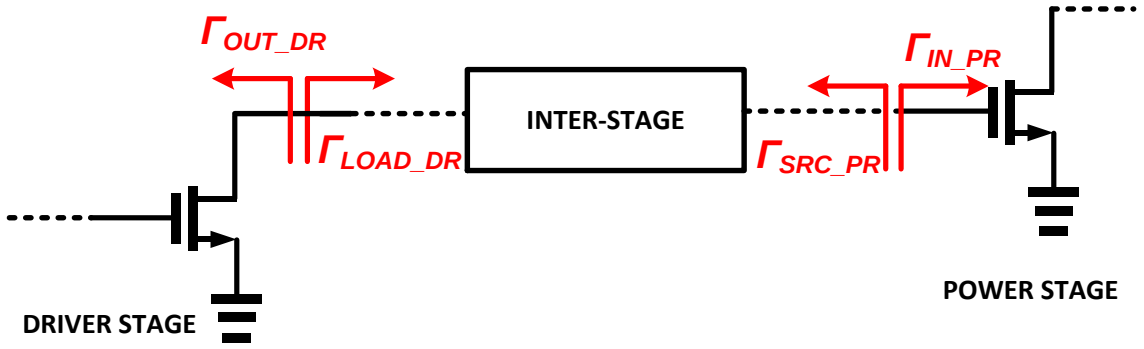


Figure 4-2: Inter-stage matching methodology structure

The design of this stage had some complication associated with it. Firstly, since neither the optimum load impedance of the driver (Z_{LOAD_DR}) nor the optimum source impedance of the power stage (Z_{SRC_PR}) are conjugate matched to their respect transistors, there was no physical impedance matching. Hence, a proper impedance matching network cannot be built by merely matching the values of Z_{LOAD_DR} and Z_{SRC_PR}. In order to match the optimum impedances of the two stages, an optimization loop technique was devised as shown in Figure 4-3.

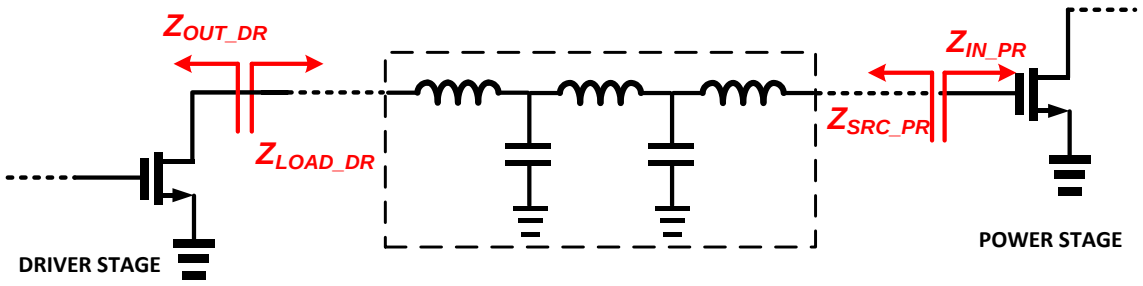


Figure 4-3: Optimization structure for inter-stage design

As seen from the figure, Z_{LOAD_DR} is matched to the input impedance of the power stage (Z_{IN_PR}) and Z_{SRC_PR} is matched to the output impedance of the driver (Z_{OUT_DR}). The matching network is optimized to match the real and imaginary impedances in both directions of the matching network.

The impedance transformation from Z_{LOAD_DR} to Z_{IN_PR} had some limitation during the design. The input impedance of the power stage varied versus frequency (imaginary part) as seen from Figure 4-4.

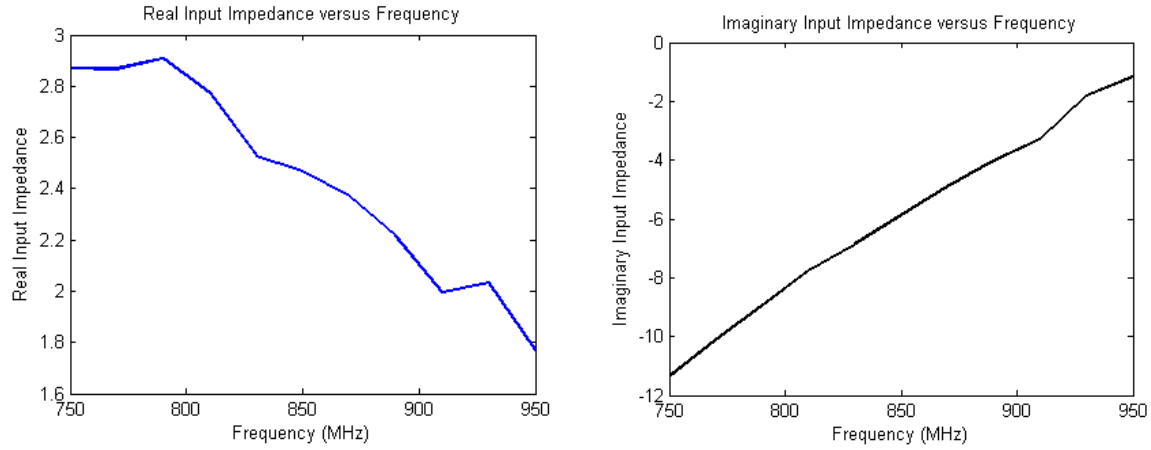


Figure 4-4: Input impedance of the power stage a) Real impedance b) Imaginary impedance

In order achieve good AM/PM, this varying input impedance (Z_{IN_PR}) needs to be matched to load impedance (Z_{LOAD_DR}) versus frequency, however, there is drawback. The matching network also causes a variation in the real part of Z_{LOAD_DR}; which must remain constant versus frequency. Variation in the real or imaginary parts of Z_{LOAD_DR} results in either a very steep drop of gain or added AM/PM, respectively.

Different matching techniques were tested to overcome this limitation, such as tapered line, multi-section matching networks (up to 5 sections) and the combination of the above two techniques. It was concluded that this limitation would have to result in a trade-off between AM/PM (variable imaginary part) and the bandwidth. Hence, the bandwidth of performance was limited to 100MHz even though the continuous wave (CW) performance fared well for a larger bandwidth as seen from section 4.2.

Hence, the design of the two stage power amplifier was limited to a bandwidth of 100MHz to maintain the AM/AM and AM/PM performance for optimized linearity. The final driver load impedance of the two stage amplifier is shown below.

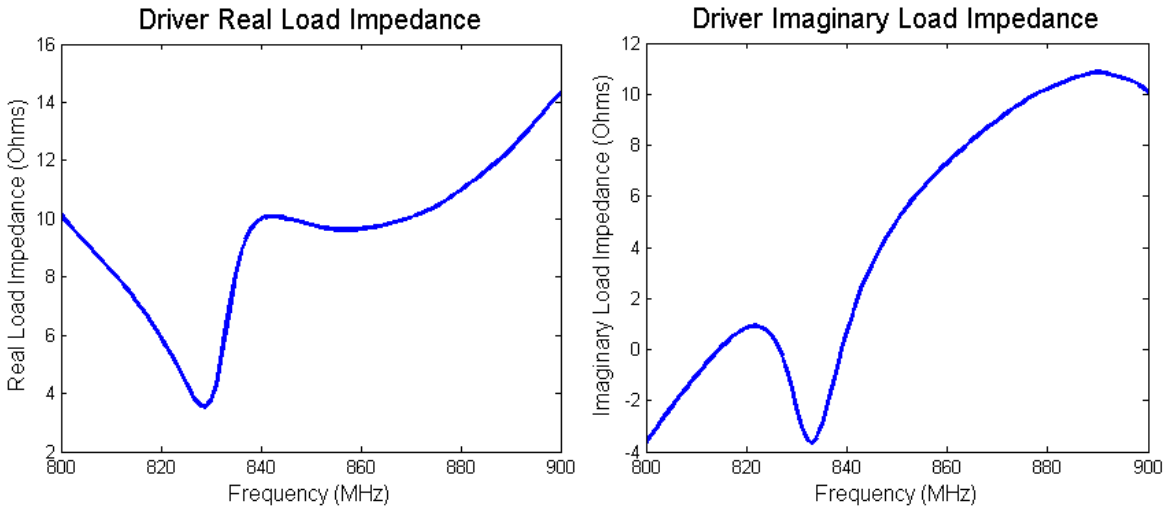


Figure 4-5: Driver load impedance versus frequency of the two stage design

Once the inter-stage matching network was built, the source impedance of the driver and the load impedance of the power stage were optimized along with the harmonic impedance terminations.

4.1.2 Input and Output Matching Networks

The input and output matching networks for the two stage amplifier were designed to transform the optimum source impedance of the driver and optimum load impedance of the power stage to 50Ω termination. Distributed transmission line matching is used to achieve a wide bandwidth of about 200MHz.

Once the design of the matching networks was completed, the biasing points and harmonic terminations were tuned to provide the optimized performance intended by the design. The final biasing points, fundamental impedance and harmonic terminations are shown in the table below.

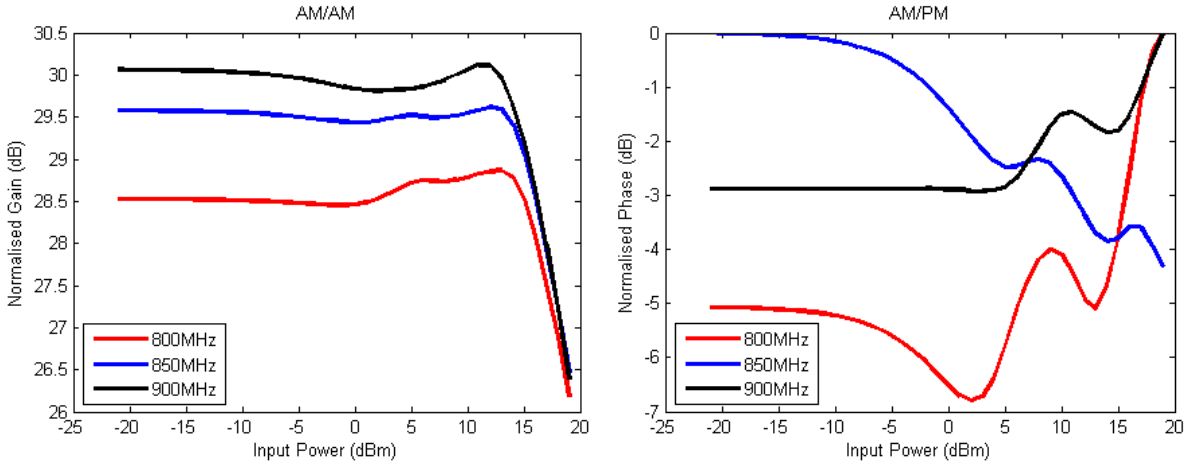
Table 4-1: Summary of final design biasing points, fundamental and harmonic impedances

	Power Stage	Driver Stage
Drain Biasing Current	400mA	15mA
Drain Biasing Voltage	28V	15V
Load Fundamental Impedance	8+j5 Ω	10+j4 Ω
Source Fundamental Impedance	6-j5 Ω	20-j24 Ω
$Z_O(2\omega_0)$ (Gate)	34 Ω	50 Ω
Electrical Length (Gate)	57°	110°
$Z_O(2\omega_0)$ (Drain)	50 Ω	34 Ω
Electrical Length (Drain)	80°	20°

4.2 Simulation Results

In this section, relevant simulation results have been presented. The simulation results were performed first at the schematic level and then converted to layout using the Momentum tool in ADS2011. After completing both the DC and harmonic balance analyses, the following results were obtained. Momentum simulations provided a good indication of the expected measurement results after fabrication.

Figure 4-6, below shows the AM/AM and AM/PM results for the two stage power amplifier design at three frequencies across the bandwidth.



a) **b)**

Figure 4-6: Simulated a) AM/AM and b) AM/PM of the two stage power amplfier

As seen above, the AM/AM curves have only 1.5 dB of compression at maximum output power of 46dBm. The amount of AM/PM deviation is limited to 7° within the bandwidth. The goal is to pass the mask of ACLR and EVM and study the effects of AM/AM and AM/PM of the two stage power amplifier on these two metrics.

The following figure shows, maximum efficiency, maximum output power and small signal gain versus frequency.

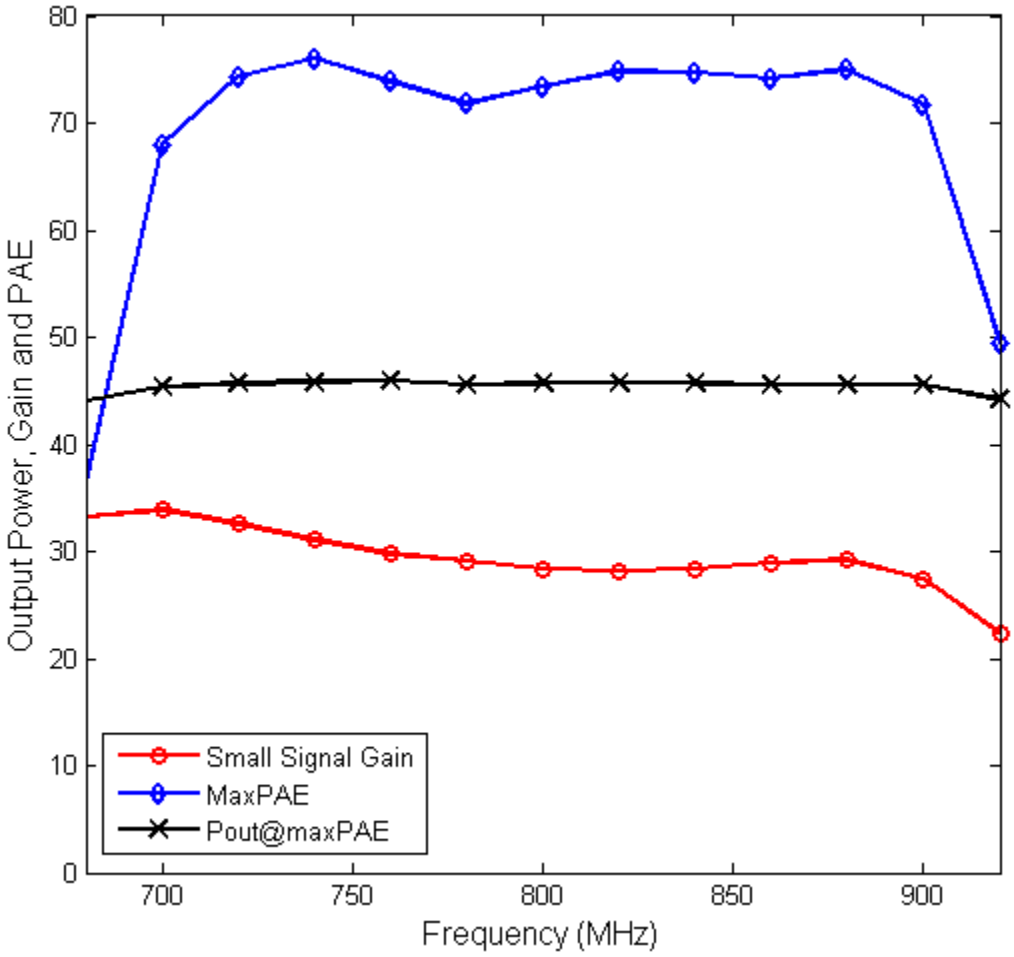


Figure 4-7: Simulated maximum efficiency, maximum output power and small signal gain vs. frequency

As seen from these plots, the two stage power amplifier has a pretty flat response over the design bandwidth. As mentioned from section 4.1.1, even though the CW bandwidth is about 200MHz, the total system bandwidth is limited to 100MHz due to the linearity performance.

4.3 Measurement Results

The following figure shows the fabricated power amplifier. The two stage power amplifier was implemented on Rogers RT/Duroid 6010 substrate with ε_r =10.9 and thickness of 0.05 inches. The transistors used in the driver and power stages were CREE 45W and 6W packaged transistors respectively.

4.3.1 Continuous Wave Measurements

The first step in determining the validity of our measurements and analyzing the power amplifier is to perform CW measurements. While doing so, it was determined that there is a bias point shift in measurements as compared to simulation. Hence, the power stage needed to be up-biased to 700mA in order to get same results as simulations. Figure 4-8 below shows the maximum power added efficiency, small signal gain and maximum output power for the nonlinear driver.

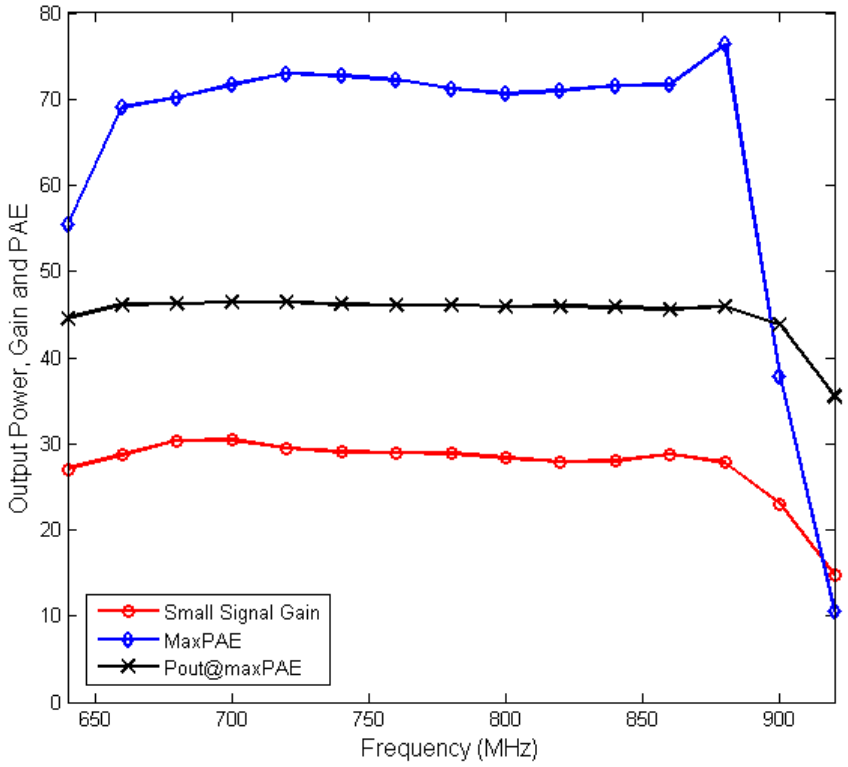


Figure 4-8: Measured maximum efficiency, maximum output power and small signal gain vs. frequency with nonlinear driver

As seen from Figure 4-8 when compared with Figure 4-7 (simulation results), there is an obvious frequency shift and the measurement bandwidth spans from 700MHz to 880MHz.

Similarly, Figure 4-9 shows the results of maximum efficiency, maximum output power and small signal gain versus frequency for the linear driver.

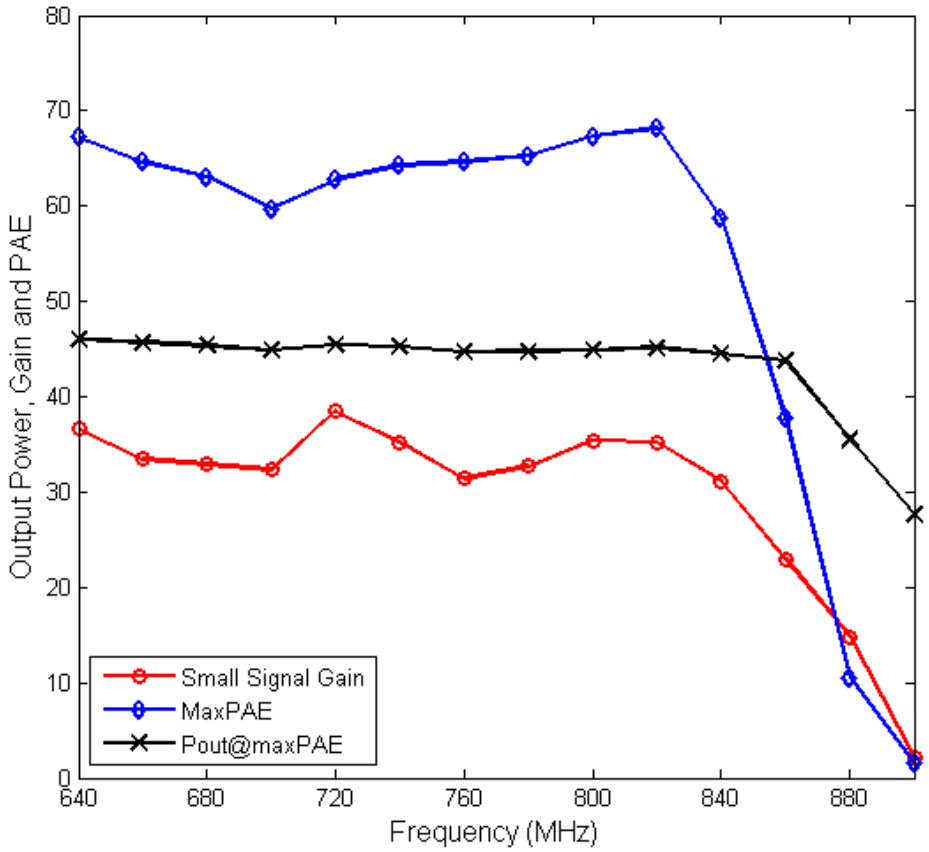


Figure 4-9: Measured maximum efficiency, maximum output power and small signal gain vs. frequency with linear driver

Comparing the PAE from Figure 4-8 and Figure 4-9, we notice that the nonlinear driver has about 5% greater maximum PAE at higher power at the same output power. However, there is an approximately 5dB drop in gain in the nonlinear driver versus the linear driver. Gain is one of the tradeoffs made in this design in order to improve linearity and efficiency.

The next set of measurements were carried out using a 5MHz LTE signal with a peak to average power ratio of 9dB and a 20MHz WCDMA 4 carrier signal with a peak to average power ratio of 7.14dB, in order to evaluate the performance of the power amplifier using both the linear and

nonlinear drivers. The power amplifier was also linearized using two types of DPD, memory DPD and memory-less DPD to allow for comparison of the linearity of two stage power amplifier with linear and nonlinear drivers.

4.3.2 5MHz LTE Measurements

A 5MHz LTE signal was used to test the bandwidth and linearity of the power amplifier. A static fit of the output signal is shown in Figure 4-10 with nonlinear driver and linear driver.

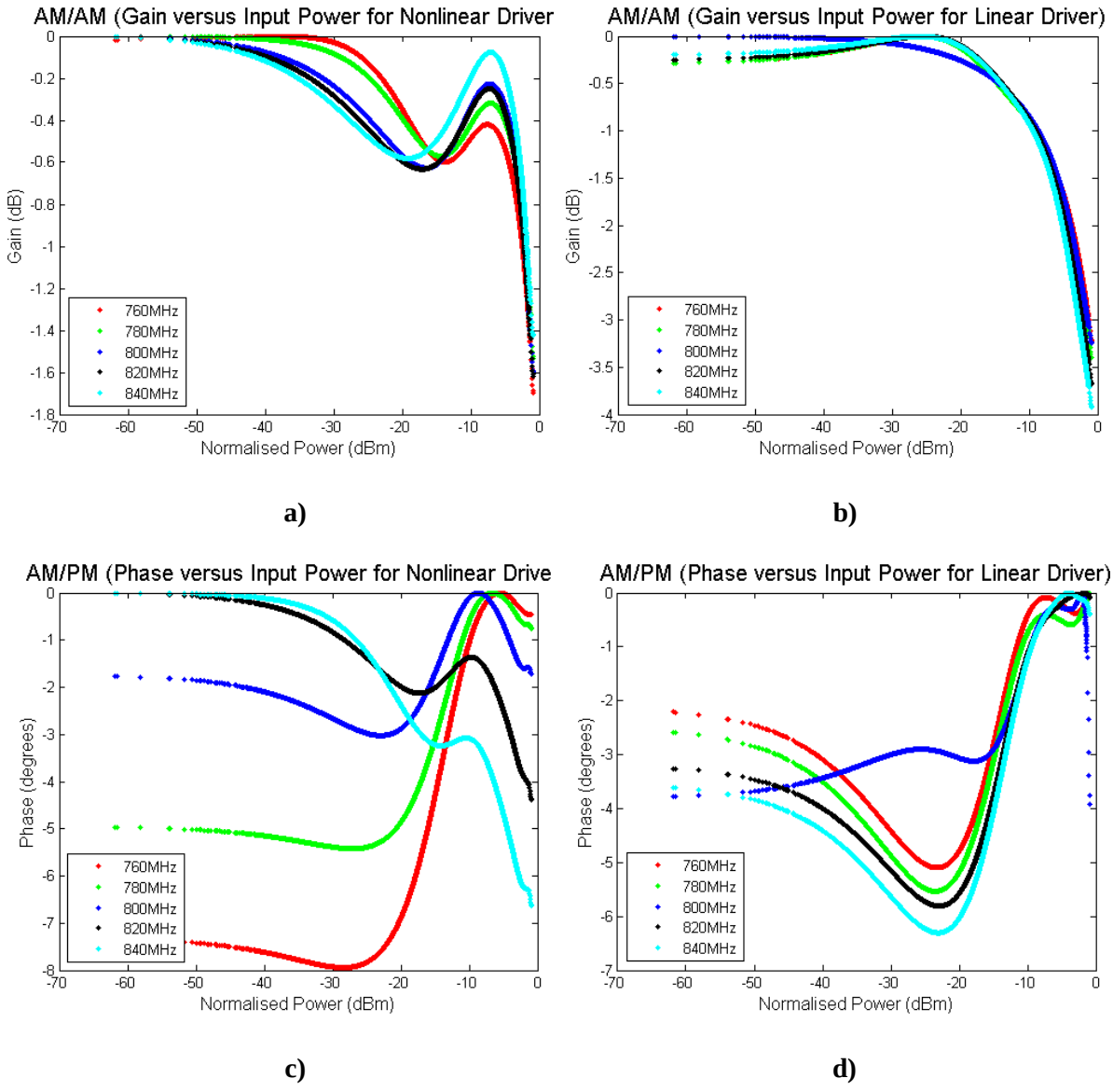


Figure 4-10: Static AM/AM for a) nonlinear driver, b) linear driver and AM/PM for c) nonlinear driver, d) linear driver

The above measurements have no DPD applied to them so that the linearity of the amplifier can compared. When comparing the AM/AM of the linear driver and nonlinear driver (Figure 4-10a. and Figure 4-10b.), it is clear that the linear driver has a significantly higher compression at peak power. The static amplitude nonlinearity generated in the linear driver is quite large as compared to the nonlinear driver. Hence, it will be observed that ACLR and EVM reflect the same, when discussed later in this chapter. This observation is consistent with the theory discussed in section 2.4.1.

The AM/PM of the linear driver has a consistent value over the most of the frequency range which could account for the lower memory effects seen in the two stage power amplifier as there is a flat phase response observed over the frequency bandwidth. The AM/PM of the nonlinear driver is sufficiently low and will result in low static phase nonlinearity. However, since AM/PM varies a lot versus frequency, it could result in significant memory effects.

Figure 4-11 below depicts the ACLR and EVM versus frequency at peak and 5dB back-off average power levels for the nonlinear and linear driver cases respectively, for a 5MHz LTE input signal.

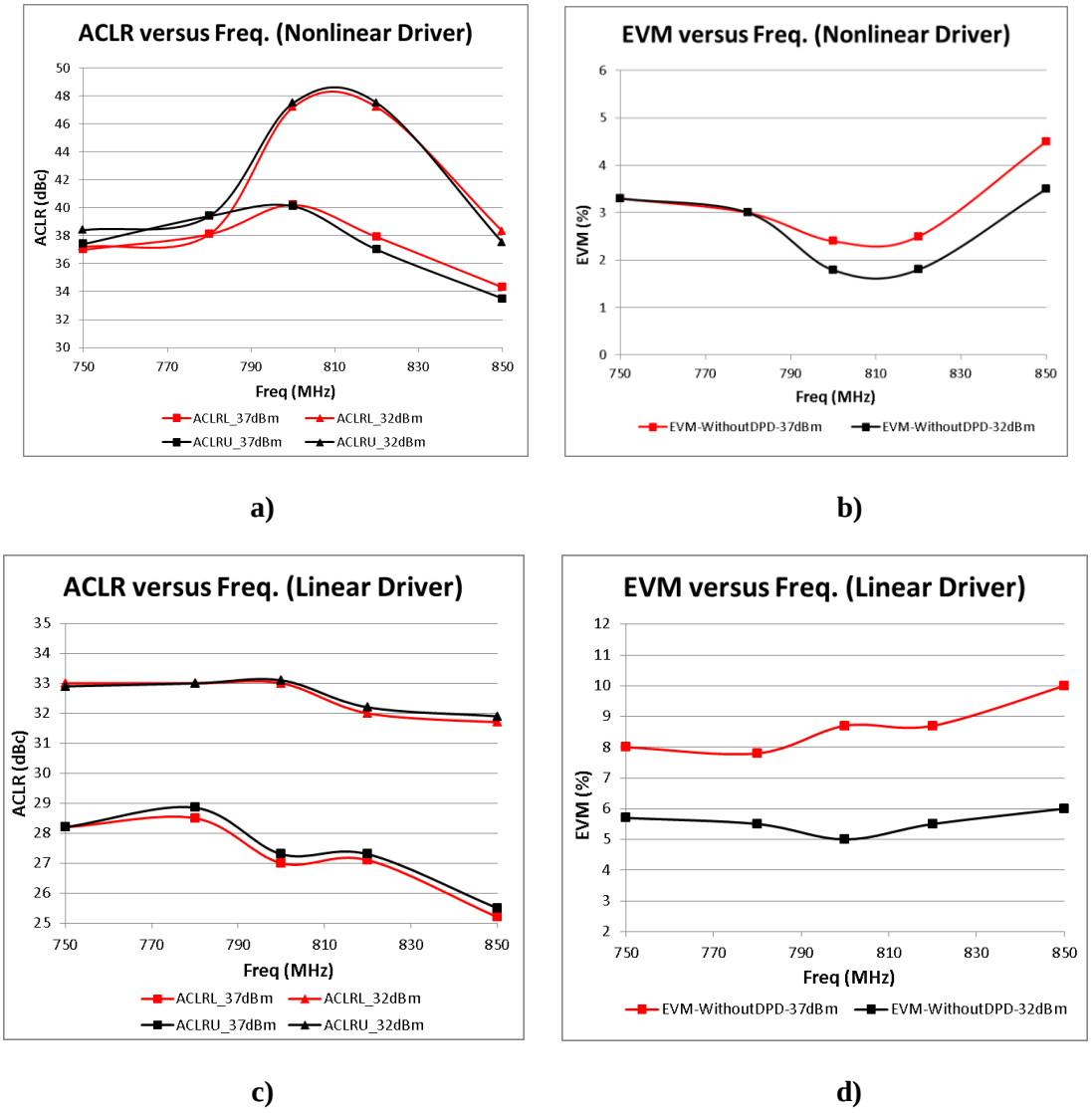


Figure 4-11: Nonlinear driver a) ACLR and b) EVM, linear driver c) ACLR and d) EVM vs. frequency

The results of the nonlinear driver (Figure 4-11 a and b) indicate that 800MHz has the best results over the bandwidth seen. As the carrier frequency moves away from 800MHz the ACLR declines and EVM increases, worsening the nonlinearity. This can be corroborated by the static nonlinearity seen in Figure 4-10 where 800MHz has the minimum AM/PM and results in the best ACLR and EVM. The AM/PM starts to increase as on either side of 800MHz, which worsens the nonlinearity.

The linear driver measurements show that ACLR is lower and EVM is higher than the nonlinear driver measurements. Even though the values of ACLR and EVM are almost constant over the

frequency range, linearity is much worse compared to the nonlinear driver. Hence, the slow compression of the two stage amplifier with a linear driver results in higher nonlinearity that compromises the ACLR and EVM. Since the total phase of AMPM is relatively similar in both cases, the nonlinearity is dominated by AM/AM. Therefore, the linearity results seen in Figure 4-11 can be explained with their corresponding static output signal fits from Figure 4-10.

In order to conduct a complete and thorough comparison between a power amplifier employing a linear versus a nonlinear driver, measurements were made using a 20MHz WCDMA 4 carrier input signal with frequency ranging from 760MHz to 840MHz. Each measurement was done versus back-off power and assessed at different frequency points across the bandwidth. The following figures show ACLR, EVM and efficiency of the two stage power amplifier employed with linear driver and nonlinear driver at different carrier frequencies. Memory-less DPD (red) and memory DPD (blue) have been employed to linearize the amplifiers and are compared for the two cases.

The first measurement was taken at 800MHz as it is the center of the bandwidth of this design. Figure 4-12 shows the ACLR, EVM and efficiency of the two stage system with either at linear driver or a nonlinear driver.

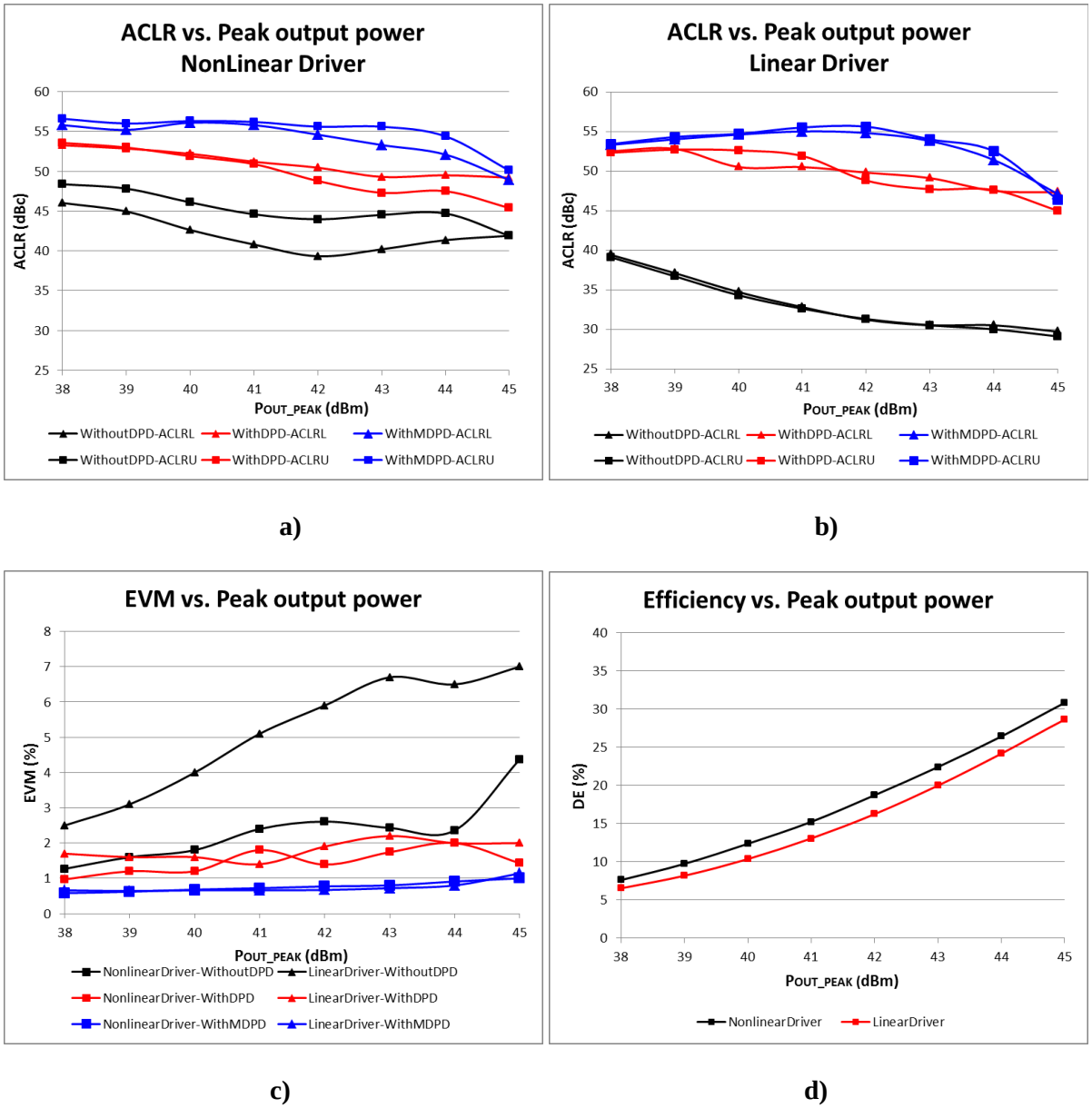


Figure 4-12: ACLR and EVM versus peak output power at 800MHz WCDMA 4 carrier signal

The above measurements indicate that the linear driver has a much worse ACLR and EVM even at 8dB back-off power levels without any DPD. The nonlinear case continues to have at least 10dB greater ACLR and almost always stays above 40dBc. If the power is backed off further, DPD is no longer required as the amplifier passes the mask. Figure 4-10 clearly justifies the improvement in static nonlinearity of the nonlinear driver as the EVM results without DPD can be maintained below 3% at almost all times. As expected from the CW measurements, the efficiency of the nonlinear case

is higher than the linear case at all times. These measurements indicate that there is a possibility of eliminating the use and need for of DPD at lower power levels, making the choice of a nonlinear driver more favorable for future applications.

Figure 4-13 and Figure 4-14 provide the same results for 820MHz and 840MHz respectively. Like the measurements made at 800MHz, these measurements have been linearized with memoryless (red) and memory (blue) DPD.

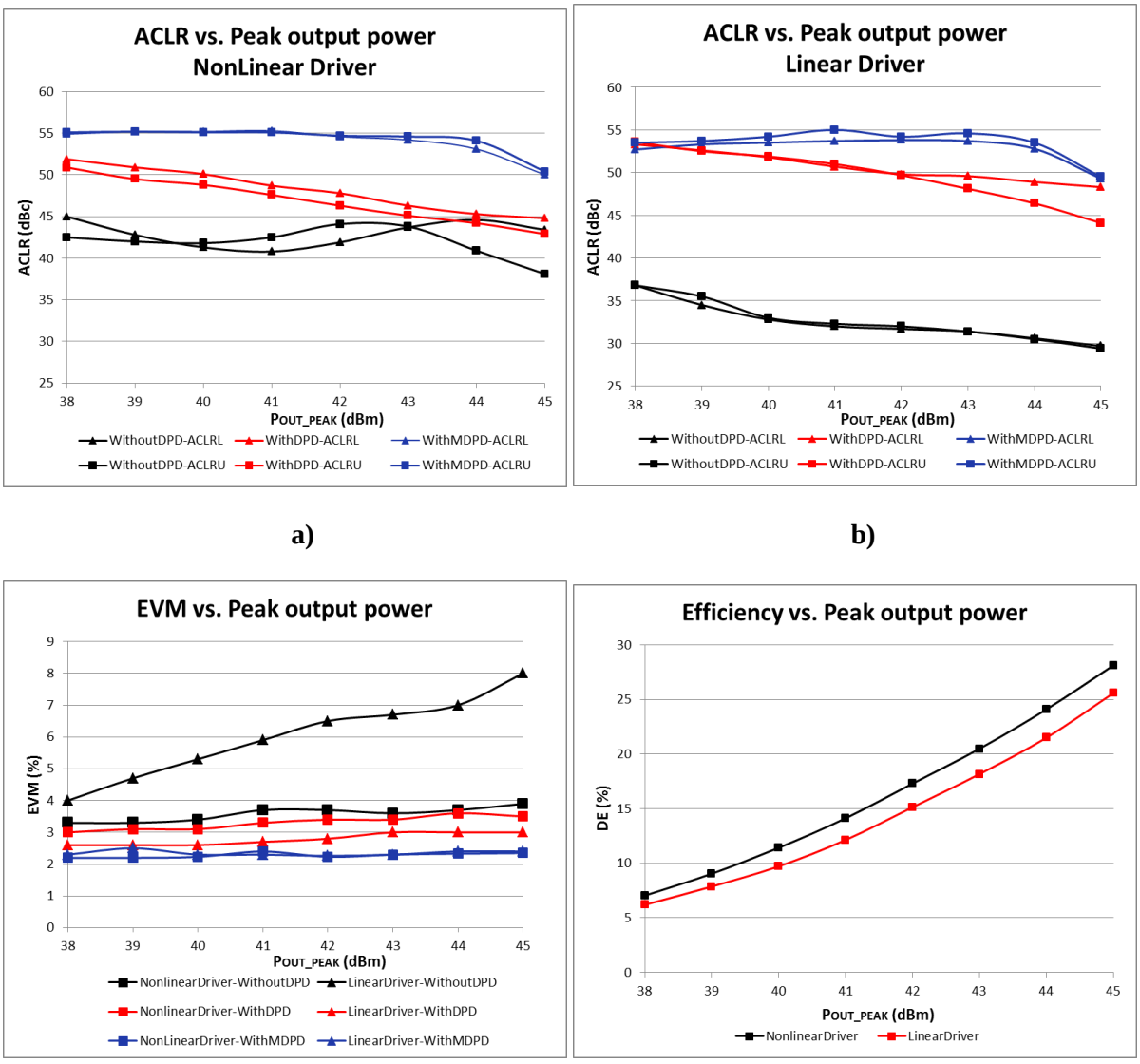


Figure 4-13: ACLR and EVM versus peak output power at 820MHz WCDMA 4 carrier signal

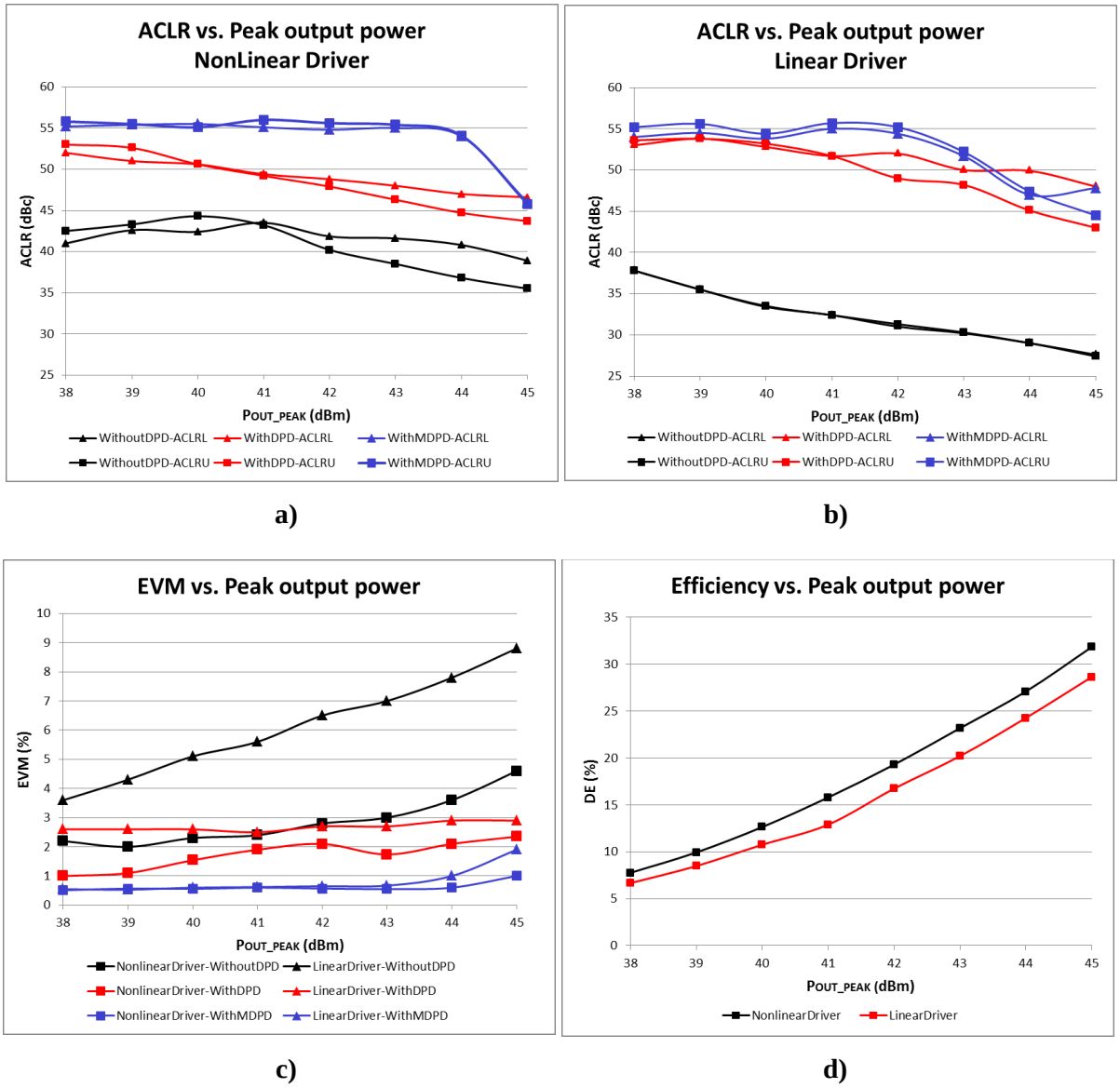


Figure 4-14: ACLR and EVM versus peak output power at 840MHz WCDMA 4 carrier signal

Figure 4-13 and Figure 4-14 both corroborate the conclusions made while examining the measurements at 800MHz. However, the linearity performance has degraded as compared to the results at 800MHz. This is to be expected as the results from section 4.3.2 explain that as the bandwidth increases the linearity without the use of DPD degrades due to the increase in the value of AM/PM. However, the ACLR has been maintained above 40dBc and EVM below 3% at most power levels.

The following figures show the summary measurements at 760MHz and 780MHz respectively.

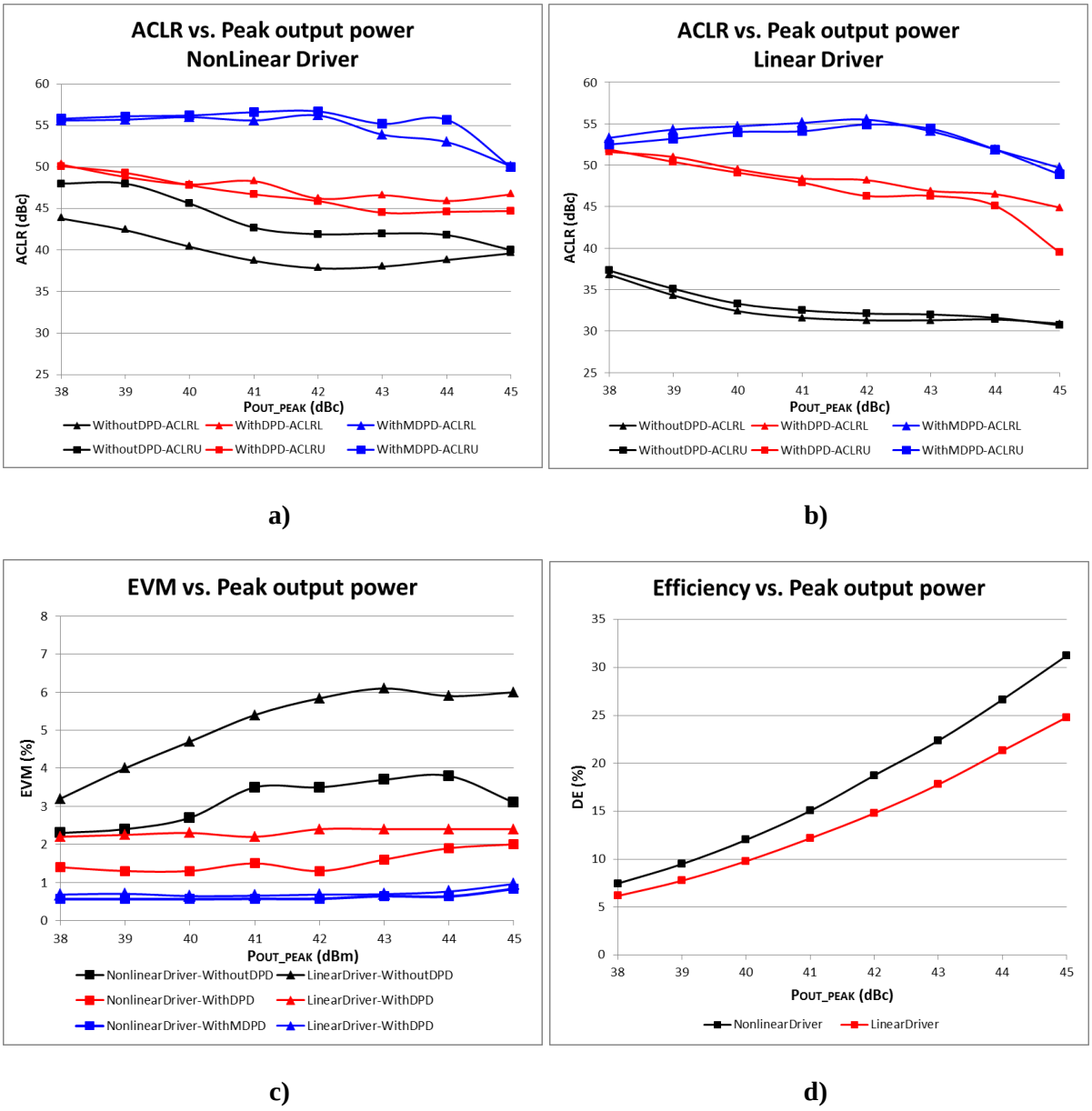


Figure 4-15: ACLR and EVM versus peak output power at 780MHz WCDMA 4 carrier signal

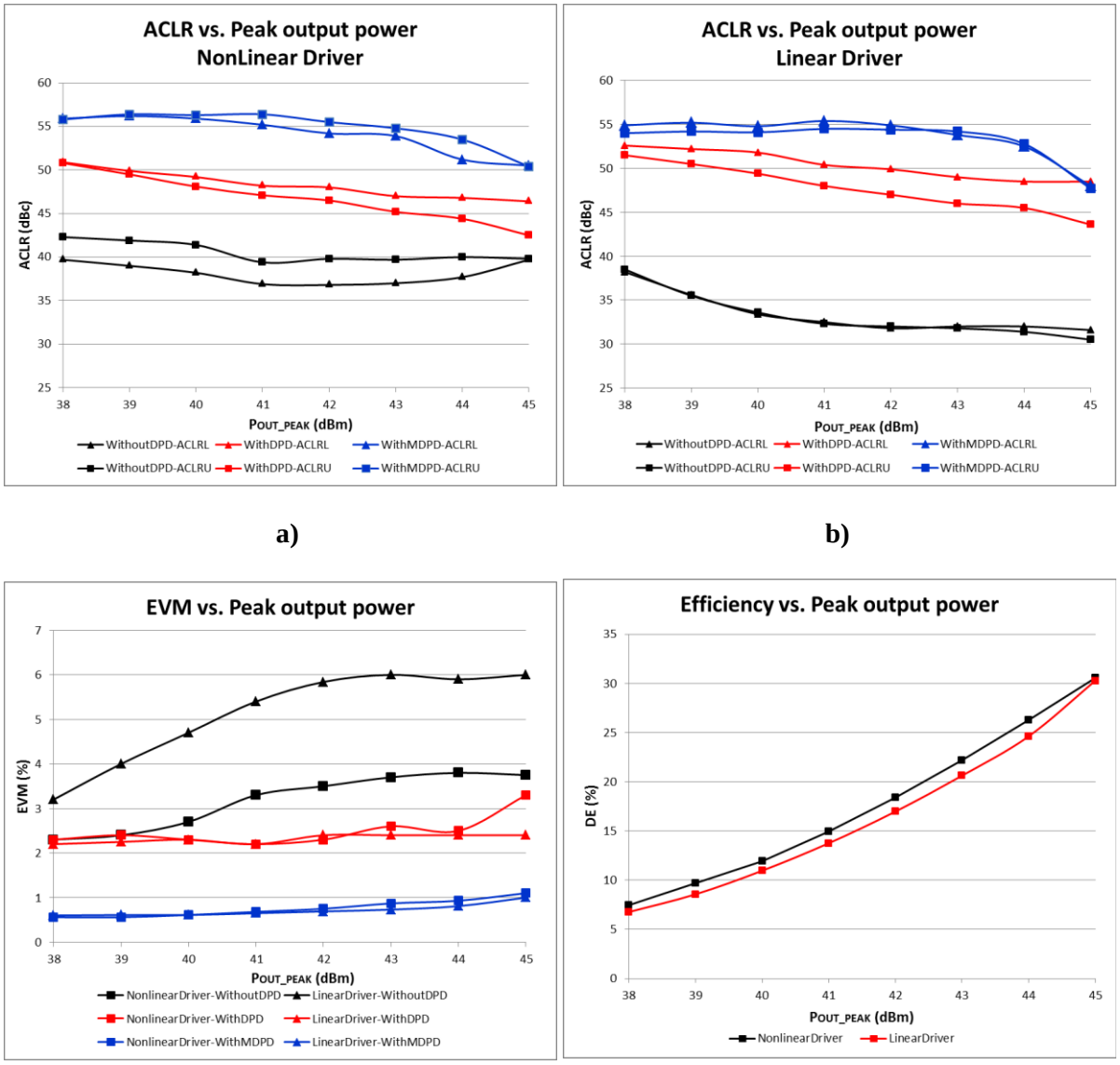


Figure 4-16: ACLR and EVM versus peak output power at 760MHz WCDMA 4 carrier signal

The results shown in Figure 4-15 and Figure 4-16, clearly indicate that two stage power amplifier with a nonlinear driver performs better in linearity compared to linear driver. The efficiency of the nonlinear driver is also always better in all cases. However, the results are not linear enough to completely eliminate the need for use of DPD. In addition, as explained in the previous section the performance starts to degrade as the carrier frequency moves away from 800MHz.

Additional measurement results (ACLR and EVM versus peak output power) using a 5MHz LTE signal can be found in Appendix A.

Chapter 5
Conclusions and Future Work

5.1 Conclusions

In recent wireless communication research, the most important criterion has become minimization of the tradeoff between linearity and efficiency in order to have the best power amplifier performance. This thesis research focused on building a power amplifier that was linear by design and did not require the use of DPD at back-off power levels (where the efficiency is as low as 5-10%). This was accomplished through a thorough study of targeted sources of nonlinearity and by reducing their effects through circuit analysis and analog pre-distortion.

The major sources of nonlinearity associated with GaN have been analyzed in this report, the input capacitance, the knee region and the transconductance. The effects of these nonlinearities on linearity metrics were investigated and their mitigation has been discussed. The derived circuit analysis used to build a design methodology of a two stage power amplifier and a progressive design solution was formulated.

The two stage power amplifier consists of both driver and power stages. The two stages work together to provide the necessary gain and linearize the nonlinearities whilst maintaining the efficiency of the two stage system. The amplifier design proposed in this thesis was also compared with the existing multistage power amplifiers that use linear drivers to boost gain.

As seen from the measurement results, the amplifier solution has been successful in reducing the effects of key sources of nonlinearity. It was found that the linear driver lost a lot of its potency due the nature of the Gm curves of GaN HEMT transistors and hence, caused the system to be more nonlinear than that of the nonlinear driver. In addition, 10% efficiency was gained at peak power using the nonlinear driver. Both power amplifier designs were shown to be linearizable with memoryless and memory DPD.

The fabricated amplifier of the proposed design dabout 70% peak efficiency in CW measurements and maintained linearity of above 40dBc ACLR and below 3% EVM over the 80MHz bandwidth

using modulated signals. The need for DPD was eliminated at back-off power levels, at 800MHz, as the nonlinearity was reduced significantly and the signal passed the spectrum mask. The results show that the ACLR and EVM of the proposed design do not pass the mask for other frequencies; however, the results were much better than those of the linear driver design. Since the design methodology aimed at reducing the variation of AM/AM and AM/PM, rather than improving ACLR and EVM, the design could not be fully optimized for linearity. Due to the direct link missing between the different linearity metrics, ACLR and EVM were not able to meet mask specifications.

5.2 Future Work

Based on the promising results of this thesis work, further research could be done in order to design multistage amplifiers that provide better linearity results at higher power levels. Firstly, in order to improve linearity performance under modulated signal, the ACLR and EVM need to be considered during the course of design. The direct relationship of ACLR and EVM with AM/AM and AM/PM needs to be evaluated and the design criteria of the two stage linear amplifier should be based on this investigation.

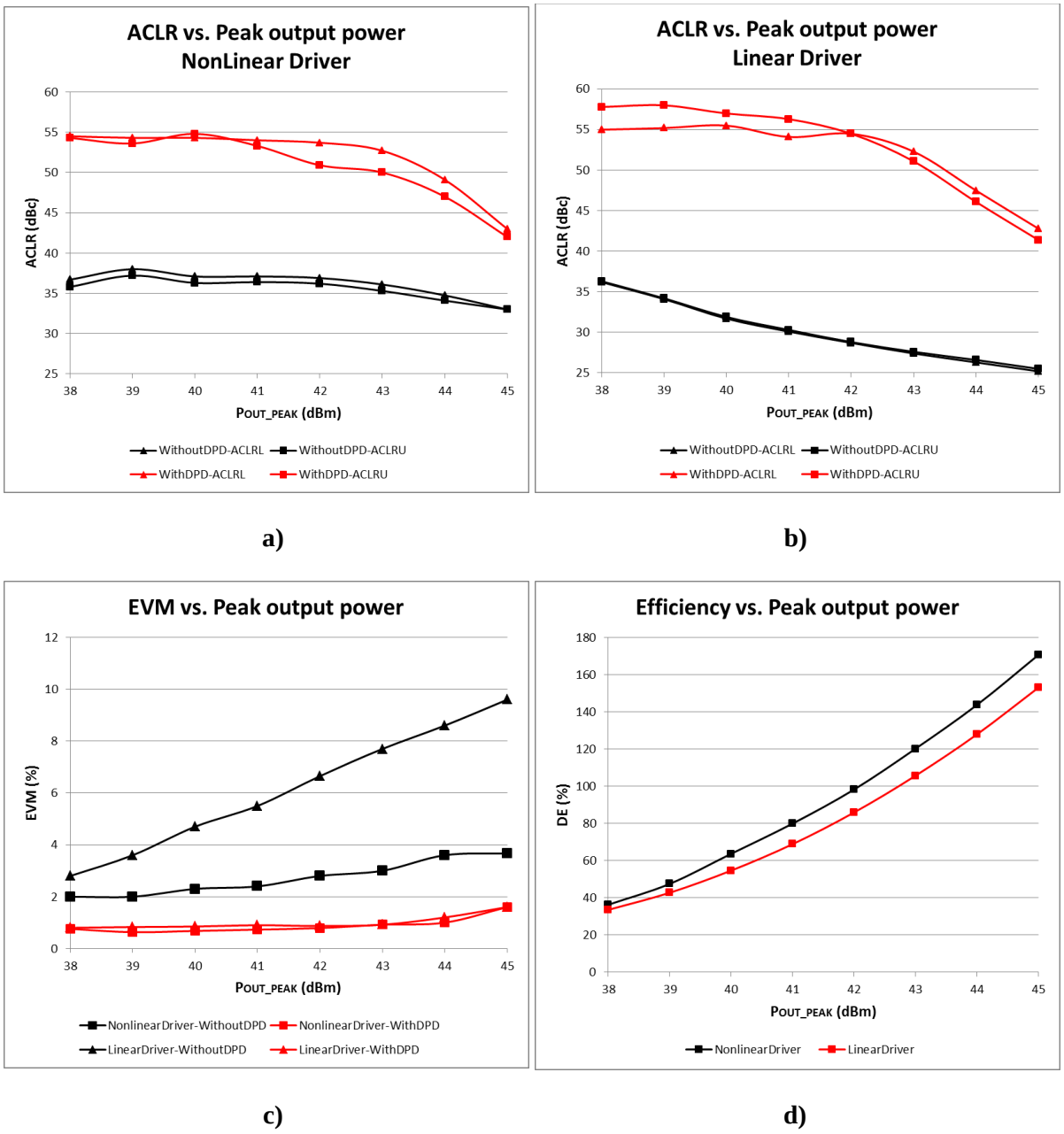
Another approach to improve the two stage design as presented in this thesis is the distributed pre-distortion amplifier methodology as proposed in [22]. The two stage amplifier can be built with multiple parallel branches in order to have more freedom to control the different nonlinearities associated with GaN HEMT. In order ease the constraints on the inter-stage matching network of the two stage amplifier, the nonlinear input capacitor can be linearized by redesigning the driver stage using LDMOS technology and utilizing its nonlinear output capacitance. This potential solution could help with improvement in AM/PM across a wider bandwidth and also improve ACLR and EVM at higher power levels.

Revised design methods should allow the designer to predict the feasibility of implementing circuit pre-distortion to build linear and highly efficient power amplifiers for future products.

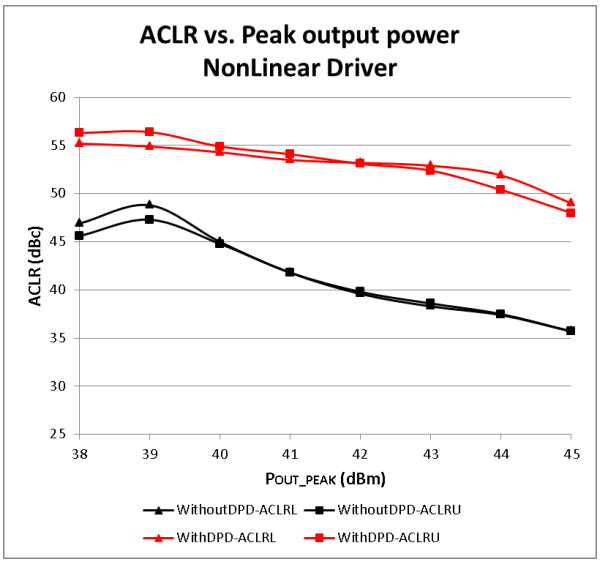
Appendix A

Sample Appendix

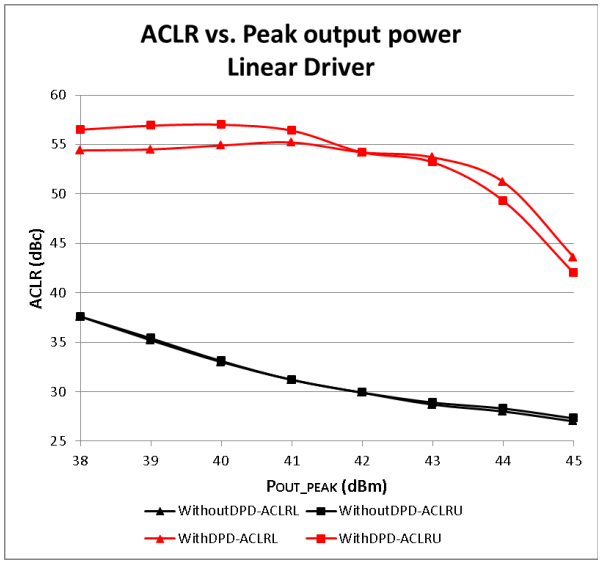
The measurements below show the ACLR and EVM results versus power for LTE 5MHz input signal at 760MHz, 800MHz and 840Mhz.



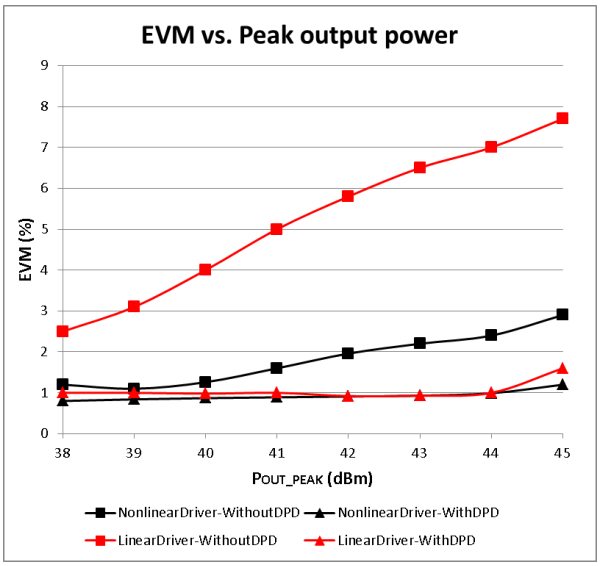
Figure_Apx 1: ACLR and EVM versus peak output power at 840MHz for LTE 5MHz signal



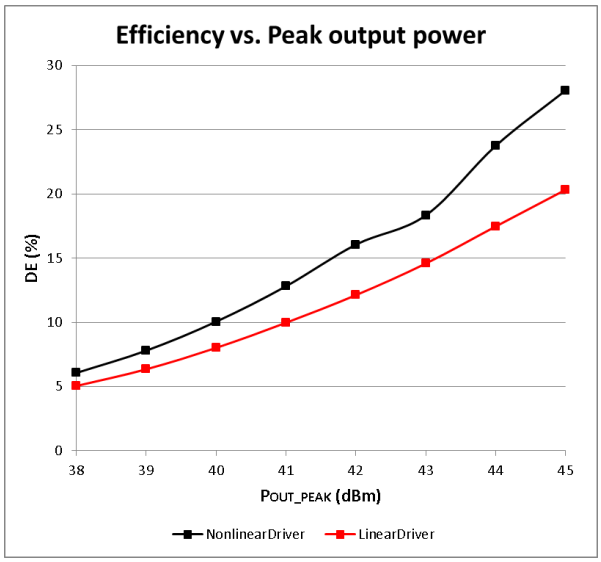
a)



b)

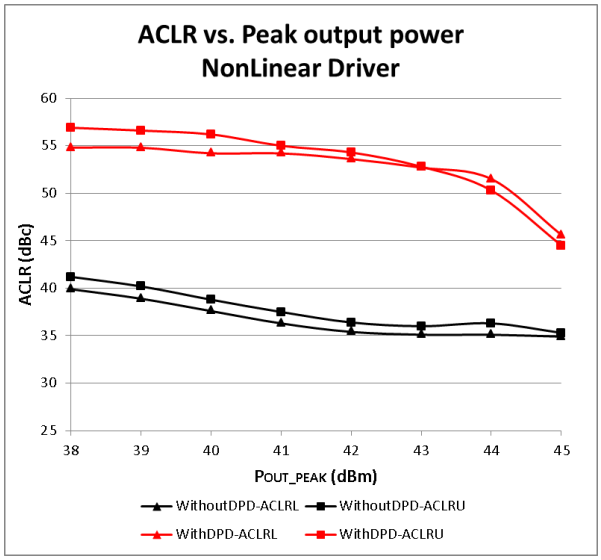


c)

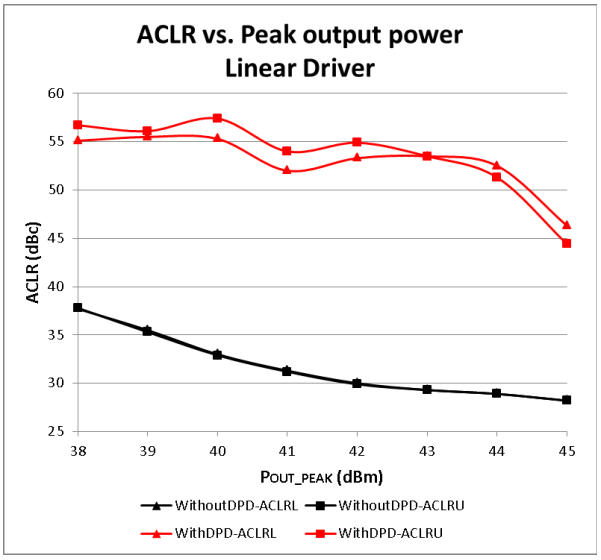


d)

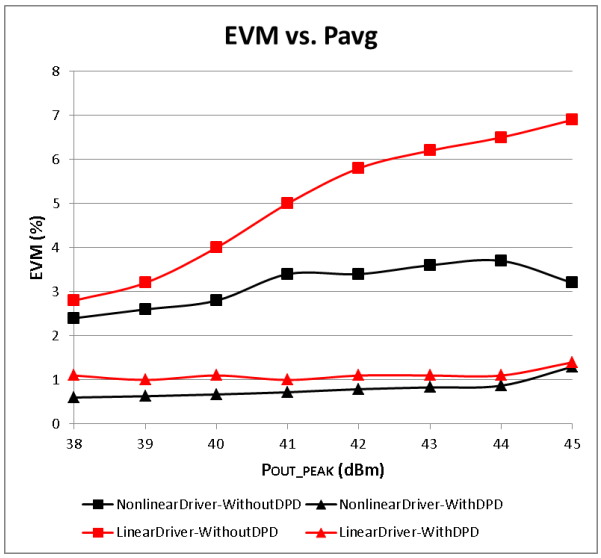
Figure_Apx 2: ACLR and EVM versus peak output power at 800MHz for LTE 5MHz signal



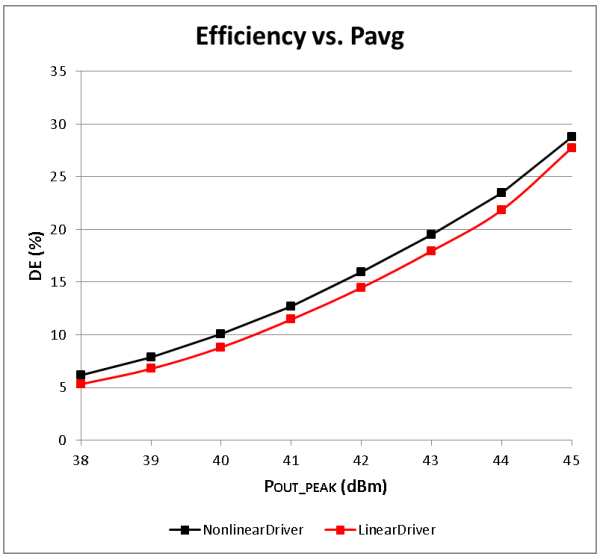
a)



b)



c)



d)

Figure_Apx 3: ACLR and EVM versus peak output power at 760MHz for LTE 5MHz signal

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