CDMA Channel Selection
Using Switched Capacitor Technique

by

Amir Hossein Nejadmalayeri

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

CDMA channel selection requires sharp as well as wide-band filtering. SAW filters which have been used for this purpose are only available in IF range. In direct conversion receivers this has to be done at low frequencies.

Switched Capacitor technique has been employed to design a low power, highly selective low-pass channel select filter for CDMA wireless receivers.

The topology which has been chosen ensures the low sensitivity of the filter response.

The circuit has been designed in a mixed-mode 0.18μ CMOS technology working with a single supply of 1.8 V while its current consumption is less than 10 mA.

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To

my dearest mother

and

my dearest father

who are far beyond any appreciation.

Those who have been, and will be the best,

ALWAYS *the best!*

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Chapter 1

Introduction

This thesis deals with the design of a baseband CDMA channel select filter. In this chapter the motivations for this research, the contributions and the thesis scope are discussed.

1.1 Motivations

CDMA wireless receivers require wide-band as well as sharp channel select filtering [11]. Up to now, channel selection has been done using bulky as well as expensive off-chip SAW filters in *intermediate frequency (IF)* range. But with recent improvements in *direct conversion* methods the demand for DC channel selection has been substantially increased.

Two methods, i.e., *switched capacitor (SC)* and *continuous time (CT)* can be utilized to perform channel selection at DC. Albeit both can be well integrated into the whole mobile transceiver, due to the inherent nature of integrated continuous time method in which poles and zeros of the filter's transfer function are determined by ratios of transconductances and capacitors, they are not accurate. The process related variations of capacitor and transconductor values are uncorrelated, so that even a 40% degradation from the desired frequency response has been reported [19]. In order to combat this crucial obstacle, utilizing tuning methods in integrated continuous time filters is inevitable [38] [22]. This problem increases the complexity of the whole filtering circuitry. On the other hand, SC filters deliver very accurate frequency response without any need for an extra tuning block [5], provided that some fundamental aspects such as high gain, large bandwidth, large phase margin, high slew rate and highly matched integrated capacitors have been carefully considered in the design process.

Moreover, the fact that the final circuit is to be used in a wireless receiver demands for

both low voltage and low power design.

Based on the foregoing discussions, a highly selective CDMA channel filter has been designed in a 0.18μ mixed-mode CMOS process, operating with a single supply of 1.8 V.

1.2 Original Contributions

The contributions of this thesis can be divided to two different categories, i.e., analysis and design.

Chapter 4 contains the analysis of the effects of nonidealities of fully differential op-amps on the characteristics of bilinear switched capacitor differential integrators which includes step-by-step derivation of all mathematical relationships. The major contributions in that context are two-fold as follows:

- Utilization of a more realistic model for the operational amplifier by the inclusion of the effect of finite-gain and finite band-width simultaneously
- Inclusion of the op-amp input capacitance in the analysis which gives rise to the concept of *effective* unity-gain frequency

The contributions in the design context include applying the well established SC technique to stringent requirements of CDMA wireless receivers using an advanced sub-micron CMOS process.

Moreover, certain design guidelines and techniques presented in Sec. 5.5 try to develop an innovative approach to the circuit design in sub-micron technologies.

1.3 Thesis Scope

Integrated filters design in general and SC ones in particular are multi-disciplinary areas. They cover wide range of subjects from basic circuit theory, filter theory, integrated circuit design as well as advanced topics like sensitivity, noise and distortion analysis.

Based on the foregoing discussions, to keep the thesis as concise as possible, the majority of the basics are assumed to be known.

The thesis starts with a quick overview of discrete time (DT) systems and their characteristics. Then, in order to derive the appropriate DT circuits from the well-know CT ones, Bruton's theory is presented, and following that the SC blocks which comply with the previously discussed requirements are presented.

The next chapter quickly reviews one of the most important theorems of the circuit theory and its applications to the analysis of the filters are presented.

Based on the theories developed in the previous chapters, the design of the desired channel select filter are fully discussed. It includes, derivation of the block diagram parameters from the system level requirements followed by the transistor level design of the integrated circuits.

Mathematics and physical interpretations are fully incorporated in all parts of this thesis. It has been tried hard to justify all the arguments, either by presenting mathematical proof or giving deep insights into the physics of the problems.

Chapter 2

Discrete-Time Systems and Switched Capacitor Technique

2.1 DT Signals

A signal which does not change continuously by time is called *discrete time(DT)*. Depending on the time domain characteristics or the values that the signal can accept, DT signals can be classified into different categories.

A DT signal can consist of either short period or wide pulses. The former is called *sampled* signal and the latter *sampled-and-held* (Fig. 2.1).

The time difference between the moments that the values of consecutive samples change, can be equal or different (Fig. 2.2).

Signals which consist of equally spaced samples could be represented by *Z-transform*, as follows

$$X(z) = \sum_{n=-\infty}^{n=+\infty} x(nT) \cdot z^{-n} \tag{2.1}$$

A DT signal can accept either any values or in opposite, it might consist of only quantized values, called *digital* signals. The former is called *analog-sampled*.

The subject of SC technique is to deal with *equally spaced analog sampled* signals which in most cases are sampled-and-held, but not necessarily. As a result, from this point, all the signals which will be called DT in this thesis are assumed to have these properties, unless otherwise explicitly mentioned.

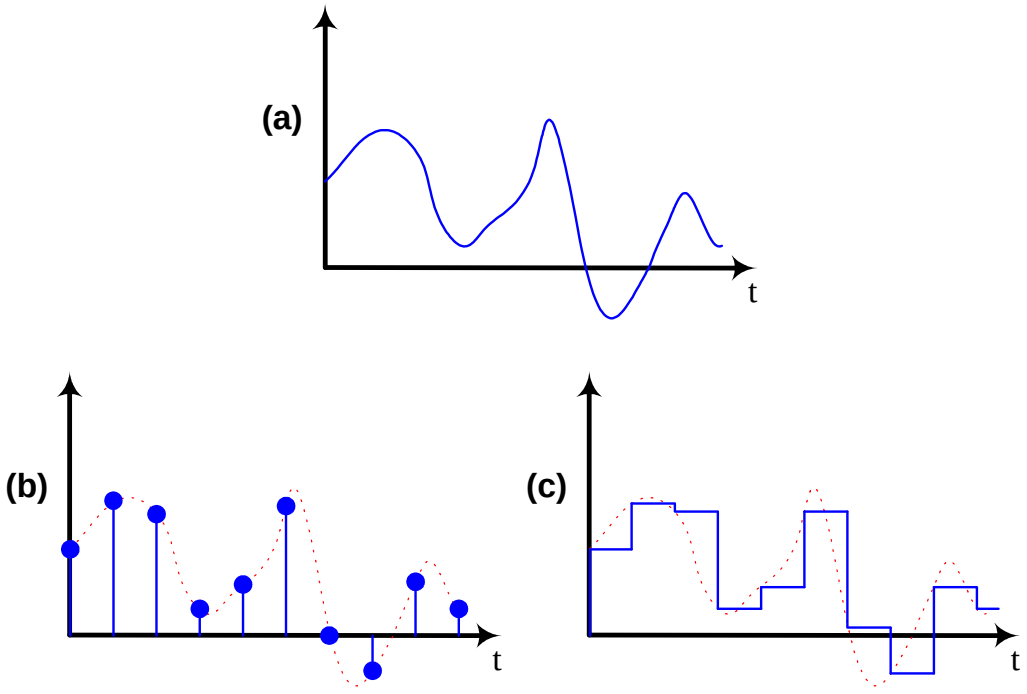

Figure 2.1: CT signals and two different DT representation. (a)Original CT signal (b)Sampled DT (c)Sampled-and-held

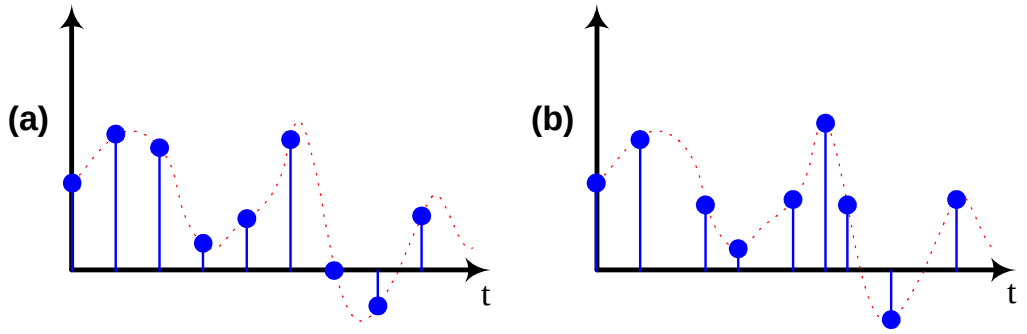

Figure 2.2: Two different scheme of sampling. (a) is the popular one in which the samples are equally spaced, whereas in (b) samples have been taken at different moments

The complex variable z is an exponential function of $j\omega$, in which ω is the real frequency. Consequently, the spectrum of a DT signal which is obtained by substituting $z = \exp(j\omega)$ will be periodic.

This is a very basic, yet a crucial property of DT signals, and it will be seen that it has severe effects on the characteristics as well as design requirements of SC circuits.

2.2 Nyquist Criterion

For every DT signal which consists of equally spaced samples, there exist infinite number of CT signals which have exactly the same values at the moments that the samples have been taken. As a result, a DT signal by itself cannot uniquely express a corresponding CT signal. However, putting some restrictions on the CT signal can establish a *one-to-one* relationship between DT domain and CT domain.

Nyquist criterion deals with this restriction and proposes the condition through which there exists one and only one CT signal for a specific DT signal.

Sampling a CT signal $x(t)$ results in a DT signal $x(nT)$ in which $T = 1/f_s$ is sampling period and f_s sampling frequency.

If the original signal $x(t)$ has a finite bandwidth BW, for some values of f_s there will be DT signals from which $x(t)$ can be uniquely reconstructed. Depending on whether this signal is low-pass (LP) or band-pass (BP), as it is shown in Fig. 2.3, the sampling could be classified into two different categories. Nyquist criterion is presented for both cases as the following.

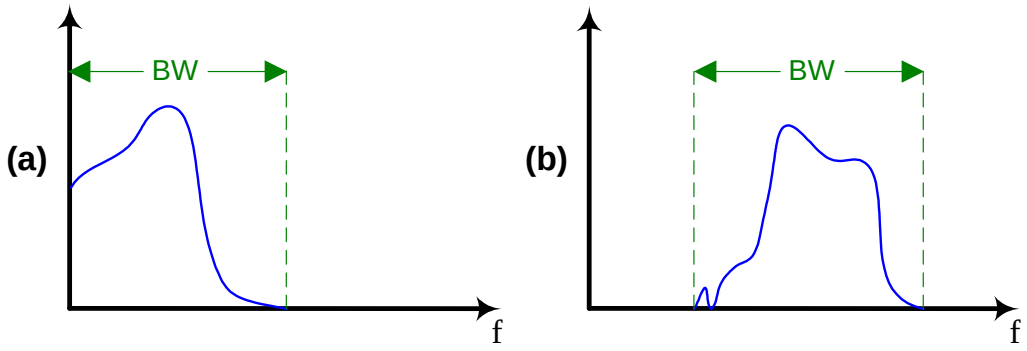

Figure 2.3: Frequency spectrum of (a)LP (b)BP signals

2.2.1 Over-sampling: LP Signals

For an LP signal, i.e., a signal which has DC value, the sampling frequency f_s has to be higher than twice the signal bandwidth BW (Fig. 2.4).

$$-BW \leq f \leq BW \longrightarrow f_s > 2 \cdot BW \tag{2.2}$$

This condition ensures that *aliasing* won't happen and as a result the original CT signal can be exactly reconstructed from the DT one.

Since in this case, f_s is higher than the signal bandwidth, it is known as *over-sampling*, and the ratio

$$OSR = \frac{f_s}{BW} \tag{2.3}$$

is called *over-sampling ratio*.

It should be noted that since the magnitude components of negative frequencies are exact replicas of the positive ones—which is a basic property of double-sided Fourier transform—therefore for LP signals, BW is defined from the DC up to the highest frequency component.

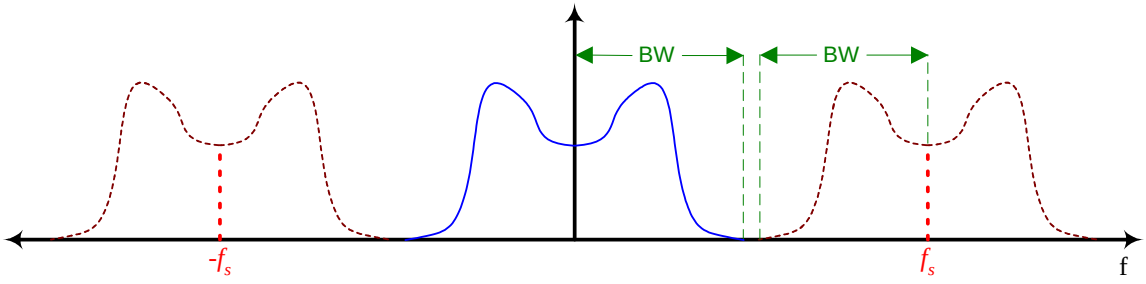

Figure 2.4: Frequency spectrum of an over-sampled LP signal.

2.2.2 Under-sampling: BP Signals

For BP signal, i.e., those which do not contain DC value, or in other words their frequency spectrum consists of components in range f_0 up to $f_0 + BW$ where BW is the signal bandwidth and f_0 is greater than zero, still the Nyquist criterion for LP signal is applicable,

which in this case, it gives rise to the values of f_s that will be greater than $2(f_0 + BW)$. But this results in severe practical difficulties. In most cases f_0 is orders of magnitude larger than BW, so that the very high value of required sampling frequency makes the processing of signal in DT domain absolutely difficult, if not impossible. For instance in mobile communication f_0—carrier frequency—is in the range of GHz but BW, at the worst case, is in the range of tens of MHz.

Fortunately, placing one more restriction on the original CT signal can result in a new version of Nyquist criterion for BP signals which itself consequently gives rise to very relaxed requirements for f_s. This extra condition requires that

$$f_0 > BW \tag{2.4}$$

which as stated earlier, it is easily satisfied in most practical cases.

Therefore Nyquist criterion changes to the following, i.e., for BP signals, sampling with a frequency in the range

$$BW < f_s < f_0 \tag{2.5}$$

gives rise to a DT signal from which the original CT signal can be exactly reconstructed, provided that Eq. 2.4 is held.

Since in this case, the sampling frequency is less than signal bandwidth, it is known as *under-sampling*, and the ratio

$$USR \;=\; \frac{BW}{f_s} \tag{2.6}$$

is called *under-sampling ratio*.

Under-sampling of a BP signal can result in a typical frequency spectrum as shown in Fig. 2.5.

2.3 Bruton's Theory

When Bruton published his excellent paper [4] in 1975, SC filters had not been known at that time. Nevertheless, in about five years they were emerged as the optimum choice for

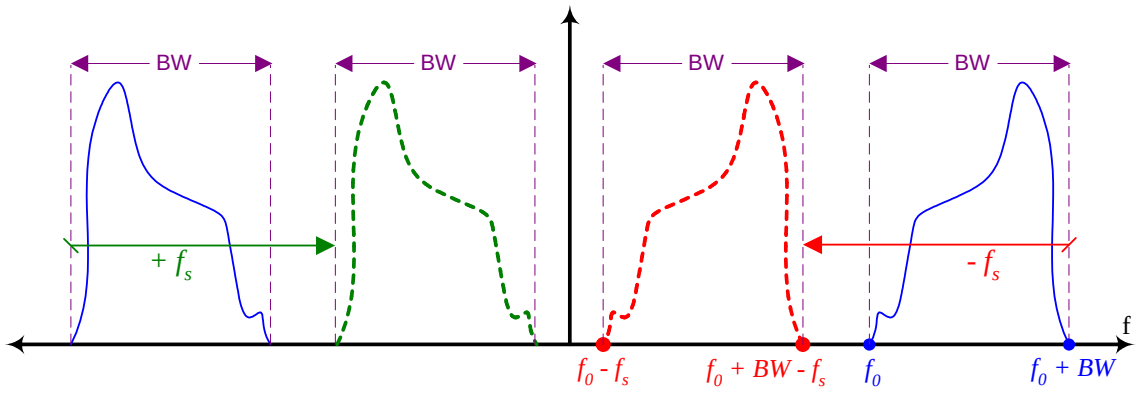

Figure 2.5: Frequency spectrum of an under-sampled BP signal

analog sampled filtering, henceforth Bruton's paper written on DT filters—mainly digital ones—had a profound effect on SC technique.

As it will be thoroughly reviewed in Chap. 3, sensitivity is a major concern in filter design, and as Orchard's theorem [30] states, the sensitivity of attenuation function is very low in pass-band for passive LC filters, and any network which can simulate the governing equations of these circuits will inherit their insensitivity characteristics and will be immune to first order perturbations in reactive element values.

This simulation of governing Kirchhoff's equations can be performed in two different ways, i.e., impedance simulation and signal flow graph (SFG) method, that both of them will be treated in detail in Sec. 2.6. For our current discussion, it should be just noted that in either case the realization of the desired TF reduces to a network consisting of integrators with different gains.

As a result, integrators are the most fundamental blocks in transfer function realization and any attempt to generate a desired frequency response reduces to providing suitable integrators with specific characteristics which are basically the subject of investigation in Bruton's theory.

The ultimate goal in this theory is to design low-sensitivity DT filters, and based on the foregoing discussions a premier choice for the realization of these networks will be substitution of CT integrators with their DT counterparts in an original low-sensitivity CT circuit. Nevertheless, with regard to this methodology, several fundamental questions have yet to be answered which are classified as follows

- *Is there a direct relationship between reactive element values of an LC filter and the*

constituting parameters of the DT filter?

A positive answer to this question leads to the fact that since the original filter is insensitive to the perturbations of reactive element values, therefore the resulting DT network will also be immune to first order variations of the parameters of its constituting components.

- *What type of discrete integrators has to be employed to retain the insensitivity significance of original LC network?*

  This is in fact the highlight of Bruton's theory and a major concern in DT filter design.

In order to answer these questions, the concept of lossy and loss-less integration will be introduced and based on that, these concerns will be addressed.

The frequency response of an ideal integrators is written as the following

$$I(j\omega) = \frac{1}{j\omega} \tag{2.7}$$

whereas real integrators have some gain error as well as phase error with respect to the ideal case, as follows

$$I(j\omega) = \frac{1}{j\omega}(1+\epsilon)\cdot e^{j\theta} \tag{2.8}$$

in which ϵ and θ are gain and phase errors respectively.

On the other hand, the frequency relationship of a non-ideal integrator can be expressed in another form using the concept of quality factor which will be

$$I(j\omega) = \frac{1}{j\omega}(1+\frac{j}{Q}) \tag{2.9}$$

in which Q is the *quality factor*. It is evident that for the ideal case where the quality factor Q is infinite, Eq. 2.9 reduces to Eq. 2.7.

Applying Taylor's series expansion to Eq. 2.8 and keeping the most significant terms with the assumption that $\epsilon \ll 1$ results in

$$I(j\omega) \simeq \frac{1}{j\omega}(1+j\theta) \tag{2.10}$$

Comparing Eq. 2.9 and Eq. 2.10 suggests that with a good approximation

$$Q \simeq \frac{1}{\theta} \tag{2.11}$$

This relationship implies that Q degradation—which stands for *ohmic losses* in reactive elements or in other words the existence of parasitic resistances—is solely dependent on the *phase deviations* from the ideal case. This statement is of invaluable significance, since as stated earlier for LC networks the sensitivity of attenuation function is zero with respect to the variations of reactive element values, whereas having finite Q for such an element corresponds to the existence of parasitic resistance, so that as a result Orchard's theorem would not be applicable.

In order to obtain a DT network which has inherited the low-sensitivity properties of the LC prototype, the DT integrators that are substituted for their CT counterparts must have zero phase degradation to ensure the infinite quality factor of the integrator or in other words the lack of loss in the element. Amplitude degradation is not of significant importance, since it can be appropriately compensated in the prototype network.

Two infamous types of integrators which have this property are to be closely examined.

2.3.1 Bilinear Transformation and Bilinear Integrator

This type of integrator is based on infamous bilinear transformation in complex number theory which is described as follows

$$s_{ct} \;=\; \frac{2}{T}\,\tanh s\frac{T}{2} \;=\; \frac{2}{T}\,\frac{1-e^{-sT}}{1+e^{-sT}} \;=\; \frac{2}{T}\,\frac{z-1}{z+1} \tag{2.12}$$

where T is the sampling period as before and $z = \exp(sT)$.

This transformation has the property of mapping the entire left half plane (LHP) of s_{ct} domain onto the unit circle in Z domain. The $j\omega_{ct}$ axis is correspondingly mapped into the perimeter of the unit circle. This implicitly states that a discrete transfer function obtained by applying bilinear transformation to an original continuous one is stable iff the original one is stable.

When Eq. 2.12 is written in terms of real frequencies, we get

$$\omega_{ct} = \frac{2}{T}\tan\left(\omega T/2\right) \tag{2.13}$$

Therefore the frequency response of a bilinear DT integrator—which is obtained by applying Eq. 2.13 to the original CT one (Eq. 2.7)—will be

$$I(j\omega) \;=\; \frac{1}{j}\cdot\frac{T/2}{\tan\left(\omega T/2\right)} \;=\; \frac{1}{j\omega}\cdot\frac{\omega T/2}{\tan\left(\omega T/2\right)} \tag{2.14}$$

As it is easily seen the deviation of this TF from the ideal case is only in the form of a real multiplier. The great outcome of this fact is that a bilinear integrator has no phase error comparing to an ideal one, so that based on the foregoing discussions, it is in fact a loss-less integrator. Conclusively, Orchard's sensitivity theorem is applicable to any DT network obtained by applying a bilinear transformation to an original passive LC circuit or in other words all the excellent insensitivity properties are retained in DT domain.

The trigonometric relationship 2.13 shows that in the process of moving from CT domain to DT, a frequency scaling happens which is widely known as *warping*.

In the case of bilinear transform, the warping effect shows itself in terms of *frequency compression*, or in other words, the DT filter will have more selectivity—sharper frequency response—comparing to the original CT one [25]. This is due to the infamous trigonometric inequality

$$\omega T/2 \leq \tan\left(\omega T/2\right) \tag{2.15}$$

where $|f| \leq f_c/2$ or in other words $|\omega T/2| \leq \pi/2$.

2.3.2 Loss-less Discrete Integrator(LDI)

This type of integrator is based on the following transformation

$$s_{ct} = \frac{1}{T}(e^{sT/2} - e^{-sT/2}) = \frac{1}{T}(z^{1/2} - z^{-1/2}) \tag{2.16}$$

or in terms of real frequencies

$$\omega_{ct} = j\frac{2}{T}\sin\omega\frac{T}{2} \tag{2.17}$$

Therefore the frequency response of a DT integrator obtained through this transformation will be

$$I(j\omega) = \frac{1}{j\omega} \cdot \frac{\omega T/2}{\sin(\omega T/2)} \tag{2.18}$$

As it is evident, there is no phase degradation, so that sensitivity properties are preserved under this transform.

It should only be mentioned that under this transformation, the warping effect appears in terms of sin function, whereas for bilinear transform this was tan (Eq. 2.13). Therefore in this case a frequency expansion occurs which results in less selectivity. Hence this is considered as one of the shortcomings of LDI transformation.

The other problem which is in fact a crucial one, is the fact that under this transformation the whole LHP in s_{ct} domain is mapped onto the whole plane in Z domain. This can be easily verified, since by applying $z \longrightarrow 1/z$, the relationship 2.16 does not change. More precisely, for every pole in original CT-TF there exist two poles in DT-TF which are inverse of each other. One of these is inside the unit circle and the other outside. The latter stands for inherent instability of TFs obtained through this transform, although there are certain ways to address this issue [25].

2.4 SC Resistor

Decades of attempt to realize inductor-less filters led to the invention of SC filters in late 1970's. In fact, the idea proposed by Fried [9], ignited heavy research on the potentials of employing switched capacitors to implement discrete filters, so that finally after half a decade the earliest versions of SC filters emerged.

In this section the idea that a periodically switched capacitor shows the behavior of a resistor is presented. Albeit in subsequent sections, SC filters are treated in a much more fundamental way, it is worthwhile knowing the fact that there are always different ways to look into a problem and SC technique is not an exception. The material in this section gives us a crude viewpoint of the essence of the technique and it is invaluable in understanding the physical nature of filtering CT signals in a rather odd way by switching capacitors.

Consider Fig. 2.6 in which a capacitor is periodically switched between two nodes of network N. The two switches are controlled by two phases of a clock signal with period $T = 1/f_c$. The second terminal of the capacitor is permanently connected to ground.

During phase ϕ_1, the capacitor is charged up to voltage V_1. In phase ϕ_2, the capacitor

voltage becomes V_2. Therefore total charge difference during the whole clock period will be

$$\Delta q = C\,(V_2 - V_1) \tag{2.19}$$

This net charge difference is provided through nodes 1 and 2, and the average current passing from node 2 to 1 is defined as the total passed charge divided by the whole period, as follows

$$I_{av} = \frac{\Delta q}{T} = C\frac{(V_2 - V_1)}{T} \tag{2.20}$$

This relationship clearly shows that on average the switched capacitor acts as an equivalent resistor with value

$$R_{eq} = \frac{1}{f_c \cdot C} \tag{2.21}$$

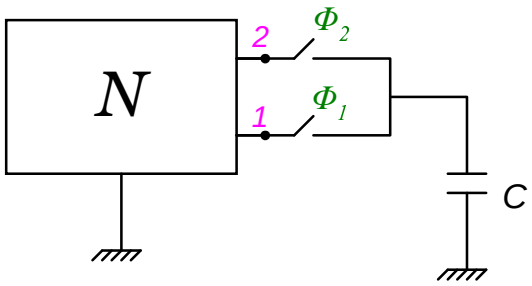

Figure 2.6: Switched capacitor acting as an equivalent resistor.

2.5 SC Integrator

The fact that a switched capacitor acts as an equivalent resistor on average, can promote the idea of realization of an integrator using only capacitors, op-amps and switches which basically stands for implementing a fully integrated filter in CMOS technology.

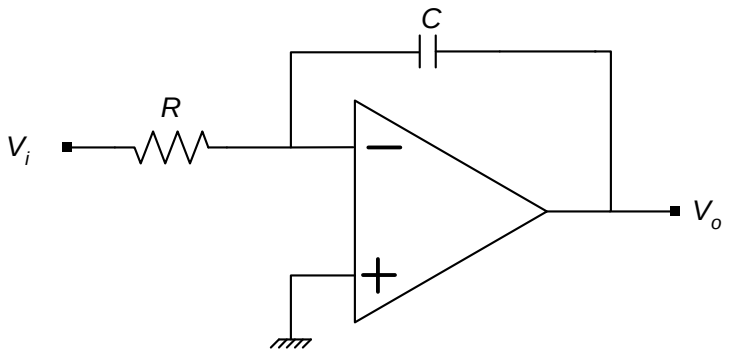

Figure 2.7: Typical CT integrator.

A typical CT integrator is shown in Fig. 2.7. A crude idea for implementing a SC integrator would be substitution of the resistor R with an equivalent SC one as it was proposed in Sec. 2.4.

But since often, the simplest way of doing something is not the best one, the resultant SC integrator is not of practical significance. This is due to systematic as well as practical shortcomings of the circuit. Nevertheless, theoretically it sheds light on a way that lead us to more complicated, yet deliberate way of performing discrete integration. As a result, in this section the basic integrator will be introduced. Then its drawbacks will be closely examined, so that the trends will become evident. In continuation, more elaborate ways of discrete integration will be presented, and by the end of this section all the aspects of discrete integrators will be covered in full details.

2.5.1 Basic Integrator

The most basic form of SC integrator is obtained by replacing resistor R in Fig. 2.7 with the SC equivalent resistor presented in Sec. 2.4. The resultant circuit is drawn in Fig. 2.8.

From this point, whenever a SC circuit is under investigation, it will be mathematically treated, so that the exact behavior of the circuit can be obtained. Since SC circuits are discrete-time, Kirchhoff's laws cannot easily be applied to them. As a result the analysis of SC circuits will mainly be based on charge conservation principle which itself is in fact the basis of KCL.

Also, from this point, whenever a SC circuit is examined, it is assumed that there exist two non-overlapping clock signals which control the switches all across the network. The

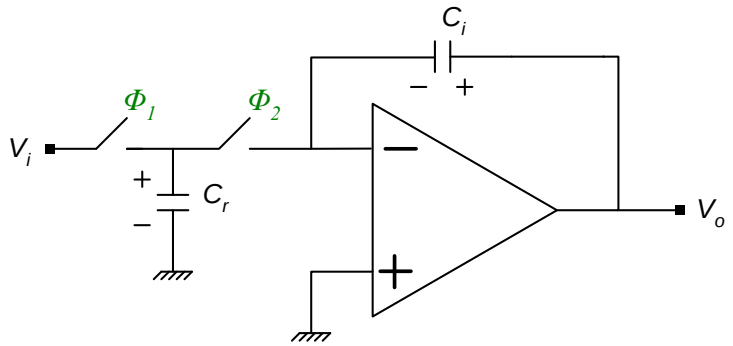

Figure 2.8: Basic SC integrator.

assumption of being non-overlapping is crucial, otherwise during transients two switches which have to be alternatively on and off can conduct simultaneously and result in severe degradation in desired characteristics of the network.

Assuming that the operational amplifier is ideal and the input V_i changes only once per clock cycle, i.e., at moments $..., n-1, n, ...$ the charge stored in resistive capacitor C_r and integrating capacitor C_i during phase ϕ_1 will be

$$q_1[n-1] = C_r V_i[n-1/2] = C_r V_i[n-1] \tag{2.22}$$

$$q_2[n-1] = C_i V_o[n-1/2] = C_i V_o[n-1] \tag{2.23}$$

and at the end of phase ϕ_2 it becomes

$$q_1[n] = 0 \tag{2.24}$$

$$q_2[n] = C_i V_o[n] \tag{2.25}$$

therefore the net charge difference for both capacitors will be

$$\Delta q_1 = q_1[n] - q_1[n-1] \tag{2.26}$$

$$\Delta q_2 = q_2[n] - q_2[n-1] \tag{2.27}$$

and from charge conservation principle

$$\Delta q_1 = \Delta q_2 \tag{2.28}$$

which gives rise to the following relationship

$$-C_r V_i\left[n-1\right] = C_i\left(V_o\left[n\right] - V_o\left[n-1\right]\right) \tag{2.29}$$

Taking Z transform, the transfer function of the integrator will be

$$\frac{V_o}{V_i} = -\frac{C_r}{C_i}\frac{1}{z-1} = -\frac{f_c \cdot C_r}{C_i}\frac{T}{z-1} \tag{2.30}$$

Comparing this to the transfer function of the analog integrator of Fig. 2.7, i.e.,

$$\frac{V_o}{V_i} = -\frac{1}{R \cdot C}\frac{1}{s_{ct}} \tag{2.31}$$

it is seen that utilization of the basic DT integrator stands for applying the following transformation between CT and DT domains

$$s_{ct} = \frac{1}{T}\left(z-1\right) \tag{2.32}$$

The frequency response of the basic SC integrator is given by

$$I(j\omega) = \left.\frac{V_o}{V_i}\right|_{z=e^{j\omega T}} = -\frac{f_c \cdot C_r}{C_i} \cdot \frac{1}{j\omega} \cdot \frac{\omega T/2}{\sin(\omega T/2)} \cdot e^{-j\omega T/2} \tag{2.33}$$

As it can be easily seen, the deviation from the ideal frequency response (2.7) has been appeared in two forms: gain or warping effect as well as phase difference. As it was thoroughly discussed previously the warping effect can be pre-compensated, but the phase degradation is equivalent to having loss in the integrator or in other words the DT filter obtained by merely replacing integrating elements by this block do not inherit the insensitivity characteristics of the original one.

A second problem which is of extreme practical significance is the sensitivity of the integrator to parasitic capacitances present in the actual real-life circuit. In real life, the switches are implemented by single MOS transistors, NMOS mainly, or an NMOS and

a PMOS in parallel as it is shown in Fig. 2.9. The latter is known as *transmission gate*. Consequently, the parasitic capacitances of these transistors, i.e., source-bulk C_{sb} and drain-bulk C_{db} are in parallel with the resistive capacitor C_r, so that the total capacitance that contribute to the integrator gain will be $C_r + C_{sb} + C_{db}$. If the values of these capacitors were known, it might be possible to pre-compensate for this extra capacitance by properly reducing C_r value. However, these capacitor do not have known values and to make the situation even worse, they are largely dependent on operating conditions such as applied voltage, etc. This stands for a major degradation of the characteristics of the integrator, so that a network consisting of a few of these imprecise devices can be unacceptably inaccurate. Therefore a new scheme should be employed to combat this problem in a proper way, and in fact, this is the subject of investigation of the rest parts of SC integrators study.

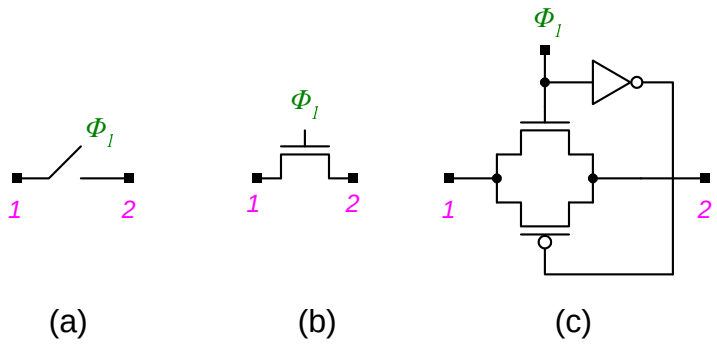

Figure 2.9: (a)Ideal switch schematic (b)NMOS implementation (c)Transmission gate.

2.5.2 Stray Insensitive Integrator

The susceptibility of basic SC integrator to stray capacitances—mainly due to C_{sb} and C_{db} of the transistors used as switching elements—requires a different switching scheme so that the effect of these parasitic components can be effectively eliminated.

Compensation for these stray capacitors through adjustment of other circuit elements is not practical, since not only the values of these parasitic elements are not exactly known but also they are subject to large variations due to ambient as well as circuit operating conditions.

Two methodologies can be adopted to address this issue:

- **Preventing charge build-up on stray capacitors.**

If during two consecutive clock cycles the voltage of the terminals of the switched capacitor is kept at a constant level, the stored charge in these parasitic component do not change and therefore they do not contribute to governing equations of the circuit which are based on charge conservation.

- **Disposing the stored charge of stray capacitors.**

  The other way to cancel the effect of parasitic capacitances is to constantly keeping terminals of the switched capacitor connected to voltage sources. The fact that the stray capacitor is switched between two voltage source, ensures that its voltage is known at all moments, so that it has no effect on the total circuit behavior. In fact, this is one of the early results of basic circuit theory in which every element that is placed in parallel with a voltage source can be simply discarded. It is obvious, yet worthwhile mentioning that the common ground of the circuit can be used as a voltage source.

Following this guideline, two kinds of stray-insensitive integrators are examined afterwards, known as inverting and non-inverting. As it will be evident shortly, their difference is beyond just a minus sign in their transfer function—which itself is also of great importance since it introduces the idea of implementing *negative resistors* using SC technique—and expands to different warping and phase degradations.

Inverting Integrator

The stray insensitive integrator is depicted in Fig. 2.10. It has two extra switches comparing to the basic SC integrator of Fig. 2.8, yet it is completely immune to parasitic capacitances.

Unlike the basic integrator, in this structure both terminals of the switched capacitor are floating. Therefore stray elements at both nodes have to be considered.

The parasitics at the right node of the capacitor are effectively eliminated through the first scheme presented previously, i.e., this node is switched between two points which have the same potential—in this case zero—and they are common ground and virtual ground provided by the operational amplifier at its inverting node.

For the left node the second scheme has been employed. This node is alternatively switched between two voltage source, i.e., input V_i and common ground.

During phase ϕ_2, C_r is grounded at both ends, so that it has no charge. Assuming that ideally there is no leakage through the op-amp input terminals, the charge stored in C_i remains unchanged. During phase ϕ_1, C_r is charged up to the input voltage V_i and again

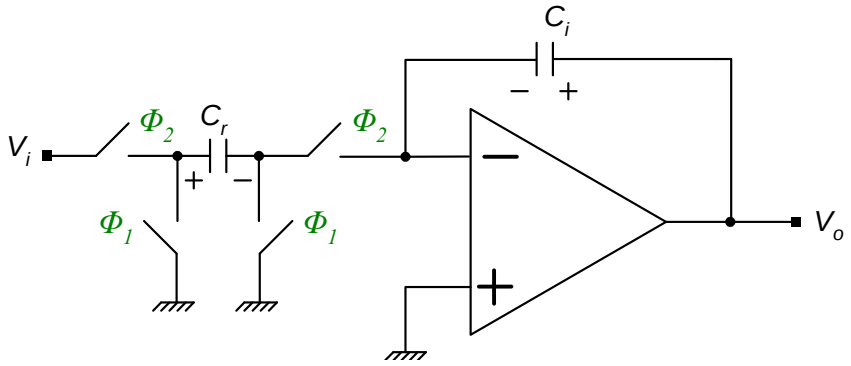

Figure 2.10: Stray insensitive inverting integrator.

since there is no current passing through the inverting input terminal of the op-amp, this amount of charge has to be provided by C_i. Mathematically this can be written as follows

$$q_1[n-1/2] = 0 \tag{2.34}$$
$$q_2[n-1/2] = q_2[n-1] = C_i V_o[n-1] \tag{2.35}$$

$$q_1[n] = C_r V_i[n] \tag{2.36}$$
$$q_2[n] = C_i V_o[n] \tag{2.37}$$

$$\Delta q_1 = q_1[n] - q_1[n-1/2] = C_r V_i[n] \tag{2.38}$$
$$\Delta q_2 = q_2[n] - q_2[n-1/2] = C_i\left(V_o[n] - V_o[n-1]\right) \tag{2.39}$$

Applying charge conservation

$$\Delta q_1 + \Delta q_2 = 0 \tag{2.40}$$

gives rise to the following transfer function

$$\frac{V_o}{V_i} = -\frac{C_r}{C_i}\frac{z}{z-1} \tag{2.41}$$

and the frequency response is given by

$$I(j\omega) = -\frac{f_c \cdot C_r}{C_i} \cdot \frac{1}{j\omega} \cdot \frac{\omega T/2}{\sin(\omega T/2)} \cdot e^{j\omega T/2} \tag{2.42}$$

Non-inverting Integrator

The stray insensitive non-inverting SC integrator is shown in Fig. 2.11. The structure is similar to inverting integrator in Fig. 2.10, unless the switching sequence is different for the left hand terminal of C_r. The methodology described earlier have been used exactly in the same manner as the inverting case to neutralize the stray capacitors.

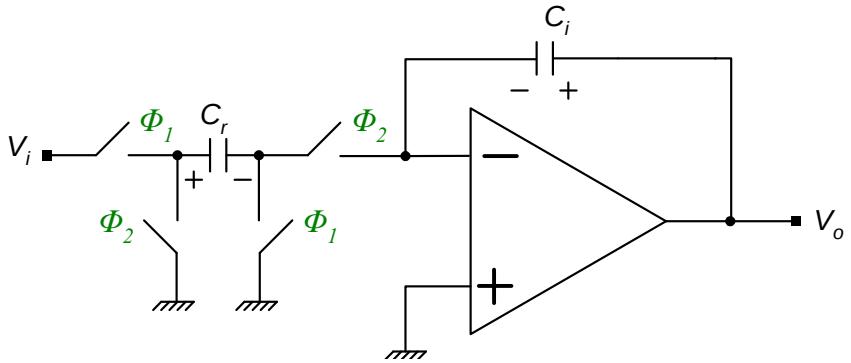

Figure 2.11: Stray insensitive non-inverting integrator.

During phase ϕ_1, C_r is charged up to V_i. In the next cycle, the positive terminal is connected to ground and the negative terminal to the op-amp input. That basically stands for a sudden voltage drop of the op-amp's inverting terminal. The op-amp tries to bring this node voltage to zero in order to provide a virtual ground, therefore a current in opposite direction of the previous cycle flows into C_r. This current is passing through C_i, but in reality it is provided by the active element, i.e., the operational amplifier. The opposite direction of current flow in C_r in consecutive clock cycles, can be considered as having a negative equivalent resistor. In fact this is the case, and that is the reason of the lack of a minus sign in the transfer function of this block. It should be noted that this effect only exist as long the active element is present in the circuit. This is based on energy conservation principle. Without the existence of an active element, reversing of the current flow direction is not possible, since there would be no source to provide extra amount of

energy. The equations governing the block are written in a way similar to the inverting integrator as follows

$$q_1[n-1/2] = C_r V_o[n-1/2] = C_r V_o[n-1] \tag{2.43}$$
$$q_2[n-1/2] = q_2[n-1] = C_i V_o[n-1] \tag{2.44}$$

$$q_1[n] = 0 \tag{2.45}$$
$$q_2[n] = C_i V_o[n] \tag{2.46}$$

$$\Delta q_1 = q_1[n] - q_1[n-1/2] = -C_r V_i[n-1] \tag{2.47}$$
$$\Delta q_2 = q_2[n] - q_2[n-1/2] = C_i\left(V_o[n] - V_i[n-1]\right) \tag{2.48}$$

Applying charge conservation

$$\Delta q_1 + \Delta q_2 = 0 \tag{2.49}$$

gives rise to the following transfer function

$$\frac{V_o}{V_i} = \frac{C_r}{C_i}\frac{1}{z-1} \tag{2.50}$$

and the frequency response is given by

$$I(j\omega) = \frac{f_c \cdot C_r}{C_i} \cdot \frac{1}{j\omega} \cdot \frac{\omega T/2}{\sin(\omega T/2)} \cdot e^{-j\omega T/2} \tag{2.51}$$

2.5.3 Fully Differential Integrator

The great immunity of differential circuits to power supply noise and other types of interference, motivates the designer to apply this technique to SC circuits. In order to do that, the existence of a stray insensitive differential SC integrator is essential. The integrator which is presented in this section, not only shows immunity to stray capacitance but also it has a true bilinear transfer function. This is in fact of great significance, since as it will

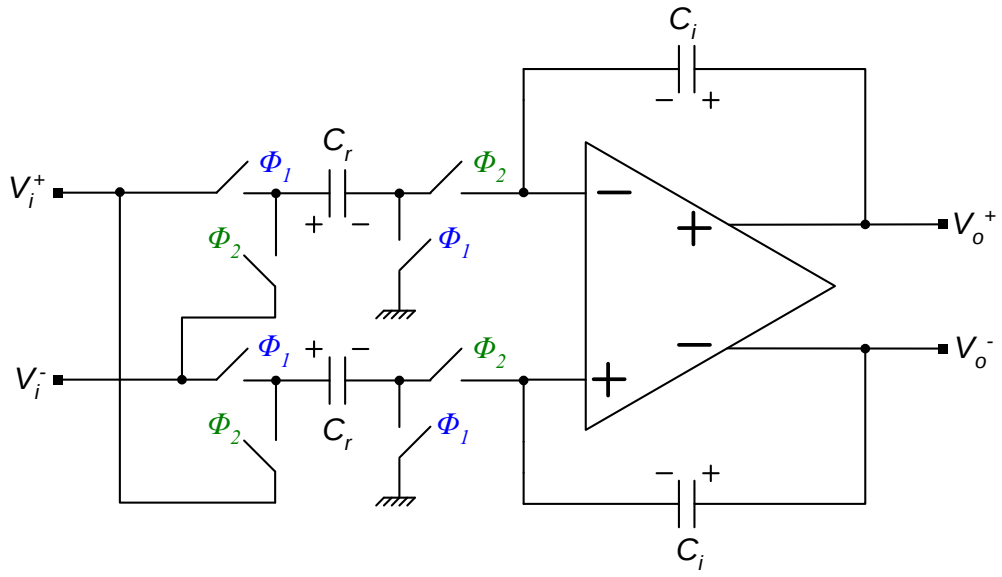

Figure 2.12: Stray insensitive fully differential bilinear integrator.

be seen later a direct consequence of having a true bilinear integrator makes the derivation of a DT filter from a CT prototype, a simple as well as a straightforward task.

In order to achieve this goal, the ideas behind single-ended inverting and non-inverting integrators can deliberately be combined to obtain a fully-differential integrator (Fig. 2.12). As it was shown in previous section, inverting integrator provides a minus sign but no phase delay from input to output. Non-inverting has no sign change but provides half a cycle delay. Their difference is only due to the timing difference in the switches connected to the left hand terminal of capacitor C_r. This kindles the idea of switching the ground connection of the left hand terminal of C_r with the inverse voltage of V_i. In this case, the stray insensitivity remain unchanged since the new connection is also a voltage source and the associated terminal of C_r is switched back and forth between two voltage sources, henceforth the parasitic capacitance present at this node has no effect on the circuit behavior. Furthermore, there exists an inverting TF from one input and a non-inverting TF from the other one to the output. If the switching scheme is kept the same for the other half circuit of the block but the inputs are switched together, then the TFs will be different for these half circuits, and consequently looking differentially at the output provides a true bilinear integration.

It should be noted that the negative sign of voltage requires no extra circuitry in

differential networks, since by just swapping two lines the opposite voltage will be obtained, whereas in single ended case this requires an extra active element for sign inversion.

$$\begin{aligned} q_r[n-1/2] &= C_r V_i^+[n-1/2] = C_r V_i^+[n-1] && (2.52)\\ q_i[n-1/2] &= q_i[n-1] = C_i V_o^+[n-1] && (2.53)\\ q_r'[n-1/2] &= C_r' V_i^-[n-1/2] = C_r' V_i^-[n-1] && (2.54)\\ q_i'[n-1/2] &= q_i'[n-1] = C_i' V_o^-[n-1] && (2.55) \end{aligned}$$

$$\begin{aligned} q_r[n] &= C_r V_i^-[n] && (2.56)\\ q_i[n] &= C_i V_o^+[n] && (2.57)\\ q_i'[n] &= C_i' V_i^+[n] && (2.58)\\ q_i'[n] &= C_i' V_o^-[n] && (2.59) \end{aligned}$$

$$\begin{aligned} \Delta q_r &= q_r[n] - q_r[n-1/2] = C_r\left(V_i^-[n] - V_i^+[n-1]\right) && (2.60)\\ \Delta q_i &= q_i[n] - q_i[n-1/2] = C_i\left(V_o^+[n] - V_o^+[n-1]\right) && (2.61)\\ \Delta q_r' &= q_r'[n] - q_r'[n-1/2] = C_r'\left(V_i^+[n] - V_i^-[n-1]\right) && (2.62)\\ \Delta q_i' &= q_i'[n] - q_i'[n-1/2] = C_i'\left(V_i^-[n] - V_i^+[n-1]\right) && (2.63) \end{aligned}$$

From charge conservation

$$\begin{aligned} \Delta q_r + \Delta q_i &= 0 && (2.64)\\ \Delta q_r' + \Delta q_i' &= 0 && (2.65) \end{aligned}$$

and assuming

$$\begin{aligned} C_r' &= C_r && (2.66)\\ C_i' &= C_i && (2.67) \end{aligned}$$

$$\begin{aligned} &C_i\left[\left(V_o^+[n] - V_o^-[n]\right) - \left(V_o^+[n-1] - V_o^-[n-1]\right)\right] = \\ &C_r\left[\left(V_i^+[n] - V_i^-[n]\right) + \left(V_i^+[n-1] - V_i^-[n-1]\right)\right] \qquad (2.68) \end{aligned}$$

$$C_i\left(V_o\left[n-1\right] \;-\; V_o\left[n-1\right]\right) \;=\; C_r\left(V_i\left[n\right] \;+\; V_i\left[n\right]\right) \tag{2.69}$$

Therefore, the transfer function of stray-insensitive fully differential integrator of Fig. 2.12 will be a true bilinear one as follows

$$\frac{V_o}{V_i} = \frac{C_r}{C_i} \cdot \frac{z+1}{z-1} \tag{2.70}$$

and the frequency response is given by

$$I(j\omega) = \frac{2 \cdot f_c \cdot C_r}{C_i} \cdot \frac{1}{j\omega} \cdot \frac{\omega T/2}{\tan\left(\omega T/2\right)} \tag{2.71}$$

2.5.4 Fully Differential Damped Integrator

As it will be seen in Sec. 3.1.2 the insensitivity properties of the prototype CT filter is retained iff it is doubly terminated one. That means that the original fitler hast to be terminated by resistive loads at both ends. As a direct consequence, when the equivalent SFG of the the prototype filter is derived, two special integrators appear at both ends which are no longe loss-less.

This might seem somewhat contradictory, since up to now, all our efforts have been concentrated to realize loss-less integrators, and now suddenly we need integrators which are *not* loss-less. This can be clarified by noting that the essence of Bruton's theory lies on the fact that in order to preserve sensitivity properties of the CT prototype circuit, the discrete integrators must not show any phase difference with regard to their CT counterparts. Subtlity is in the fact that there is no restriction on having loss-less integrators in CT domain, but the DT integrators must show a loss behavior exactly equal to the original CT ones.

Coclusively, in order to prevent any confusion, the integrators which are not in fact loss-less will be called *damped*, and the terminology *lossy* is kept exclusively for those integrators which show different loss behavior with respect to their CT counterparts.

In order to realize a damped integrator, the original one in Fig. 2.12 can be used, provided that by some means an appropriate portion of the charge delivered by the source to C_r is damped and not delivered to the integrating capacitor C_i. To do this, a CT damped integrator gives the idea of inserting equivalent SC *positive* resistors between input and

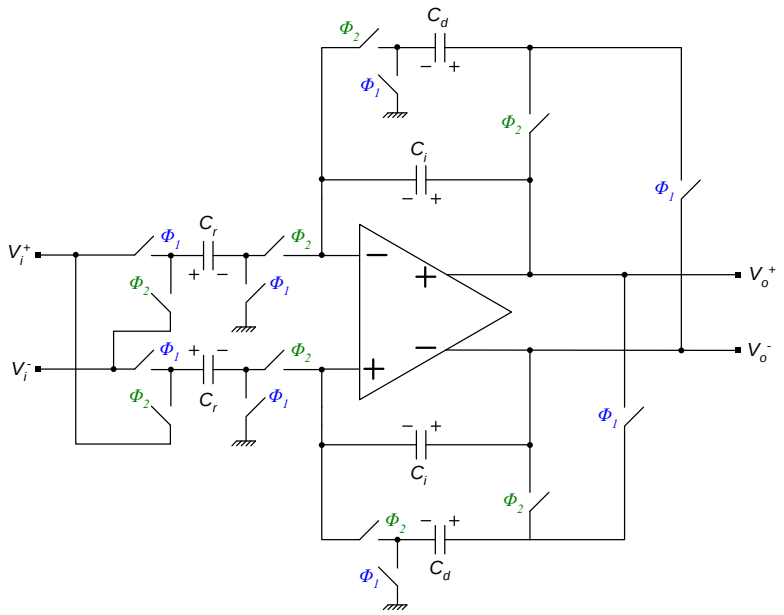

Figure 2.13: Stray insensitive fully differential bilinear damped integrator.

output nodes with different polarities. Based on this the SC bilinear differential damped integrator can be realized as given in Fig. 2.13.

The equations can be easily written in a way similar to Sec. 2.5.3 so that the TF of the circuit will be obtained as the following

$$\frac{V_o}{V_i} = \frac{1}{\frac{C_d}{C_r} + \frac{C_i}{C_r} \cdot \frac{z-1}{z+1}} \tag{2.72}$$

and the frequency response is given by

$$I(j\omega) = \frac{1}{\frac{C_d}{C_r} + j\,\frac{C_i}{C_r}\,\tan\left(\omega T/2\right)} \tag{2.73}$$

2.6 SC Filter Synthesis

Filter synthesis have been the subject of study for a century. By the time, several methods have been developed for the realization of a desired transfer function. More or less, all the methods available for designing analog filters can be realized using SC techniques. The full

coverage of these methods require hundreds of pages of mathematical as well as illustrative discussions which is not the aim of this thesis. Therefore, it is assumed that the reader is familiar with the basics of CT filter theory. A very brief overview of the methods which can be used for SC realization of desired TFs are given, and then one of them, i.e., *leapfrog ladder simulation* which is the premier choice for LP filters—the subject of this work—will be covered in details.

The available filter synthesis methods which can be employed to SC circuits are classified as follows:

1. **Cascade**

   The transfer function is split into a series of second-order terms and one first-order if necessary, each of which can easily be realized by the infamous bi-quad blocks [35] [36]. The great advantage of this method is that they can readily be tuned, i.e., changing the place of every single pole or zero is a simple task, since it is reduced to tuning one block independent of the others, and ideally the behavior of each block has no effect on the others. However, these kinds of filters are strongly vulnerable to element variations or in other words they show high sensitivity to random variations of constituting components. This greatly affects the preciseness of these filters and as a result they are not very suitable for integrated technology in which the absolute tolerance of element values can be extremely high.

2. **LC Ladder Simulation**

   Based on Orchard's theorem (Sec. 3.1.2), the sensitivity of LC passive filters is extremely low in pass-band. On the other hand, any network that can simulate the governing equations of an LC ladder structure will inherit all its properties, including the magnificent immunity to element value variations in pass-band.

   This task can be done in two different ways:

   - **Element substitution**

     In this method either the impedance of inductors are directly simulated or after some transformations, e.g., Bruton's, new networks are obtained and then the resultant components are replaced by SC blocks [3] [36].

   - **Leapfrog structure**

     Simulation of fundamental state variable equations of the network is the basis of this method.

The voltages of capacitors and the currents of inductors are considered as state variables and Kirchhoff's laws, i.e., KCL and KVL that relate these variables together are written. In fact, the relationship between current-voltage or voltage-current of these elements is in the form of integration. Consequently a network consisting of a series of interconnections between several integrators is obtained and these integrators are subsequently replaced by suitable SC blocks.

This results in an efficient as well as straight-forward way of implementing a desired TF which has very low sensitivity to element value variations. The filter designed in this work is based on this topology. Conclusively, this method will be treated thoroughly, later in this chapter.

3. **Wave Filter**

   The generality of Orchard's theorem is so significant which does not restrict it to LC passive or better to say lumped networks. It can be applied to a much broader extent to include even distributed networks, like microwave filters.

   Since in distributed networks the governing equations are dealt with wave variables instead of voltages and currents for lumped circuits, these networks are known as *wave filters*.

   In fact, some deviations from the extensive research on wave filters initiated by Fettweis—the father of SC technique—in 1960's led circuit designers to the utilization of periodically switched capacitors to implement accurate, integrated, highly selective filters. A good introduction to wave filters can be found in [24] and [28] presents a SC filter based on this method.

2.6.1 Leapfrog LC Ladder Simulation

A typical doubly terminated ladder network is shown in Fig. 2.14. It consists of a number of impedances Z_{2k-1} in parallel branches and admittances Y_{2k} in series branches, alternatively placed in a chain.

The voltages V_{2k-1} and the currents I_{2k} are the circuit variables. Therefore the governing equations of the network based on KVL and KCL are as follows

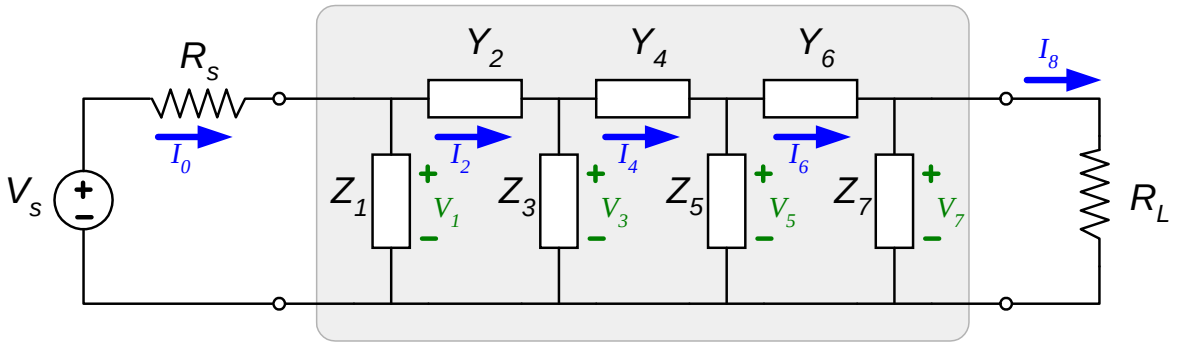

Figure 2.14: General ladder network.

$$I_2 = Y_2 (V_1 - V_3) \tag{2.74}$$
$$I_4 = Y_4 (V_3 - V_5) \tag{2.75}$$
$$I_6 = Y_6 (V_5 - V_7) \tag{2.76}$$

$$V_1 = Z_1 (I_0 - I_2) \tag{2.77}$$
$$V_3 = Z_3 (I_2 - I_4) \tag{2.78}$$
$$V_5 = Z_5 (I_4 - I_6) \tag{2.79}$$
$$V_7 = Z_7 (I_6 - I_8) \tag{2.80}$$

Obtaining the Norton equivalent circuit of the source shown in Fig. 2.15 results in a resistor R_s in parallel with impedance Z_1. On the other hand, load resistance R_L and impedance Z_7 are in parallel. Therefore by defining two new impedances

$$Z_1' \triangleq Z_1 \| R_s \tag{2.81}$$
$$Z_7' \triangleq Z_7 \| R_s \tag{2.82}$$

two variables I_0 and I_8 becomes redundant and as a result the equations 2.77 and 2.80 can be rewritten as

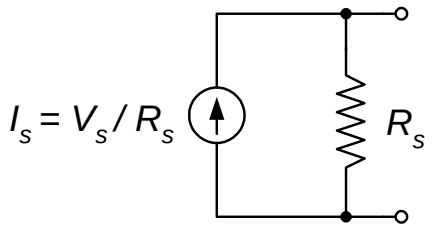

Figure 2.15: Norton equivalent circuit of the source.

$$V_1 = Z_1^{'}(I_s - I_2) \tag{2.83}$$
$$V_7 = Z_7^{'} I_6 \tag{2.84}$$

where I_s is given by

$$I_s \triangleq \frac{V_s}{R_s} \tag{2.85}$$

In order to obtain a Signal Flow Graph (SFG), an impedance scaling is desirable. That could be done by multiplying all the admittances by a truly real impedance R_0 and dividing all the impedances by R_0. In this way all the impedances and admittances in the network convert to dimensionless voltage transfer function. Moreover, all the state variables of type current, are multiplied by R_0, so that they become voltage variables. R_0 can accept any values, which in its simplest form it will be 1 Ω.

The aforementioned discussion can be easily seen by multiplying both sides of Eq. 2.74–2.76 by R_0 and a modification in right sides of Eq. 2.83–2.84.

Based on these, the new state variables are given by

$$u_1 = V_1 \tag{2.86}$$
$$u_3 = V_3 \tag{2.87}$$
$$u_5 = V_5 \tag{2.88}$$
$$u_o = V_7 \tag{2.89}$$

$$u_s = R_0 I_s = \frac{R_0}{R_s} V_s \tag{2.90}$$
$$u_2 = R_0 I_2 \tag{2.91}$$
$$u_4 = R_0 I_4 \tag{2.92}$$
$$u_6 = R_0 I_6 \tag{2.93}$$

and the dimensionless voltage transfer functions are as follows

$$z_1 = Z_1^{'}/R_0 = \left(Z_1 \| R_s\right)/R_0 \tag{2.94}$$
$$z_3 = Z_3/R_0 \tag{2.95}$$
$$z_5 = Z_5/R_0 \tag{2.96}$$
$$z_7 = Z_7^{'}/R_0 = \left(Z_7 \| R_l\right)/R_0 \tag{2.97}$$

$$y_2 = R_0 Y_2 \tag{2.98}$$
$$y_4 = R_0 Y_4 \tag{2.99}$$
$$y_6 = R_0 Y_6 \tag{2.100}$$

Also, as it can be seen from Eq. 2.74–2.79, every state variable is proportional to the difference between two others. But, combining adders and integrators can be easily done by duplexing the switched capacitor at the input of an integrator and connecting each one to the associated input signal. Moreover two types of integrators, i.e., inverting and non-inverting are readily available. Therefore, by properly changing the signs of some variables—in a special manner that will be seen shortly—a network consisting of only adder-integrators will be obtained and there will be no need for subtracters or sign-inverters.

These new voltage variables and dimension-less voltage transfer functions together with the argument just presented, describe a SFG as depicted in Fig. 2.16.

It should be noted that negative sign of block transfer functions correspond to utilization of inverting integrators in single-ended realization. For the differential realization, the same integrator can be used for all the blocks and sign inversion will be done readily by just swapping the wires.

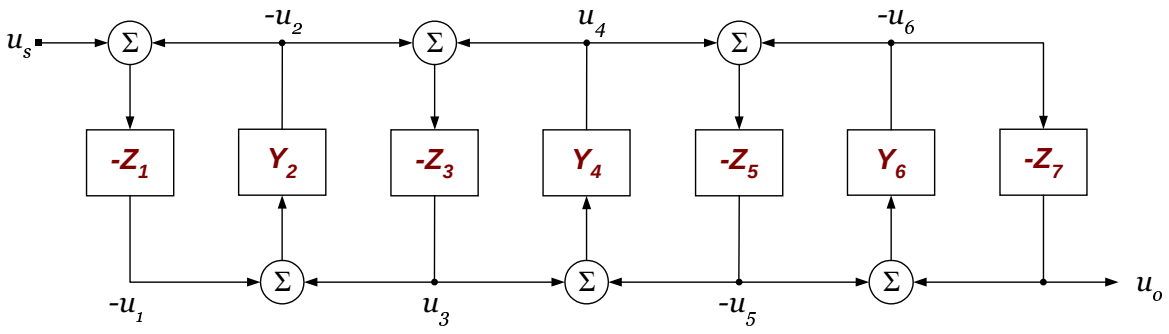

Figure 2.16: SFG of the ladder network.

Once the SFG is obtained, the remaining task will be realization of each block transfer function using appropriate SC circuits. For fully differential case, the integrator presented in Sec. 2.5.3 is a true bilinear stray insensitive one and can easily be substituted for the SFG blocks. Also for resistive termination at both ends, the SC integrator presented in Sec. 2.5.4 gives an exact bilinear transform of the CT circuit. A complete procedure of these steps are given in Chap. 5 where a 7^{th}-order LP elliptic filter will be designed.

For single ended design, the derivation of a SC network that can realize the bilinear transform of the original CT network in a parasitic insensitive manner is not a straightforward task. It requires some frequency or element transformations, to obtain a network that utilize the integrators presented in Sec. 2.5.2— which are neither bilinear nor loss-less (according to Bruton's definition of a lossy integrator)—nevertheless, their total transfer function is the bilinearly transformed version of the original CT ladder network. Interested readers are referred to the literature [25] [26] [6] [17].

2.6.2 Dynamic Range Optimization

The SFG obtained in previous section simulates a passive LC ladder network, so that the ratio of output voltage u_o over input u_s has a maximum value of one. However, this is not the case for the intermediate state variables of SFG. In fact the transfer function from input to any of these variables can have a value much higher than one. Ideally this poses no difficulties, but in practice that this circuit is to be realized in an MOS integrated circuit, working with low-voltage supplies, this suddenly becomes a severe problem. And if the

filter is to be used for wireless applications this is in fact a bottleneck, since it must be extremely linear while working with very low levels of voltage—typically less than 2 V. It is obvious that if an intermediate state variable of the graph which corresponds to an internal node of the final circuit has a maximum value higher than the output voltage, there will be ranges of frequencies that these voltages reach to the saturation level while the output voltage—which from circuit theory has the most impact on linearity performance of the whole network—can be at levels much less than its maximum. In conclusion, a method should be found that limit the maximum value of all the variables of the network to a common level. In other words, the transfer function from the input to any node of the circuit must have a maximum value of one.

It can be shown that the input-output transfer function is in fact a function of loop TFs of the graph [36]. That means changing the TF of every individual block in a way that loop TFs remain unchanged, guarantees that the input-output relationship completely retains its frequency characteristics except for a constant gain factor.

Consider the new SFG of Fig. 2.17 The input is multiplied by a gain factor K, so that the maximum value of the output voltage u_o does not change. In this respect, the TF $u_o(j\omega)/u_s(j\omega)$ remains absolutely unchanged.

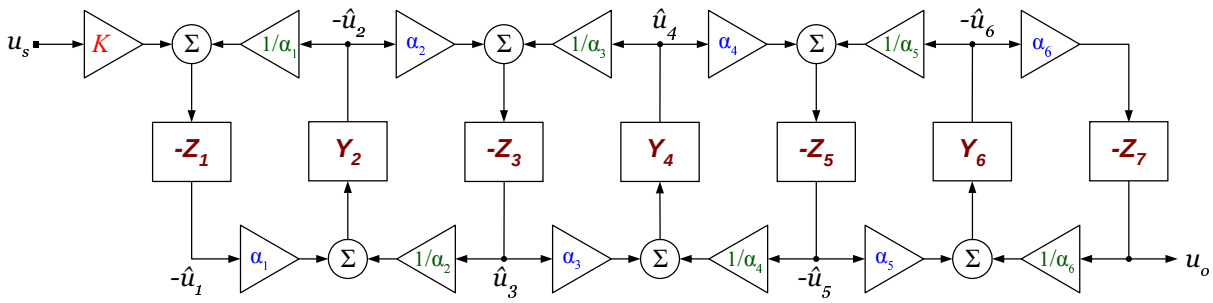

Figure 2.17: New SFG of the ladder network for dynamic range optimization.

For the new graph we have

$$\hat{u_6}(j\omega) \;=\; \frac{u_o(j\omega)}{\alpha_6 \cdot z_7(j\omega)} \tag{2.101}$$

therefore the maximum value of $|\hat{u_6}(j\omega)|$ will be

$$Max\left(|\hat{u_6}(j\omega)|\right) \;=\; Max\left(\left|\frac{u_o(j\omega)}{\alpha_6 \cdot z_7(j\omega)}\right|\right) \;=\; \frac{1}{\alpha_6} \cdot Max\left(\left|\frac{u_o(j\omega)}{z_7(j\omega)}\right|\right) \tag{2.102}$$

It should be noted that since α_6 is a constant—independent of frequency—it could be taken out of $Max()$ function. Equation 2.102 suggests that how α_6 can be selected to make the maximum value of $\left|i_6(\hat{j\omega})\right|$ and $|v_o|$ equal, i.e.,

$$\alpha_6 \;=\; \frac{Max\left(|u_6(j\omega)|\right)}{Max\left(|u_o(j\omega)|\right)} \tag{2.103}$$

In a similar fashion the other gain factors in Fig. 2.17 are defined as follows

$$\alpha_k \;\stackrel{\Delta}{=}\; \frac{m_k}{m_{k+1}} \tag{2.104}$$

$$m_k \;\stackrel{\Delta}{=}\; Max\left(|u_k(j\omega)|\right) \tag{2.105}$$

and K is given by

$$K \;\stackrel{\Delta}{=}\; \frac{k_0}{\prod_{k=1}^{n} \alpha_k} \;=\; k_0 \frac{m_1}{m_{n+1}} \tag{2.106}$$

in which k_0 is an arbitrary gain factor which only affects the ratio of output over input variable, leaving the internal variables untouched. In order to keep the overal gain of the final circuit exactly equal to the protoype one, k_0 should be selected as 1.

With the introduction of these gain factors, the SFG of Fig. 2.17 presents the desired frequency response and simultaneously all the internal and output voltages experience similar maximum values, so that the optimum linearity performance can be achieved.

Chapter 3

Fundamental Issues in Filter Design

3.1 Sensitivity

Any physical system is subject to deviations from the desired characteristics. Ambient conditions—like temperature, humidity, etc.—in addendum to aging and human errors are only few reasons behind these unwilling variations.

This problem is even worse for such sophisticated systems like integrated circuits. Some component parameters may even experience tens of percents of error during the lengthy as well as complicated fabrication process. And by the end of fabrication process, even if the permanent deviations from the ideal characteristics lie between certain bounds that the device could be used for the required task, working conditions, ambient parameters, etc. might all affect the characteristics of the components.

Based on these facts, employing certain techniques to combat the deviations of circuit elements will be inevitable. To achieve this goal, an exact knowledge of the effects of individual element variations on desired parameters has to be gained. And *sensitivity analysis* is the one responsible for this extremely important task.

The study of sensitivity of electrical circuits has been an ongoing research field for around one hundred years, nevertheless some breakthroughs which happened during three decades of 60's to 80's brought deep insights into the various aspects of the area.

The aim of this section is to expose the reader to some fundamental theorems and properties of electrical networks. As the reader moves forward through the section, the obtained knowledge clearly justifies why ladder simulation technique has been chosen as a premier choice for the architecture of the filter under investigation of this thesis.

The infamous Tellegen's theorem is presented, since it's the foundation for the deriva-

tion of all sensitivity analysis formulas. Then Orchard's theorem to which it was referred for several times in previous chapter, and later on the general sensitivity analysis formulas for doubly terminated reciprocal lossless networks which was formulated by his own and his colleagues twenty years after proposition of the aforementioned theorem.

But before moving forward, it is necessary to give a sound description of *sensitivity*. Some functions and notations that will be used later, is also introduced here.

- **Sensitivity**

  First order sensitivity which will be referred to as *sensitivity* in short, is a figure of merit that shows how constituting elements of a circuit affect its properties. The sensitivity of function P with respect to element x is defined as follows

$$S \triangleq \frac{d(\ln P)}{d(\ln x)} \triangleq \frac{x}{P} \cdot \frac{dP}{dx} \tag{3.1}$$

- **Transducer function: Loss and Phase**

  Transducer function $H(j\,\omega)$ or transducer coefficient $\theta(j\omega)$ determines signal transmission properties of the filter —relationship between input and output power or voltage, depending on the network structure. The loss $\alpha(j\omega)$ (in nepers), and the phase $\beta(j\omega)$ (in radians), are the real and the imaginary part of the transducer coefficient, respectively, as it is given by

$$\alpha(j\omega) + j\beta(j\omega) = \theta(j\omega) \triangleq \ln H(j\omega) \tag{3.2}$$

$$\alpha(j\omega) = \ln|H(j\omega)| \tag{3.3}$$

$$\beta(j\omega) = \angle H(j\omega) \tag{3.4}$$

  Unless otherwise explicitly mentioned, all the networks which are dealt with here, are assumed to be passive, so that α may never be negative.

- **Doubly terminated filters**

  The transducer function $H(j\,\omega)$ of a doubly terminated filter, Fig. 3.1, is given by

$$H(j\,\omega) \triangleq \frac{V_s}{2\,V_2}\sqrt{\frac{R_2}{R_1}} \tag{3.5}$$

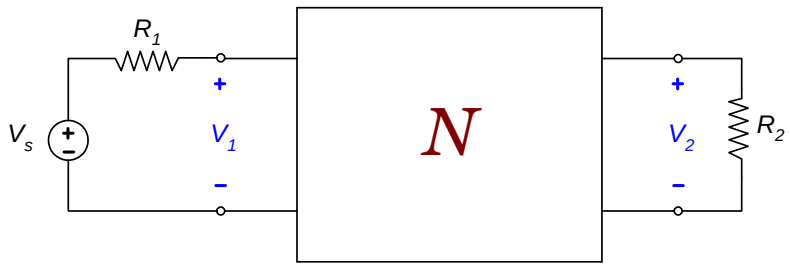

Figure 3.1: A doubly terminated filter.

as a result the loss can be written in terms of maximum available power and power delivered to the load as the following

$$\alpha \;=\; \frac{1}{2}\ln|H(j\,\omega)|^2 \;=\; \frac{1}{2}\ln\frac{|V_s|^2/4R_1}{|V_2|^2/R_2} \;=\; \ln\frac{P_{max}}{P_2} \tag{3.6}$$

- **Singly terminated filter**

  The transducer function $H(j\,\omega)$ of a singly terminated filter, Fig. 3.2, is given by

$$H(j\,\omega) \;\triangleq\; \frac{V_s}{V_2} \tag{3.7}$$

  The main difference between singly and doubly terminated filters is that in singly terminated case, there is no upper bound for the output voltage, and as it will be seen later in this chapter, this the basis for far inferiority of loss function sensitivity of singly terminated networks comparing to doubly terminated ones.

  It should be noted that both networks in Fig. 3.2 can contain resistive elements, yet there shouldn't be any resistance in series with the voltage source in case (a) and any resistance in parallel with output port in case (b).

  The reason for this unboundedness is that in case (a) for some frequencies the impedance seen by the source is zero, so that the output delivered by the source will be infinite. For case (b) it can be interpreted in a different way by noticing that since the output voltage is taken across a purely reactance element, therefore regardless of the amount of power delivered by the source, this voltage which has no associated real power can approaches infinity.

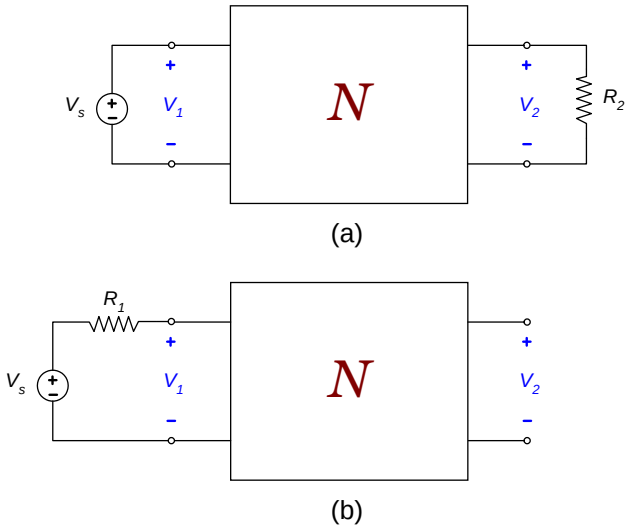

Figure 3.2: Singly terminated filters. (a)Resistive termination at output port. (b)Resistive termination at input port

3.1.1 Tellegen's Theorem

Tellegen's theorem in its most complete form deals with special operators known as Kirchhoff's. In order to be able to present this theorem in its most concise form, a more formal representation of Kirchhoff's laws, followed by the introduction of Kirchhoff's operators are given. Later on, the strong form as well as its weak forms will be introduced. Interested readers can consult books dealing with fundamentals of circuit theory or some monographs written specially on the topic, e.g., [33]. The notations used in this section is adopted from this reference.

Consider a network with b branches, n nodes and s separate parts. This network is represented by a matrix B, $(b-n+s)\times b$, known as *loop matrix*. Vectors $\mathbf{v}$ and $\mathbf{i}$, both $b\times 1$, represent branch voltages and currents respectively. There exist only $b-n+s$ independent currents in the network, given by vector $\bar{\mathbf{i}}$, $(b-n+s)\times 1$.

KVL and KCL are stated as the following

$$B\ \mathbf{v} = 0 \tag{3.8}$$

$$\mathbf{i} = B^t\ \bar{\mathbf{i}} \tag{3.9}$$

A direct corollary of these relations is the *actual power* theorem, give by

$$\mathbf{v^t}\ \mathbf{i}\ =\ 0 \tag{3.10}$$

which states that at any given point of time, regardless of nature and constituting laws of network elements, the sum of the power of the total branches of the network is zero. In fact, as it will be seen later, this is a special case of the Tellegen's theorem.

Kirchhoff's Operators

Consider operator $\Lambda\{\}$ that maps an n-dimension space to a new n-dimension space.

- **Kirchhoff Voltage Operator**

  Operator $\Lambda\{\}$ is called a *Kirchhoff voltage operator* iff when acts upon branch voltages of a network, vector $\mathbf{v}$, the resulting mapped voltages, $\mathbf{v'} = \Lambda\{\mathbf{v}\}$ also obeys KVL.

  Laplace transform or Fourier transform are some typical examples of Kirchhoff voltage operators.

- **Kirchhoff Current Operator**

  Operator $\Lambda\{\}$ is called a *Kirchhoff current operator* iff the set of currents $\mathbf{i'}$ yielded by applying it on the branch currents of the network, $\mathbf{i'} = \Lambda\{\mathbf{i}\}$, also obey KCL.

  Derivation with respect to time, d/dt, is an example of Kirchhoff current operators.

It should be noted that many Kirchhoff voltage operators are also Kirchhoff current operators and vice versa, like all the three examples introduced here, nevertheless that is not always true [33].

Strong Form of Tellegen's Theorem

Let $\Lambda'\{\}$ and $\Lambda''\{\}$ be Kirchhoff *voltage* operator and Kirchhoff *current* operator, respectively.

The most general statement of Tellegen's theorem, known as *strong form* is as follows

$$\Lambda'\{\mathbf{v^t}\}\ \Lambda''\{\mathbf{i}\}\ =\ 0 \tag{3.11}$$

For a network with ports—port current is defined in opposite direction of a normal branch [33]— in which voltages and currents of the ports are defined by vectors $\mathbf{v_p}$ and

$\mathbf{i_p}$, and branch voltages and currents are given by vectors $\mathbf{i_b}$ and $\mathbf{v_b}$, respectively, Eq. 3.11 can be written in the following form

$$\Lambda'\{\mathbf{v_p^t}\}\ \Lambda''\{\mathbf{i_p}\} \quad = \quad \Lambda'\{\mathbf{v_b^t}\}\ \Lambda''\{\mathbf{i_b}\} \tag{3.12}$$

The Eq. 3.12 is very generic and has extensive range of applications. As a simple example, $\Lambda'\{\}$ and $\Lambda''\{\}$ can be considered as two operators that select voltage and current sets of the network from two different moments. For these types of operators, the resulting relationship is known as *quasi power* theorem.

Weak Forms of Tellegen's Theorem

If $\Lambda'\{\}$ and $\Lambda''\{\}$ are both Kirchhoff voltage operators and Kirchhoff current operators simultaneously, then a direct consequence of Eq. 3.12 will be

$$\Lambda''\{\mathbf{v_p^t}\}\ \Lambda'\{\mathbf{i_p}\} \quad = \quad \Lambda''\{\mathbf{v_b^t}\}\ \Lambda'\{\mathbf{i_b}\} \tag{3.13}$$

Adding or subtracting Eq. 3.12 and Eq. 3.13 gives rise to two different versions of Tellegen's theorem known as *weak forms*.

- **Sum form**

$$\Lambda'\{\mathbf{v_p^t}\}\Lambda''\{\mathbf{i_p}\} \ + \ \Lambda''\{\mathbf{v_p^t}\}\Lambda'\{\mathbf{i_p}\} \quad = \quad \Lambda'\{\mathbf{v_b^t}\}\Lambda''\{\mathbf{i_b}\} \ + \ \Lambda''\{\mathbf{v_b^t}\}\Lambda'\{\mathbf{i_b}\} \tag{3.14}$$

- **Difference form**

$$\Lambda'\{\mathbf{v_p^t}\}\Lambda''\{\mathbf{i_p}\} \ - \ \Lambda''\{\mathbf{v_p^t}\}\Lambda'\{\mathbf{i_p}\} \quad = \quad \Lambda'\{\mathbf{v_b^t}\}\Lambda''\{\mathbf{i_b}\} \ - \ \Lambda''\{\mathbf{v_b^t}\}\Lambda'\{\mathbf{i_b}\} \tag{3.15}$$

Reciprocity

The concept of reciprocity and reciprocity theorem are extensively used in sensitivity analysis. Therefore they are briefly explained here.

An LTI m-port network is said to be *reciprocal* iff

$$\mathbf{V_p^t}\ \tilde{\mathbf{I}}_\mathbf{p} \ = \ \tilde{\mathbf{V}}_\mathbf{p}^\mathbf{t}\ \mathbf{I_p} \tag{3.16}$$

in which $(\mathbf{V_p}, \mathbf{I_p})$ and $(\tilde{\mathbf{V}}_\mathbf{p}, \tilde{\mathbf{I}}_\mathbf{p})$ are port voltage-current phasor sets of the network for two experiments with different excitations, provided that the frequency of excitation be equal for both experiments.

Reciprocity theorem states that a network consisting of reciprocal elements is itself reciprocal, which is easily proved using Tellegen's theorem and the definition of a reciprocal element [33].

It should be emphasized that many network elements, but not all of them, are reciprocal. Gyrators are one of those elements which are *not* reciprocal.

3.1.2 Orchard's Theorem

The theorem that Orchard presented with a qualitative proof [30], has left an enormous impact on the design of real-life electrical filters. For more than a decade before his argument, there was an extensive search for inductor-less filters, and this had made cascade active filters a hot topic. Nevertheless, the researchers had never been able to realize precise filters. No matter how careful the design had been done, still the final frequency response used to experience major deviations from the desired output. But ever since the introduction of his argument, the doubly terminated filters with points of maximum power transfer in their pass-band has been the premier choice for designers, and their attempts have been focused on finding different methods to simulate the behavior of this type of networks.

Orchard's theorem, in its comprehensive form [31], states that for any two port network, the sensitivity of the filter insertion loss to the variations of reactive element values, at points where maximum power transfer to the load occurs, is zero.

This is quite general and may include even networks with dissipative elements, like resistors. Therefore, the essence of this argument is not based on zero loss, rather on the condition of having maximum power transfer. And a direct corollary of this theorem is that it is *not* applicable to *singly terminated* filters, since for these networks there is no upper bound for power transfer, so that the condition of maximum power transfer will never satisfy.

His argument is based on the fact that if there exists a point of maximum power transfer, i.e., a point where the filter neither reflects back any portion of the input power nor consumes any part of that, any changes in element values, including source or load immittances, if any, will only cause reflection or consumption of a portion of the power. In other words, a change, increase or decrease, in an element value, causes the condition of

maximum power transfer to be disturbed. This basically stands for a quadratic relationship between element values and the filter loss function. Conclusively, the first derivative of filter loss function with respect to any element value, at points that the condition of maximum power transfer exist, is zero.

Quite opposite, the sensitivity of cascade filters' loss to element value variations is very high, so that regardless of how much care has been taken in the design process, the frequency response may never be accurate due to these unwilling deviations.

3.1.3 Sensitivity Formulas for Reciprocal Lossless Two-Ports

The formulas derived in [32], express the sensitivity of transducer coefficient $\theta(j\omega)$ (Eq. 3.2) of singly or doubly terminated, reciprocal lossless two-ports in terms of some parameters of the network which are mainly stored reactive power, reflection coefficient and the power delivered to the load.

For the doubly terminated case which is of our main interest, deviations of transducer coefficient in terms of tolerance of reactive elements—inductors and capacitors—in the network is given by

$$\Delta\theta \;=\; \sum_i \frac{|I_i|^2 \,+\, \rho_1^* \, I_i^2}{2\,P_2}\, L_i\, \Delta z_i + \sum_j \frac{|V_j|^2 \,-\, \rho_1^* \, V_j^2}{2\,P_2}\, C_j\, \Delta y_j \tag{3.17}$$

where Δz_i and Δy_j are the relative tolerances of inductor impedance and capacitor admittance, respectively, as given by

$$\Delta z_i \;=\; \frac{\Delta r_i}{L_i} + j\omega \frac{\Delta L_i}{L_i} \tag{3.18}$$

$$\Delta z_i \;=\; \frac{\Delta g_j}{C_j} + j\omega \frac{\Delta C_j}{C_j} \tag{3.19}$$

As it is seen, Eq. 3.17 takes into account even small parasitic dissipations of reactive elements. Moreover, Orchard theorem for the reactive components can be easily derived from this relationship. At points where the maximum power transfer exist, i.e., the reflection coefficient ρ_1 in Eq. 3.17 is zero, and the component tolerance is restricted to variations of reactive elements, ΔL_i and ΔC_j in Eq. 3.18, transducer coefficient will contain only complex deviations from its nominal value—$\Delta\theta$ is pure complex in Eq. 3.17—which basically stands for attenuation keeping its nominal value to a first order approximation.

For the case of variations of either terminating resistances, the interested reader is referred to [31].

Chapter 4

Op-Amp Non-Ideality Effects on Bilinear Differential SC Integrator

4.1 Introduction

The effects of op-amp non-idealities on SC filter characteritics have been studied for the single-ended integrators of Sec. 2.5.2 in [27].

Nevertheless, certain issues lead us to generalize that work, so that it could address our own problem. They are summarized as follows:

- The circuit under the investigation of this thesis is fully differential and the integrators are bilinear ones.
- The effect of op-amp input capacitance has not been considered in [27] and as it will be seen shortly this in fact has profound outcomes with regard to the characteristics of the integrtor.
- The analysis in [27], considers two different models for the operational amplifier; one for very low frequencies neglecting any frequency dependency of the op-amp TF and the other for very high frequencies neglecting the finite gain of the amplifier. Nevertheless, the subtlity lies in the fact that the major deviations of the filter TF from the ideal case happens at the edge of pass-band, and for our case as it will be seen in Sec. 5.1, this is in fact comparable to the BW of the op-amp. For frequencies around the BW of the op-amp, neither the effect of finite BW nor the effect of finite gain can be neglected. This is based on the fact that the differential equation which

describes the input-output relationship of the op-amp, i.e., Eq. 4.2 is very vulnerable to the variations of its coefficients for input signal with frequencies around op-amp's BW. As a result these two non-idealities can not be separated in order to obtain precise knowledge of the sensitivity of the total SC filter.

Based on the foregoing discussion, a detailed derivation of the respective formulas is given in the following section.

4.2 Derivation of Formulas

First order frequency response of an operational amplifier with DC gain A_0 and bandwidth ω_B is given by

$$\frac{V_o}{V_p} \;=\; \frac{A_0}{1 \,+\, j\omega/\omega_B} \tag{4.1}$$

which in time domain the corresponding differential equation is

$$\frac{dv_o}{dt} \;+\; \omega_B v_o \;=\; A_0\,\omega_B\,v_p \tag{4.2}$$

Writing the KCL during phase Φ_1

$$C_p\frac{dv_p^-}{dt} \,+\, C_i\frac{dv_p^-}{dt} \;=\; C_i\frac{dv_o^+}{dt} \tag{4.3}$$

$$C_p\frac{dv_p^+}{dt} \,+\, C_i\frac{dv_p^+}{dt} \;=\; C_i\frac{dv_o^-}{dt} \tag{4.4}$$

Subtracting Eq. 4.4 from Eq. 4.3 gives rise to

$$-\left(1 \,+\, \frac{C_p}{C_i}\right)\frac{dv_p}{dt} \;=\; \frac{dv_o}{dt} \tag{4.5}$$

KCL should also be written during clock phase Φ_2 for the top section

$$(C_i \,+\, C_p \,+\, C_r)\,\frac{dv_p^-}{dt} \;=\; C_i\frac{dv_o^+}{dt} \,+\, C_r\frac{dv_i^-}{dt} \tag{4.6}$$

$$(C_i \,+\, C_p \,+\, C_r)\,\frac{dv_p^+}{dt} \;=\; C_i\frac{dv_o^-}{dt} \,+\, C_r\frac{dv_i^+}{dt} \tag{4.7}$$

And by subtracting Eq. 4.7 from Eq. 4.6

$$-\left(1 + \frac{C_p + C_r}{C_i}\right)\frac{dv_p}{dt} = \frac{dv_o}{dt} \tag{4.8}$$

A comparison of Eq. 4.5 and Eq. 4.8 shows that during both phases of clock, KCL results in equations in the following general form

$$-(1 + \alpha_k)\frac{dv_p}{dt} = \frac{dv_o}{dt} \tag{4.9}$$

where α_k is given by

$$\alpha_1 = \frac{C_p}{C_i} \qquad \text{during phase } \phi_1 \tag{4.10}$$

$$\alpha_2 = \frac{C_p + C_r}{C_i} \qquad \text{during phase } \phi_2 \tag{4.11}$$

Therefore the following two first order differential equations—given by Eq. 4.2 and Eq. 4.9—determines the evolution of op-amp's input and output voltages.

$$\frac{dv_o}{dt} + \omega_B v_o = A_0 \omega_B v_p \tag{4.12}$$

$$-(1 + \alpha_k)\frac{dv_p}{dt} = \frac{dv_o}{dt} \tag{4.13}$$

By differentiating we get

$$-(1 + \alpha_k)\frac{d^2v_p}{dt^2} = \frac{d^2v_o}{dt^2} \tag{4.14}$$

$$\frac{d^2v_o}{dt^2} + \omega_B\frac{dv_o}{dt} = A_0\omega_B\frac{dv_p}{dt} \tag{4.15}$$

Putting 4.9 and 4.14 into 4.15 gives rise to

$$\frac{d^2v_p}{dt^2} + \left(1 + \frac{A_0}{1 + \alpha_k}\right)\frac{dv_p}{dt} = 0 \tag{4.16}$$

Normally

$$\frac{A_0}{1 \; + \; \alpha_k} \ll 1 \tag{4.17}$$

so that Eq. 4.16 can be written in the form

$$\frac{d^2 v_p}{dt^2} \; + \; \omega_{t,k} \, \frac{dv_p}{dt} \; = \; 0 \tag{4.18}$$

where $\omega_{t,k}$ is *effective unity-gain frequency* of the op-amp during clock phase ω_k, defined as follows

$$\omega_{t,k} \; \stackrel{\Delta}{=} \; \frac{\omega_B \, A_0}{1 \; + \; \alpha_k} \tag{4.19}$$

The evolution equation (Eq. 4.18) of the input node of the op-amp has the following solution

$$v_p(t) \; = \; C_0 \; + \; C_1 \, e^{-\omega_{t,k} \, t} \tag{4.20}$$

in which initial values are given by

$$v_p|_{t=0^+} \; = \; C_0 \, + \, C_1 \tag{4.21}$$

$$\left. \frac{dv_p}{dt} \right|_{t=0^+} \; = \; -C_1 \, \omega_{t,k} \tag{4.22}$$

Using Eq. 4.2 and Eq. 4.9 and Eq. 4.22 we get

$$C_1 \, \omega_{t,k} \; = \; \frac{A_0 \, \omega_B}{1 \; + \; \alpha_k} \; v_p|_{t=0^+} \; - \; \frac{\omega_B}{1 \; + \; \alpha_k} \; v_o|_{t=0^+} \tag{4.23}$$

Using the definition of $\omega_{t,k}$ (Eq. 4.19) into Eq. 4.23 and then applying the result to Eq. 4.21, C_0 and C_1 are obtained as follows

$$C_0 \; = \; \frac{1}{A_0} \; v_o|_{t=0^+} \tag{4.24}$$

$$C_1 \; = \; v_p|_{t=0^+} \; - \; \frac{1}{A_0} \; v_o|_{t=0^+} \tag{4.25}$$

Assuming that the output voltage of the operational amplifier does not jump—since it acts as an integrator—or in other words

$$v_o|_{t=0^+} = v_o|_{t=0} \tag{4.26}$$

and considering the fact that equations 4.24 and 4.25 are valid during both clock phases, the following relationship will be obtained

$$\text{during clock phase } \phi_1 \qquad C_0 = \frac{1}{A_0}\, v_o[n-1] \tag{4.27}$$

$$C_1 = v_p[n-1] - \frac{1}{A_0}\, v_o[n-1] \tag{4.28}$$

$$\text{during clock phase } \phi_2 \qquad C_0 = \frac{1}{A_0}\, v_o[n-1/2] \tag{4.29}$$

$$C_1 = v_p[n-1/2]^+ - \frac{1}{A_0}\, v_o[n-1/2] \tag{4.30}$$

Consequently the values of v_p at the moments of transition will be

$$v_p[n-1/2]^- = \frac{1}{A_0}\left(1 - e^{-\omega_{t,1}\,T/2}\right) v_o[n-1] + e^{-\omega_{t,1}\,T/2}\, v_p[n-1] \tag{4.31}$$

$$v_p[n] = \frac{1}{A_0}\left(1 - e^{-\omega_{t,2}\,T/2}\right) v_o[n-1/2] + e^{-\omega_{t,2}\,T/2}\, v_p[n-1/2]^+ \tag{4.32}$$

It is worthwhile mentioning that at the moment of transition from ϕ_2 to ϕ_1, v_p experiences no voltage jump, so that

$$v_p[n-1]^+ = v_p[n-1]^- = v_p[n-1] \tag{4.33}$$

In order to obtain $v_o(t)$, Eq. 4.2 can be solved using the known $v_p(t)$, but since we are mainly interested in the boundary values of these voltage variables at the moments of transitions, we can directly integrate Eq. 4.9 to get

$$-(1+\alpha_k)\left[v_p(t) - v_p|_{t=0^+}\right] = \left[v_o(t) - v_o|_{t=0^+}\right] \tag{4.34}$$

which results in

$$-(1+\alpha_k)\left(v_p[n-1/2]^- - v_p[n-1]\right) = (v_o[n-1/2]-v_o[n-1]) \quad (4.35)$$

$$-(1+\alpha_k)\left(v_p[n]-v_p[n-1/2]^+\right) = (v_o[n-1/2]-v_o[n-1/2]) \quad (4.36)$$

Also, in order to find the relationship between the values of v_p, just before and after of switching from ϕ_1 to ϕ_2, the following equation—based on charge conservation principle—can be written

$$\sum \Delta q = 0 \quad (4.37)$$

$$\Delta q_p + \Delta q_i + \Delta q_r = 0 \quad (4.38)$$

in which

$$\Delta q_p = C_p\left(-v_p^-[n-1/2]^+ + v_p^-[n-1/2]^-\right) \quad (4.39)$$

$$\Delta q_i = C_i\left[\left(v_o^+[n-1/2]-v_p^-[n-1/2]^-\right)-\left(v_o^-[n-1/2]-v_p^-[n-1/2]^+\right)\right] \quad (4.40)$$

$$\Delta q_r = C_r\left[\left(v_i^-[n] - v_p^-[n-1/2]^-\right) - v_i^+[n-1]\right] \quad (4.41)$$

Based on this and also an equation derived in a similar way for the second input node of the op-amp, the following relationships are obtained

$$(C_i+C_p+C_r)\,v_p^-[n-1/2]^+ - (C_i+C_p)\,v_p^-[n-1/2]^- = C_r\left(v_i^-[n] - v_i^+[n-1]\right) \quad (4.42)$$

$$(C_i+C_p+C_r)\,v_p^+[n-1/2]^+ - (C_i+C_p)\,v_p^+[n-1/2]^- = C_r\left(v_i^+[n] - v_i^-[n-1]\right) \quad (4.43)$$

And subtracting Eq. 4.42 from Eq. 4.43 gives rise to

$$C_r\,(v_i[n]+v_i[n-1]) = (C_i+C_p+C_r)\,v_p[n-1/2]^+ - (C_i+C_p)\,v_p[n-1/2]^- \quad (4.44)$$

It is necessary to mention that it has been assumed that input signal v_i changes only once per clock cycle at the beginning of clock phase ϕ_2; and $[n-1/2]^+$ refers to the moment after the settlement of the input signal.

In order to simplify the notations, the following variables are defined

$$p_1 \triangleq v_p[n-1] \tag{4.45}$$
$$p_2 \triangleq v_p[n-1/2]^- \tag{4.46}$$
$$p_3 \triangleq v_p[n-1/2]^+ \tag{4.47}$$
$$p_4 \triangleq v_p[n] \tag{4.48}$$
$$x \triangleq v_o[n-1/2] \tag{4.49}$$

Also k_1 and k_2 are defined as follows

$$k_1 \triangleq \omega_{t,1}\, T/2 \tag{4.50}$$
$$k_2 \triangleq \omega_{t,2}\, T/2 \tag{4.51}$$

Using equations 4.45–4.51 into 4.31, 4.32, 4.35, 4.36, and 4.44 the following 5-th order system of linear equations describes the relationship between the boundary values of voltage variables v_i, v_p and v_o

$$p_2 = \frac{1}{A_0}\left(1 - e^{-k_1}\right) v_o[n-1] + e^{-k_1}\, p_1 \tag{4.52}$$
$$p_4 = \frac{1}{A_0}\left(1 - e^{-k_2}\right) v_o[n-1] + e^{-k_2}\, p_3 \tag{4.53}$$
$$-(1+\alpha_1)\, p_2 + (1+\alpha_1)\, p_1 = x - v_o[n-1] \tag{4.54}$$
$$-(1+\alpha_2)\, p_4 + (1+\alpha_2)\, p_3 = v_o[n-1] - x \tag{4.55}$$
$$(1+\alpha_2)\, p_3 - (1+\alpha_1)\, p_2 = \frac{C_r}{C_i}\,(v_i[n] + v_i[n-1]) \tag{4.56}$$

Our goal is to eliminate intermediate variables p_2, p_3, and x. Since there exist five equations, after elimination of these three variables, there will be two independent relations between six variables p_1, p_4, $v_i[n-1]$, $v_i[n]$, $v_o[n-1]$, and $v_o[n]$. The Z transform neglects the effect of initial conditions, i.e., the transformation of p_4 is related to the transform of p_1, so that finally there will be two independent equations in Z domain with three variables, and by the elimination of V_p a relationship between V_o and V_i will be obtained.

Adding 4.54 to 4.55 gives rise to

$$-(1 + \alpha_1)\, p_2 \;+\; (1 + \alpha_1)\, p_1 \;-\; (1 + \alpha_2)\, p_4 \;+\; (1 + \alpha_2)\, p_3 \;=\; v_o[n] \;-\; v_o[n-1] \tag{4.57}$$

and by using Eq. 4.56 into Eq. 4.57 we get

$$\frac{C_r}{C_i}\,(v_i[n] + v_i[n-1]) \;+\; (1 + \alpha_1)\, p_1 \;-\; (1 + \alpha_2)\, p_4 \;=\; v_o[n] \;-\; v_o[n-1] \tag{4.58}$$

In addition to this relationship, we need one other in which the variables p_2, p_3 and x have been eliminated.

Substituting in Eq. 4.53 from Eq. 4.54 for x gives

$$p_4 \;=\; \frac{1}{A_0}\,(1 - e^{-k_2})\,[-(1 + \alpha_1)\, p_2 \;+\; (1 + \alpha_1)\, p_1 \;+\; v_o[n-1]] \;+\; e^{-k_2}\, p_3 \tag{4.59}$$

On the other hand, multiplying Eq. 4.56 by factor $\exp(-k_2)$ and employing Eq. 4.53 we get

$$(1 + \alpha_2)\,\left[p_4 \;-\; \frac{1}{A_0}\,(1 - e^{-k_2})\, x\right] \;-\; (1 + \alpha_1)\, e^{-k_2}\, p_2 \;=\; e^{-k_2}\,\frac{C_r}{C_i}\,(v_i[n] + v_i[n-1]) \tag{4.60}$$

Using Eq. 4.54 into this relationship, we get

$$\begin{aligned}(1 + \alpha_2) \quad & \left[p_4 \;-\; \frac{1}{A_0}\,(1 - e^{-k_2})\,((1 + \alpha_1)\,(p_1 - p_2) + v_o[n-1])\right] \\ - \qquad & (1 + \alpha_1)\, e^{-k_2}\, p_2 \;=\; e^{-k_2}\,\frac{C_r}{C_i}\,(v_i[n] + v_i[n-1])\end{aligned} \tag{4.61}$$

And by using Eq. 4.52 we can substitute for $(p_1 - p_2)$ as well as p_2 to get

$$-\beta_1\, p_1 \;+\; \beta_2\, v_o[n-1] \;=\; e^{-k_2}\,\frac{C_r}{C_i}\,(v_i[n] + v_i[n-1]) \tag{4.62}$$

in which

$$\beta_1 \;=\; (1 \,+\, \alpha_1)\,\left[\frac{1}{A_0}\,(1 \,+\, \alpha_2)\,(1 \,-\, e^{-k_1})\,(1 \,-\, e^{-k_2}) \;\;+\;\; e^{-(k_1+k_2)}\right] \tag{4.63}$$

$$\begin{aligned}\beta_2 \;=\; \frac{1}{A_0}\,\{ & \\ & \frac{1}{A_0}\,(1 \,+\, \alpha_1)\,(1 \,+\, \alpha_2)\,(1 \,-\, e^{-k_1})\,(1 \,-\, e^{-k_2}) \;\; - \\ & \left[(1 \,+\, \alpha_1)\,(1 \,-\, e^{-k_1})\,e^{-k_2} \,+\, (1 \,+\, \alpha_2)\,(1 \,-\, e^{-k_2})\right]\}\end{aligned} \tag{4.64}$$

Taking Z transforms of Eq. 4.62 and Eq. 4.58

$$-\beta_1\,V_p \;+\; \beta_2\,V_o \;=\; e^{-k_2}\,\frac{C_r}{C_i}\,(z \,+\, 1)\,V_i \tag{4.65}$$

$$\frac{C_r}{C_i}\,(z \,+\, 1)\,V_i \;-\; [(1 \,+\, \alpha_2)\,z \,-\, (1 \,+\, \alpha_1)]\;V_p \;=\; (z \,-\, 1)\,V_o \tag{4.66}$$

and solving for V_o/V_i gives rise to

$$\frac{V_o}{V_i} \;=\; \frac{C_r}{C_i}\,\frac{z \,+\, 1}{z \,-\, 1}\,H_n(z) \tag{4.67}$$

$$H_n(z) \;=\; \frac{1 \;+\; \dfrac{e^{-k_2}}{\beta_1}\;[(1 \,+\, \alpha_2)\,z \,-\, (1 \,+\, \alpha_1)]}{1 \;+\; \dfrac{1}{z \,-\, 1}\dfrac{\beta_2}{\beta_1}\;[(1 \,+\, \alpha_2)\,z \,-\, (1 \,+\, \alpha_1)]} \tag{4.68}$$

Function H_n determines the phase and amplitude deviations from the ideal bilinear integrator due to finite gain, finite bandwidth and input capacitance of the operational amplifier.

Once the phase and amplitude deviations of the integrator are known through H_n, the realations presented in Sec. 3.1.3 or Blostein's formulas [2] can be employed to estimate the variations of overal filter TF w.r.t non-idealities of constituting operational amplifiers.

Chapter 5

Design of a CDMA SC Channel Select Filter

5.1 Filter Bandwidth and Clock Frequency

CDMA channel selection requires very selective as well as linear filtering. Phase linearity is also of extreme importance. The filter designed in this work is based on the first two categories. In order to have sharp filtering, a 7-th order elliptic transfer function is selected and to increase the linearity performance of the filter, SC technique has been employed in the common-mode feedback (CMFB) circuitry of the differential operational amplifiers, as it will be seen later.

The bandwidth of the filter is 612 kHz, based on IS-95 CDMA specifications [11].

$$f_{BW} \;=\; 612 \text{ kHz} \tag{5.1}$$

Since the filter is a SC one, the second major parameter is the clock frequency, as all the frequency specifications are relative to that frequency. The selection of clock frequency is somewhat arbitrary, although an upper bound and a lower bound limits the range of frequencies which can be selected for the clock signal.

Quite interestingly, the upper bound is determined by circuit limitations, whereas the lower bound is specified solely by the system specifications.

Having higher clock frequency stands for shorter time period between two consecuitve edges of the clock pulse. In other words, when the clock edge triggers the switches of the integrators, shorter period of time is available for the otuput of the integrator to reach

to its final value. This issue, known as the *settling time* of the integrator depends on the unity gain frequency of the operational amplifier.

On the other hand, since SC fitlers are DT circuits, before sampling the input signal, it has to be band-limited. Moreover, SC filters have periodic frequency response with a period equal to clock frequency f_c. As a result the band-limiting circuit or so called *anti-aliasing filter* must show considerable attenuation at frequencies around f_c.

CDMA band has frequencies up to 25 MHz, therefore to satisfy the aforementioned requirement, the clock frequency f_c has to be higher than this vaule. The higher the clock frequency, the simpler the realization of anti-aliasing filter will be.

In addition, the othe factor affecting the lower bound of the clock frequency is posed by the degradation due to the frequency response of the S/H block at the input of the SC filter which is given by $\text{sinc}(\pi f/f_c)$. As f_c decreases, the effect of sinc function becomes more apparant. It is obvious that S/H effect is only important for frequencies lying in the BW of the filter, and it shows its largest degradation at the BW edge. For LP filters this is in fact the bandwidth frequency f_{BW}, which in this case is 612 kHz. For a ratio of f_c, 50 times higher than f_{BW}, the effect of sinc function is less than 0.1%. This results in frequencies equal or higher than 30 MHz which in fact satisfy the requirements imposed by the anti-aliasing filter, as stated earlier.

Now that the range of clock frequency is known, the remaining task will be the determination of the exact value of f_c. For this task, again the sepecifications of CDMA comes into place. The carrier frequency of the CDMA base station is 1930 MHz. The direct conversion receiver will generate this frequency in order to extract the frequency band of interest. Therefore assuming that an accurate clock at the frequency of the carrier is already available in the system, it is highly desirable to generate the required clock signal of the SC channel selection filter using this signal. To minimize the amount of circuitry required for this task, the ratio between frequencies of these two signals should be a power of 2. Ratios of 64 and 128 correspond to 30.15625 MHz and 15.078125 MHz, respectively. The former is in fact 49.3 times the bandwidth frequency which is very close to 50, that was explained before. Consequently

$$f_c \;=\; 30.15625 \text{ MHz} \tag{5.2}$$

is chosen as the filter clock frequency.

5.2 CT Prototype Filter

Knowing the bandwidth and clock frequency of the filter, a CT prototype should be selected to satisfy these in addition to high selectivity requirements.

Elliptic fitlers provide the optimum selectivity, and obviously, increasing the order of the filter, improves its sharpness. Nevertheless, in practice, filters of the order of 8 or higher are seldom designed, otherwise the poles of the high order filter would be very close to the $j\omega$ axis, so that small variations of element values or parasitic effects might cause them to fall into the righ half plane and result in unstability. On the other hand from filter theory it is known that an 8th order elliptic filter has also its maximum pass-band loss at DC. This is indeed quite undesired. To avoid this problem, the filter order is selected as 7.

Considering the fact that the ratio of clock frequency over filter bandwidth is around 50, in order to obtain a maximum attenuation of less than 1% throughout the filter pass-band, the reflection coefficient ρ is selected to be 10%—corresponding to 0.044 dB attenuation. Therefore the maximum attenuation in pass-band due to intrinsic properties of the elliptic filter as well as the effect of S/H block is given by

$$1 \; - \; 10^{-0.044/20}\,\mathrm{sinc}(\pi\frac{f_{BW}}{f_c}) \; = \; 1 - 0.994273 \; \simeq \; 0.57\,\% \tag{5.3}$$

The last parameter which has to be known to uniquely specify the filter is the modular angle θ. It basically represents the trade-off between fitler sharpness and rejection of the out of band signals. The higher the value of θ, the smaller the transit band of the filter will be, but the lower value of θ means, the larger the out of band attenuation.

CDMA channel filter must have more than 50 dB attenuation for frequencies higher than 800 kHz, therefore the ratio between stop-band (f_{SB}) and pass-band (f_{BW}) frequencies of the prototype filter is determined by applying pre-warping (Eq. 2.13) and given by

$$\frac{\omega_{ct,SB}}{\omega_{ct,PB}} \; = \; \frac{f_{ct,SB}}{f_{ct,PB}} \; = \; \frac{\tan(\pi\, f_{BW}/f_c)}{\tan(\pi\, f_{SB}/f_c)} \; = \; 1.3084 \tag{5.4}$$

A value of 52° for θ is a good choice for the modular angle of the prototype elliptic filter, since it provides slightly more than 53 dB rejection of out of band frequencies, while the transit band is less than 27 % of the filter bandwidth which meets the requirement of Eq. 5.4.

Therefore, the CT prototype filter is a doubly terminated elliptic one with the following specifications

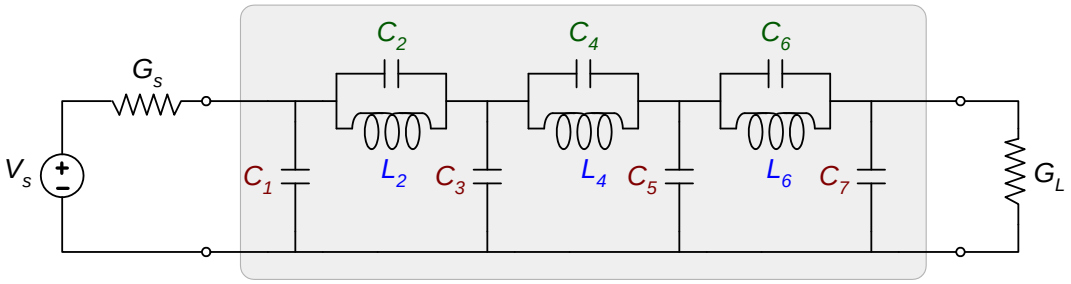

Figure 5.1: CT prototype filter: Doubly terminated 7th-order LP elliptic

$$n = 7 \tag{5.5}$$

$$\rho = 10\,\% \tag{5.6}$$

$$\theta = 52° \tag{5.7}$$

Realization of this filter is a classical problem and the element values can be found in any filter handbook [40].

The normalized prototype filter has the structure shown in Fig. 5.1 and the element values are given in Table 5.1.

As it can be seen in Fig. 5.1 capacitors in series branches form complete loops with their two adjacent capacitors in parallel branches, so that based on circuit theory their voltage variables are not independent of each other. On the other hand realization of the admittance of every series branch in this form results in a rather complicated circuit. To combat this problem, a simple modification to the circuit which is explained by the following example results in a new network that can easily be realized by 7 integrators. This stands for 4 varialbes, (v_1, v_3, v_5, and v_7), corresponding to every capacitor in each parallel branch and 3 variables, (i_2, i_4, and i_6) corresponding to every inductor current in each series branch.

Writing KCL at the node which consists of capacitor C_3 gives rise to

$$C_3 s\, v_3 = i_2 + C_2 s\,(v_1 - v_3) - i_4 - C_4 s\,(v_3 - v_5) \tag{5.8}$$

G_s	1
C_1	0.90504
C_2	0.13022
L_2	1.28752
C_3	1.44739
C_4	0.63601
L_4	0.94676
C_5	1.28991
C_6	0.47479
L_6	0.94158
C_7	0.65382
G_L	1

Table 5.1: CT prototype filter element values

Solving for v_3 results in

$$v_3 = \frac{(i_2 - i_4) + (C_2\, s\, v_1 + C_4\, s\, v_4)}{(C_2 + C_3 + C_4)\, s} \tag{5.9}$$

In a similar way the TFs of the rest of voltage variables can be calculated as follows

$$v_1 = \frac{(i_s - i_2) + C_2\, s\, v_2}{(C_1 + C_1)\, s + G_s} \tag{5.10}$$

$$v_5 = \frac{(i_4 - i_6) + (C_4\, s\, v_4 + C_6\, s\, v_6)}{(C_4 + C_5 + C_6)\, s} \tag{5.11}$$

$$v_7 = \frac{i_6 + C_5\, s\, v_5}{(C_6 + C_7)\, s + G_l} \tag{5.12}$$

The consequence of this modification on the circuit implementation is twofold. First, in every integrator which simulate the nodal voltage of every parallel capctior, the effective integrating capacitor is the sum of the corresponding capacitor in the CT prototype filter as well as its two adjacent series capacitors. Second, there exists direct coupling between every

voltage variable and its two adjacent voltage variables. The possibility of the realization of the latter is indeed a unique property of SC cirvuits, since they can simultaneously deal with DT and CT signals [20]. A very delicate and important consequence of this property is the fact that although the direct realization of true DT filters using bilinear integrtors is not possible [4] [7]—due to the necessity for delay free loops, yet they can easily be implemented using SC technique.

Moreover the implementation of the filter with the source in its original form requires an extra voltage variable, but by changing the source into its Thevenin equivalent circuit, the source resistance can be absorbed into capacitor C_1, so that their equivalent impedance can easily be implemented by the damped integrator presented in Sec. 2.5.4. The load resistance is also absorbed into capacitor C_7 in a similar way.

5.3 Filter SFG and DR optimization

Based on the discussions presented in Sec. 2.6.2, in order to obtain a a DR optimized SFG suitable for realization with SC bilinear differential integrators, the maximum value of state variables—voltages of parallel capacitors and currents of inductors in this case—of the prototype filter in Fig. 5.1, must be measured. This is done and they can be found in Table 5.2. Based on these extremums, the scaling factors α_i have been calculated according to Eq. 2.104 and Eq. 2.105 and are given in Table 5.3–5.4.

Overal gain factor K can also be calculated using Eq. 2.106. A value of 2 has been chosen for k_0, in order to compensate for the half gain drop of doubly terminated filters.

$$K \;=\; 2 \times \frac{0.5}{0.989898} \;=\; 1.01020509 \tag{5.13}$$

Using Eq. 5.9–5.12 and element values of the prototype filter from Table 5.1, the capacitor ratios of Table 5.5 can easily be calculated. It should be noted that in this table, $C_{k,k}$ represents the integrating capacitor of every stage. $C_{k,k-1}$ and $C_{k,k+1}$ represent the equivalent SC resistors that transmit signals to stage k, from the outputs of stages $k-1$ and $k+1$, respectively. Capacitors $C_{k,k-2}$ and $C_{k,k+2}$ are direct coupling ones from the output of stages $k-2$ and $k+2$ to the input of stage k.

The next phase is to introduce scaling factors for DR optimization. This is done by applying scaling factors α_k from Table 5.4 to the third column of Table 5.5 and factors $1/\alpha_k$ to the elements of column 4, i.e., $C_{k,k+1}$. For direct coupling capacitors, the scaling factors of Table 5.4 have to be used, i.e., scaling factors $\alpha_k \alpha k + 1$ are applied to column 2,

and $1/(\alpha_k\alpha_{k+1})$ to column 5. Conclusively, all the signal paths from any node to any other one experience the same amount of gain. The equivalent SFG is depicted in Fig. 5.2.

Final capacitor ratios are derived from Table 5.6 by applying the frequency scaling factor

$$f_B \;=\; \tan(\pi f_{BW}/f_c) \;=\; \tan(\pi 0.612/30.15625) \;=\; 0.063844295 \qquad (5.14)$$

to the non-switched capcitors, i.e., columns 1, 2 and 5. The results are given in Table 5.7.

V_1	0.989898	0.177941
I_2	1.39743	0.169288
V_3	1.11832	0.166388
I_4	1.86657	0.164572
V_5	0.862783	0.161478
I_6	1.08103	0.160664
V_7	0.5	

Table 5.2: State variable's extremums of the CT prototype filter

	α_k	$1/\alpha_k$
$k = 1$	0.70837037	1.4116909
$k = 2$	1.24957973	0.80026906
$k = 3$	0.89913103	1.66908397
$k = 4$	2.16342927	0.46222912
$k = 5$	0.79811199	1.25295699
$k = 6$	2.16206	0.46252185

Table 5.3: Integrators' scaling factors for DR optimization

5.4 WATSCAD Simulation

Before implementing the electronic circuit of the obtained SFG, the capaciotr ratios should be tested to make sure that the functionality meets the required specifications. This task

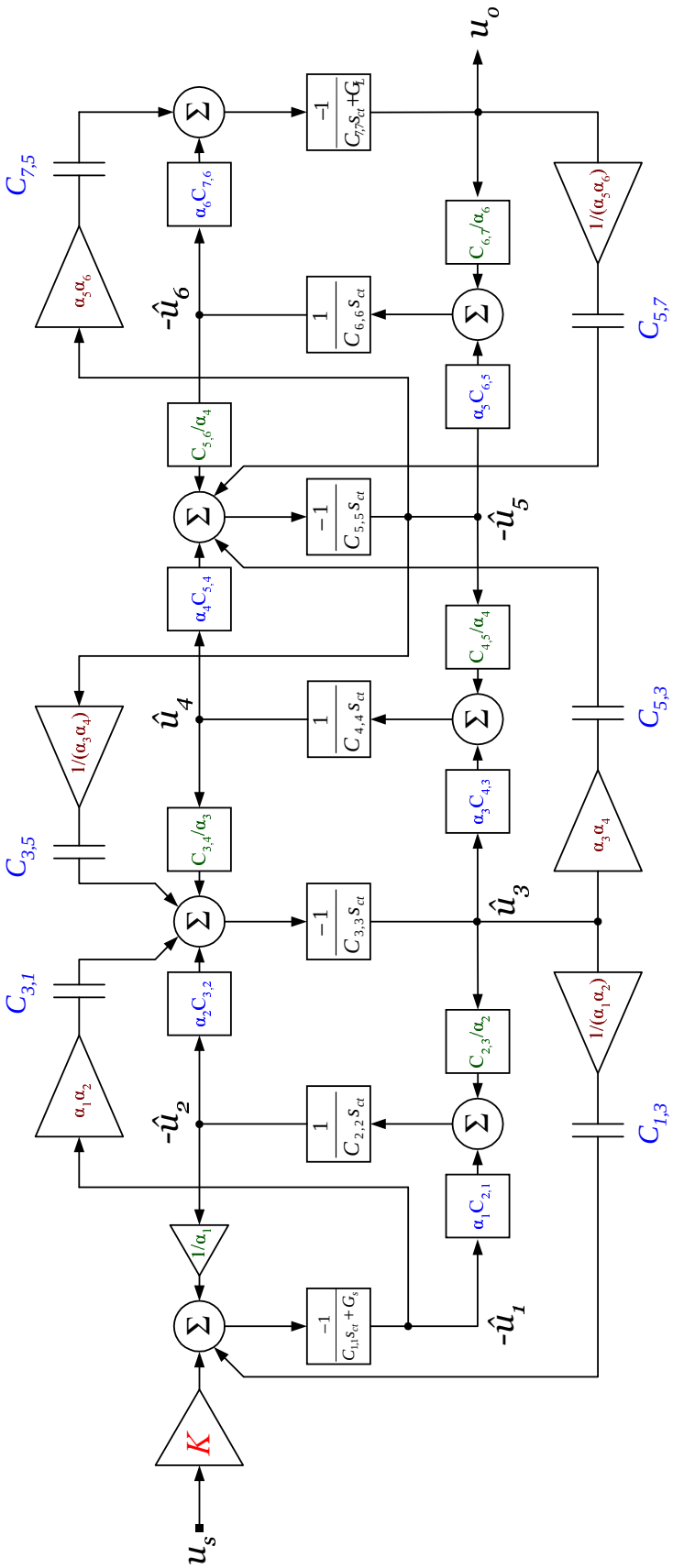

Figure 5.2: Final SFG: optimized for DR

	$\alpha_k\alpha_{k+1}$	$1/(\alpha_k\alpha_{k+1})$
$k = 1$	0.88516525	1.12973256
$k = 3$	1.29617760	0.77149921
$k = 5$	1.725566	0.57952

Table 5.4: Coupling capacitors' scaling factors for DR optimization

	$C_{k,k}$	$C_{k,k-2}$	$C_{k,k-1}$	$C_{k,k+1}$	$C_{k,k+2}$
stage 1	1.03526	0	1	1	0.13022
stage 2	1.28752	0	1	1	0
stage 3	2.21362	0.13022	1	1	0.63601
stage 4	0.94676	0	1	1	0
stage 5	2.40071	0.63601	1	1	0.47479
stage 6	0.94158	0	1	1	0
stage 7	1.12861	0.47479	1	0	0

Table 5.5: Primitive capacitor value ratios

	$C_{k,k}$	$C_{k,k-2}$	$C_{k,k-1}$	$C_{k,k+1}$	$C_{k,k+2}$
stage 1	1.03526	0	1.01020509	1.41169090	0.14711377
stage 2	1.28752	0	0.70837037	0.80026907	0
stage 3	2.21362	0.11526622	1.24957973	1.66908398	0.49068121
stage 4	0.94676	0	0.59913103	0.46222912	0
stage 5	2.40071	0.82438192	2.16342927	1.25295700	0.27515030
stage 6	0.94158	0	0.79811199	0.46252185	0
stage 7	1.12861	0.81928148	2.16206	0	0

Table 5.6: Capacitor value ratios: normalized pass-band frequency, optimized for DR

	$C_{k,k}$	$C_{k,k-2}$	$C_{k,k-1}$	$C_{k,k+1}$	$C_{k,k+2}$
stage 1	16.215729	0	15.823282	22.111930	2.3043071
stage 2	20.166988	0	11.095514	12.534963	0
stage 3	34.672895	1.8054651	19.572712	26.143590	7.6857537
stage 4	14.829514	0	9.3844503	7.2400960	0
stage 5	37.603367	12.912653	33.886735	19.625611	4.3097990
stage 6	14.748378	0	12.501176	7.2446813	0
stage 7	17.677910	12.832763	33.865288		0

Table 5.7: Final capacitor value ratios

can easily be done using WATSCAD program. The source code for the whole filter is given in App. A.

The transfer functions for intermediate state variables are depicted in Fig. 5.3, and as it is seen the maximum value of all of them is 1.

The overal desired TF is shown Fig. 5.4 and Fig. 5.5 which correspond to the required specifications.

The filter phase response is also shown in Fig. 5.6.

5.5 A Low-Voltage, High Performance Operational Amplifier

The main block of a SC filter is an *operational amplifier*. In this section the design procedure of a low-voltage, high performance op-amp which meets the required specifications for the final SC filter have been thoroughly discussed. This includes selecting a suitable topology, determination of the biasing currents, sizing of the transistors, and the design of a large dynamic range(DR) SC common-mode feedback (CMFB) circuitry. Following that, the op-amp will be fully characterized to obtain the lower as well the upper bounds of its different characteristics.

5.5.1 Op-Amp Sepcifications

In order to minimize the effect of op-amp finite bandwidth on the integrator characteristic, the *effective* unity gain frequency of the operational amplifier—as it is defined in Sec. 4.2—

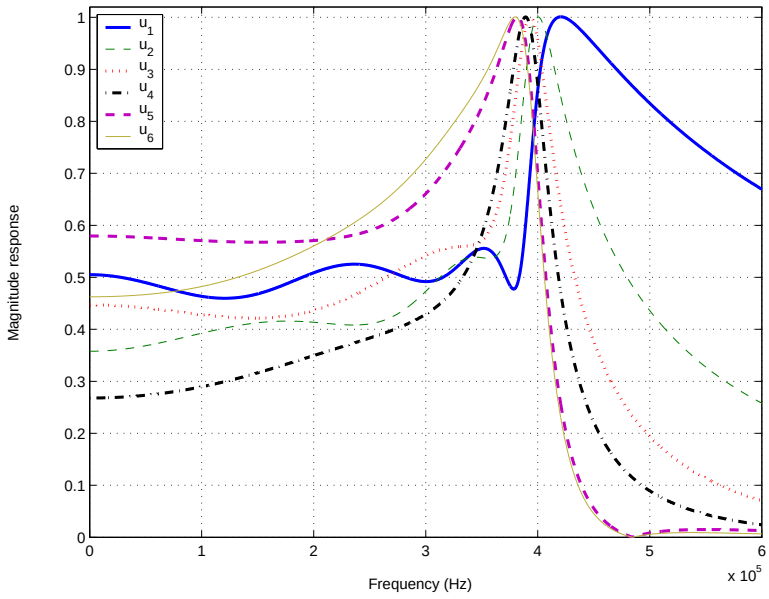

Figure 5.3: Magnitude response of internal SFG variables.

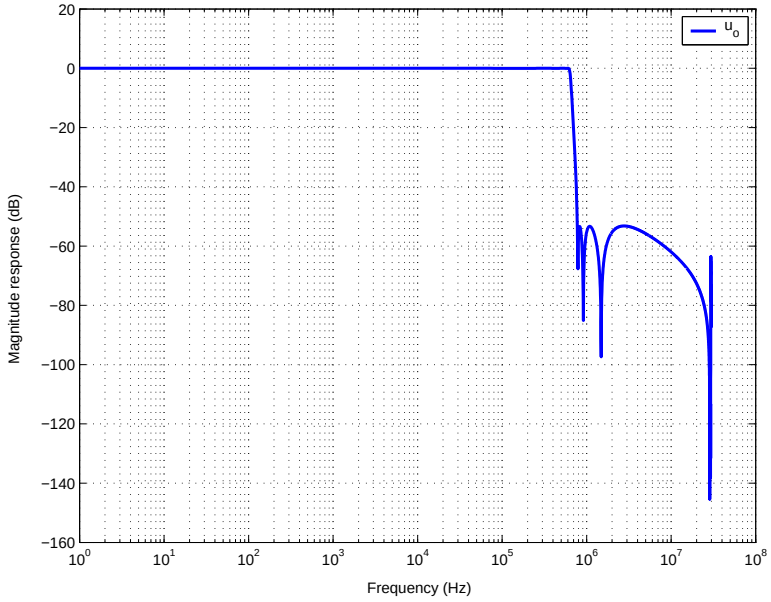

Figure 5.4: Overal TF for fruquencies close to f_c.

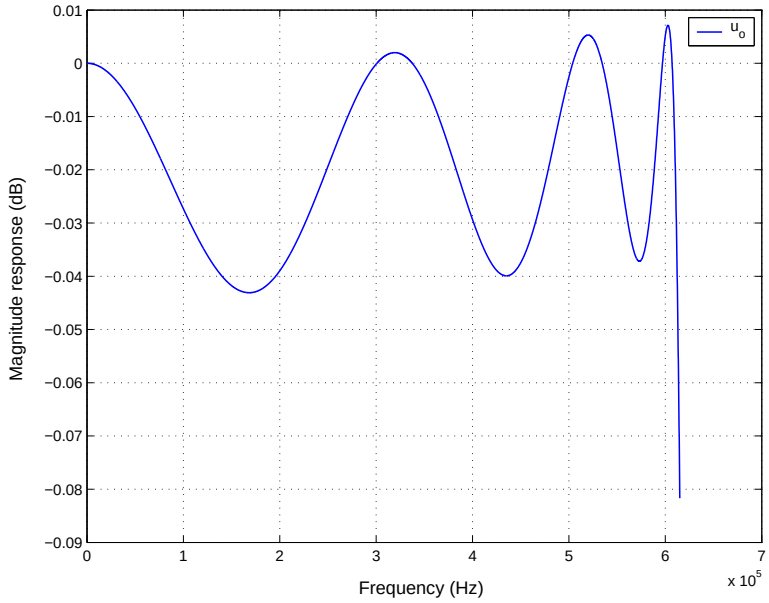

Figure 5.5: Overal TF in the pass-band.

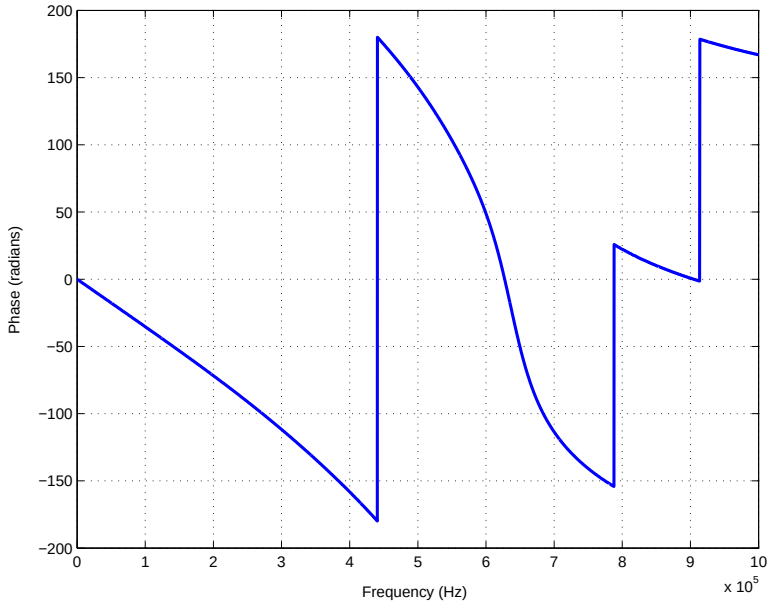

Figure 5.6: Phase response of the SC filter.

has to be a few times larger than the clock frequency—30 MHz in our case. This basically means the settling time of the op-amp is determined by the system clock.

Another parameter which is based on the clock frequency is the slew-rate (SR) performance. And it will be seen shortly, the limitations imposed on SR will determine the required biasing currents.

The fact that the final filter will be incorporated into a wireless transceiver also means that low-voltage as well as low-power design is inevitable. The implications of low-vlotage design itself are twofold:

- Utilizing stacked configurations is very limited, so that in order to obtain high DC gain, multiple stages must be cascaded.
- The second which is a subtle, yet very important problem is that, utitlizing low resistance ouput stages, i.e., source follower configuration—like the op-amp used in [29]—is very difficult for MOS threshold voltages around 0.5 V and power supplies less than 2 V.

This results in a high output resistance amplifier. If the dominant pole that determines the amplifier's bandwidth is placed at one of the internal nodes, this will be a major problem in terms of stability. This amplifier is utilized in a SC filter so that all the loads are capacitive. Having a high output resistance along with a totally capacitive load simply stands for a low frequency pole at the output node. The higher the load capacitance is, the closer this pole to the amplifier's dominant pole will be, resulting in major degradation in phase margin, so that eventually it might be totally unstable.

The problems discussed above require a multistage, high output resistance operational amplifier which has a dominant pole at the last stage, meanwhile showing a reasonable phase margin. In this case, the outcome of utilizing this amplifier in a SC filter will be an increase in load capacitance that simply stands for lower bandwidth as well as larger phase margin—better stability.

5.5.2 Amplifier Topology

A two-stage folded cascode structure with input PMOS transistors Fig. 5.7 can comply with all the aforementioned characteristics. This op-amp has a core cascode structure, M_1-M_6 and M_2-M_5 pairs, in addition to three cascade sub-blocks. They are M_{13}-M_{12}, M_7-M_9 and M_5-load pairs. The first one is a current source, the second one active load and the last one a voltage amplifier.

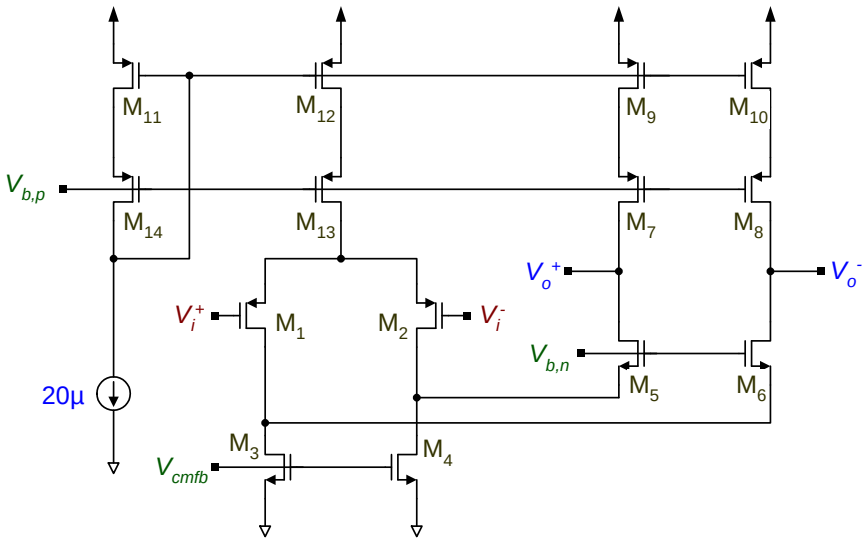

Figure 5.7: Op-Amp schematic

Following that, the properties of the cascade block and the cascode structure are quickly examined.

Cascade Block Properties

An NMOS cascade structure is shown in Fig. 5.8. The port of interest could be either source or drain as it is depicted in Fig. 5.9.

The structure in Fig. 5.9(a) is used as an enhanced active load where its output impedance is given by

$$r_o = r_{ds} + (1 + \frac{g_m}{g_{ds}}) r_L \simeq (1 + \frac{g_m}{g_{ds}}) r_L \simeq \frac{g_m}{g_{ds}} r_L \tag{5.15}$$

On the other hand, the structure in Fig. 5.9(b) is utilized as a voltage amplifier, where its voltage gain and its input admittance are given by

$$A_v = \frac{g_m + g_{ds}}{g_L + g_{ds}} \tag{5.16}$$

$$g_{in} \;=\; \frac{g_m \;+\; g_{ds}}{1 \;+\; g_{ds}/g_L} \tag{5.17}$$

For ($g_m \gg g_{ds}$)—which is usually the case unless either W/L ratio is very low or the drain-source voltage becomes very low—and ($g_{ds} \gg g_L$) they reduce to the followings

$$A_v \;\simeq\; \frac{g_m}{g_{ds}} \tag{5.18}$$

$$g_{in} \;\simeq\; \frac{g_m}{g_{ds}}\, g_L \;\simeq\; A_v \cdot g_L \tag{5.19}$$

The factor g_m/g_{ds} which has appeared in all the foregoing equations is the maximum gain that can be obtained from a transistor—when its load impedance approaches infinity—and called *intrinsic gain*. It is the key factor in having a high performance cascade structure, no matter whether it is to be used as an active load or as a voltage amplifier. As long as the load impedance is much higher than the output impedance of the buffer transistor, intrinsic gain plays the main role in the combined block.

In conclusion, to design a suitable cascade block, the optimum values of g_m and g_{ds} have to obtained. Transconductance g_m is determined by current handling and noise performance of the transistor, and then to reach to the desired intrinsic gain level, the channel length of the buffer transistor is increased, provided that the the aspect ratio remains constant. This basically means that after setting the g_m, both W and L are increased by a common factor.

Folded Cascode Structure

The advantages of the folded cascode structure are based on the following reasons

- PMOS transistors have lower $1/f$ noise.
- Having PMOS transistors at the input, makes setting the input CM voltage at the ground level possible. Since the op-amp operates in an environment that clock signals exist, this is is the best vlaue for the CM voltage, in terms of the stability of the voltage level and injected noise.

Figure 5.8: Cascade structure

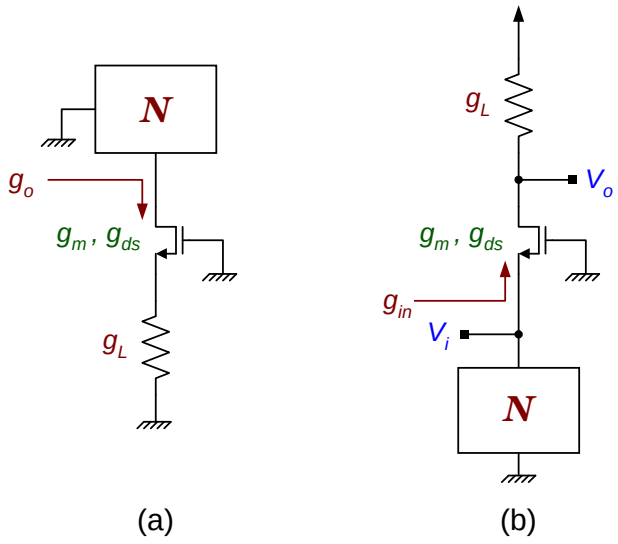

Figure 5.9: Simplified cascade structure: Looking into (a) drain (b) source

- The internal nodes are connected to the sources of M_5 and M_6, resulting in low impedance nodes. With proper design and biasing of the transistors connected to these nodes, the load capacitance of each of them can be made low enough so that the associated poles are placed at very high frequencies.

- The output nodes of the op-amp are high impedance ones, so that with proper selection of their load capacitance, they can easily provide the dominant poles.

- With proper selection of biasing voltages, i.e., $V_{b,n}$ and $V_{b,p}$, a peak-to-peak voltage swing of around 1V—for a 1.8V supply—can be achieved at the output. This is mainly due to the folding the original cascode block—which utilizes the same kind of transistors—by employing a PMOS-NMOS cascode structure—M_1-M_5 and M_2-M_6 pairs.

5.5.3 Non-idealities and Design Guidelines

The main source of non-ideality stems from channel length modulation effect [39]. Specially for such a deep sub-micron technology like 0.18 μ, this plays a crucial role in most deviations from the ideal characteristics.

The outcomes of non-ideality effects are more apparent when either the channel is very short or the drain-source voltage is very low. In either cases, the the characteristics of the transistor is not a mere function of the aspect ratio W/L, i.e., the absolute value of channel length as well as channel width directly affect the transistor performance. This results in the design guidelines that has been fully considered in this work:

- Whenever it is necessary to generate an integer multiple of a fixed current, like biasing transistors M_9–M_{12}, the lenght and the width of the transistor should be kept constant, and only the number of fingers has to found in a way to obtain the desired current.

- Whenever either a larger output resistance, M_3, M_4, M_9–M_{12}, or a higher intrinsic gain, M_5 and M_6 is desired, the channel length is increased, keeping the aspect ratio constant.

- If mixed-signal technology is available, i.e., the realization of twin well transistors is possible, in order to combat body effect, the bulk is connected to the source.

- Whenever only the transconductance of the transistor is important and its output resistance does not have much effect on the circuit performance, the lowest value of the channel length is desired, since it decreases the device prasitic capacitances. This is applicable to the input transistors M_1 and M_2. It should be noted the device matching requirements impose lower bounds on the channel length which are normally larger than the technology minimum feature.

5.5.4 Biasing Currents

Slew-Rate Requirements

As stated earlier, the biasing currents is mostly determined by slew rate consideration which itself depends on the clock frequency of the discrete time filter.

For an output voltage change of ΔV_o and total load capacitance of C_{load}, the required current at the slew rate limiting conditions is given by:

$$I_o = C_{load}\,\frac{\Delta V_o}{T/2} \tag{5.20}$$

where T is the clock period.

On the other hand, the integrators used in this work are bilinear differential ones whose TFs are given by Eq. 2.70 which can be re-written as

$$C_i\,\Delta V_o \;=\; (z\,+\,1)\,C_r\,V_i \tag{5.21}$$

For frequencies inside the PB of the filter which are much less than the clock rate, $\omega T/2$ approaches zero, and consequently $z = \exp(\omega T/2)$ approaches unity, so that Eq. 5.21 becomes

$$C_i\,\Delta V_o \;\simeq\; 2\,C_r\,V_i \tag{5.22}$$

Since the output peak-to-peak swing of every opamp is around 1 V, and the inputs of every integrator are fed from the outputs of other op-amps, therefore the amplitude of the input signal V_i is about 0.5 V. An approximate value of input capacitance C_r is 0.5 pF. Also, the load capacitance of each stage consists of the integrating capcitor and the input capacitors of other stages connected to the op-amp output. Therefore C_{load} can roughly

be estimated as two times the integrating capacitor C_i. Based on these and combining Eq. 5.20 and Eq. 5.22, the required output current I_o at the slew-rate limiting conditions is 200 μA.

Conclusively, the biasing currents will be selected in a way to make the op-amp able to provide

$$I_o \;=\; 300\ \mu\text{A} \tag{5.23}$$

output current at the limiting conditions, making sure that there will not be any degradations due to driving current capabilities.

Slew-Rate Performance of Folded Cascode Structure

Now that the required output current is known, in order to choose the biasing currents of the transisitors, the current handling capabilities of the selected topology, folded-cascode in this case, has to be examined. The aim of this section is to cover this issue. In order to do that, first a basic current model is presented for the structure under investigation and using the linear programming technique, the biasing currents will be found to minimize power dissipation.

The voltage gain of the first stage is small—around 5—therefore the variations of drain voltages of M_3 and M_4 are very low, so that it can be assumed that they are equal together. They have also equal gate-source voltage so that their total current at any time will be constant and equal to $2I_b$.

Transistors M_9 and M_{10} also share the same biasing voltage and have equal as well as constant drain-source voltages so that their currents are constant and equal to $I_b^{'}$ all the time. The same situation holds for M_{11} and M_{12} except for a scaling factor due to the difference between the number of their fingers. Therefore the biasing current of M_{12} is constant at all time at a level of $2I_b^{''}$. In conclusion a basic current model of the folded cascode structure is drawn in Fig. 5.10.

The currents of transistors M_1, M_2, M_5 and M_6 are represented by variables u, v, y and x, respectively. Variable i_o is the output current and since the op-amp is fully differential, the output currents at both output nodes are equal but with opposite polarity at any moment. The extremums of i_o has already been determined by the required slew-rate performance, so that variations of i_o will be between $-I_o$ and I_o, where I_o is given by Eq. 5.23.

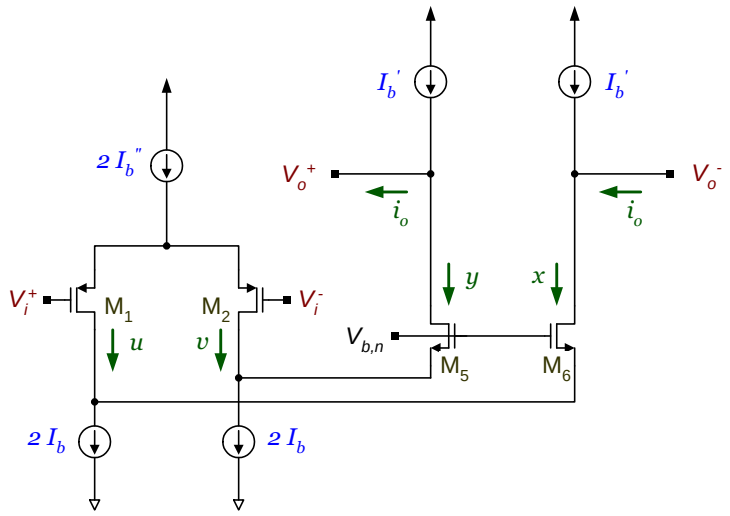

Figure 5.10: The current model of the folded cascode structure (Fig. 5.7).

The equations describing Fig. 5.10 are given as follows

$$x = I_b' + i_o \tag{5.24}$$
$$y = I_b' - i_o \tag{5.25}$$
$$x + u = 2I_b \tag{5.26}$$
$$y + v = 2I_b \tag{5.27}$$
$$u + v = 2I_b'' \tag{5.28}$$

Subtracting Eq. 5.25 from Eq. 5.24 results in

$$x - y = 2i_o \tag{5.29}$$

Variables x and y are the total currents of transistors, so that they can never accept negative values. Equation Eq. 5.29 together with the extremum values of i_o specify the range of variations of x and y which is given by the hatched region in x–y plane as it is depicted in Fig. 5.11.

On the other hand, adding Eq. 5.24 to Eq. 5.25 gives rise to

$$x + y = 2I_b' \tag{5.30}$$

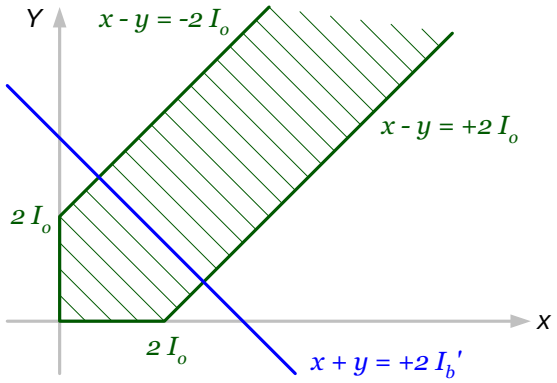

Figure 5.11: Finding the optimum value of biasing current $I_b^{'}$ by applying the linear programming technique to Eq. 5.29 and Eq. 5.30. Output current i_o in Eq. 5.29 ranges between $-I_o$ and $+I_o$ which is represented by the hatched region.

which imposes the second limitation on x and y, and it is shown by the associated line in Fig. 5.11. As a result, x and y can only vary over this line provided that they are placed inside the hatched region. And to satisfy the requirements of slew-rate performance, at the limits they must have a maximum value of $2I_o$. As it is seen for values of $I_b^{'} < I_o$ they cannot reach to this extremum at their limits. For $I_b^{'} > I_o$ they can, but there exists an extra amount of current that do not contribute to the output current—since some parts of the line is outside the hatched region—and it shows itself as unnecessary current consumption. To achieve the current driving requirements and at the same time keeping the power conusmption at its minimum level, $I_b^{'}$ has to be selected equal to I_o.

A similar procedure gives rise to the optimum value of I_o for $I^{''}{}_b$, and since combining Eq. 5.26, Eq. 5.27, Eq. 5.28, and Eq. 5.30 results in

$$I_b^{'} + I_b^{''} = I_b \tag{5.31}$$

the optimum value of I_b is also I_o.

5.5.5 Amplifier Design

The amplifier in Fig. 5.7 is composed of two stages which every single of them plays its own role. To obtain the size of different transistors the guidelines presented in Sec. 5.5.3

have been fully incorporated into the design procedure.

1. **Input Stage**

   The input stage should provide the following goals:

   - Large transconductance
   - Large output impedance (comparing to the input impedance of the output stage)
   - Low noise level
   - Low input capacitance

     This is important when the op-amp is utilized in closed loop configuration, since as it was seen in Chap. 4, it affects the effective unity gain frequency of the amplifier.
   - Large bandwidth
   - Highly matched input transistors
   - Delivering enough current to the output stage at slew-rate limiting conditions

   The latter has already been fully discussed, and the currents have been chosen in a way to make sure that the op-amp consumes the minimum amount of power while it can easily drive the capacitvie loads.

   Knowing the current of input PMOS transistors, M_1 and M_2, their aspect ratio W/L is found, so that their *over-drive* voltge, i.e., $V_{GS} - V_t$, will be around 0.2 V.

   Since the intrinsic gain of these transistor is not important, therefore the minimum value of channel length is desired. But in order to have highly matched input transistors, L has to be increased. A channel lenght of 1.6 times the technology minimum feature is a good compromise between input capacitance and matching issue [21].

   Current sources M_3 and M_4 are designed to provide the desired current at a drain-source voltage of around 0.2 V, while they have much higher impedance comparing to the other impedances connecting to their drains. In this way, it becomes inevitable to increase their L and W by a common factor in order to reach to the required ouptput impedance level.

   For current sources M_{12} and M_{13}, the key factor is to have very large output impedance. They form a cascade structure, therefore, for M_{12} the key factor is to have high impedance while M_{13} must have very large intrinsic gain. This makes sure that the

common-mode rejection of the amplifier will be very high, which is quite desirable. It should be noted having low levels of drain capacitance for M_{12} is desired since in that case the common-mode rejection remains large even for high frequencies.

2. **Output stage**

   The role of the output stage is to provide

- High voltage gain
- Low input impedance
- High output impedance
- Low input capacitance
- Large and at the same time symmetrical output voltage swing

Transistors M_5 and M_6 together with their active loads, form a cascade block, operating in the amplifying mode, so that the key factor will be the intrinsic gain. Their aspect ratio is found to satisfy the required overdrive and drain-source voltage requirements, and then their sizes are adjusted so that an intrinsic gain of around 250 is obtained. This also makes sure that the output impedance seen from the drain is very high, as they form another cascade block together with M_3 and M_4. The active load of the output stage is also a cascade structure. M_7 and M_8 must have large intrinsic gains while M_9 and M_{10} should provide high impedance with total drain capacitance at the lowest possible level. Similarly, to obtain these goals, the aspect ratios are found to meet biasing vlotage requirements and then their sizes are adjusted to reach to the desired levels of intrinsic gain and ouput impedance.

A subtle, yet crucial point in the design of this stage is that since the dominant pole of the op-amp is placed at the output node—as it is high impedance node and also the amplifier drives wholly capacitve loads of the SC filter—in order to have good stability the second pole which is associated to the input of this stage has to be far away from the dominant one. Subtlity arises from the fact that albeit this is a low-impedance node, in the normal amplifying mode of transistors M_5 and M_6, i.e., pinch-off region, the capacitances seen from their sources are in fact huge which may result in phase margin degradation. Therefore, it is not possible to up-scale these two transistors to reach to very high levels of intrinsic gain, since keeping g_m constant, g_{ds} decreases inversely with the first power of channel length, but for input

capacitance, it increase with square of L. Therefore a trade-off between intrinsic gain of these transistors and stability of the amplifier is compulsory.

Based on the discussion presented here and in previous sections, the transistors' sizes as well as their number of finger have been found and are listed in Table 5.8.

	Finger	W (μ)	L (μ)
M_1	4	64	0.3
M_2	4	64	0.3
M_3	30	15	4.8
M_4	30	15	4.8
M_5	4	72	0.9
M_6	4	72	0.9
M_7	8	50	0.6
M_8	8	50	0.6
M_9	15	7	1
M_{10}	15	7	1
M_{11}	1	7	1
M_{12}	30	7	1
M_{13}	8	100	0.6
M_{14}	2	6	0.3

Table 5.8: Op-Amp transistors' sizes

5.5.6 Common-Mode Feedback (CMFB) Circuitry

The output nodes of the op-amp are high impedance ones, so that they can experience large common-mode (CM) voltage variations without major changes in their biasing currents. This fact may cause the output CM voltage to reach to rail voltage levels which makes the whole amplifier malfunction. To prevent this event, a mechanism has to control the CM voltage of these nodes. The circuitry which does this task in differential amplifiers is called *common-mode feedback (CMFB)* block, and it is a crucial section of differential circuits. The peformance of CMFB circuitry directly affects the linearity and the available range of voltage swing. In other words, the *dynamic range (DR)* of the circuit strongly depends on the performance of the CMFB block.

	tt	ff	fs	ss	sf	
Gain	1572	3844	672	562	2635	
BW	108	45	247	280	63	kHz
GBW	170	174	166	158	165	MHz
f_T	149	152	147	94	96	MHz
Phase Margin	61	62	62	37	36	degrees
V_{cmfb}	669.293	562.508	567.278	778.838	773.188	mV
Output CM	902	905	902	891	890	mV

Table 5.9: Op-Amp characteristics for different models. Load capacitance has been 2 pF per output node in addition to 2 pF per node due to SC CMFB circuitry.

The task of the CMFB block can be described as follows. It measures both positive and negative output sinals, and a block called *averager* generates the CM voltage of these two signals, which is basically their average. This signal, then will be compared with a reference voltage to generate a feedback signal which will feed a specific control node in the op-amp to set the common-mode voltage of the output nodes at a specific level.

The key point in designing an efficient CMFB block is that the CM signal loop has to be faster than the main diffential signal loop, or in other words, its gain-bandwidth product (GBW) has to be higher. In this case, perturbations in the main signal path will be overcome by the CM loop, so that the output level will be set at the desired level.

CMFB circuitry can be designed either as a CT block or a DT one. A couple of circuits for both cases have been proposed in [15] [21]. Normally a CT one consists of some kind of differential amplifier whose input is connected to the output of the main op-amp. As a result the range of common-mode voltage which is accepted by this amplifier will determine the output CM voltage range. Usually this is quite limited so that it drastically degrades the DR of the whole op-amp.

Quite opposite a specific structure of capacitors and switches can be set up to act as an averager as well as a comparator. Since ideally these capacitors and switches can work at any voltage level, therefore they do not affect the range of CM output voltages, resulting in much better DR performance.

In this work, the structure shown in Fig. 5.12 has been employed [37] [15].

The minimum value of C_0 is determined by parasitic capcitances based on process specifications and the factor α should be chosen large enough to make sure that after

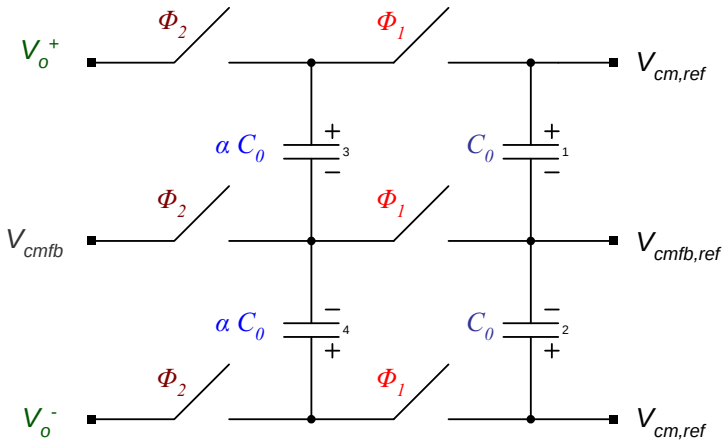

Figure 5.12: SC CMFB circuitry

reaching to steady state conditions the swiching of the transitors which are connected to the opamp outputs do not affect their voltages very much, so that the variations of V_{cmfb} remains very small, resulting in a stable CM voltage at the opamp outputs.

In this work C_0 has been chosen as 200 fF and a value of 10 has been selected for α.

5.5.7 Op-Amp Characterization

The designed operational amplifier has been fully characterized for typical as well as worst case scenarios of transistor models. The typical case is labeled as *tt* and corner models are represented by *ff*, *fs*, *ss*, *sf* standig for "fast NMOS-fast PMOS", "fast NMOS-slow PMOS", "slow NMOS-slow PMOS", "slow NMOS-fast PMOS", respectively.

Since the op-amp is a fully differential one, four different transfer functions are needed to fully describe the relationship between the input and the output ports and they can be represented in matrix form as follows

$$\begin{bmatrix} v_{o,d} \\ v_{o,cm} \end{bmatrix} = \begin{pmatrix} A_{d,d} & A_{d,cm} \\ A_{cm,d} & A_{cm,cm} \end{pmatrix} \begin{bmatrix} v_{i,d} \\ v_{i,cm} \end{bmatrix} \tag{5.32}$$

where $v_{i,d}$, $v_{i,cm}$, $v_{o,d}$ and $v_{o,cm}$ are differential input, CM input, differential output and CM output, respectively and defined as follows

$$v_{i,d} = v_i^+ - v_i^- \tag{5.33}$$

$$v_{i,cm} = \frac{v_i^+ + v_i^-}{2} \tag{5.34}$$

$$v_{o,d} = v_o^+ - v_o^- \tag{5.35}$$

$$v_{o,cm} = \frac{v_o^+ + v_o^-}{2} \tag{5.36}$$

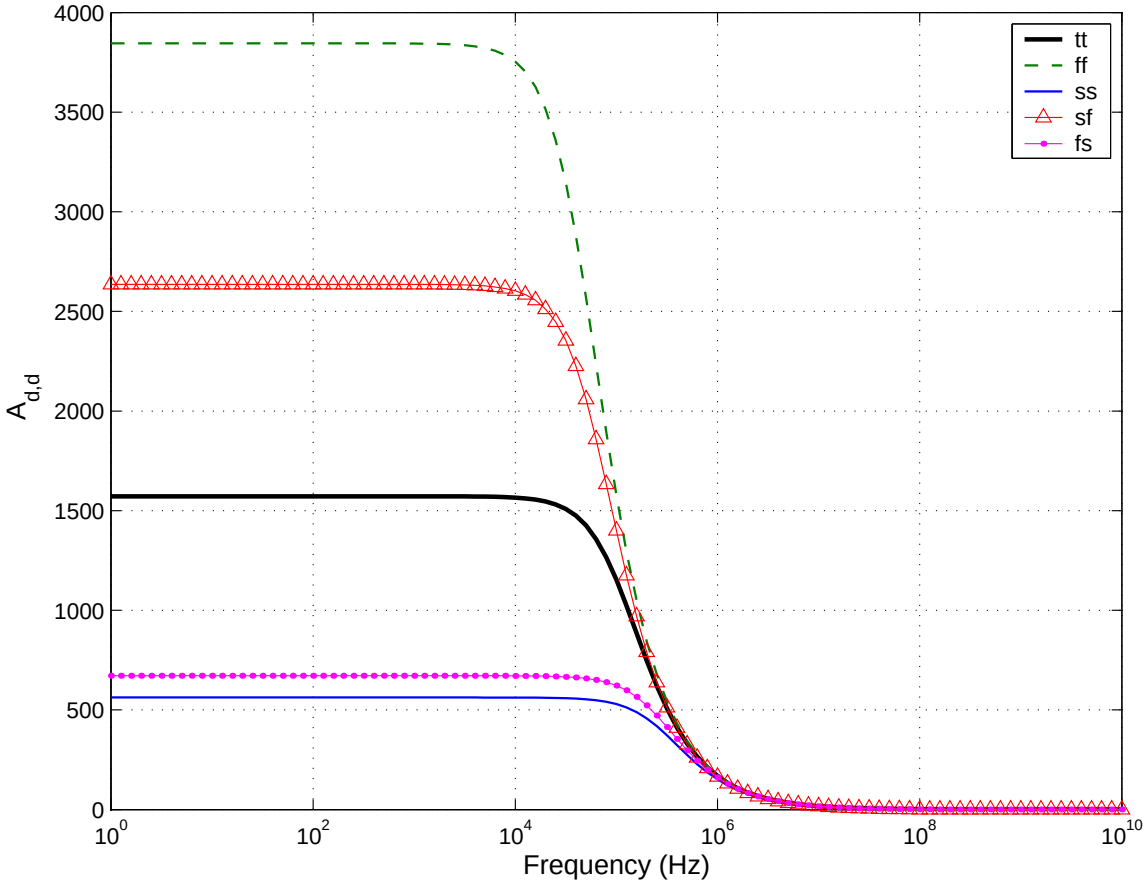

Figure 5.13: Differential gain of the operational amplifier for typical as well as worst case scenarios.

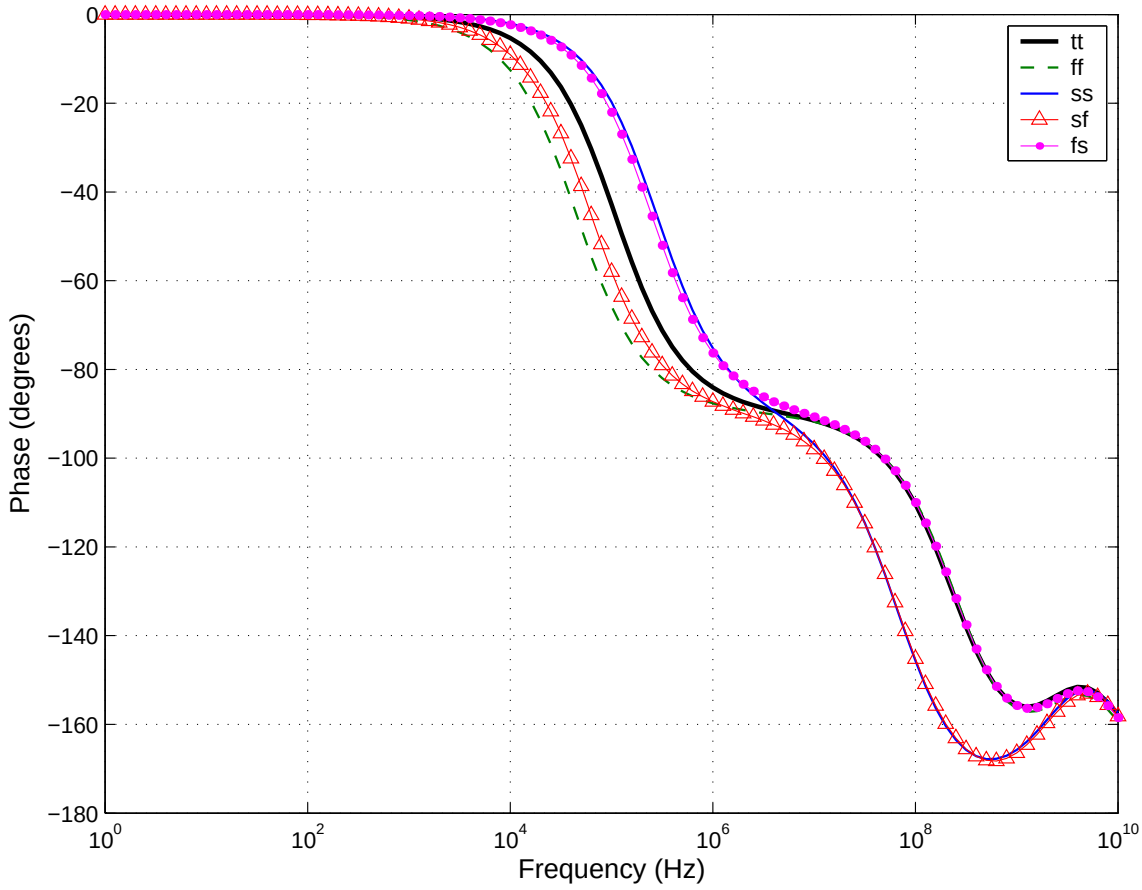

Figure 5.14: Phase response of the operational amplifier for typical as well as worst case scenarios.

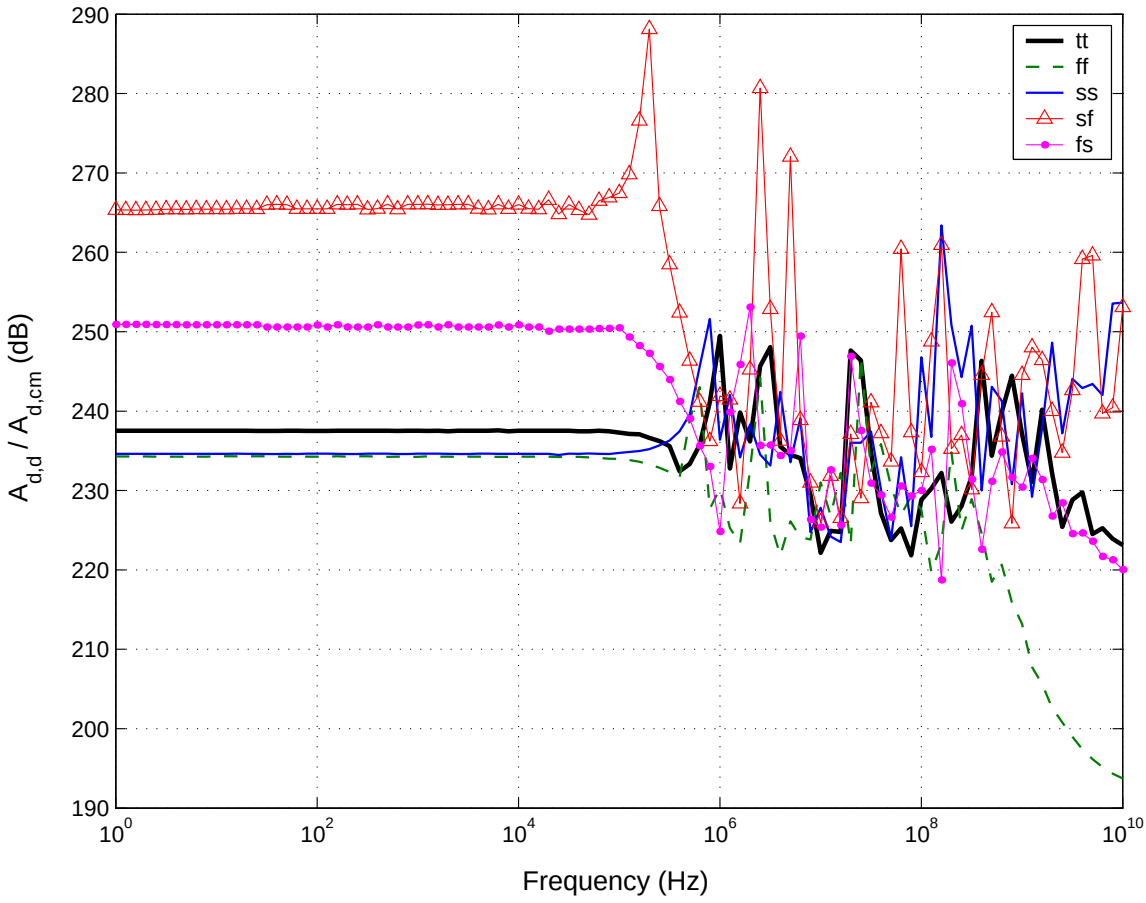

Figure 5.15: Common-mode rejection of the operational amplifier for typical as well as worst case scenarios.

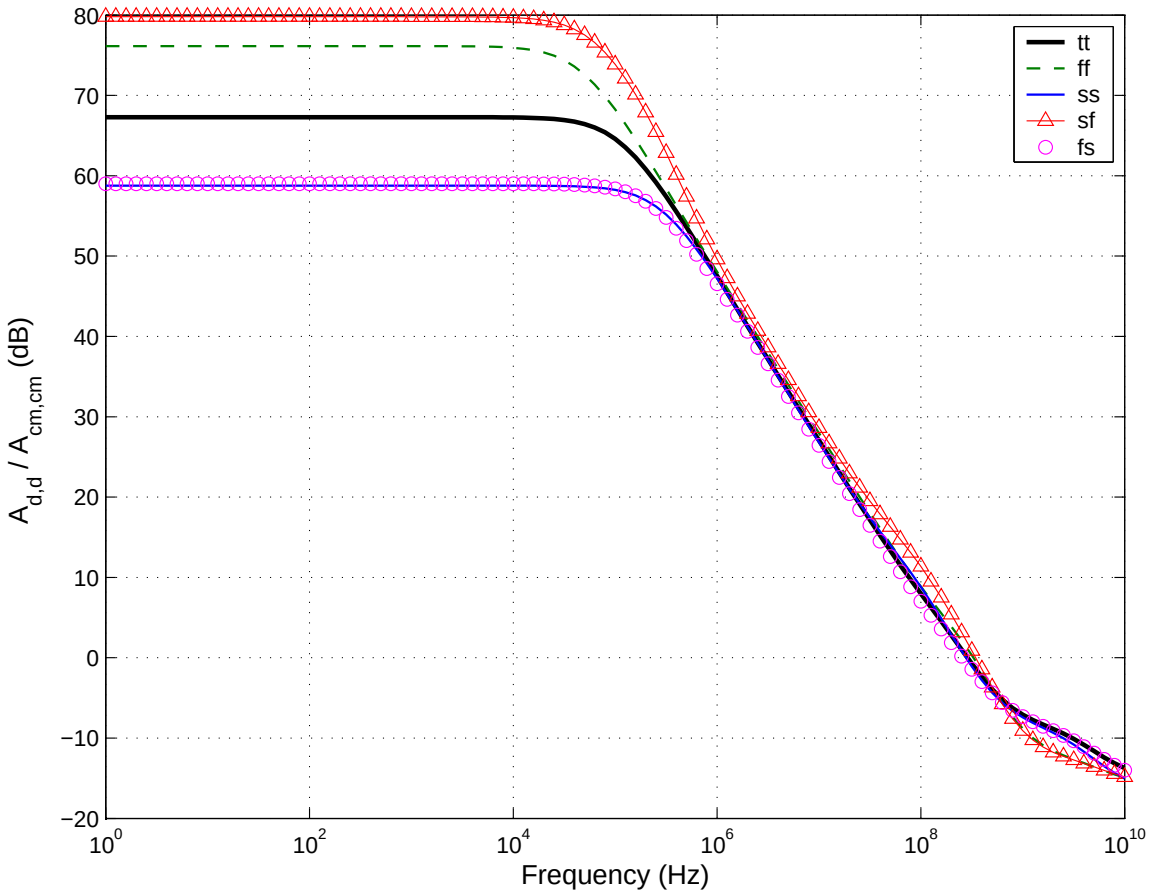

Figure 5.16: Differential-to-differential over CM-to-CM gain of the operational amplifier for typical as well as worst case scenarios.

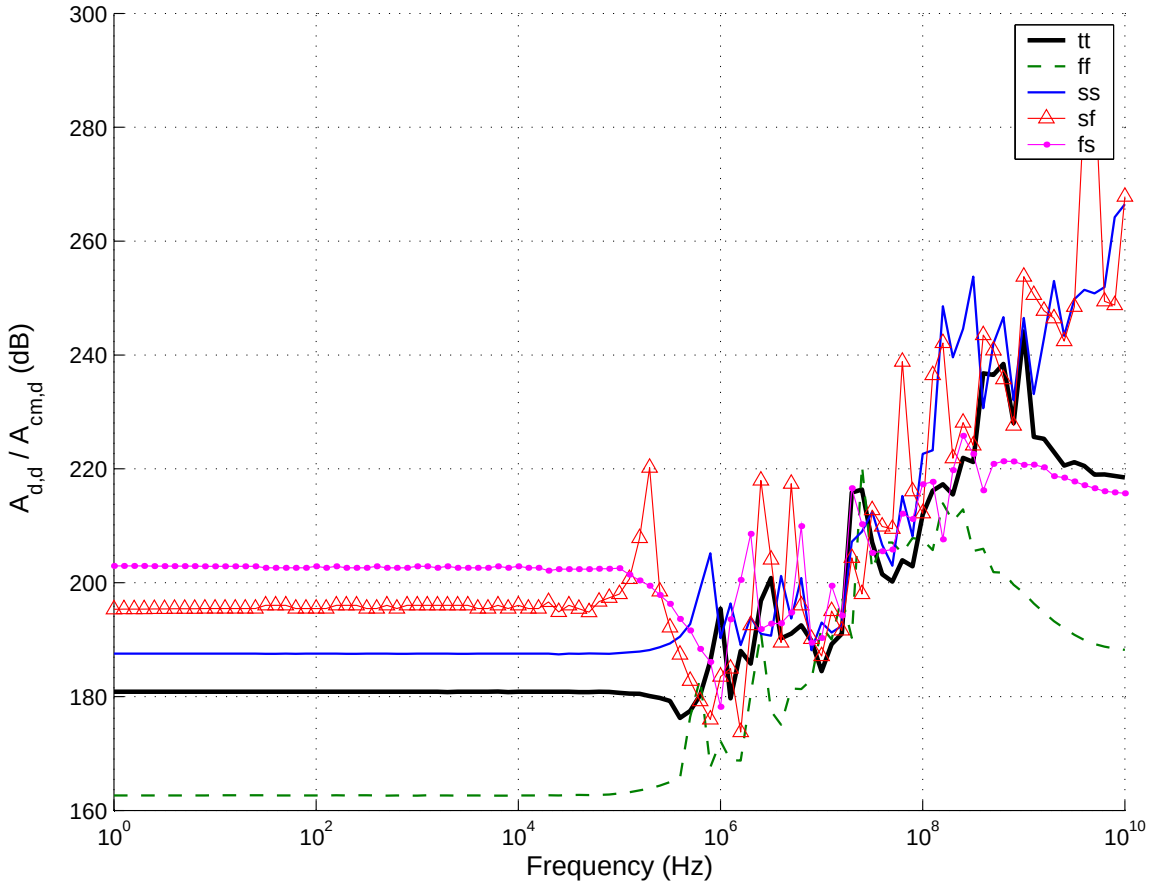

Figure 5.17: Differential-to-differential over differetial-to-CM gain of the operational amplifier for typical as well as worst case scenarios.

Chapter 6

Conclusions and Future Work

This research has proved that by careful consideration of both system level and device level it is possible to push the SC technique to much higher frequency ranges suitable for wide-band wireless telecommunications.

The designed circuit can easily be integrated into the whole mobile receiver front-end and it fully comply with the low-voltage low-power requirements of wireless communications.

The chosen architecture ensures that the filter response experience very low variations due to undesired changes of circuit element values.

In continuation of this work, future research might be continued by thorough noise analysis of the filter in order to find the main system level or device level parameters affecting the noise characteristics of the circuit. This shall include rigorous mathematical analysis which should be simplified to extract concise, yet insightful relationships for the noise performance of the filter. The non-idealities associated with the deep sub-micron technologies and the outcomes of the applying high clock frequencies should be considered in this noise analysis in order to obtain precise knowledge over the circuit behavior. Some old as well as recent studies of the noise performance of DT systems might be used as an starting point for this research [18] [1] [14] [12] [13] [10] [8] [16] [34] [23] .

Appendix A

WATSCAD Source Code

```
* Elliptic 7th-order
*
* Recalculation with MATLAB for better accuracy of
* Capacitor valuse!!!!!!!
*
* !!!!!! Doubly Terminated  !!!!!!!!!!!
* Low sensitivity: Orchard's theorem (Y'1966)
*
* fully differential
*
* similar clock phases for subsequent stages
*
*
* Optimized for Max Dynamic Range(DR)
*
* Elliptic 7th LC doubly prototype, rho = 10%, theta = 52degrees
*
* c = [0.90504 0.13022 1.44739 0.63601 1.28991 0.47479 0.65382]
* l = [0 1.28752 0 0.94676 0 0.94158 0]
*
* Max values (input=1)
* m = [0.989898 1.39743 1.11832 1.86657 0.86657 0.862783 1.08103 0.5]
*
```

```
* Frequencies of Max (radians)
* wm = [0.177941 0.169288 0.166388 0.164572 0.161478 0.160664]
*
* Stage 1 -------------------------------
*
* /vlsi_export/sun4/cad/bin/watscad ellip7_doubly_dr_opt_new.txt
*
* >> fseek(fid,0,-1);[x,nx] = fscanf(fid,'%f',[2,128]);
* >> fs = 30.156250e6 ; ff = x(1,:) ; zz = exp(j * 2 * pi * ff / fs) ;
* >> c1 = 1 ; c2 = 8.317284374 ; c3 = 1 ;
* resistive >> yy = c1 ./ ((c2*((zz-1)./(zz+1))) + c3) ; uu = abs(yy) ;
* capacitive >> yy = c1 ./ (c2 + (c3*((zz+1)./(zz-1)))) ; uu = abs(yy) ;
*
*
* alpha = tan( pi * f_bw / f_clk); f_bw=612 kHz; f_clk=30.15625 MHz;
* def alpha 0.063842953
*
*0 maxswi 200
*
g gnd
cl.q 1 0
*
*
*********************************************************************
* Stage 1
*
*
op.1 vgnd1p vgnd1n out1n out1p
*
* integrating capacitors (Stage 1)
*
c.1i1p out1p vgnd1p 16.21572848
c.1i1n out1n vgnd1n 16.21572848
*
* inputs from (Stage 0) to (Stage 1)
```

```
*
c.1r0p sig1p0 gnd1p0 1.01020509
s.1g0gp gnd1p0 gnd q
s.1g0vp vgnd1p gnd1p0 q c
s.1s0gp sig1p0 out0p q
s.1s0vp sig1p0 out0n q c
*
c.1r0n sig1n0 gnd1n0 1.01020509
s.1g0gn gnd1n0 gnd q
s.1g0vn vgnd1n gnd1n0 q c
s.1s0gn sig1n0 out0n q
s.1s0vn sig1n0 out0p q c
*
* inputs from (Stage 2) to (Stage 1)
* 1 / alpha1 = 1.41169090
*
c.1r2p sig1p2 gnd1p2 1.41169090
s.1g2gp gnd1p2 gnd q
s.1g2vp vgnd1p gnd1p2 q c
s.1s2gp sig1p2 out2n q
s.1s2vp sig1p2 out2p q c
*
c.1r2n sig1n2 gnd1n2 1.41169090
s.1g2gn gnd1n2 gnd q
s.1g2vn vgnd1n gnd1n2 q c
s.1s2gn sig1n2 out2p q
s.1s2vn sig1n2 out2n q c
*
* damping switched-capacitors (simulating Source Resistance)
*
c.1d1p dmp1vp dmp1op 1.0
s.1d1gp dmp1vp gnd q
s.1d1vp vgnd1p dmp1vp q c
s.1dp1n dmp1op out1n q
s.1dp1p dmp1op out1p q c
```

```
*
c.1d1n dmp1vn dmp1on 1.0
s.1d1gn dmp1vn gnd q
s.1d1vn vgnd1n dmp1vn q c
s.1dn1p dmp1on out1p q
s.1dn1n dmp1on out1n q c
*
* inputs from (Stage 3) to (Stage 1)
*
* 1 / alpha1 / alpha2 =
*
*
c.1c3p vgnd1p out3n 2.30430714
c.1c3n vgnd1n out3p 2.30430714
*
*
*
*
* Stage 2 --------------------------------
*
* /vlsi_export/sun4/cad/bin/watscad stage_02_watscad.txt
* >> fs=30.156250e6; zz=exp(j*2*pi*ff/fs); yy=(1 + zz)./(zz - 1);
* >> fseek(fid,0,-1);[x,nx] = fscanf(fid,'%f',[2,128]);
*  >> yy=(cr/ci).*(1+zz)./(1-zz);
*
**********************************************************************
* Stage 2
*
*
op.2 vgnd2p vgnd2n out2n out2p
*
c.2i2p out2p vgnd2p 20.16698677
c.2i2n out2n vgnd2n 20.16698677
*
* inputs from (Stage 1) to (Stage 2)
```

```
* alpha1 =
*
c.2r1p sig2p1 gnd2p1 0.70837037
s.2g1gp gnd2p1 gnd q
s.2g1vp vgnd2p gnd2p1 q c
s.2s1gp sig2p1 out1p q
s.2s1vp sig2p1 out1n q c
*
c.2r1n sig2n1 gnd2n1 0.70837037
s.2g1gn gnd2n1 gnd q
s.2g1vn vgnd2n gnd2n1 q c
s.2s1gn sig2n1 out1n q
s.2s1vn sig2n1 out1p q c
*
* inputs from (Stage 3) to (Stage 2)
* 1 / alpha2 =
*
c.2r3p sig2p3 gnd2p3 0.80026907
s.2g3gp gnd2p3 gnd q
s.2g3vp vgnd2p gnd2p3 q c
s.2s3gp sig2p3 out3n q
s.2s3vp sig2p3 out3p q c
*
c.2r3n sig2n3 gnd2n3 0.80026907
s.2g3gn gnd2n3 gnd q
s.2g3vn vgnd2n gnd2n3 q c
s.2s3gn sig2n3 out3p q
s.2s3vn sig2n3 out3n q c
*
*
*
*
*
* Stage 3 -------------------------------
*
```

```
*
* >> fseek(fid,0,-1);[x,nx] = fscanf(fid,'%f',[2,128]);
*  >> yy=(cr/ci).*(1+zz)./(1-zz);
*
**************************************************************************
* Stage 3
*
*
*
op.3 vgnd3p vgnd3n out3n out3p
*
c.3i3p out3p vgnd3p 34.67289461
c.3i3n out3n vgnd3n 34.67289461
*
* inputs from (Stage 2) to (Stage 3)
* alpha2 =
*
c.3r2p sig3p2 gnd3p2 1.24957973
s.3g2gp gnd3p2 gnd q
s.3g2vp vgnd3p gnd3p2 q c
s.3s2gp sig3p2 out2p q
s.3s2vp sig3p2 out2n q c
*
c.3r2n sig3n2 gnd3n2 1.24957973
s.3g2gn gnd3n2 gnd q
s.3g2vn vgnd3n gnd3n2 q c
s.3s2gn sig3n2 out2n q
s.3s2vn sig3n2 out2p q c
*
* inputs from (Stage 4) to (Stage 3)
* 1 / alpha3 =
*
c.3r4p sig3p4 gnd3p4 1.66908398
s.3g4gp gnd3p4 gnd q
s.3g4vp vgnd3p gnd3p4 q c
```

```
s.3s4gp sig3p4 out4n q
s.3s4vp sig3p4 out4p q c
*
c.3r4n sig3n4 gnd3n4 1.66908398
s.3g4gn gnd3n4 gnd q
s.3g4vn vgnd3n gnd3n4 q c
s.3s4gn sig3n4 out4p q
s.3s4vn sig3n4 out4n q c
*
* inputs from (Stage 5) to (Stage 3)
*
* 1 / alpha3 / alpha4 =
*
c.3c5p vgnd3p out5n 7.68575367
c.3c5n vgnd3n out5p 7.68575367
*
* inputs from (Stage 1) to (Stage 3)
*
* alpha1 * alpha2 = 0.91809978
*
c.3c1p vgnd3p out1n 1.80546501
c.3c1n vgnd3n out1p 1.80546501
*
*
* Stage 4 --------------------------------
*
* /vlsi_export/sun4/cad/bin/watscad stage_04_watscad.txt
* >> fs=30.156250e6; zz=exp(j*2*pi*ff/fs); yy=(1 + zz)./(zz - 1);
* >> fseek(fid,0,-1);[x,nx] = fscanf(fid,'%f',[2,128]);
*  >> yy=(cr/ci).*(1+zz)./(1-zz);
*
*
**************************************************************************
* Stage 4
*
```

```
*
op.4 vgnd4p vgnd4n out4n out4p
*
c.4i4p out4p vgnd4p 14.82951441
c.4i4n out4n vgnd4n 14.82951441
*
* inputs from (Stage 3) to (Stage 4)
* alpha3 =
*
c.4r3p sig4p3 gnd4p3 0.59913103
s.4g3gp gnd4p3 gnd q
s.4g3vp vgnd4p gnd4p3 q c
s.4s3gp sig4p3 out3p q
s.4s3vp sig4p3 out3n q c
*
c.4r3n sig4n3 gnd4n3 0.59913103
s.4g3gn gnd4n3 gnd q
s.4g3vn vgnd4n gnd4n3 q c
s.4s3gn sig4n3 out3n q
s.4s3vn sig4n3 out3p q c
*
* inputs from (Stage 5) to (Stage 4)
* 1 / alpha4 =
*
c.4r5p sig4p5 gnd4p5 0.46222912
s.4g5gp gnd4p5 gnd q
s.4g5vp vgnd4p gnd4p5 q c
s.4s5gp sig4p5 out5n q
s.4s5vp sig4p5 out5p q c
*
c.4r5n sig4n5 gnd4n5 0.46222912
s.4g5gn gnd4n5 gnd q
s.4g5vn vgnd4n gnd4n5 q c
s.4s5gn sig4n5 out5p q
s.4s5vn sig4n5 out5n q c
```

```
*
*
*
* Stage 5 -------------------------------
*
* /vlsi_export/sun4/cad/bin/watscad stage_05_watscad.txt
* >> fseek(fid,0,-1);[x,nx] = fscanf(fid,'%f',[2,128]);
*  >> yy=(cr/ci).*(1+zz)./(1-zz);
*
**************************************************************************
* Stage 5
*
*
op.5 vgnd5p vgnd5n out5n out5p
*
c.5i5p out5p vgnd5p 37.60336680
c.5i5n out5n vgnd5n 37.60336680
*
* inputs from (Stage 4) to (Stage 5)
* alpha4 =
*
c.5r4p sig5p4 gnd5p4 2.16342927
s.5g4gp gnd5p4 gnd q
s.5g4vp vgnd5p gnd5p4 q c
s.5s4gp sig5p4 out4p q
s.5s4vp sig5p4 out4n q c
*
c.5r4n sig5n4 gnd5n4 2.16342927
s.5g4gn gnd5n4 gnd q
s.5g4vn vgnd5n gnd5n4 q c
s.5s4gn sig5n4 out4n q
s.5s4vn sig5n4 out4p q c
*
* inputs from (Stage 6) to (Stage 5)
* 1 / alpha5 =
```

```
*
c.5r6p sig5p6 gnd5p6 1.25295700
s.5g6gp gnd5p6 gnd q
s.5g6vp vgnd5p gnd5p6 q c
s.5s6gp sig5p6 out6n q
s.5s6vp sig5p6 out6p q c
*
c.5r6n sig5n6 gnd5n6 1.25295700
s.5g6gn gnd5n6 gnd q
s.5g6vn vgnd5n gnd5n6 q c
s.5s6gn sig5n6 out6p q
s.5s6vn sig5n6 out6n q c
*
* inputs from (Stage 3) to (Stage 5)
*
* alpha3 * alpha4 =
*
c.5c3p vgnd5p out3n 12.91265317
c.5c3n vgnd5n out3p 12.91265317
*
* inputs from (Stage 7) to (Stage 5)
*
* 1 / allpha5 / alpha6 = 0.61302532
*
c.5c7p vgnd5p out7n 4.30979902
c.5c7n vgnd5n out7p 4.30979902
*
*
*
* Stage 6 --------------------------------
*
* /vlsi_export/sun4/cad/bin/watscad stage_06_watscad.txt
* >> fs=30.156250e6; zz=exp(j*2*pi*ff/fs); yy=(1 + zz)./(zz - 1);
* >> fseek(fid,0,-1);[x,nx] = fscanf(fid,'%f',[2,128]);
*  >> yy=(cr/ci).*(1+zz)./(1-zz);
```

```
*
*************************************************************************
* Stage 6
*
*
*
op.6 vgnd6p vgnd6n out6n out6p
*
c.6i6p out6p vgnd6p 14.74837782
c.6i6n out6n vgnd6n 14.74837782
*
* inputs from (Stage 5) to (Stage 6)
* alpha5 =
*
c.6r5p sig6p5 gnd6p5 0.79811199
s.6g5gp gnd6p5 gnd q
s.6g5vp vgnd6p gnd6p5 q c
s.6s5gp sig6p5 out5p q
s.6s5vp sig6p5 out5n q c
*
c.6r5n sig6n5 gnd6n5 0.79811199
s.6g5gn gnd6n5 gnd q
s.6g5vn vgnd6n gnd6n5 q c
s.6s5gn sig6n5 out5n q
s.6s5vn sig6n5 out5p q c
*
* inputs from (Stage 7) to (Stage 6)
* 1 / alpha6 =
*
c.6r7p sig6p7 gnd6p7 0.46252185
s.6g7gp gnd6p7 gnd q
s.6g7vp vgnd6p gnd6p7 q c
s.6s7gp sig6p7 out7n q
s.6s7vp sig6p7 out7p q c
*
```

```
c.6r7n sig6n7 gnd6n7 0.46252185
s.6g7gn gnd6n7 gnd q
s.6g7vn vgnd6n gnd6n7 q c
s.6s7gn sig6n7 out7p q
s.6s7vn sig6n7 out7n q c
*
*
*
* Stage 7 --------------------------------
*
* /vlsi_export/sun4/cad/bin/watscad stage_07_watscad.txt
* >> fseek(fid,0,-1);[x,nx] = fscanf(fid,'%f',[2,128]);
*  >> yy=(cr/ci).*(1+zz)./(1-zz);
*
**************************************************************************
* Stage 7
*
*
*
op.7 vgnd7p vgnd7n out7n out7p
*
*
c.7i7p out7p vgnd7p 17.67791020
c.7i7n out7n vgnd7n 17.67791020
*
* inputs from (Stage 6) to (Stage 7)
* alpha6 =
*
c.7r6p sig7p6 gnd7p6 2.16206000
s.7g6gp gnd7p6 gnd q
s.7g6vp vgnd7p gnd7p6 q c
s.7s6gp sig7p6 out6p q
s.7s6vp sig7p6 out6n q c
*
c.7r6n sig7n6 gnd7n6 2.16206000
```

```
s.7g6gn gnd7n6 gnd q
s.7g6vn vgnd7n gnd7n6 q c
s.7s6gn sig7n6 out6n q
s.7s6vn sig7n6 out6p q c
*
* damping switched-capacitors (simulating Load Resistance)
*
c.7d7p dmp7vp dmp7op 1.0
s.7d7gp dmp7vp gnd q
s.7d7vp vgnd7p dmp7vp q c
s.7dp7n dmp7op out7n q
s.7dp7p dmp7op out7p q c
*
c.7d7n dmp7vn dmp7on 1.0
s.7d7gn dmp7vn gnd q
s.7d7vn vgnd7n dmp7vn q c
s.7dn7p dmp7on out7p q
s.7dn7n dmp7on out7n q c
*
* inputs from (Stage 5) to (Stage 7)
*
* alpha5 * alpha6 =
*
c.7c5p vgnd7p out5n 12.83276283
c.7c5n vgnd7n out5p 12.83276283
*
*
*
*
*
*
*
*
* switched inputs
*
vs.0p out0p gnd 0.5 cos 0.5 500k 0
```

```
vs.0n gnd out0n 0.5 cos 0.5 500k 0
*
#
shold no
*
*ytype real
ytype mag
*ytype phase
*
output v(out7p,out7n)
*output add v(out0p,out0n)
*output add v(out1p,out1n) v(out2p,out2n) v(out3p,out3n)
output add v(out4p,out4n) v(out5p,out5n) v(out6p,out6n)
*
phi equal
swf 30.156250Me
*xax 1 2000k lin 2048
xax 1 3000K lin 4096
band 1
kfile ellip7_doubly_dr_opt
ufile ellip7_doubly_dr_opt
freq
append no
wrt ve7_3
wr all
```

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