Bottom-Gate TFTs With Channel Layer Deposited by Pulsed PECVD

by

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Author's Declaration for Electronic Submission of a Thesis

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Abstract

Nanocrystalline silicon (nc-Si:H) is a promising material for Thin-Film Transistors (TFTs) offering potentially higher mobilities and improved stability over hydrogenated amorphous silicon (a-Si:H). The slow growth rate of nc-Si:H can be overcome by using pulsed Plasma-Enhanced Chemical Vapour Deposition (PECVD). Pulsed PECVD also reduces powder particle formation in the plasma and provides added degrees of freedom for process optimization. Unlike high frequency PECVD, pulsed PECVD can be scaled to deposit films over large areas with no reduction in performance.

For this thesis, silicon thin films were deposited by the pulsed PECVD technique at a temperature of 150 °C and TFTs were made using this material. Radio Frequency (RF) power and silane (SiH_4) flow rate were varied in order to study the effect of different levels of crystallinity on the film.

Raman spectroscopy, Atomic Force Microscope (AFM), X-Ray Diffraction (XRD), electrical conductivity, Hall mobility, optical band gap, and stability under light-soaking were measured using films of two different thicknesses, 50 nm and 300 nm. From the Raman data we see that the 50 nm films deposited with high hydrogen dilution are mostly amorphous, indicating the presence of a thick incubation layer. The 300 nm samples deposited with hydrogen dilution, on the other hand, showed very high crystallinity and conductivity, except for 300-2 which was surprisingly, mostly amorphous. AFM and XRD measurements were also performed to confirm the Raman data and get an estimate for the crystallite grain size in the 300 nm samples. The conductivity was measured for all films, and the Hall mobility and carrier concentration was measured for one of the 300 nm films. The thin samples which

are mostly amorphous show low conductivity whereas the thick high crystallinity films show high conductivity, and n-type behaviour possibly due to oxygen doping. The optical gap was also measured using Ultra Violet (UV) light and results indicate the possible presence of small crystallites in the 50 nm films. The conductivity's stability under light-soaking was measured to observe the material's susceptibility to degradation, and the 300 nm with high crystallinity were much more stable than the a-Si:H films. All the results of these measurements varied depending on the film and these results are discussed.

Bottom-gate TFTs were fabricated using a pulsed PECVD channel layer and a amorphous silicon nitride (a-SiN:H) gate dielectric. The extracted parameters of one of the best TFTs are $\mu_{sat} \leq 0.38\,\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$, $V_{t,sat} \geq 7.3\,\mathrm{V}$, $I_{on/off} > 10^6$, and $S < 1\,\mathrm{V/decade}$. These parameters were extracted semi-automatically from the basic Field-Effect Transistor (FET) model using a computer program. Extraction using a more complicated model yielded similar results for mobility and threshold voltage but also gave a large power parameter α of 2.31 and conduction band tail slope of 30 meV. The TFT performance and material properties are presented and discussed.

On this first attempt at fabricating TFTs using a nc-Si:H channel layer deposited by pulsed PECVD, results were obtained which are consistent with results for low temperature a-Si:H TFTs and previous pulsed PECVD TFTs. The channel layer was mostly amorphous and non-crystalline, possibly due to the amorphous substrate or insufficient hydrogen dilution in the plasma. The 300 nm films showed, however, that high crystallinity material deposited directly on glass can easily be obtained, and this material showed less degradation under light-soaking than the purely amorphous counterpart. Pulsed PECVD is a promising technique for the growth of nc-Si:H and with further materials development and process optimization for TFTs, it may prove to be useful for the growth of high-quality nc-Si:H TFT channel layers.

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To my Family and Nasha

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Chapter 1

Introduction

Hydrogenated amorphous silicon (a-Si:H) is used extensively in Thin-Film Transistors (TFTs) for Flat-Panel Displays (FPDs) and large-area imagers, and it is also a promising photovoltaic material. a-Si:H TFTs have a low off-current and sufficient on-current for most applications; however, they suffer from poor carrier mobility and threshold voltage (V_t) shift. The low mobility (μ) of a-Si:H places a limitation on pixel sizes for display and imaging applications, and its poor hole mobility prohibits a usable p-type device. Its drifting threshold voltage also means that it cannot be used easily or reliably in column multiplexer and row shift register circuits [1]. Vertical TFTs [2] have also been proposed although results in this area so far have been mixed. Polycrystalline silicon (Poly-Si) can overcome the disadvantages of a-Si:H TFTs; however, it has some drawbacks, in that it requires large, expensive laser annealing systems.

Alternatively, nanocrystalline silicon (nc-Si:H) is deposited by Plasma-Enhanced Chemical Vapour Deposition (PECVD) and can thus be easily integrated into standard PECVD systems with little additional cost. In theory, nc-Si:H TFTs can deliver equal or better mobility, and more importantly, improved stability over their amorphous counterparts due to higher material crystallinity; however, this is not always the case in practise. As such, they can be useful not only as switching devices in FPDs, allowing for higher resolution displays, but perhaps also in row shift registers and column multiplexers thus reducing packaging costs [1].

Recently, nc-Si:H films deposited by pulsed PECVD for use in solar cells have been reported [3]. Pulsed PECVD is the same as conventional PECVD at 13.56 MHz, except the plasma is modulated with a frequency in the kHz range. During the off-cycles, large powder particle precursors can be collected, thus reducing the density of powder particles in the resulting film [4]. This allows the growth rate to be increased without compromising the material's quality. Unlike Very-High Frequency (VHF)-PECVD, pulsed PECVD is scalable to large chamber dimensions and it also adds degrees of freedom in process optimization, allowing one to trade off deposition rate for quality. Because of these advantages and its success so far as a solar cell material, pulsed PECVD may be a promising deposition technique for the channel layer of nc-Si:H TFTs. A more complete description of pulsed PECVD is provided in section §2.2.

In this thesis, the experimental results from the electrical (conductivity, mobility), optical (energy band gap), stability (under light-soaking), and structural (crystallinity, AFM, XRD) characterizations of films grown by pulsed PECVD are presented and discussed, along with the characteristics and extracted parameters of bottom-gate TFTs made with a pulsed PECVD-grown active layer.

1.1 Drawbacks of Hydrogenated Amorphous Silicon

Although a-Si:H is ubiquitous in Liquid Crystal Displays (LCDs) as a pixel switch, it does have some disadvantages and limitations. Due to its amorphous nature, carriers travel very slowly in a-Si:H, due to excessive trapping in localized states and scattering due to the lack of a periodic lattice. a-Si:H thus has electron mobilities as low as 0.1–1 $\mathrm{cm^2\ V^{-1}\ s^{-1}}$ and hole mobilities which are so low that p-type devices are not practical in any application. a-Si:H also suffers from light-induced degradation as well as bias stress induced degradation due to the creation of metastable states.

1.2 The Crystalline and Polycrystallaine Silicon Solutions

Although crystalline silicon (c-Si) can be used to overcome all the limitations of a-Si:H, c-Si lacks the capability of large-area low-cost manufacturing, and the temperatures required for bulk crystalline formation make it impossible to integrate c-Si with plastic or glass substrates. Poly-Si has been proposed as an alternative to a-Si:H, as it can have mobilities of up to $400\,\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$ and is also more stable; however, it suffers from high leakage currents [5] which "prevents a wider use of such devices [poly-Si TFTs] in active-matrix liquid crystal displays (Active-Matrix Liquid Crystal Displays (AMLCDs)) as switching elements within the pixel matrix" [6]. Poly-Si can and is being used, however, for the row and column driver circuits, as well as more complex display circuitry and processing. It can be integrated on the same substrate as a-Si:H in a hybrid process by creating poly-Si from a-Si:H by laser annealing a-Si:H. The main disadvantage of poly-Si is the extra laser processing required, which increases processing costs and processing time. There is another added disadvantage of poly-Si, which is that it is difficult to control the grain size accurately and uniformly, the lack of which leads to inhomogeneity across devices.

1.3 Motivation for Nanocrystalline Silicon

nc-Si:H can be considered as a compromise solution between a-Si:H and poly-Si. nc-Si:H is similar to a-Si:H, in that it usually contains some a-Si:H material, although it contains tiny crystallites of silicon as well. The morphology of nc-Si:H can be seen in Figure 1.1, an AFM image of nc-Si:H where many small crystallites (grains) are visible. The percentage of nc-Si:H which is crystalline is called the crystalline fraction (X_c). These crystallites, or crystalline grains of silicon, are usually about tens of nanome-

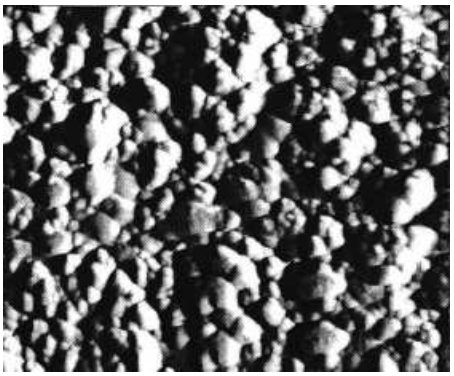

Figure 1.1: AFM morphology of nc-Si:H samples deposited by PECVD showing the crystalline grain structure. From [7].

tres in size[1]. It is the hope of researchers that nc-Si:H can retain some of the advantages of a-Si:H such as low leakage current, low-cost, and simple low-temperature processing, yet at the same have improved electrical characteristics over a-Si:H, such as higher mobility and greater stability, due to the crystalline content in the film. With nc-Si:H it may also be possible to fabricate a high quality p-type material due to the higher doping efficiency in the crystallites, which currently isn't possible with a-Si:H. Since the silicon grains in nc-Si:H have a band gap closer to the silicon band gap of 1.1 eV (a-Si:H has a band gap of around 1.7 eV), it is currently being used in thin film solar cell research, to improve the efficiency of solar cells by absorbing low-energy (red-infrared) light in "tandem" or "micromorph" cells. Work using nc-Si:H in TFTs is still preliminary. Some research groups have grown nc-Si:H for use in TFTs with field-effect electron mobilities of up to $\mu_n = 40\,\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$ [8], while others have grown nc-Si:H with mobilities of only about $\mu_n = 1\,\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$ [9] which is comparable to the mobility of a-Si:H. Although most TFTs with a nc-Si:H active layer fabricated thus far have leakage currents which are too high

[1]There is a big discrepancy in the literature about whether to call this material microcrystalline silicon (μc-Si) or nc-Si:H; rarely is the grain size actually in the micron range when deposited by low temperature PECVD, so it has become more appropriate in recent times to call this material nc-Si:H instead.

for high-sensitivity sensor applications, such as medical imaging, they can be suitable for LCD applications.

1.4 Requirements of TFTs for Flat-Panel Applications

Since the first TFTs with a-Si:H active layers were created, a-Si:H has become the most widely used amorphous semiconductor. a-Si:H is most useful as the active material in TFTs as it provides a high resistance ideal for LCDs and large-area sensors. The highest quality amorphous silicon available has a field-effect mobility of $1\,\mathrm{cm}^2$ V^{-1} s^{-1}, much lower than c-Si which has a field-effect mobility of at least $200\,\mathrm{cm}^2$ V^{-1} s^{-1}. The mobility of a-Si:H devices is limiting the size of displays, because with large displays, faster TFT switching is required to maintain an adequate refresh rate. The low mobiliby of a-Si:H devices also prohibits their use in driver circuitry and restricts their use solely to on-pixel TFTs.

LCDs require switches with low off-currents (or leakage currents), and less than 1 nA (10^{-9} A) is often quoted as the acceptable value for an active matrix pixel switch [10]. Obtaining a current as low as 1 pA can easily be achieved by reducing the width (W) for a field-effect TFT, however this would subsequently cause the on-current to decrease as well. Another figure of merit is thus needed, and that is the on-off current ratio, which is independent of W/L. One quoted value of the minimum level of the on/off current ratio required for an LCD display is 4×10^5 [11], although this of course depends on the display. Intrinsic a-Si:H TFTs satisfy this requirement. For large-area sensor applications such as scanners and x-ray imaging arrays, leakage currents must be < 1 pA (10^{-12} A). LCDs must also be manufactured with materials that can be processed over large areas. Bulk c-Si is currently limited to wafers of about 300 mm, whereas a-Si:H can theoretically be deposited on substrates of any size using roll-to-roll processing[2]. nc-Si:H

[2]In roll-to-roll processing, one dimension (length) can be almost limitless (on the order of kilometers range), however the other dimension is limited by the space in a manufacturing facility for example, or the width of a particular

is a good alternative to a-Si:H because it offers higher mobility, can be deposited over large areas, and currently the leakage currents are suitable for display applications, although not necessarily for sensing applications. It overcomes many of the disadvantages of poly-Si as well as c-Si.

1.5 Overview of the Thesis

In this thesis the material properties of a-Si:H and nc-Si:H films deposited by pulsed PECVD are studied along with TFTs deposited using these materials. The electrical properties, such as conductivity and Hall mobility are measured as well as structural measurements using Raman spectroscopy, XRD, and AFM to determine crystal grain structure (crystalline orientation and crystal size) and crystal fraction. The optical band gap was also measured, as well as the stability against light-soaking.

Bottom-gate TFTs using this material are fabricated using an active layer deposited by pulsed PECVD with high hydrogen gas (H_2) dilution. The characteristics of the TFTs such as its DC static electrical characteristics are measured and discussed, as well as its long-term stability, where the shift in the threshold voltage, V_t with time is measured. Important device parameters such as field-effect mobility, threshold voltage, sub-threshold slope, on-off ratio, and α (power parameter) are extracted according to a simple Field-Effect Transistor (FET) model as well as a more complicated physical model.

processing machine.

Chapter 2

Background

This section will provide an introduction to the history of the development of a-Si:H and nc-Si:H materials as well as the devices which use these materials, with an emphasis on TFTs. A brief introduction to LCDs, a-Si:H/nc-Si:H physics, the growth of nc-Si:H by PECVD, and AMLCDs will follow.

2.1 History of a-Si:H and nc-Si:H

2.1.1 Hydrogenated Amorphous Silicon (a-Si:H)

Amorphous silicon (a-Si) was first used as a semiconductor in the 1960s; however, this material was prepared by sputtering a silicon target or by thermal evaporation and it had very poor characteristics due to its high defect density of states in the mid-gap region. Sterling and Swann [12] were the first to use PECVD to grow a-Si:H (as well as silicon oxide (SiO) and amorphous silicon nitride (a-SiN:H)) from silane (SiH_4) gas in 1965. The use of SiH_4 gas (which contains hydrogen) caused some hydrogen to be incorporated into the film. This hydrogen passivated dangling bond defects within the a-Si and led to a much better quality material. Chittick then used this technique to deposit a-Si:H and was the first to study its properties such as electrical conduction, optical properties, and doping [13]. This material had much better

characteristics than the sputtered material, due to the presence of hydrogen leading to passivation of defects. Following Chittick, the most significant research in the field of a-Si:H came from Spear and Le Comber from Dundee University in Scotland, who measured the conductivity of a-Si:H, the hall effect mobility, demonstrated its photoelectric properties, and were the first to show n-type and p-type doping of a-Si:H [14].

The first devices to use a-Si:H in a practical way were solar cells. Sanyo first commercialized calculators powered by a-Si:H solar cells in 1979, after Carlson and Wronski at RCA began research in this area in 1976 [15]. The TFT concept was pioneered by Weimer [16] but TFTs at that time were made using other materials such as cadmium sulfide (CdS) for the channel layer. The first TFTs made using a-Si:H came from Le Comber et al. [17] in 1979. In 1981, Snell et al. [18] used a-Si:H TFTs for the first time to switch an LCD matrix. This was the beginning of the LCD, and twenty-two years later in 2003, monthly sales of LCDs (which use primarily a-Si:H TFT technology) surpassed that of Cathode Ray Tube (CRT) displays for the first time in history. Displays using a-Si:H TFTs should soon be available on flexible low-temperature substrates as well as the traditional glass substrate. a-Si:H TFTs are now being used as active switching elements in x-ray imagers [19] and with further research, a-Si:H could be a promising alternative to c-Si for large-area, low-cost, and possibly flexible solar panels [20].

2.1.2 Nanocrystalline Silicon (nc-Si:H)

nc-Si:H is a close relative of poly-Si. Poly-Si has long been used as a gate conductor in Complementary Metal Oxide Silicon (CMOS) processing. This particular poly-Si material is made at high temperature, however, and is also heavily doped so that it can be used as a "polysilicon" gate. It is possible to form poly-Si using Low Pressure Chemical Vapour Deposition (LPCVD) at high temperature and low pressure [21] but this is incompatible with low temperatures processes on glass of plastic. At low temperatures the only options are to either crystallize a-Si:H into poly-Si or nc-Si:H (sometimes called fine-grained poly-Si) using laser crystallization,

or to grow nc-Si:H from a plasma heavily diluted with H_2 or other etchant gases such as SiF_4 [10] or $SiCl_2H_2$ [22] using PECVD. Doped nc-Si:H (n^+ doped nanocrystalline silicon (n^+-nc-Si:H)) is already frequently used for high-conductivity source and drain contact material in TFTs.

The first studies of nc-Si:H materials grown by pulsed PECVD using hydrogen dilution and began in earnest in 1981 by Spear et al. [23] and Veprek et al. [24] in silicon plasmas highly diluted with hydrogen. Research began on this material's optical properties [25], its microstructure [26] using Raman spectroscopy [27], and its electrical properties such as Hall mobility and Density of States (DOS) were studied in detail [28]. Solar cells using nc-Si:H began to appear around this time as well, as researchers realized its potential for both highly doped n [29] and p [30] layers, but also as an intrinsic layer [29] for tandem or "micro-morph" solar cells where a layer of nc-Si:H and a layer of a-Si:H is used as the intrinsic layer in a p-i-n solar cell to optimize the light efficiency of the cell. It was also discovered that nc-Si:H could be deposited at low temperatures ($< 150\,^{\circ}C$), opening the door for electronics on flexible substrates using nc-Si:H materials [31].

Thin-film device engineers have long known about the ease of which nc-Si:H can be doped, as evidenced by the use of doped nc-Si:H layers in solar cells. This is due to its crystalline content which promotes substitutional doping in the crystalline silicon lattice which allows for the creation of a donor state. Doping in a-Si:H is very inefficient because dopant atoms will mostly bond in their lowest energy configuration instead, which does not lead to a donor state. Doped n^+-nc-Si:H is currently the state-of-the-art in highly conductive source and drain contacts for TFTs [32] and was studied extensively by Kanicki et al. [33]. In that same year, the same group used nc-Si:H for the channel layer of TFTs and obtained good results [34]. Recently, top-gate TFTs using a silicon oxide dielectric have demonstrated high channel mobility and good performance [10, 22].

2.2 Pulsed PECVD

There are many different methods of depositing nc-Si:H. Thermal and/or laser crystallization can be used to produce nc-Si:H in the same way that poly-Si is produced, only using a different processing regime. The high temperatures required for thermal crystallization makes deposition on flexible plastic substrates impossible and laser crystallization adds significant costs to the process. Standard PECVD deposition using SiF_4 or $SiCl_2H_2$ gases with or without SiH_4 is also possible. One disadvantage of this technique is that it requires additional gases and gas lines which adds cost to the system. VHF PECVD uses higher frequency microwaves to excite the plasma. This technique has the advantage of increasing the slow growth rates which usually affect nc-Si:H growth. The disadvantage is that it is not scalable due to the nonhomogeneous plasma which is created. Standard SiH_4 PECVD with high H_2 dilution is the simplest and lowest cost solution. Pulsed PECVD with high H_2 dilution uses a modulated plasma, and with very little added cost (that of a pulse generator) several advantages are obtained:

- Increased growth rate
- Reduced powder particles
- Increased degrees of processing freedom

This section provides an introduction to PECVD growth of silicon films as well as the pulsed PECVD technique.

2.2.1 Conventional a-Si:H Film Growth

In the distant past, silicon thin films were being deposited by sputtering or by LPCVD. In LPCVD, SiH_4 gas is decomposed at high temperature into its constituent atoms: silicon and hydrogen. The substrate was normally heated to 500–800 ^oC, a temperature much higher than the glass transition temperature of most glasses and the melting temperature of flexible plastic substrates. PECVD, on the other hand, can be carried out at low temperature (even

room temperature) which allows silicon films of sufficient quality to be deposited on plastic at low temperature.

2.2.2 Conventional PECVD

High temperature plasmas like those formed in the Sun are normally created at extremely high temperatures ($> 4000\,\mathrm{K}$). The thermal energy causes atoms to separate from molecules and atoms to separate from ions. These ions and electrons are in thermal equilibrium. The plasmas used in PECVD are cold plasmas and are driven electrically by a source. The electric field acts primarily on the charged ions and electrons. There is continual recombination and ionization in the cold plasma and the electric field is the external energy source which allows this process to occur. The electric field acts most efficiently on the electrons, allowing them to attain very large velocities and a high effective temperature. The ions are not easily affected by the electrons or the electric field, and their energy is easily lost in collisions with the chamber walls. The electrons are not in thermal equilibrium with the ions which are at the ambient temperature which is why this is deemed a cold plasma. The high effective temperature of the electrons allows them to cause high-temperature/high-energy type reactions, which will lead to the creation of radicals which can be deposited on a substrate [35].

The basic inelastic collision reactions which occur in a SiH_4 plasma in order are:

$$\begin{aligned} SiH_4 + e^- &= SiH_2 + H_2 + e^- \\ SiH_4 + e^- &= SiH_3 + H + e^- \\ SiH_4 + e^- &= Si + 2H_2 + e^- \\ SiH_4 + e^- &= SiH + H_2 + H + e^- \end{aligned} \tag{2.1}$$

These reaction products adsorb on the film surface and the growth of a silicon film begins. Silicon-silicon bonds are formed, and some hydrogen is removed by reactions with other radicals in the plasma and ion bombardment by hydrogen. The silicon-hydrogen

molecules (radicals) on the right-hand side of the chemical formulae above can combine with other SiH_4 molecules to form larger "powder" molecules. These macroscopic "dust" particles are extremely detrimental to film quality should they become incorporated into the film. The core of the first stage of powder formation is formed by the SiH_x particles where $x = 0$–2 [36].

2.2.3 Pulsed PECVD

It is reported by Kirimura et al. [36] that "a higher-energy electron is generated during the transient phase of a DC pulse discharge compared with that in a stationary plasma and an efficient generation of radicals is observed." This is illustrated in Figure 2.1(b). These high energy electrons are generated and then they decay on a certain time scale. If we modulate the Radio Frequency (RF) plasma at a frequency corresponding to that time scale, we can effectively have those high energy electrons present continually and can take advantage of an increased radical density which will lead to faster growth (see Figure 2.1(c)).

If the plasma is modulated and the amount of radicals is increased, then there should be an even greater probability of creating large powder particles. These particles as well as other ions can be extracted from the chamber simply by turning off the RF plasma for brief periods which are sufficiently long enough [3, 4, 37]. This is shown in Figure 2.1(b) and (c) where the plasma was shut off after 0.6 ms. This leads to a reduction in the amount of powder particles, to levels which are actually well below the levels seen in conventional Continuous Wave (CW) a-Si:H growth by PECVD. This allows one to increase the RF power beyond levels used in conventional a-Si:H processing and which would normally lead to a great degree of powder formation. Kirimura et al. [36] also found that their films deposited by pulsed PECVD had a lower defect density than those deposited by CW PECVD.

This increased growth rate without loss of quality in the films is a great advantage for solar cell processing where thick $\approx 1\,\mu$m films need to be grown and "time is money." Traditionally, the RF power was increased, but this led to powder formation, as described above. Pulsed PECVD is also advantageous for growing

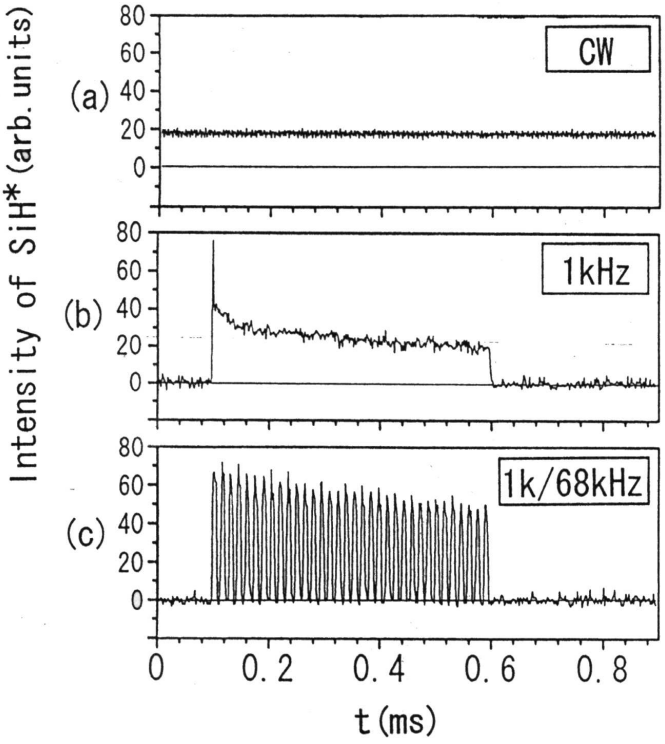

Figure 2.1: Intensity of SiH radicals in the plasma for (a) Continuous Wave (CW) case, (b) single modulated case at 1 kHz, and (c) dual-modulated case at 1 kHz and 68 kHz. From [36].

nc-Si:H for TFTs with H_2 dilution of SiH_4. The growth of nc-Si:H is normally a very slow process because of the hydrogen etching process which slows growth, but at the same time leads to some crystallinity in the film. To increase the growth rate, again, the RF power could be increased; however, this leads to powder formation and as a direct result, poor quality films. The growth rate does not need to be increased a great deal, however, since the active channel layer in a TFT is only about 50 nm anyways. What is necessary is high crystallinity in this thin layer. This is normally achieved by increasing the hydrogen dilution, however, if it is increased too much, the film may grow prohibitively slow, or perhaps not at all, as etching may dominate. Pulsed PECVD could be used together with increased H_2 dilution to obtain higher crystallinity thin films

at the same growth rate. This is just one example of how pulsed PECVD provides extra degrees of freedom in PECVD processing.

In summary,

- High energy electrons during transient phase leads to increased radical density, which leads to an increased growth rate of nc-Si:H compared to standard PECVD
- Turning off the plasma for brief periods allows radicals to escape from chamber, thus reducing powder particle formation
- Pulsed PECVD provides increased processing degrees of freedom, and is a promising technique for depositing thin film devices such as nc-Si:H solar cells and TFTs
- Pulsed PECVD is a low cost deposition technique compared to other techniques for nc-Si:H deposition

2.3 nc-Si:H Film Growth

The easiest way to fabricate nc-Si:H films using current a-Si:H processing techniques is to use PECVD with high (at least 95 %) hydrogen dilution. There are several theories concerning the mechanisms of nc-Si:H film growth. Matsuda [38] describes three models of nc-Si:H growth: the "surface-diffusion model," the "etching model," and the "chemical annealing model."

In the surface-diffusion model, the increased flux density of hydrogen atoms near the growing surface realizes full coverage of bonded hydrogen on the growing surface, and the increased hydrogen atom recombination reactions leads to some local heating at the surface [39]. All this leads to an increased surface diffusion length for silicon film precursors such as SiH_3 which have a better chance of finding the most energetically favourable bonding sites leading to the formation of crystals. This is illustrated in Figure 2.2 which shows a surface completely covered with hydrogen, and a silicon atom which is able to travel further to fill a vacant site in the crystalline lattice.

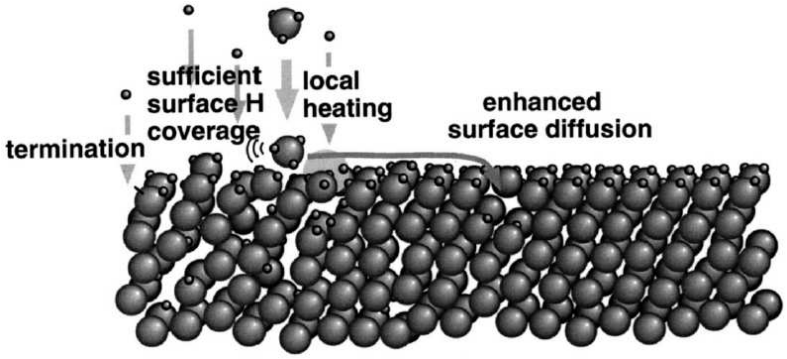

Figure 2.2: Surface diffusion model of nc-Si:H film growth. From [38].

The etching model as proposed in [40] states that due to the increase of bonded hydrogen at the surface, weak Si-Si bonds can be broken by etching when a hydrogen atom breaks a weak Si-Si bond, allowing a SiH_4 or SiH_3 species to leave the surface, which may allow a new film precursor to replace it, forming a stronger Si bonds in its place. Figure 2.3 illustrates the hydrogen bombardment of the film and shows SiH_x radicals leaving the film, making room for new radicals to fill gaps along the crystalline-amorphous boundary, making stronger Si-Si bonds and allowing the crystallites to enlarge. The etching process leads to slower growth but the slower process allows more etching reactions to occur leading to crystal growth by the formation of primarily strong Si bonds [38].

In both these models, hydrogen is a key element in explaining the growth process of nc-Si:H by PECVD.

2.4 a-Si:H and nc-Si:H Physics

a-Si:H devices have been studied for many years (since the late 1960s), hence it is a relatively well-understood material, unlike nc-Si:H. In fact, amorphous semiconductors in general have been under study for even longer. The first successful xerography machine (photocopier) was made in 1956 using amorphous selenium

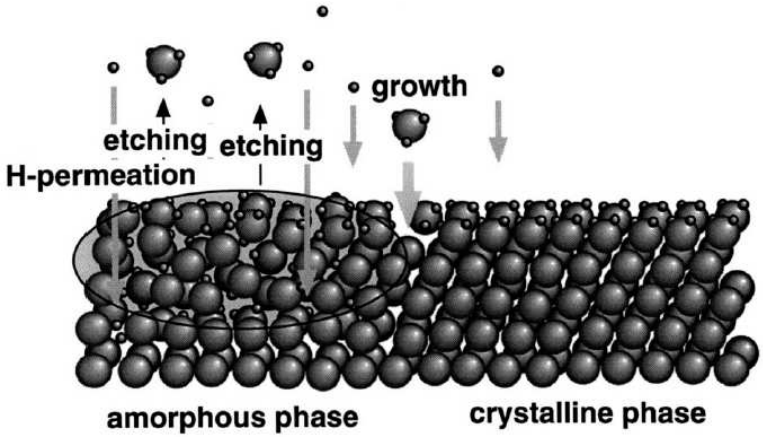

Figure 2.3: Etching model of nc-Si:H film growth. From [38].

as the photoconductor (xerography technology was invented in 1938).

A study of a-Si:H is first necessary in order to study the material properties of nc-Si:H. Since anywhere between 20 % and 80 % of nc-Si:H is made up of a-Si:H, clearly nc-Si:H will share some of a-Si:H's properties, and it is important to understand the physics of a-Si:H devices in order to understand the physics of nc-Si:H devices.

a-Si:H has no long-range order, unlike c-Si. It does, however, have some short-range order, which makes it somewhat similar to c-Si. c-Si and a-Si:H have band gaps (of $\approx 1.1\,\text{eV}$ and $\approx 1.7\,\text{eV}$ respectively), and the main chemical bond in both materials is the silicon-silicon bond. Their similarities end there, however. What follows is a discussion of the physics of a-Si:H and the certain unique effects which must be taken into account when modelling a-Si:H devices such as TFTs.

2.4.1 Basic Physics of a-Si:H

a-Si:H has considerable bonding disorder at an atomic level, and since the DOS is mostly determined by local bonding configurations, a-Si:H will have a modified DOS [41]. The bonding disorder arises from stretched bonds and bent bonds (see the left-hand side

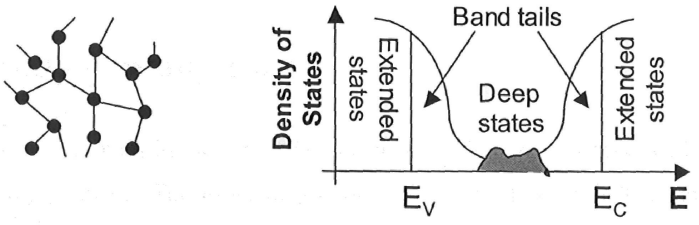

Figure 2.4: Atomic structure and band model for a-Si:H. From [19].

of Figure 2.4), which lead to a "blurring" of the conduction and valence band edge. This is referred to as the band tails, and these are shown on the right-hand side of Figure 2.4.

Un-hydrogenated a-Si also contains a large number of defect states in the mid-gap region, not just the band tails. This is due primarily to dangling bonds and impurities in the material. These mid-gap states are very highly concentrated in un-hydrogenated a-Si, but by incorporating hydrogen in the film (as in hydrogenated a-Si:H) the dangling bonds can be passivated by hydrogen and the number of these states in the mid-gap is greatly reduced.

The states located in the band tails are localized states. Localization occurs when the potential function in the semiconductor is not periodic, and it is explained in terms of the Anderson model [14]. Although the potential function in silicon does vary over many lattice spacings, it is not enough to create complete localization in the material. Instead, only the band tail states are localized. Above a certain energy in the conduction band, and below a certain energy in the valence band, there are extended states, which are not localized. The energies at which this transition to extended states occurs are sometimes called the conduction band and valence band mobility edges, and the energy spanned between these two levels is sometimes referred to as the "mobility gap". The carriers excited into the localized band tail states do not contribute very much to current because they can only travel via phonon assisted hopping. The carriers promoted to the extended states, however, can conduct much more easily in the material and have a much higher mobility. The band tail states are key to the

conduction mechanism in a-Si:H. Almost all models of electrical transport in a-Si:H makes use of some assumption about the band tail states. Some of the key ways in which the differences between c-Si and a-Si:H manifest themselves are discussed below.

2.4.2 V_t vs. V_{ON}

In a-Si:H TFTs the definition of threshold voltage is different than that used in a standard Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) model. In these devices, the threshold voltage is found by extrapolating the $\log I_D$ vs. V_{GS} curves with low drain bias. The is the point where the drain current becomes linear, and for a-Si:H TFTs devices is called V_{ON} [42]. The threshold voltage in a-Si:H TFTs actually occurs at a much lower gate bias, and this is only seen, if one looks at the gate to channel capacitance (C_{gc}) vs. V_{GS} plot, as shown in Figure 2.5.

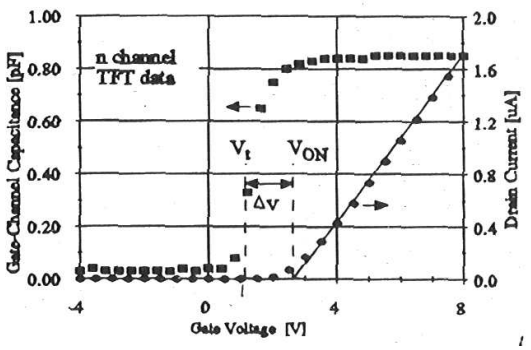

Figure 2.5: Gate to channel capacitance (C_{gc}) vs. V_{GS} for a poly-Si TFT, which resembles that of a-Si:H although to a lesser extent. From [42].

The reason that the V_t and V_{ON} voltages do not coincide in a-Si:H TFTs is that all of the carriers which are initially in the channel when $V_{GS} > V_t$ are trapped in trap states and not available for conduction. Defining V_t through the use of the C_{gc} vs. V_{GS} curve is necessary in order for any model to scale correctly with W/L.

2.4.3 Field Effect Channel Mobility

The region between V_t and V_{ON} is called the pseudo-subthreshold regime [42], and in order to take this current into account, an alternate definition of the mobility is used. An effective mobility, called μ_{FET} is used by Shur et al. [42], and is defined as

$$\mu_{FET} = \mu_0 \left(\frac{V_{GS} - V_t}{V_{AA}} \right)^{\gamma} \tag{2.2}$$

where μ_0 is the band mobility in a-Si:H[1], V_{AA} is an extracted parameter, and represents the gate voltage above V_t where the effective mobility μ_{FET} approaches μ_0. γ is an extracted parameters which like V_{AA}, can be extracted from I_D vs. V_{GS} measurements. So unlike c-Si MOSFET devices, the mobility in a-Si:H TFTs is often a much stronger function of the gate voltage.

2.4.4 Bias Stress Effects (Metastability)

Gate bias stress can cause alterations in the DOS in a-Si:H. This will effect a change in the sub-threshold slope, as well as cause shifts in the threshold voltage. The two main causes for metastability in a-Si:H devices are [19]:

1. Carrier trapping in the gate dielectric (normally a-SiN:H dielectric):
   a) Due to interface traps (fast states)
   b) Due to interface and bulk traps (slow states)
2. Deep-defect state creation in the intrinsic a-Si:H active layer or near the a-Si:H-a-SiN:H interface.

The stability of nc-Si:H has been shown to be much better than in a-Si:H [43]. It is believed that this may be due to the lower microstructural stress in these films compared to a-Si:H films; however the main reasons for the increased stability in nc-Si:H is the

[1]The band mobility is the mobility of electrons in higher energy states, as opposed to lower energy states which are prone to trapping in the band tail states.

lower hydrogen content in nc-Si:H and the more highly ordered structure which leads to fewer neutral dangling bond states.

2.5 Active-Matrix Liquid Crystal Display (AMLCD)

As mentioned above in section §2.1.1, it was discovered that a-Si:H was a great material for switching pixels in LCDs. More precisely, a-Si:H is used for the switching TFT in AMLCD. Prior to AMLCDs, LCDs used a passive matrix as in watches, calculators, or cheap hand held video games. As the pixel density/resolution increased, however, passive matrix technology was no longer suitable as crosstalk became an issue with displays larger than 100×100 pixels. Active-pixel technology was invented so that the voltage applied at each pixel was well isolated from the other pixels [11]. The TFT made a suitable low-conductivity switch when turned off, had sufficient conductivity in the on-state such that it could charge a liquid crystal pixel's capacitance, and polarize the liquid crystal.

Figure 2.6 shows a schematic of an AMLCD. Each pixel has one TFT and a pixel capacitance made up of the capacitance of the liquid crystal layer and an extra storage capacitance. The gate lines connect to the gates of the TFTs and run horizontally in "rows." The data lines connect to the drain contacts of the TFTs and run vertically in "columns."

The TFT and pixel itself can be seen more clearly in Figure 2.7. An adjacent gate line is used to form an capacitance in parallel with the capacitance of the liquid crystal, creating an additive capacitance C_{add}. In some pixels the extra storage capacitance C_{add} is necessary when the liquid crystal capacitance is not large enough. The total capacitance needs to be large enough so that the charge on the LCD pixel will remain from frame to frame and will not dischange too soon, before the frame time, which is equal to the inverse of the refresh rate.

LCDs operate by turning pixels on or off row-by-row. A gate voltage is applied to a gate line at row i (see Figure 2.6) and

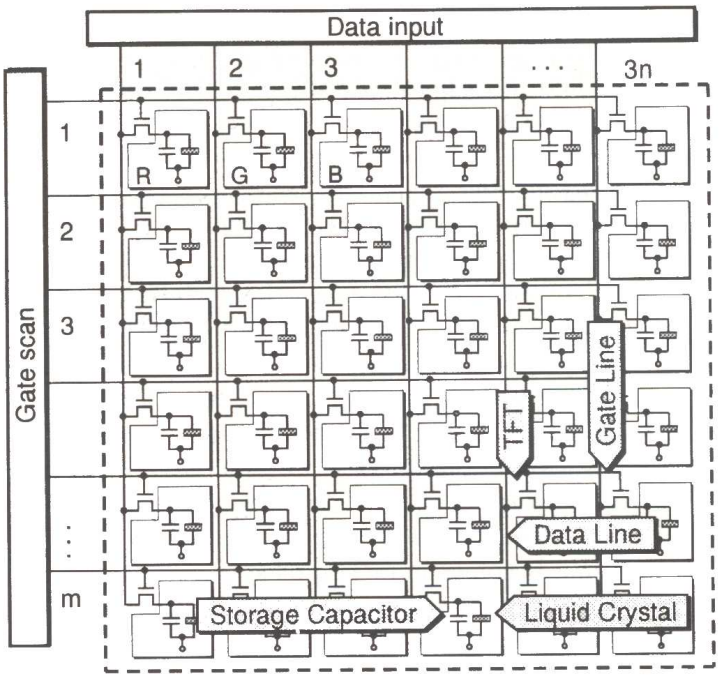

Figure 2.6: Schematic of an AMLCD panel with a single TFT at each pixel. From [11].

then data voltages are applied, where the voltage on column line j corresponds to the desired on or off state at the pixel at row i, column j. A typical waveform for this process is shown in Figure 2.8. LCD pixels operate by charging two electrodes which alters the polarization of the liquid crystal sandwiched between those two electrodes due to the electric field. When a voltage is applied across the liquid crystal the material becomes polarized and opaque, thus blocking the always-on back light from passing through the material. The liquid crystal only works effectively if it operates in AC mode, however, so on the next cycle, the pixel must be discharged and then charged in the subsequent cycles. The V_g signal shown in Figure 2.8 is applied to one pixel and the V_d is applied causing the pixel voltage V_n to charge up. In the following cycle V_n discharges, and is then charged again. This pixel is in the ON state. In the OFF state, the V_d line is held at ground

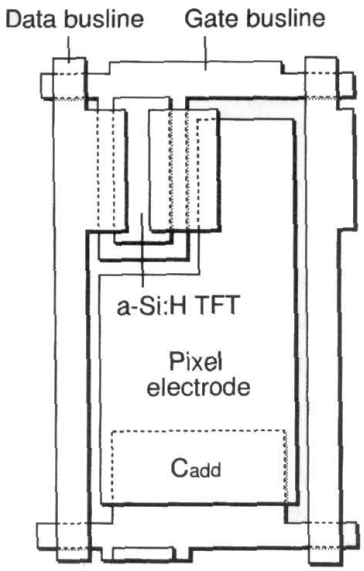

Figure 2.7: Schematic of a single pixel in an AMLCD. From [11].

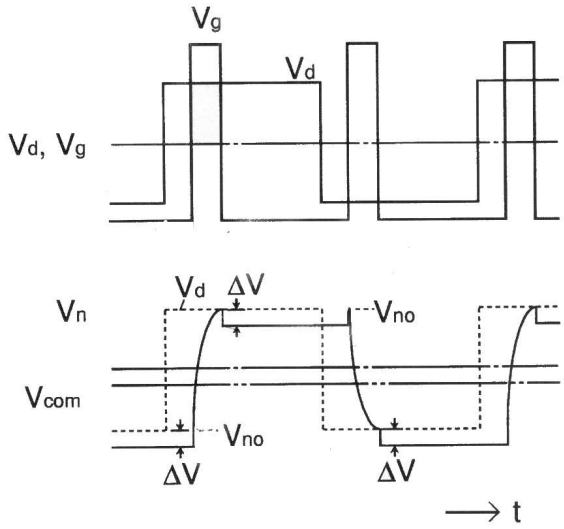

Figure 2.8: Typical waveforms used to charge and discharge an LCD pixel during each cycle, while in the "ON" state. From [11].

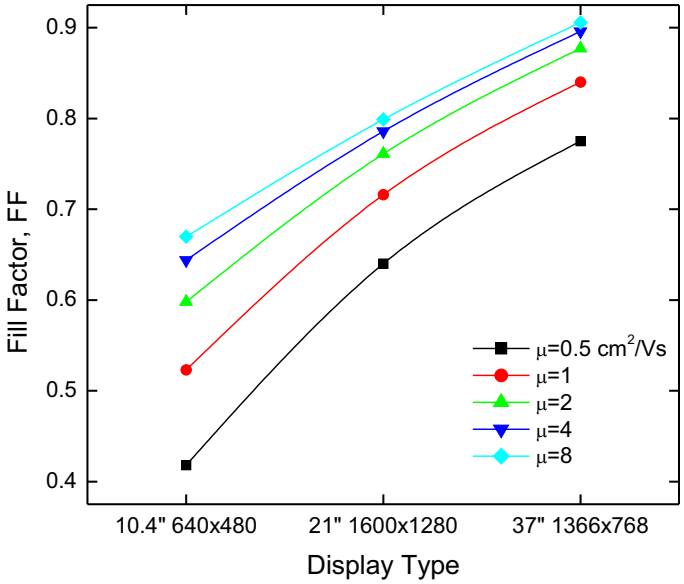

Figure 2.9: Plot of estimated fill factor for three LCD display designs using TFTs with varying mobility

and the pixel remains in the discharged OFF state.

A model of an LCD display has been created in order to see exactly what impact the improved mobility of nc-Si:H could have on LCD display charactersistics, such as resolution, fill factor, display area, and refresh rate. The equations used in the model are given in Appendix A.1.

The model was implemented in the Python language, with custom libraries to solve a set of non-linear algebraic equations. The source code is available in Appendix A.2. Mathematica was used to verify some of the equations.

Figure 2.9 shows the estimated fill factor for three LCD display designs. Figure 2.10 shows the estimated resolution for three LCD display designs. Each curve is a solution to the model with the mobility as a varying parameter. Clearly by increasing the mobility we can improve the resolution (ie. the number of pixels we can pack into the same area) due to the smaller TFT size necessary to achieve the same electrical performance in the LCD. Alternatively, we can increase the fill factor of each pixel, by allowing the extra

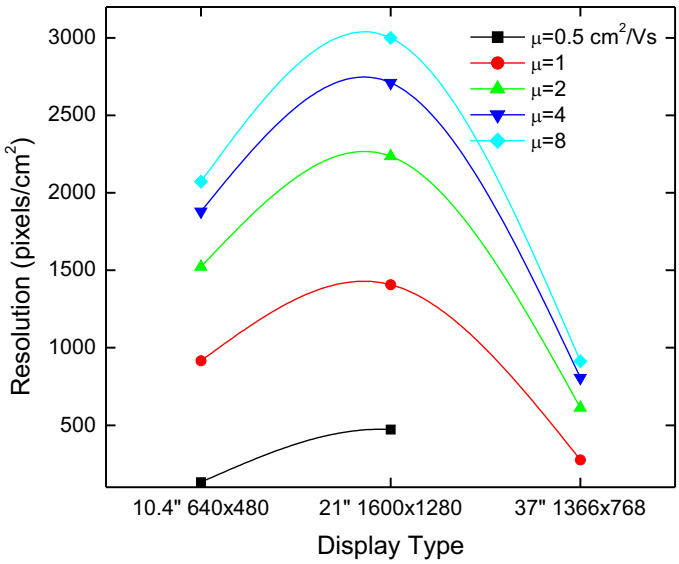

Figure 2.10: Plot of estimated display resolution for three LCD display designs using TFTs with varying mobility

space freed up by the higher mobility, smaller nc-Si:H TFT to be used as active area instead.

One of the main problems affecting TFTs is that of instability under voltage bias stress. Pixel-switching TFTs are less-affected by this since they are used in AC mode which means that during negative voltage cycles, a negative shift in threshold voltage will compensate for a positive shift during the positive voltage cycle [1]; however, they are still supseptable to some degree of instability and threshold-voltage shift compensation circuits are required [44], especially in Organic Light Emitting Diode (OLED) applications where the driving TFT does not operate in AC mode. If TFTs for OLED pixel-switching applications had a channel layer with a higher mobility, threshold-voltage shift compensation circuits could be incorporated with less impact on the fill factor since the driving TFT could be made smaller. On the other hand, if the stability of a pixel switching TFT were improved, by using a nc-Si:H channel layer for example, then threshold-voltage shift compensation circuits would not be required. Another advantage of a TFT with higher stability under gate bias stress, is that they

could be used in applications where positive voltages may be applied for long periods of time, unlike pixel-switching TFTs, such as column multiplexer and row shift register circuits [1] where a-Si:H currently cannot be used due to their high instability.

Chapter 3

Material Characterization

Several films were deposited by pulsed PECVD using different processing conditions. These films are the same films which are used later to fabricate TFTs. It is important to study a TFT material's properties in order to understand why the performance of the TFTs using that material is good or bad.

The structural analysis includes Raman spectroscopy, XRD, and AFM measurements. Electrical characterization includes two-probe conductivity, Hall effect measurements, and the stability of the conductivity under light-soaking. The optical band-gap was also measured.

3.1 Processing Conditions

A series of four silicon thin films were deposited at 150 °C using different processign conditions. The films were deposited by pulsed PECVD, using a standard 13.56 MHz PECVD process, but modulated at a pulse frequency of 65 kHz. All depositions for material characterizations were done at MVSystems, Inc., Golden, Colorado.

Material characterization was done using films of two different thicknesses (50 nm and 300 nm) grown on Corning 1737 glass with a thin (30 nm) SiN cap to prevent any contamination or post-oxidation. This cap was etched in Buffered Hydrofluoric Acid (BHF) prior to any material or electrical characterization.

Table 3.1: nc-Si:H channel layer deposition parameters.

Film	Si_4 Flow Rate	H_2 Flow Rate	Power	Pressure
1	20 sccm	0 sccm	2 W	0.4 Torr
2	4 sccm	100 sccm	100 W	1.8 Torr
3	2 sccm		40 W	
4	3.5 sccm		100 W	

Film 1 is intended to be an amorphous film and is produced with an RF power of 2 W, a plasma pulsing frequency of 60 kHz, a SiH_4 flow rate of 20 sccm, and a pressure of 0.4 Torr. Films 2, 3, and 4 are intended to be nc-Si:H films all deposited with slightly different conditions. For these films the H_2 flow rate, plasma pulsing frequency, and pressure were kept constant at 100 sccm, 60 kHz, and 1.8 Torr respectively. Only the SiH_4 flow rate and RF power were varied, between 2–4 sccm and 40–100 W respectively. This was done in order to produce differing degrees of $\langle 220 \rangle$ or $\langle 111 \rangle$ grain orientation in the crystallites [3, see Figure 2]. For films 2, 3, and 4, a plasma with a high concentration of H_2 (much higher than SiH_4) was used to grow nc-Si:H films. We define the hydrogen dilution ratio as:

$$R = \frac{[H_2]}{[H_2] + [SiH_4]}, \tag{3.1}$$

where $[H_2]$ and $[SiH_4]$ are the gas phase concentrations of H_2 and SiH_4 respectively. Film 2 was produced with a SiH_4 flow ratio of 4 sccm ($R = 96\,\%$) and a power of 100 W. Film 4 used the same RF power but with a decreased SiH_4 flow of 3.5 sccm ($R = 96.6\,\%$). Film 3 used a decreased RF power of 40 W and an even lower SiH_4 flow rate of 2 sccm ($R = 98\,\%$). The 50 nm films are labelled 50-1, 50-2, 50-3, 50-4, and the 300 nm films are labelled 300-1, 300-2, 300-3, 300-4, where the suffix denotes the process conditions used in Film 1, 2, 3, and 4 as described above. The growth rates of all the films was approximately 0.4-0.58 Å/s

The deposition parameters are summarized in Table 3.1.

3.2 Structural Characterization

There are many techniques used to obtain information about the crystallinity of nc-Si:H films. These include High Resolution Transmission Electron Microscopy (HRTEM), Spectroscopic Ellipsometry (SE), XRD, and Raman spectroscopy [45]. HRTEM is a good technique for determining the crystalline grain size but doing so is almost impossible unless the crystalline fraction is very small. Otherwise the crystalline regions will appear to overlap in the image. SE is another technique which measures the dielectric constant as a function of energy. This data is fitted to a model from which the film thickness and crystalline fraction can be extracted. XRD is commonly used to extract the crystalline plane orientation as well as the grain size (from the width of the peaks) although it is not as straightforward to find the crystalline fraction. Furthermore, to obtain a high signal to noise ratio long scan times ranging from a few hours to several days are required. AFM is another technique, in addition to XRD, which is used to find the surface roughness or grain size of a thin film.

3.2.1 Raman Spectroscopy

Raman spectroscopy is one of the easiest and most studied techniques for obtaining the crystalline fraction in nc-Si:H; however, it is still innaccurate as there are so many different ways to do the extraction. Most methods involve Gaussian or Lorentzian peak-fitting and compare the intensities or areas of crystalline and amorphous peaks. Some methods use 2, 3, or even 5 peaks, and the final result is sensitive to the fitting technique used, such as, whether or not the peaks were allowed to vary during the fitting and the range of data points used in the fitting [45].

In Raman spectroscopy a sample is irradiated with radiation in the visible to near-infrared spectrum and the shift in the incoming frequency/wavelength is measured. Most of light in a solid which is not absorbed is scattered by Rayleigh scattering, where a photon is absorbed and then re-emitted with the same energy but a different momentum direction (elastic scattering). Raman scattering is innelastic scattering in which the scattered photons have a

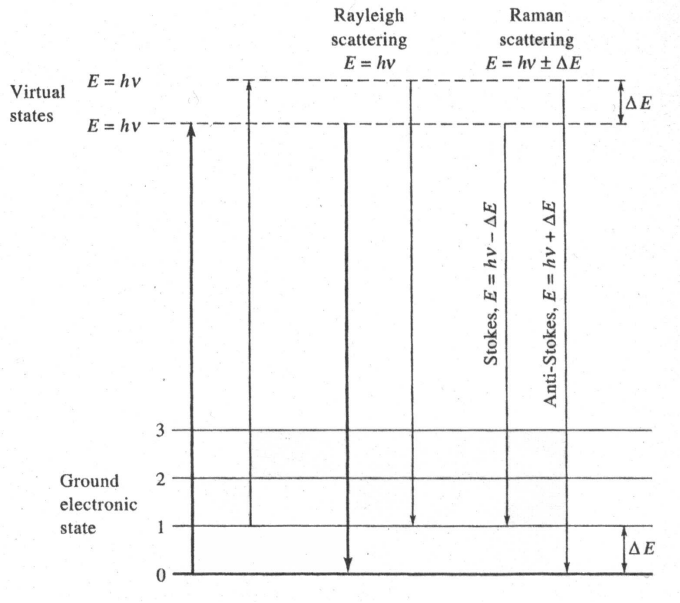

Figure 3.1: Energy band diagram illustrating initial excitation process on the two left-hand transitions, Rayleigh in the middle two, and Raman scattering (Stokes and anti-Stokes) on the right two transitions. From [47].

higher or lower energy than the incoming photons. This difference in energy is due to the vibrational energy levels (phonons) which can be excited by incoming photons. It is thus possible to observe light with less energy as the vibrational energy is subtracted from the incident photon energy (Stokes) or light with greater energy than the incident photon energy (anti-Stokes) [46, 47]. This is illustrated in Figure 3.1.

Since phonons have negligible momentum, in crystalline silicon only the phonon with 64 meV and zero momentum can be excited and this leads to a sharp peak at $520\,\mathrm{cm}^{-1}$ in c-Si. In a-Si:H the momentum selection rules are relaxed and a number of phonon modes are allowed. These form a broad peak centred around $480\,\mathrm{cm}^{-1}$ which is an indication of the broad distribution of bond lengths in a-Si:H. Raman spectroscopy is a measure of vibrational modes in a material. c-Si shows only one large narrow peak since it is a very ordered material, whereas the atomic bonds

in a-Si:H have a broad distribution of vibrational modes due to its disordered, amorphous structure.

The spectrum of nc-Si:H is not exactly a sum of the spectra of these two materials. The reason being that the spectrum from small crystallites is different from that of large crystallites. Many different methods have been employed to determine the crystalline fraction, some of which are better than others. It is often difficult to make definitive conclusions about the material in question in absolute terms, thus Raman is usually used to compare samples grown under different processing conditions in relative terms.

3.2.1.1 Experiment

Raman measurements were done using a 632.5 nm wavelength He-Ne laser. For each sample, ten readings were taken at 100 % laser power, using a 50× objective, and each scan lasting 10 s. A reference crystalline silicon sample showed an sharp peak at a Raman shift of 519.9 cm^{-1}.

The simplest method to find the the crystalline fraction is to find the intensity at 480 cm^{-1} (due to a-Si:H) and 520 cm^{-1} (due to c-Si) and take the intensity of the latter divided by the sum of the two. This method is the most inaccurate as the tail of the a-Si:H peak at 480 cm^{-1} greatly enhances the c-Si peak at 520 cm^{-1} leading to an overestimation of the crystalline fraction [48, 49]. This method will be referred to in later tables as *Intensity*. More accurate methods usually involve fitting Gaussian or Lorentzian peaks in addition to a background/baseline level to the raw data. The fitting software used for this thesis is called *Fitt*[1]. Several different fitting methods are used for the 300 nm samples. The 400–550 cm^{-1} range was used for the fitting. The first method, called *Gauss-1*, fits three Gaussian peaks and calculates their area. The crystalline fraction is then given by $X_c = (I_{500} + I_{520})/(I_{500} + I_{520} + 0.8I_{480})$, where I_n denotes the area of the Gaussian peak fitted to the data at wavenumber n [48]. The peak at 480 cm^{-1} is from the a-Si:H phase and the peaks at 500 and 520 cm^{-1} are from

[1] *Fitt* 1.2 software, provided for free by Kim [50].

the c-Si phase. The 0.8 factor is due to the larger cross-section of a-Si:H compared to the c-Si crystallites.

The above method does not always produce great fits. One variant (*Gauss-2*) of the above fitting procedure is to allow the peaks to shift slightly in order to fit the data better. Another variant (*Gauss-3*) allows only the c-Si peaks at 500 and 520 cm^{-1} to shift. An example of the output of the *Fitt* software using the latter technique with sample 300-3 is shown in Figure 3.2. On the bottom of the figure, the graph shows the fitted a-Si:H peak, which is represented by the dashed red line, and the crystalline peaks, which are represented by the dashed green and blue lines. The solid black line is the total best fit curve (or the summation of the amorphous and crystalline contributions) to the raw data represented by black dots. The fitted baseline which is automatically calculated is represented by a dashed black line and the error between the fit and measured data is the solid green line. It is a very good fit to the raw measured Raman data represented by the black dots, as can be seen from the small error represented by the green line.

The top of Figure 3.2 shows a summary of the parameters for the fit Gaussian curves. B-E is the peak location, INT is the intensity of the peak, G-W is the Gaussian width of the peak, B-L is the baseline (a constant for all the curves), and AREA is the area of the Gaussian peak. The AREA is what is used in calculating X_c as described above in the *Gauss-1*, *Gauss-2*, and *Gauss-3* methods.

3.2.1.2 Results

Attempting to extract the crystalline fraction from the 50 nm film data in Figure 3.3 does not yield any useful result as the films appear amorphous; however, one can see that the peak widths (Full-Width Half Maximum (FWHM)) of the 50-2, 50-3, and 50-4 samples are much less than that of 50-1. This may indicate that the Si films in 50-2, 50-3, and 50-4 have a different structure than the 50-1 film.

The FWHM of the 50 nm films was extracted and the values obtained are given in Table 3.2. The 50 nm samples appear most-

```
                    === CURVE PARAMETERS ===

          1           2           3
      ---------------------------------
 B-E    480.0000   500.8961<  516.3804<
 INT     18.7314<    5.8706<   10.7839<
 L-W      0.0000     0.0000     0.0000
 G-W     85.6734<   27.5153<   14.3593<
 LSE      0.0000     0.0000     0.0000
 LSI      0.0000     0.0000     0.0000
 LSW      0.0000     0.0000     0.0000
 ASY      0.0000     0.0000     0.0000
 BACK     0.0000     0.0000     0.0000
 B-L      0.0862<

AREA  682235.3125 213817.3438 392769.7812


 chi^2= 175948.062

 file= /home/david/research/Raman/mar19-04/tab delimited/s7.csv
```

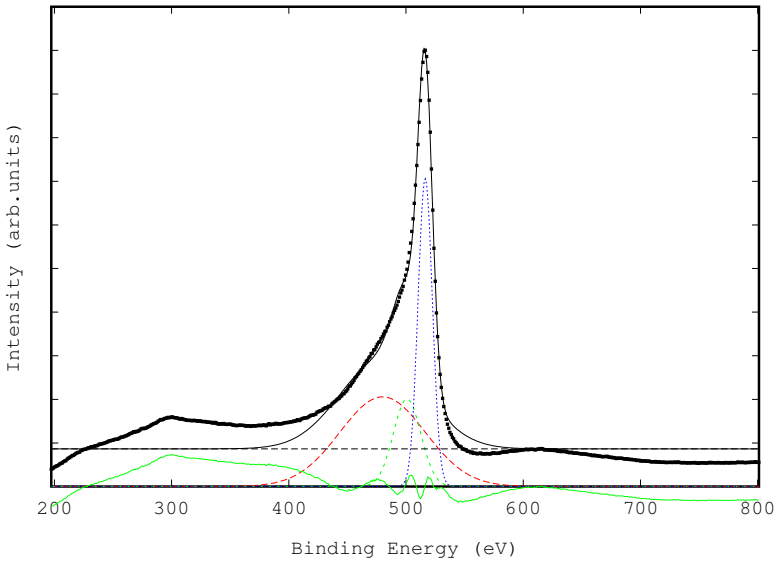

Figure 3.2: Example output from *Fitt* peak analysis software for sample 300-3. The data on top shows a summary of parameters. The graph on the bototm shows the fitted curves (red, dashed green, and blue), the error curve (dashed green), the total fitted curve (solid black), as well as the original data points (black dots).

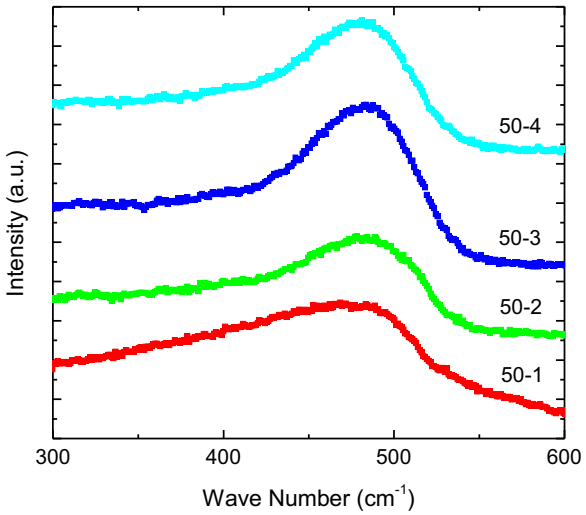

Figure 3.3: Raman measurements of 50 nm films.

Table 3.2: Summary of FWHM results obtained from Raman data for 50 nm films

Sample	FWHM (cm^{-1})	75% width (cm^{-1})
50-1	296	147
50-2	213	72
50-3	129	59
50-4	161	62

ly amorphous according to the Raman data of Figure 3.3; however, one can see that the FWHM of the 50-2, 3, and 4 samples is much less than that of 50-1 indicating a different material structure. The FWHM of a-Si:H films is a measure of the order in the film. A lower FWHM indicates less variation in Si-Si bond angle and a lower Urbach edge, and hence more order in the amorphous film [51]. From Table 3.2 we see that 50-2, 50-3, and 50-4 which were deposited under high hydrogen dilution have a lower FWHM than 50-1. Samples 50-3 and 50-4, whose 300 nm counterparts, 300-3 and 300-4 showed high crystallinity, show the lowest FWHM. This indicates that 50-3 and 50-4 have the highest order of all the 50 nm films, possibly due to the H_2 dilution which was not present while depositing sample 50-1.

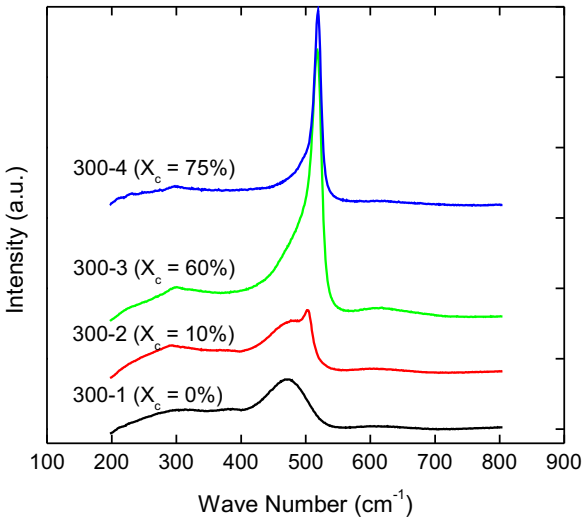

Figure 3.4: Raman measurements of 300 nm films

Table 3.3: Comparison of extracted crystalline fraction values obtained from four different Raman crystallinity extraction techniques performed on the 300 nm samples

Sample	*Gauss-1*	*Gauss-2*	*Gauss-3*	*Intensity*
300-2	10 %	20 %	10 %	26 %
300-3	60 %	56 %	60 %	76 %
300-4	75 %	31 %	79 %	80 %

The Raman data for the 300 nm samples, shown in Figure 3.4, looks much different from the data for the 50 nm samples if one compares with Figure 3.3. In Figure 3.4 one can see that samples 300-3 and 300-4 have a sharp peak at $> 500\,\mathrm{cm}^{-1}$. Sample 300-2 has a small peak at around $500\,\mathrm{cm}^{-1}$ but this is small compared to the amorphous component around $480\,\mathrm{cm}^{-1}$. Sample 300-1 is amorphous as expected.

A summary of the values obtained using different methods is shown in Table 3.3. The *Gauss-2* method is not accurate as it produces a clearly erroneous value for sample 300-4 of 31 %. *Gauss-1* and *Gauss-3* produce similar values; however, *Gauss-3* should be more accurate as it does not enforce strict peak locations

for all peaks as in *Gauss-1* which would not be accurate physically. As such, in the following discussion, data from *Gauss-3* will be used. The *Intensity* method overestimates X_c as expected due to the a-Si:H peak overlapping into the c-Si peaks.

The crystallinity is high in samples 300-3 and 300-4 (60 % and 79 % respectively) and almost negligible (10 %) in 300-2. The higher order in films 50-3 and 50-4 now makes physical sense in light of the Raman data for the 300 nm films shown in Figure 3.4. Films 50-3 and 50-4 are clearly made of a-Si:H although the material is more highly-ordered than film 50-1 which was deposited without hydrogen dilution. The incubation layer was clearly greater than 50 nm in films 300-3 and 300-4, based on the absence of crystallinity in films 50-3 and 50-4.

3.2.2 XRD

The XRD technique used for thin films is a modified form of XRD called GXRD where the x-ray beam is incident at an angle less than the total internal reflection angle. At this very small angle (typically 0.2°), part of the incident beam is reflected from the surface (specular wave) and the refracted beam is an evanescent wave which only penetrates through a small fraction of the material (only 1–10 nm deep). This evanescent wave is split into a transmitted wave and a diffracted wave. Travelling in the same direction as the diffracted wave is a specular wave which contains information about the structure of the very thin surface layer [52]. This is illustrated in Figure 3.5. The substrate is then rotated about the normal to the surface while the intensity of the diffracted specular wave is measured. Bragg diffraction peaks can be observed just as in traditional XRD. The main advantage of GXRD is it allows one to study thin films deposited on substrates. Where the substrate (polymer, glass, c-Si) would affect the data in standard XRD, in GXRD the substrate is avoided and only the structure of the thin film is measured.

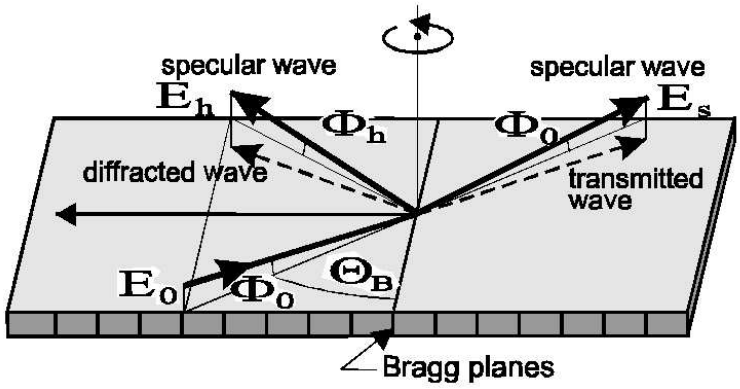

Figure 3.5: Illustration of GXRD setup showing incoming and reflected/refacted wave components . From [52].

3.2.2.1 Experiment

XRD measurements were performed on the 300 nm samples to determine the orientation of the crystal planes in the crystallites as well as the grain size. The processing conditions used (as shown in section §3.1) are known to produce differing crystallographic orientations in very thick ($\approx 0.9\,\mu m$ films [3, see Figure 2 in ref.]. XRD can also be used to determine the crystallite grain size and the crystalline fraction although this method is complicated [48] and will not be used here.

The measurements were done using a Bruker D8 Advance X-ray diffractometer [53], with a 2.2 kW copper (Cu) x-ray source. A scan speed of 0.06 °/minute was used, which gave a total scan time of 1000 minutes ($\approx$ 17 hours). A longer scan time can be used to reduce the signal-to-noise ratio even further.

3.2.2.2 Results

The XRD results are shown in Figure 3.6. The curves were smoothed using a 21-point second-order Savitzky-Golay filter, which is represented by the smooth red lines in Figure 3.6. Sample 300-2 is clearly amorphous as it cannot be distinguished from glass in Figure 3.6. The evidence of peaks in 300-3 and 300-4 confirm the presence of a crystalline phase which is also seen in the Raman

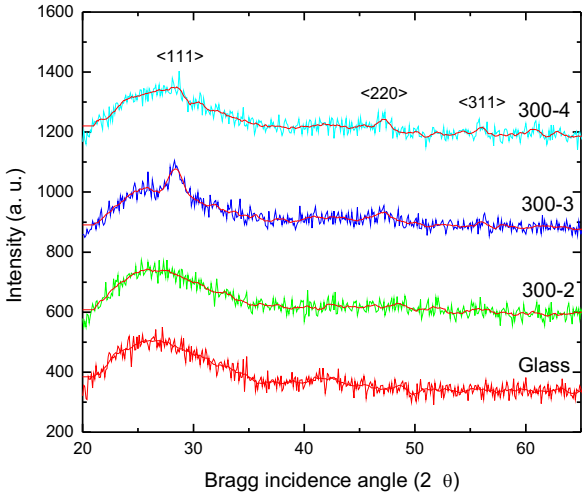

Figure 3.6: XRD curves for glass and samples 300-2, 300-3, and 300-4. The dots represent the original data, and the lines represent a 21-point second-order Savitzky-Golay moving average smoothing filter.

data of Figure 3.4. Sample 300-3 shows peaks at $2\theta = 28.3\,^\circ$, $47\,^\circ$, and $56\,^\circ$, corresponding to the the $\langle 111\rangle$, $\langle 220\rangle$, and $\langle 311\rangle$ orientations respectively. Sample 300-4 shows a very small $\langle 111\rangle$ orientation and about an equal amount of the $\langle 220\rangle$ and $\langle 311\rangle$ orientation compared to 300-3. These results are similar to the Raman measurements where it was found that samples 300-1 and 300-2 were amorphous and 300-3 and 300-4 were highly crystalline with crystalline fractions of 60 % and 75 % respectively (see Figure 3.4).

An estimate for the grain size can be estimated from XRD data using Scherrer's formula [54, See slide 9 in ref.] which is given by,

$$D = \frac{k\lambda}{\beta \cos\theta}, \tag{3.2}$$

where D is the "volume weighted" crystallite size (equal to $^3/_4\, d$ where d is the crystallite diameter), k is the Scherrer constant (somewhere between 0.9 and 1.0), λ is the x-ray wavelength, θ is the angle (in radians) at the 2θ peak, β is the "integral breadth" of the peak at 2θ, which is given by $\frac{\pi}{2}W$, where W is the FWHM

Table 3.4: Crystalline grain sizes obtained from XRD data using Scherrer's formula

Sample	Orientation	d_{XRD} (nm)	Orientation fraction
300-3	111	5.0	High
	220	4.2	High
	311	9.9	Very little
300-4	111	7.5	Little
	220	7.1	High
	311	9.0	Very little

in radians of the peak at 2θ. A summary of the grain size values obtained using the Scherrer formula for the peaks shown in Figure 3.6 along with a qualitative summary of the grain orientation is given in Table 3.4. In the important peaks, the ones that were most prominent ($\langle 111 \rangle$ and $\langle 220 \rangle$), the grain size is ≈ 5.0–$7.1\,\text{nm}$ for samples 300-3 and 300-4, while sample 300-2 showed no evidence of crystalline peaks and looked like the amorphous sample 300-1. The grain size of $< 7.1\,\text{nm}$ is smaller than other nc-Si:H results at this film thickness of 300 nm, however, it is possible that there are larger grains of contiguous crystalline material made up of many small grains (which were detected by XRD).

3.2.3 Atomic Force Microscope (AFM)

AFM is a high resolution imaging technique whereby a sharp tip is scanned across a surface and the height, z, of the material's surface is mapped out as a function of the Cartesian coordinates x and y by measuring some interaction between the probe and the sample [55]. There are several different methods of doing AFM measurements, including contact mode AFM, tapping mode AFM (TappingMode$^{\text{TM}}$), and non-contact mode AFM. Only the first two techniques will be discussed here.

In tapping mode, a cantilever tip is caused to oscillate by a piezoelectric actuator at its resonance frequency. The probe "taps" the surface and the detection electronics monitor the amplitude of the oscillations. The vertical axis stage of the cantilever is actuated so as to keep a constant amplitude of the oscillating signal, thus the

vertical position of the stage provides the topographic image of the sample surface. In contact mode AFM, a cantilever tip is scanned across the surface and the deflection from the setpoint is measured by the detection electronics. The scanner is moved vertically in order to keep the cantilever at the vertical setpoint. The distance the scanner moves vertically is stored by the electronics and forms the topographic image of the sample surface [55].

Contact mode AFM is better for rough samples and provides fast scans of the surface, although some soft samples including silicon can be damaged by scraping between the tip and sample. Tapping mode AFM provides a higher lateral resolution and eliminates scraping but provides a slower scan speed. For nc-Si:H studies tapping mode AFM is most commonly used for the reasons mentioned above [56, 57, 58].

3.2.3.1 Experiment

AFM measurements were performed in order to get an indication of the surface roughness which is approximately related to the grain size of the crystallites. Three scans each of samples 300-1, 300-2, 300-3, and 300-4 were performed, each scan being performed over a different area (and hence at a different resolution). The two-dimensional areas scanned were $10\times10\,\mu$m and $1\times1\,\mu$m. A Veeco Dimension 3100 Scanning Probe Microscopy (SPM) and Veeco NanoScope Controller was used for all AFM measurements using a a-SiN:H tip.

Before processing the AFM images, a second-order "flatten" filter was used to compensate for the z offset between scan lines (0^{th} order) and the tilt (1^{st} order) and "arch-shaped" bow (2^{nd} order) in each scan line. This filter was primarily needed for the large area ($20\times20\,\mu$m and $10\times10\,\mu$m) scans. Two different roughness measurements were used, Root Mean Square (RMS) roughness (R_q) and mean roughness (R_a). R_q is given by,

$$R_q = \sqrt{\frac{\sum_{i=1}^{N}\left(z_i - z_{avg}\right)^2}{N}}, \tag{3.3}$$

where z_{avg} is the average value of z, z_i is the value of z at point i in the region of interest, and N is the number of points. R_a is

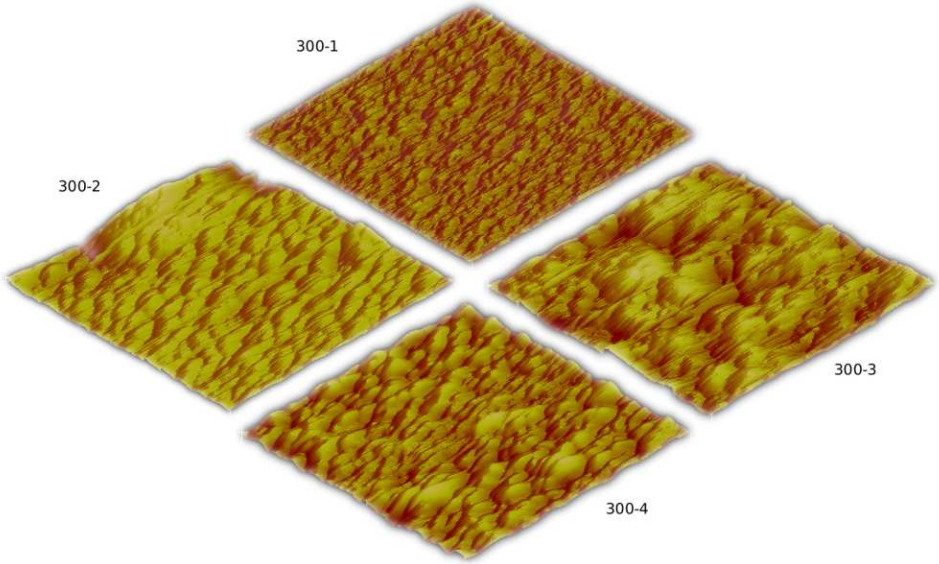

Figure 3.7: AFM images of samples 300-1, 300-2, 300-3, and 300-4 over a $1 \times 1\,\mu$m area.

given by,

$$R_a = \frac{\sum_{i=1}^{N} |z_i - z_{cp}|}{N}, \tag{3.4}$$

where z_{cp} is the z value of the centre plane.

3.2.3.2 Results

The $1{\times}1\,\mu$m and $10{\times}10\,\mu$m region AFM scans for samples 300-1, 300-2, 300-3, 300-4 are shown in Figure 3.7 and Figure 3.8 respectively. In Figure 3.7, sample 300-1 appears to be the smoothest and hence the most amorphous. Sample 300-2 definitely shows a different structure compared to sample 300-2, perhaps very tiny grains which were barely detectable using Raman spectroscopy and also not visible in the XRD plot. Samples 300-3 and 300-4 show a high roughness and clearly a different morphology compared to 300-1.

Figure 3.8 presents mostly the same results as Figure 3.7, except for sample 300-2 which shows a very unusual plot. This was

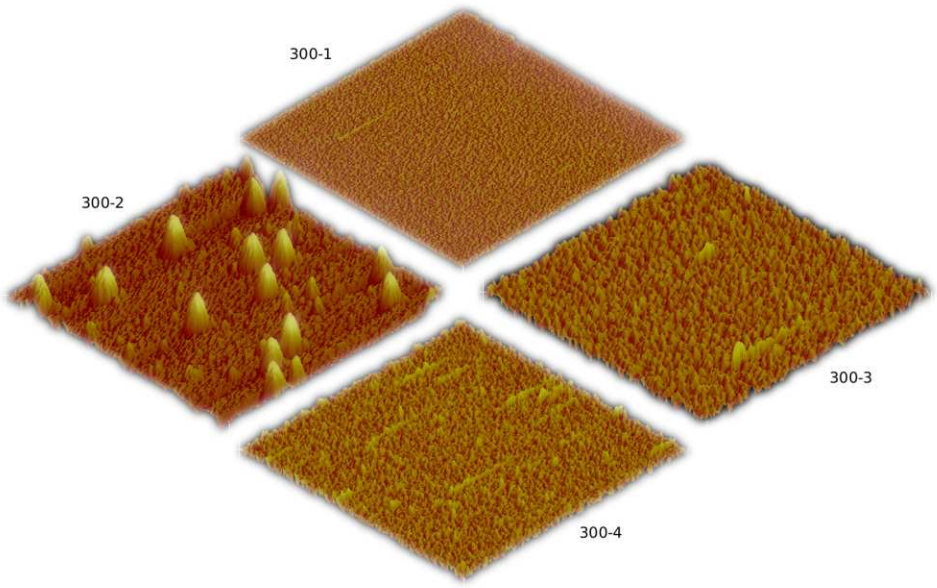

Figure 3.8: AFM images of samples 300-1, 300-2, 300-3, and 300-4 over a $10 \times 10\,\mu$m.

observable over the entire film. During Raman measurements, the strange appearance of this film was also observed as seen in Figure 3.9. The other samples looked nothing like this during Raman measurements.[2]

The results of the AFM measurement are summarized in Figure 3.10. Sample 300-1 sets a benchmark of 1–2 nm roughness for a-Si:H, while samples 300-2, -3, and -4 show roughness values R_q all in the range of 6–7 nm which are comparable to the crystalline grain size results obtained by XRD using Scherrer's formula.

[2]It is unclear whether the spots shown in Figure 3.8 and 3.9 are dirt, holes in the material, or large crystals separated by large areas of a-Si:H.

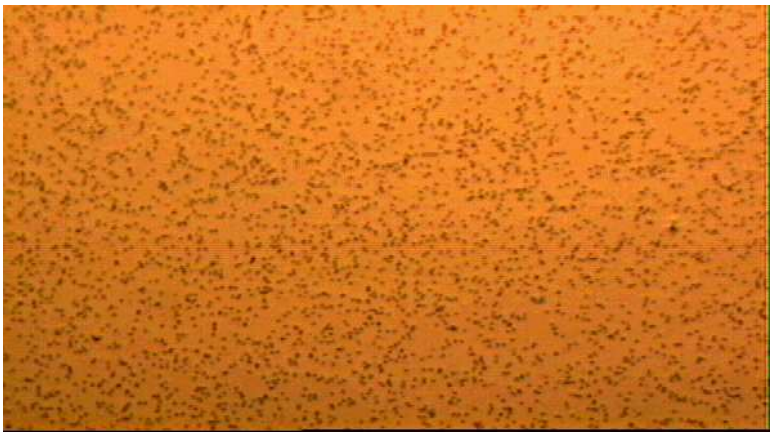

Figure 3.9: Micrograph of sample 300-2 during Raman measurements, showing unusual spots on sample

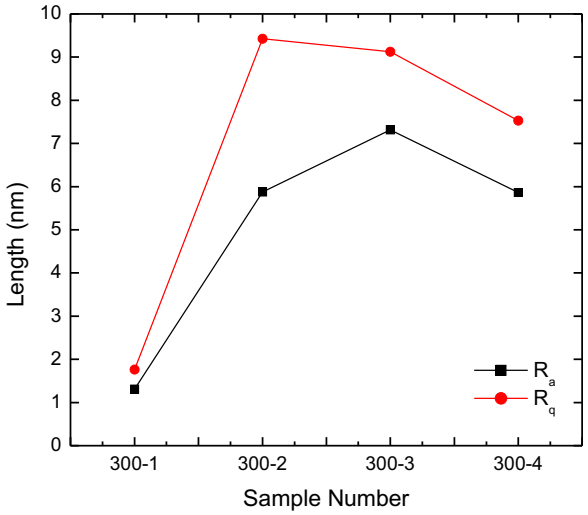

Figure 3.10: Plot of R_a and R_q acquired from AFM for the 300 nm samples over a $1 \times 1\,\mu$m area (see Figure 3.7).

3.3 Electrical and Optical Characterization

The electrical properties of the films were measured in order to determine the conductivity/resistivity as well as the mobility of the material. After determining those two parameters it is then possible to determine the concentration of free carriers in the material. The optical properties of a material are also important as it is advantageous to have low optical absorption for TFT application. One can also draw some conclusions about the material's composition based on the optical properties. Finally, the stability of the conductivity under light-soaking were also measured.

3.3.1 Two-probe conductivity

The conductivity of a material is an indication of its current-carrying capacity. The intrinsic conductivity is proportional to the speed at which the carriers can travel in the material (which is in turn related to mobility) as well as the concentration of carriers of the materials, and is given by

$$\sigma = q(n\mu_n + p\mu_p), \tag{3.5}$$

where q is the elementary charge, n and p are the concentration of electrons and holes respectively, and μ_n and μ_p are the mobilities of electrons and holes respectively.

3.3.1.1 Experiment

Initially, two-probe conductivity measurements were attempted using contacts deposited by electron beam metal evaporation through a shadow mask pattern. First aluminium was used followed by titanium, but both of these metals formed non-ohmic contacts and showed non-linear conduction behaviour. Only by using silver paste was it possible to have ohmic contacts on all samples.

Co-planar contacts were formed using a narrow strip of masking tape approximately 1 mm wide which was applied to a 1×1 cm sample after dipping the samples in BHF to remove a native oxide

layer. The silver paste was then applied on both sides of the tape and allowed to dry. The masking tape was then removed leaving two coplanar contacts. The masking tape did not cause the sample to peel.

The conductivity of the samples was measured using these co-planar electrodes with approximate spacing of 1.3 mm and a width of 10 mm. A voltage was applied and swept between 0–20 V while measuring the current. The best fit slope to this curve is taken to be the resistance, and from the resistance, the conductivity can be calculated using the formula,

$$R = \sigma \frac{L}{W \cdot t}, \tag{3.6}$$

where L is the distance between the two electrodes ($\approx$ 1.3 mm), W is the width of the two co-planar electrodes ($\approx$ 10 mm), and t is the thickness of the material, in this case either 50 nm or 300 nm, depending on which sample was used.

Photo conductivity was measured by using a 100 W tungsten filament incandescent lightbulb placed above the sample during measurement. The intensity of the lightbulb was kept constant for all measurements. The conductivity was then measured in the same way as described above for dark conductivity.

The stability under light-soaking measurements were performed by intermittently light-soaking the samples and then measuring dark conductivity (σ_d) and photo conductivity (σ_p). An Infrared (IR) filter was used to remove the IR light from the spectrum. This prevents the sample from absorbing IR light and generating electron-hole pairs, which would lead to an increase in the number of free carriers. The samples were light-soaked for 200 min. and then another 180 min. with measurements taken before and after each light-soaking step.

3.3.1.2 Results

Dark Conductivity and Photo Conductivity The dark conductivity (σ_d) and photo conductivity (σ_p) are plotted in Figure 3.11. All the 50 nm samples show a σ_{dark} value on the order

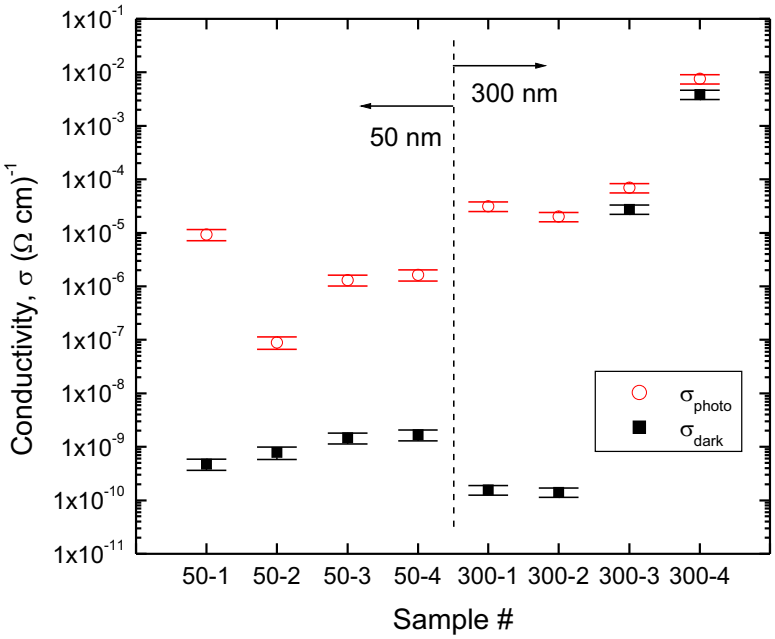

Figure 3.11: Dark conductivity (σ_d) and photo conductivity (σ_p) plotted for all samples. The short horizontal lines are error bars.

of $10^{-9}\,(\Omega \cdot cm)^{-1}$, similar to that of the a-Si:H film, 50-1. The reduced σ_{photo} in 50-3 and 50-4 compared to 50-1 may be indicative of a different film structure, which is also evident from the Raman data of Figure 3.3. nc-Si:H is known to show lower photo-response, hence the 50-3 and 50-4 films may contain tiny crystalline grains embedded in an amorphous matrix [59].

Film 300-1 accordingly shows a low σ_{dark} and high σ_{photo}, typical of a-Si:H films. Film 300-2 shows similar values of σ_{dark} and σ_{photo} even though hydrogen dilution was high during this deposition and there was some crystalline fraction, according to Figure 3.4; however, according to the Raman data in Figure 3.4 sample 300-2 is mostly amorphous. The 300-2 film easily peels off, so this may explain the low conductivity. 300-3 and 300-4 show a higher σ_{dark} ($\approx 10^{-5}$–$10^{-3}\,(\Omega \cdot cm)^{-1}$) and very small $\sigma_{photo}/\sigma_{dark}$ which is expected for these high crystallinity films [32]. This looks like n-type behaviour and may be due to native impurities and/or oxygenation contamination at the grain boundaries.

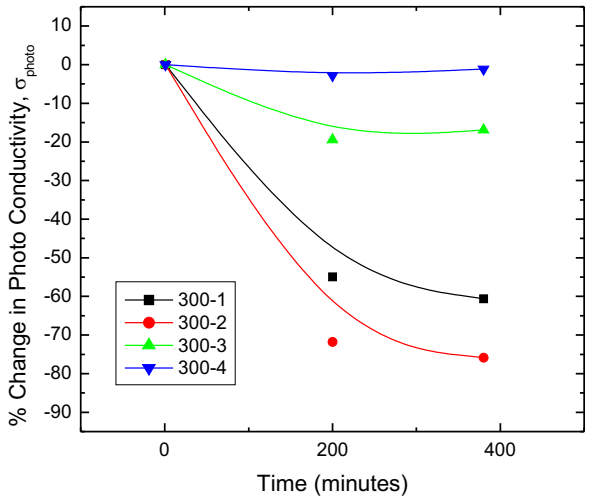

Figure 3.12: Change in photo conductivity (σ_p) in samples 300-1, 300-2, 300-3, and 300-4 versus time after light soaking.

After One Month The conductivity of the samples was measured again after one-month to determine if there was any significant absorption of oxygen which would have led to an increase in the number of free carriers due to the doping effect of oxygen in a-Si:H and nc-Si:H. There was no apparent trend and any differences in the conductivity after the one month period appear to be random or within the error bounds of the measured values. This indicates that the amount of oxygen which could be absorbed in the material had already been saturated, either during deposition or sometime before the initial two-probe conductivity was measured. Or, a stable native oxide layer had formed before the initial measurement, which blocked any further diffusion of oxygen from the air into the material.

Light Degradation The thick 300 nm samples were light-soaked as described in section §3.3.1.1. Results for the change in σ_p are shown in Figure 3.12 and the results for the change in σ_d are shown in Figure 3.13. The nc-Si:H samples, 300-3 and 300-4, show very little change whereas the more amorphous samples, 300-1 and 300-2 show a very large change in both σ_d and σ_p. Light degradation

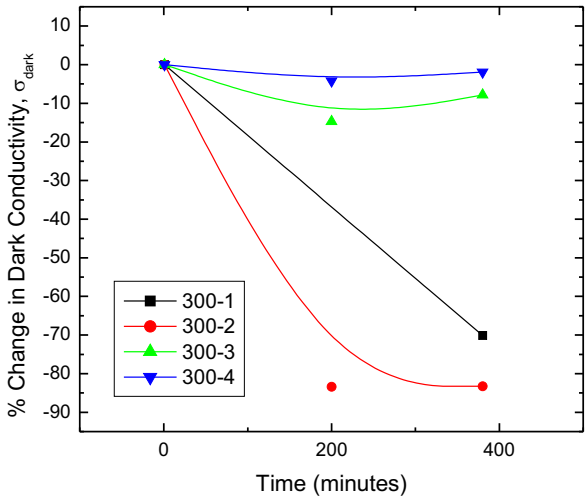

Figure 3.13: Change in dark conductivity (σ_d) in samples 300-1, 300-2, 300-3, and 300-4 versus time after light soaking.

in a-Si:H is due to the creation of metastable states and is known as the Staebler-Wronski effect [60]. This effect is readily observable in a-Si:H and much less noticeable in nc-Si:H [61, 62], due to normally lower concentrations of hydrogen in this material. 300-3 and 300-4 probably contain less hydrogen due to their higher crystalline fraction (as seen in Figure 3.4). This explains their improved stability to light-soaking over films 300-1 and 300-2.

3.3.2 Optical Band Gap

From the optical properties of a material it is possible to elucidate the electrical properties or gain some information about the structure of the material being measured. c-Si and a-Si:H have different optical band gaps so in a mixed-phase material like nc-Si:H consisting of both a-Si:H and c-Si the optical characterization can give us some idea about the material structure.

3.3.2.1 Experiment

The optical band gap was measured using a Shimadzu UV-2501 Ultra Violet (UV) spectrometer in the a-SiDIC lab at the Univer-

sity of Waterloo. The 380–900 nm range was using fairly standard instrument setup parameters. The background was measured from the ambient air, and a glass sample was used as a reference so that it would be subtracted in real time from the measurement of the glass wafer with the thin film. The UV frequency is sweeped over a certain range and the transmission through the film and the glass wafer is measured.

The transmission function is given by

$$T = \frac{(1 - R_{01})^2 (1 - R_{12})^2}{n_2} e^{-\alpha d}, \tag{3.7}$$

where R_{01} is the reflectance from air into the thin film, R_{12} is the reflectance from the glass into the air on the other side of the glass, n_2 is the reflective index of the glass wafer, n_1 (to appear) is the reflective index of the thin film, α is the optical absorbtion coefficient of the thin film (assuming absorption by the glass is negligible in comparison), and d is the thickness of the thin film. The T is what is measured by the UV spectrometer apparatus, and all other variables are known except for α which is what one wants to find, as a function of incoming frequency/wavelength, in order to find the band gap.

Re-arranging (3.7), we have

$$\alpha = -\frac{1}{d} \log \frac{T}{A}, \tag{3.8}$$

where A is given by

$$\begin{aligned} A &= \left((1 - R_{01})^2 (1 - R_{12})^2 \right) / n_2 \\ &= \left(\left(1 - \frac{n_0 - n_1}{n_0 + n_1} \right)^2 \left(1 - \frac{n_1 - n_2}{n_1 + n_2} \right)^2 \right) / n_2, \end{aligned} \tag{3.9}$$

and when $n_0 = 1$ (air), $n_1 = 3.42$ (a-Si:H), and $n_2 = 1.5$ (glass), $A \approx 0.59$ or 59 %. Taking the transmittance data T and applying (3.8), we get values for α as a function of frequency. The Tauc plot is then made by plotting $(\alpha\hbar\omega)^{1/2}$ versus $\hbar\omega$, and the x intercept will give the optical band gap E_g according to Street [14, see pages 88–89 in ref.].

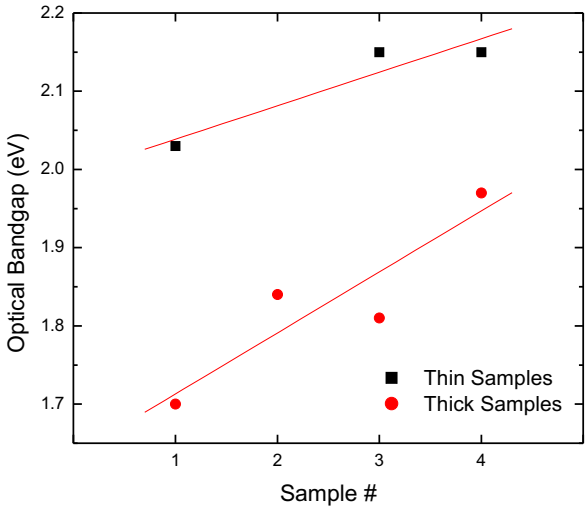

Figure 3.14: Optical band gap data for 50 nm and 300 nm samples.

3.3.2.2 Results

The optical band gap was estimated by a linear fit to the linear portion of a Tauc plot as described above and the values obtained for the band gap are shown in Figure 3.14. For the 50 nm samples, the slight upward trend may indicate the presence of a different structure in 50-3, and 50-4; possibly tiny crystalline grains [59], undetectable by Raman spectroscopy. The data for the 300 nm films shows a trend in the band gap with increasing film crystallinity, which supports the trend seen in the 50 nm samples. The reduced σ_{photo} and increased σ_{dark} of 50-3 and 50-4 in Figure 3.11, and the increased band gap in Figure 3.14 indicates that the 50-3 and 50-4 films may contain fine crystallites embedded in an amorphous matrix [59].

3.4 Hall Effect Characterization

To confirm the n-type nature of sample 300-4 (and indirectly sample 300-3) which is apparent from the conductivity data (see Figure 3.11), the Hall mobility and carrier density were calculated from the Hall voltage for this sample. The Hall mobility also pro-

vides a good metric for the material's quality compared to other nc-Si:H films.

3.4.1 Mobility

There are four different types of mobility used to describe the motion of carriers in thin-film materials like a-Si:H: free-carrier mobility, μ_0; time-of-flight or drift mobility, μ_d; field-effect mobility, μ_{FET}; and Hall-effect mobility, μ_H. Each of these mobilities will have a different value in any given material. The differences in these values stem from the physical property which is being measured, as well as differences in the measurement techniques themselves.

3.4.1.1 Time-of-flight/drift mobility

The basic definition of drift mobility is

$$\boldsymbol{v_d} = \mu_d \boldsymbol{E} \tag{3.10}$$

where $\boldsymbol{v_d}$ is the drift velocity of the carrier and $\boldsymbol{E}$ is the electric field in the sample. Carriers are constantly accelerated and decelerated by the electric field and by scattering events respectively, and in a-Si:H and nc-Si:H carriers are frequently trapped in trap states in the energy gap. The drift velocity is an average velocity of the carrier over time scales much longer than the time that it takes for a carrier to be trapped.

The drift mobility is measured on a thin-film sample with electrodes on two surfaces, to create a capacitor-like structure. An electric field is applied across the two electrodes, creating a constant electric field across the sample. Electron-hole pairs are generated at one end of the sample by photo-excitation, which then move to either electrode due to the electric field. If one wants to measure the drift mobility of electrons, then electron-hole pairs must be generated near the positive electrode, so that the electrons can move towards the positive electrode, while the holes move a short distance into the negative electrode. When a charge Q_{ph} moves a vertical distance y in the sample, it will induce a charge

of

$$Q_T = \frac{Q_{ph} y}{d} \tag{3.11}$$

on the electrodes, where d is the sample thickness. The current through the external circuit is thus

$$I = \frac{dQ_T}{dt} = \frac{Q_{ph}}{d}\frac{dy}{dt} = \frac{Q_{ph}}{d} v_{d_y} = \frac{Q_{ph}\mu_{d_y} E_y}{d}. \tag{3.12}$$

According to (3.12), the current is directly proportional to the mobility. The faster the carriers move across the sample, the higher the magnitude of the current; however, it is difficult to determine Q_{ph} with precision. Instead the transit time is measured, which is given by,

$$\tau_t = \frac{d}{\mu_d E}. \tag{3.13}$$

The transit time can be determined for many different voltages (and hence electric field magnitudes), and the mobility should remain constant at least at room temperature [14]. One of the limitations of this method is that it measures the drift mobility in the vertical direction, making it not so useful for anisotropic samples where conduction in the lateral direction is important. In order to measure the drift mobility in the lateral direction, it would be necessary to deposit electrodes on the sidewall of a thin film, which can be rather difficult.

3.4.1.2 Free carrier mobility

In amorphous semiconductors, the free carrier mobility is the mobility of carriers without the presence of traps. Or, if it were possible to measure the speed of a carrier between trapping events, this would yield the free carrier mobility. If the exact density of states were known, then the free carrier mobility can be estimated from the drift mobility [14] as follows,

$$\mu_d = \frac{\mu_0}{1 + f_{trap}} \tag{3.14}$$

where f_{trap} is the fraction of the time the carrier spends in the traps relative to the time spend in conduction states, and μ_0 is the free carrier mobility.

3.4.1.3 Field-effect mobility

The field-effect mobility is important when dealing with TFTs. It describes the mobility in the channel of the TFT during various bias conditions. It is essentially the same as the drift mobility, only it is measured under non-equilibrium conditions. The field-effect mobility, μ_{FET} can be measured in the linear or saturation region. In a-Si:H, the mobility is modelled as a weak function of the gate voltage [42], whereas in some nc-Si:H TFT, the mobility is a much stronger function of the mobility [63].

3.4.1.4 Hall-effect mobility

The Lorentz Force Law states that a charged moving through a magnetic field will experience a force perpendicular to the magnetic field and to the particle's direction. This force is proportional only to the component of the magnetic field which is perpendicular to the particle's velocity vector. It is expressed as follows,

$$\boldsymbol{F} = Q\boldsymbol{v} \times \boldsymbol{B} \tag{3.15}$$

The charge Q is positive for holes and negative for electrons. The velocity v is in the same direction as the current for holes and in the opposite direction for electrons. This leads to two sign changes when substituting holes for electrons, so the force experienced on electrons and holes is in the same direction. In a rectangular slab-type sample, like that shown in Figure 3.15 below, holes will be pushed in the negative y direction by the Lorentz force, and the electrons will be pushed in this direction as well. When the electrons and/or holes accumulate on one side of the sample due to this force, they will cause an opposing electric field in the y direction, called E_y. This will impede any further charges from approaching the edge of the sample. In steady-state these two forces in the y direction will be equal,

$$E_y Q = Q v_d B_z, \tag{3.16}$$

where we have replaced v with the drift velocity v_d. We also know that the current density in the x direction can be expressed as

$$J_x = -qnv_d, \tag{3.17}$$

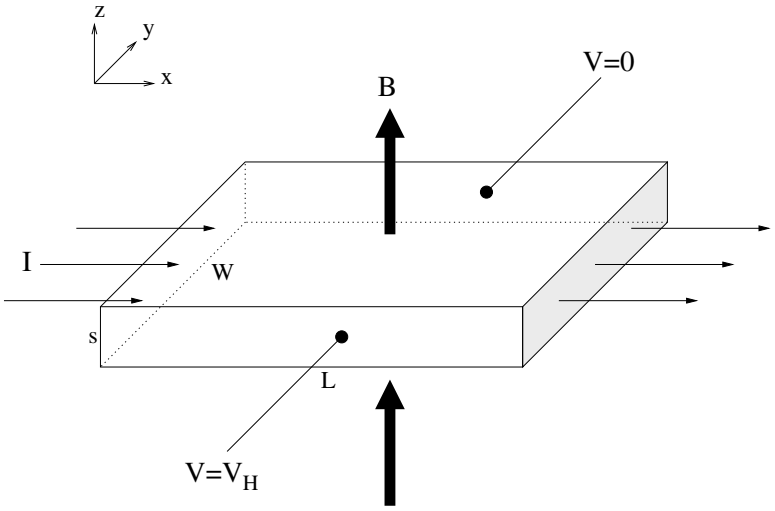

Figure 3.15: Diagram explaining Hall effect

and solving for v_d we get

$$v_d = -\frac{J_x}{qn}. \tag{3.18}$$

Assuming v_d is the same in the x and y directions, substituting v_d into (3.16) we have

$$E_y = -\frac{J_x B_z}{qn}. \tag{3.19}$$

Since E_y can be approximated as V_{H_y}/W where W is the width of the sample in the y direction, and $J_x = I_x/(tW)$, where s is the sample thickness, we can rearrange (3.19) in terms of V_{H_y}:

$$V_H = V_{H_y} = \frac{I_x B_z}{qnt} \tag{3.20}$$

where V_H is known as the Hall voltage. (3.20) is sometimes expressed in another way,

$$V_H = R_H \frac{I_x B_z}{t}, \text{ where } R_H = \frac{1}{qn}. \tag{3.21}$$

If the conductivity given by $\sigma_n = q\mu_H n$ is known, and the density of electrons, n, is known then we can find the mobility. This mobility μ_H is not exactly the same as the time-of-flight/drift mobility,

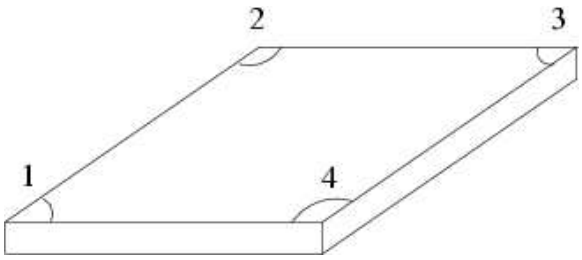

Figure 3.16: Van der Pauw geometry used in this thesis. The quarter-circles at the corners represent the metallic contacts.

and is called the "Hall mobility,"

$$\mu_H = R_H \sigma, \tag{3.22}$$

where σ is the conductivity. The Hall mobility is calculated from the measured Hall voltage V_H using the formula

$$V_H = \mu_H \frac{I_x B_z}{\sigma_n t}. \tag{3.23}$$

Performing a Hall experiment where the applied current/voltage, the conductivity, and the magnetic field are known will allow one to solve for μ_H.

3.4.2 van der Pauw Measurements

Van der Pauw presented a new method to measure the Hall effect and conductivity using a simple geometry which had advantages over previous methods which used six-probe geometries which were difficult to fabricate. An example Van de Pauw geometry is shown in Figure 3.16. Van der Pauw's method is a general method which applies to any material, as long as it is thin, has no holes, and has four contacts placed along the periphery of the material.

Once the required sample is available, the measurement is performed as follows: First find R_S, the sheet resistance. This is related to the resistivity by the thickness t,

$$\rho = R_S \times t[\Omega \cdot \text{cm}]. \tag{3.24}$$

So if the resistivity and thickness are measured, then R_S is known. Next, we apply a current I between two adjacent contacts, a magnetic field B (measured in Gauss) and we measure the Hall voltage V_H across the two remaining contacts. From this we can find the sheet carrier density, n_s:

$$n_s = 10^{-8}\frac{IB}{qV_H}[\mathrm{cm}^{-2}] \tag{3.25}$$

where the sheet carrier density n_s is given by $n \cdot t$, and n is the carrier density in units of cm^{-3}. Once R_S and n_s are known we can find the Hall mobility,

$$\mu_H = \frac{1}{qn_sR_S}[\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}] \tag{3.26}$$

Further details on this procedure can be obtained at [64].

The hardest part of the measurement may be to measure the Hall voltage. What Hall voltage can one expect to have to measure in a-Si:H or nc-Si:H? Assume:

1. Magnetic field of $10,000\,\mathrm{Gauss}$ (or $1.0\,\mathrm{T}$).
2. Applied voltage is between 10 and $100\,\mathrm{V}$ to produce the injected current.
3. A square sample is used, such that the applied voltage, V_A satisfies $V_A = IR_S$.

Re-arranging (3.25) to solve for V_H,

$$V_H = 10^{-8}\frac{IB}{qn_s}. \tag{3.27}$$

Substitute for n_s using (3.26), and we get,

$$V_H = 10^{-8}IBR_S\mu_H. \tag{3.28}$$

Since we assumed a square sample and that $R_S = \frac{V_A}{I}$,

$$V_H = 10^{-8}BV_A\mu_H. \tag{3.29}$$

One sees that the Hall voltage is independent of the thickness of the sample. For the worst-case situation of an applied voltage of 10 V, a magnetic field B of 10,000 Gauss and a mobility of 0.01 cm^2 V^{-1} s^{-1} (poor quality a-Si:H), the expected Hall voltage is around 10 uV. For the best-case scenario, of an applied voltage of 100 V and a mobility of 1.0 cm^2 V^{-1} s^{-1} (good a-Si:H or nc-Si:H), the expected Hall voltage is 10 mV. These voltages are not too difficult to deal with in principle. A problem arises in the fact that there is often a voltage offset between the two Hall voltage contacts *prior to the magnetic field being applied*. If the initial voltage across these leads is too large, it may be impossible to discriminate the small change in voltage causes by the Hall effect. Another problem is that the sample resistance may be very large, which amounts to attempting to measure a small voltage from a source with a high resistance, a difficult task.

There are thus two requirements for being able to measure the Hall voltage adequately on a sample. First, the Hall voltage needs to be large enough such that it can be measured. Secondly, the resistance of the sample across the Hall voltage leads must not be too high. Measuring a small voltage across a large resistance is an impossible feat. For example, in order to measure a 10 μV Hall voltage on a sample with a resistance of $10^{13}\,\Omega$ (a conservative value for intrinsic a-Si:H one would require a resolution of about 1 μV. Ted Wilson describes the challenge as follows:

> I can't believe the $10^{13}\,\Omega$ source resistance isn't a typo? If it's not, you're going to require some form of bias current cancellation and an offset current performance in the two buffers equivalent to better than an 10^{-19} A, (0.1 atto-Amps I believe). That's one hell of an amplifier - I would guess, several orders of magnitude beyond state-of-the-art capability! [65]

and Sphero Pefhany describes it as follows:

> The $10^{13}\,\Omega$ sounds like the real bear. A 10 % (1 μV) error at $10^{13}\,\Omega$ is a current of 10^{-19} A—less than 1 electron per second—clearly in the realm of physics rather than electronics [66].

Clearly it is not possible to measure the Hall effect in intrinsic a-Si:H because of its high resistance. Doped a-Si:H is frequently used instead because of its much higher conductivity. It can also be very difficult to measure the Hall effect of nc-Si:H, which can have a conductivity as low as $10^{-8}\,(\Omega \cdot cm)^{-1}$. If doped nc-Si:H is used instead (either intentionally doped, or unintentionally doped, by oxygen for example), the conductivity is much higher, the source resistance is lowered, and the Hall voltage can be easily measured.

Gallium arsenide (GaAs) has a very low conductivity, however, Hall measurements have been performed on this material in the past. Its saving grace is that it has a very high mobility (about $10{,}000\,\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$), so according to (3.29) the Hall voltage will be very large.

A minor concern during Hall measurements is Joule heating in the sample, which does depend on the thickness of the sample. We would prefer no more than 1 mW of heating in the sample, so

$$\begin{aligned} 1\,\mathrm{mW} &> V_A^2/R_S \\ 1\,\mathrm{mW} &> V_A^2 t\sigma_d \end{aligned} \tag{3.30}$$

So for high conductivity samples, we should use thinner samples to avoid heating effects, and for low conductivity samples they should be made thicker to improve the source resistance of the Hall voltage.

3.4.2.1 Experiment

The Hall effect mobility was measured using a method similar to that described in Le Comber et al. [67]. The experiments were done at the University of Toronto using the apparatus shown in Figure 3.17 and Figure 3.18. Figure 3.17 shows the dewar with sample holder on the far right of the image. The dewar allows the sample to be cooled using liquid nitrogen or heated using a resistance heater. A control system enables the dewar and sample holder to maintain a constant temperature. It is sealed at the top which allows the chamber with the sample inside to be pumped down to low pressure vacuum. Figure 3.18 shows the magnet and cylindrical vacuum chamber in which the dewar was inserted.

Figure 3.17: Dewar and sample holder used to hold sample for Hall effect measurements

Figure 3.18: Magnet at the University of Toronto, which was used for Hall effect measurements showing cylindrical vacuum chamber in which dewar and sample holder with sample mounted was inserted

The magnet was able to produce a maximum field of $\approx 0.43\,\mathrm{T}$ (or 4300 Gauss) and that was the field strength that was used during the experiment. The measurements were done at atmospheric pressure at a constant temperature $25\,^{\circ}\mathrm{C}$.

A square sample with dimensions $1\,\mathrm{cm} \times 1\,\mathrm{cm}$ was used, with small ohmic aluminium (Al) contacts deposited on each corner by election-beam evaporation through a custom-made shadow mask.

The change in the Hall voltage was measured as the magnetic field was reversed multiple times, as in Le Comber et al. [67]. The change in Hall voltage is equal to $2V_H$.

3.4.2.2 Results

Although the sample and contacts have a suitable van der Pauw geometry, the full set of van der Pauw measurements were not performed. Normally in van der Pauw measurements, the following eight resistances are first measured to obtain the conductivity/resistivity:

$$\begin{aligned} R_{21,34} &= V_{34}/I_{21}, \\ R_{12,43} &= V_{43}/I_{12}, \\ R_{32,41} &= V_{41}/I_{32}, \\ R_{23,14} &= V_{14}/I_{23}, \\ R_{43,12} &= V_{12}/I_{43}, \\ R_{34,21} &= V_{21}/I_{34}, \\ R_{14,23} &= V_{23}/I_{14}, \text{ and} \\ R_{41,32} &= V_{32}/I_{41}, \end{aligned} \tag{3.31}$$

where the sample has contacts on the corners numbered consecutively around the perimeter as in Figure 3.16. $R_{ab,cd}$ is then the voltage measured across contacts c and d with a current applied from contacts a to b. In (3.31), every second measurement is redundant so half the measurements could be left out, although ideally it is best to perform all measurements as a consistency check. Normally the resistances calculated above are averaged, and then the actual sheet resistance of the sample, R_S is calculated according to van der Pauw's relation [68],

$$e^{-\pi \frac{R_A}{R_S}} + e^{-\pi \frac{R_B}{R_S}} = 1, \tag{3.32}$$

where

$$\begin{aligned} R_A &= (R_{21,34} + R_{12,43} + R_{43,12} + R_{34,21})/4 \\ R_B &= (R_{32,41} + R_{23,14} + R_{14,23} + R_{41,32})/4. \end{aligned} \tag{3.33}$$

If R_A and R_B are similar (ie. if $R_A/R_B < 1.4$) then $R_S \approx (\pi/\ln(2))(R_A + R_B)/2$. Interestingly, this is the same formula that is used for calculating the sheet resistance of an infinite thin sheet using the four probe technique.

In this experiment, the resistance $R_{13,13}$ was used instead as the sheet resistance R_S. Our samples are square, the contacts are relatively small compared to the sample size, and the samples demonstrate a high degree of symmetry so this two probe measurement can be shown to be a good approximation and is far easier than doing four probe measurements as described above. The suitability of this approximation was proved using a Keithley SCS-4200 at the University of Waterloo and the difference between thetwo methods was minimal.

For the measurement of the Hall voltage of sample 300-4 a voltage of $V_{13} = 100\,\mathrm{V}$ was applied to contacts 1 and 3 to generate a current from contact 1 to 3, and the Hall voltage was measured across contacts 2 and 4. $R_{13,13}$ was measured in real time during the experiment by measuring the current sourced by the 100 V source which was applied to contacts 1 and 3. The average value of $R_{13,13}$ was $6.87\,\mathrm{M\Omega}$.

The magnetic field was switched between 4300 Gauss and -4300 Gauss. The change in Hall voltage while switching between the positive and negative magnetic field was measured as shown in Figure 3.19. The change corresponds to $2V_H$. An average Hall voltage (V_H) of 1.15 mV was observed. From this Hall voltage value, one can calculate the sheet carrier density, n_s,

$$n_s = 10^{-8}\frac{IB}{qV_{avg}}, \tag{3.34}$$

where I is the applied current through contacts 1 and 3, which was on average $14.6\,\mu\mathrm{A}$, B is the magnetic field in Gauss which was on average 4310 Gauss, q is the elementary charge, and V_{avg} is the average mesaured Hall voltage, which was on average 1.15 mV as mentioned above. From this one gets an average sheet carrier density of $n_s = 3.43 \times 10^{12}\,\mathrm{cm}^{-2}$. Since

$$n_s = nt, \tag{3.35}$$

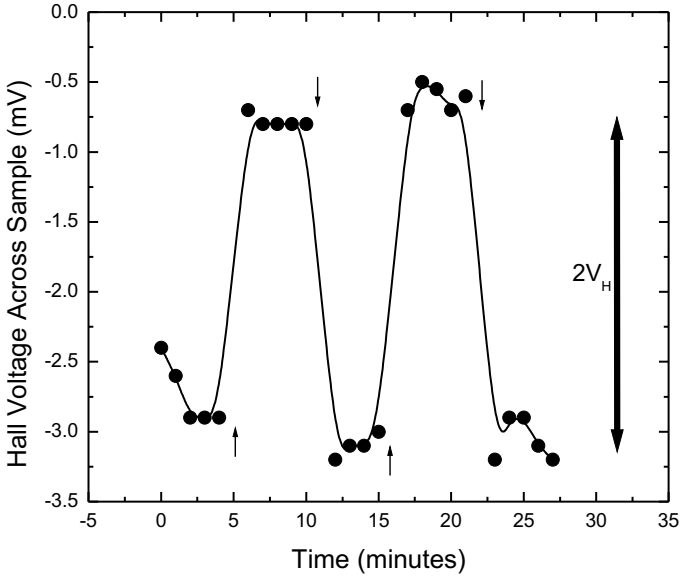

Figure 3.19: Hall voltage (V_H) measured over time on Sample 300-4 as the magnetic field was reversed at the points indicated by the arrows

where t is the thickness of the sample, we find that $n = 1.1 \times 10^{17}\,\mathrm{cm}^{-3}$. One can use a final relationship to find the Hall mobility of the sample, and that is

$$\mu_H = \frac{1}{q n_s R_S}. \tag{3.36}$$

Applying (3.36) using n_s and R_S from above one calculates a mobility of $\mu_H = 0.27\,\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$. The value for the carrier concentration, n, is much higher than that in intrinsic silicon ($\approx 10^{10}\,\mathrm{cm}^{-3}$), and therefore we conclude that the sample 300-4 is doped and that the high σ_{dark} in 300-4 (and also 300-3) is probably mostly due to oxygen contamination in the film, which is known to act as a donor along the grain boundaries of nc-Si:H [69]. High oxygen contamination in intrinsic material is not good for TFT performance as the TFT leakage current increases dramatically. It increases leakage in TFTs significantly, although bottom-gate TFTs to a lesser extent than top-gate TFTs. There are several methods to prevent oxygen contamination, however, such as depo-

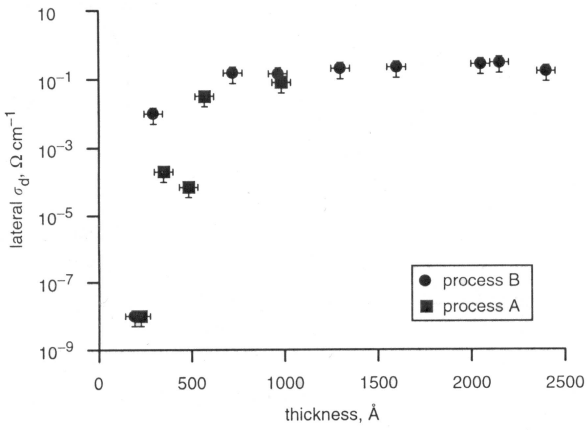

Figure 3.20: Conductivity vs. thickness for nc-Si:H films deposited by pulsed PECVD. From [4, see Figure 5].

sition of nc-Si:H by PECVD using $SiCl_2H_2$ [70], oxygen gettering of the inlet gasses [69], and p-microdoping [71].

3.5 Discussion

According to [4] the onset of crystallinity was expected to occur at a thickness of less than 50 nm, as seen in Figure 3.20, because the conductivity plotted in the figure is highly dependant on the crystallinity and shows a rapid increase at a thickness less than 50 nm. Thus one would expect to see the 50 nm films show some crystalline phase and the benefits of nc-Si:H such as better stability and higher mobility

From the results above the 50 nm samples appear to be amorphous and the 300 nm samples with the same processing conditions are crystalline. The crystallinity clearly improves the thickness, however 50 nm is too thin to see any major crystalline contribution. Samples 50-3 and 50-4 are made up of an incubation material which later developed into a crystalline structure in the corresponding 300 nm films. Small undetectable crystals may have formed in the 50nm samples, which would have become more numerous had these films been grown thicker.

Crystalline growth is affected by the substrate [4] and another reason for the lower crystallinity may be that these films were deposited directly on glass which is extremely amorphous and the roughness is low. At MVSystems, where the samples used in Figure 3.20 were deposited, textured Transparent Conductive Oxide (TCO) substrates are used which may have acted like a "seed layer" and enhanced the development of crystallites somewhat. More extensive pre-deposition treatments should be performed on the underlying substrate, whether it be glass or a-SiN:H to increase the surface roughness and improve crystallite nucleation sites.

Alternatively, the thickness dependancy is not an issue if TFT structures that can use thicker nc-Si:H layers without detrimental effect on performence are used, which can take advantage of the high crystallinity of samples 300-3 and 300-4.

Others have produced thin ($\leq 80\,\mathrm{nm}$) films at $75°C$ and $250°C$ at slightly higher hydrogen dilutions of $\geq 99\%$ with crystallinities of 65–78 % [32, 72]. These films were also deposted on glass. If even higher hydrogen dilution is used with pulsed PECVD it may be possible to produce films with even higher crystallinity and at low sample thickness.

The electrical conductivity measurements showed that the crystalline samples 300-3 and 300-4 were much less supceptible to light-induced degradation which is expected for nc-Si:H samples [61, 62]. In addition, it is believed that the 300-3 and 300-4 samples were unintentionally doped/contaminated with oxygen, which explains the high conductivity as well as the high carrier concentration observed in the Hall effect measurements of $n = 1.1 \times 10^{17}\,\mathrm{cm}^{-3}$. The conductivity did not change much after one-month exposure to air, so it is believed that the oxygen doping in the film was already saturated.

The Hall mobility was calculated to be $\mu_H = 0.27\,\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$ which is a bit lower than expected compared to other groups' results [73, 74, 75, 76] which report a minimum mobility of $0.4\,\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$, up to a maximum of 10–30 $\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$, although in some of these cases much larger sample thicknesses were used.

Chapter 4

Bottom-gate Thin-Film Transistors (TFTs)

To study the usefulness of a TFT with a channel layer grown by pulsed PECVD with high H_2 dilution, we fabricated bottom-gate TFTs. Unlike c-Si FET's, there are many different device geometries possible using thin-film technology. Top-gate, bottom-gate (also known as "inverted") are two classes of devices. The latter has its gate and dielectric below the active carrier transport layer, and the former has the gate and dielectric layer above the active layer. These two classes are further subdivided into coplanar vs. staggered devices, giving a total of four basic device structure types which are illustrated in Figure 4.1. Coplanar/staggered describes the location of the source and drain contacts relative to the gate. In coplanar TFTs, the source and drain contacts are on the same side of the active region as the gate contact. In staggered structures, the source and drain contacts are on the opposite side of the active region relative to the gate contact.

The most popular configuration for a-Si:H is the inverted staggered configuration. The reason for this is related to the characteristics of the gate dielectric which is usually a-SiN:H. When a-SiN:H is deposited by PECVD, the initial growth material is of very low quality, and its quality gradually improves as it is grown thicker. Thus if the a-SiN:H dielectric is grown on top of an active layer as in the non-inverted configurations shown in Figure 4.1, the interface (which is where conduction occurs) will have many defects.

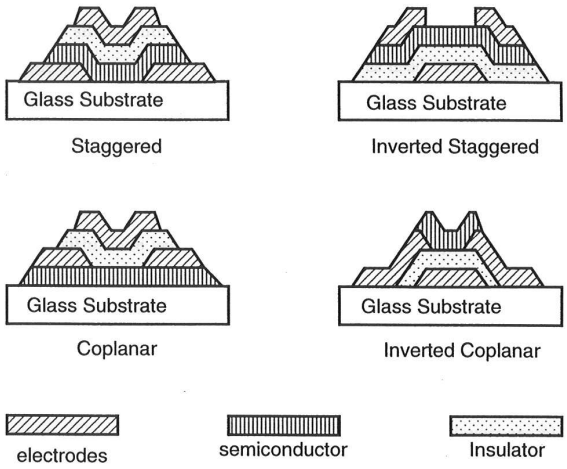

Figure 4.1: Illustration of the four different TFT structures, staggered, inverted staggered, coplanar, and inverted coplanar. From [77].

This will lead to poor mobility and conduction in the channel, as well as increased susceptibility to gate bias stress effects. Thus, the inverted staggered configuration is commonly used, where the gate is patterned first on the substrate, then the a-SiN:H layer is deposited, and then the active layer is deposited. The advantage of this structure over inverted coplanar is that it leads to an improved interface and improved a-Si:H mobility (≤ 1 cm^2 V^{-1} s^{-1}). Finally, the gate metal is deposited.

The bottom-gate process is a very standard process for a-Si:H TFTs, and is much less frequently used for nc-Si:H TFTs; however, it is the best TFT structure to use for this thesis, since so much is known about this structure with a-Si:H and the fabrication steps are well developed. It is also well-suited for collaborative development at MVS and Waterloo, as it does not allow any critical layers to be exposed during transportation. The gate metal was deposited at the University of Waterloo, then the entire tri-layer is deposited at MVSystems. The samples were then shipped to Waterloo where the rest of the fabrication steps were performed.

Two sets of TFTs were fabricated and then characterized using a Keithley SCS-4200 system. The I-V characteristics before and

after annealing, as well as threshold voltage stability under electrical bias stress were measured. The first set of TFTs, whose results are discussed in section §4.2 showed some field-effect but overall this set was not that successful due to a processing problem. The second set of TFTs are discussed in section §4.3 and were much more successful although it is believed that the active layer was primarily amorphous. The device parameters for these TFTs were extracted using two different methods.

4.1 Fabrication of Bottom-Gate Staggered TFTs

A bottom-gate TFT mask set is used which includes TFTs with five gate lengths from 25 μm to 200 μm and a constant gate width of 50 μm.

The bottom-gate process requires two metal sputtering steps, two PECVD depositions, and five lithographic steps. This is a "top-passivated" TFT as opposed to "top-etched." Each step in the fabrication process will be described below.

4.1.1 Step 1 - Substrate Preparation

Corning 1737 glass substrates were cleaned using the RCA1 cleaning procedure.

4.1.2 Step 2 - Gate Metal Deposition

The gate metal is the first film to be deposited. In our process molybdenum (Mo) was used, and it was deposited by sputtering at room temperature using an Edwards sputtering machine. A Mo target was sputtered at an RF power of 400 W, argon (Ar) pressure of 5 mTorr, and a Ar flow rate of 30 sccm. This produces a Mo film at a rate of about 15 nm/min.

4.1.3 Step 3 - Gate Metal Patterning

This is the first lithography step (mask 1), and it serves to define the TFTs' gate. Mo was wet-etched using a Phosphoric Acetic Nitric acid (PAN) solution, and after etching, the wafer looks as shown in Figure 4.2.

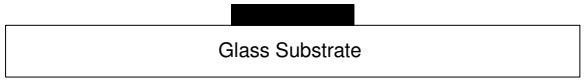

Figure 4.2: Bottom-gate process step 3: mask 1 lithography, to define the TFT gate

4.1.4 Step 4 - Deposition of a-SiN:H/i-nc-Si:H/a-SiN:H Tri-Layer

A tri-layer of a-SiN:H/i-nc-Si:H/a-SiN:H was grown on the substrate by pulsed PECVD at MVSystems. The bottom nitride was deposited at a substrate temperature 300–330 °C to a thickness of 250 nm and serves as a the gate dielectric for the TFT.

The intrinsic nanocrystalline silicon (i-nc-Si:H) layer was deposited at a substrate temperature of 150 °C in both TFT runs and is the active layer where conduction will occur. In the second process run, a thin channel thickness of 50 nm was used as a higher channel thickness leads to high source and drain resistance as the carriers have to travel from the source and drain vertically into the accumulation layer at the bottom of the channel.

The top nitride layer was deposited 150 °C in the second TFT process run to a thickness of 250 nm, and is a passivation layer, reducing the leakage at the top interface. It also prevents having to etch n^+-nc-Si:H on top of i-nc-Si:H in a following step, thus avoiding the poor etching selectivity between these two materials.

In order to compare the performance of the nc-Si:H TFTs to conventional a-Si:H TFTs, an a-Si:H channel layer was used as well. The a-Si:H channel layer in these TFTs was deposited at 200–210 °C.

The TFTs are labelled TFT-1, TFT-2, TFT-3, TFT-4, where the suffix denotes the corresponding process condition. The deposition parameters used for the i-nc-Si:H films in the second TFT run are the same as parameters used for the material characterization wafers, and are summarized in Table 3.1 in Section 3.1. After the deposition of the tri-layer, the film looks as shown in Figure 4.3.

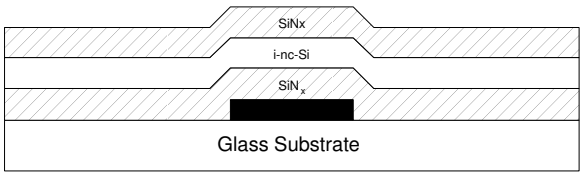

Figure 4.3: Bottom-gate process step 4: Deposition of a-SiN:H/i-nc-Si:H/a-SiN:H tri-layer

4.1.5 Step 5 - Pattering of Source/Drain Openings

In this lithography step (mask 2), source and drain contacts are opened by etching with BHF in the top a-SiN:H passivation layer, which defines the effective channel length as well as the gate overlap. After opening the source/drain contacts, the device begins to take shape as seen in Figure 4.4.

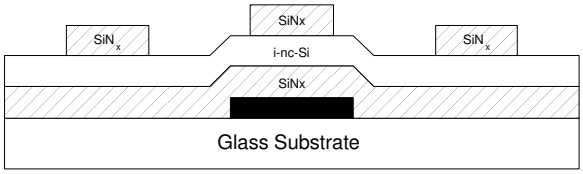

Figure 4.4: Bottom-gate process step 5: mask 2 defines the source and drain contacts and the gate length

4.1.6 Step 6 - Deposition of n$^+$-nc-Si:H/a-SiN:H Bi-layer

A bi-layer of n$^+$-nc-Si:H/a-SiN:H is deposited for the source and drain contacts at 150 °C using PECVD in the MVSystems cluster tool at the University of Waterloo. The a-SiN:H layer is needed as a mask for the etching of n$^+$-nc-Si:H by potassium hydroxide (KOH). Photoresist alone cannot be used as an etching mask when etching silicon (Si) since KOH will also damage photoresist.

4.1.7 Step 7 - Patterning to Define n$^+$-nc-Si:H Source/Drain Regions

A lithography step (mask 3) is now performed to define the source and drain regions. Part of the uppermost a-SiN:H layer was etched using a BHF wet etch and the resulting device is shown in Figure 4.5. The leftover a-SiN:H will act as a mask in the next

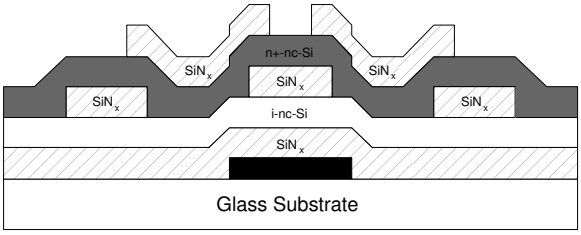

Figure 4.5: Bottom-gate process step 7: mask 3 defines the source and drain regions

step.

4.1.8 Step 8 - Etching of n$^+$-nc-Si:H and i-nc-Si:H Layers

This step is just an etching step, to etch away the unwanted n$^+$-nc-Si:H and i-nc-Si:H regions to form TFT islands (isolate the i-nc-Si:H regions). Clearly, the n$^+$-nc-Si:H layer will be etched laterally somewhat while the nc-Si:H is being etched; however, the

i-nc-Si:H film thickness (50 nm) is much less than the lateral dimensions (a few μm) so this is not a problem. The resulting device is shown in Figure 4.6.

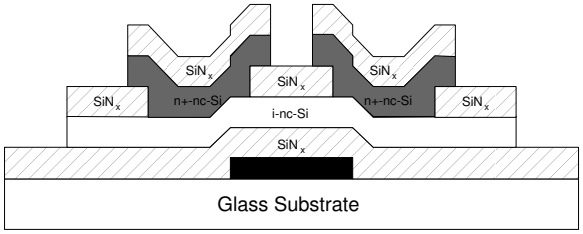

Figure 4.6: Bottom-gate process step 8: etching step to remove n^+-nc-Si:H and i-nc-Si:H outside device region

4.1.9 Step 9 - Etching of a-SiN:H to open Gate, Source, and Drain Vias

After patterning using mask 4, the bottom a-SiN:H layer was etched with BHF to open up gate contacts and the drain and source contacts. The resulting device is shown in Figure 4.7.

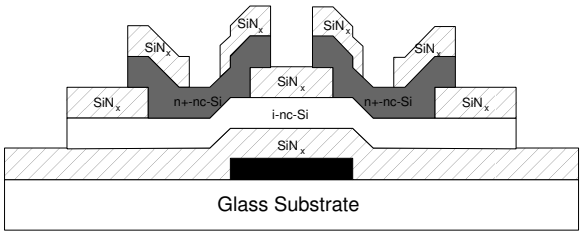

Figure 4.7: Bottom-gate process step 9: mask 4a and mask 4b are to define the openings for the gate, source, and drain contacts

4.1.10 Step 10 - Deposit Aluminium

Before deposition, the wafers were cleaned in a hot bath of methanol followed by a hot bath of water. Al was deposited for the

contact metal using the Edwards sputtering machine. The Al target was sputtered using an Ar flow rate of 30 sccm, RF power of 400 W, and a pressure of 5 mTorr.

4.1.11 Step 11 - Patterning of Final Aluminium Metallization Layer

In this final lithography step, the metal contacts are patterned. Al is etched using a PAN etchant at an elevated temperature. The final device structure is shown in Figure 4.8.

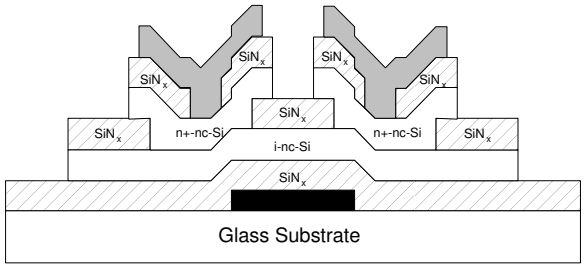

Figure 4.8: Bottom-gate process step 11: final bottom-gate device structure, after final lithography step (mask 5)

4.2 Characterization of TFTs From First Process Run

The first set of TFTs from MVSystems were fabricated using a channel layer which was 140 nm thick to improve the crystallinity of the channel layer. There was an error in the processing, namely, the top a-SiN:H layers were deposited at a high temperature (300 °C) whereas the i-nc-Si:H layer was deposited at 150 °C[1]. It is expected that the increase in temperature from 150 °C to 300 °C after the deposition of the i-nc-Si:H layer should cause damage to the i-nc-Si:H layer. This damage could be caused by hydrogen effusing from

[1]Thus in the second process run the top a-SiN:H layer was deposited at the same temperature as the channel layer.

the film, leaving dangling bond defects behind. Alternatively, it is possible that annealing can occur during this heating step and the silicon atoms can rearrange themselves and form new Si-Si bonds and crystallites (if present) can become enlarged, although in the present case, this most likely did not happen. Figure 4.9 shows the output characteristics of a one of the best TFTs in the first process run, and Figure 4.10 shows the transfer characteristics.

The leakage current is extremely high, yet gate leakage was at

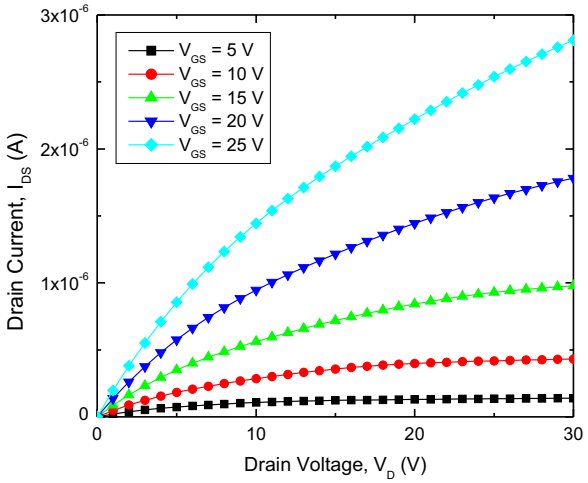

Figure 4.9: Output characteristics of one TFT from first set of TFTs with $W/L = 100/25$

acceptable levels and much lower than the I_{DS} leakage. The subthreshold slope, S is extremely high (in Volts/decade units) and it is difficult to extract any mobility or threshold voltage information because when the data is plotted on a linear axis it is highly non-linear in the above-threshold regime.

One can conclude that the channel layer must have been damaged by the heating at 300 °C before and during the a-SiN:H deposition on top of the intrinsic channel layer leading to a highly defective channel layer. This may have lead to a high subthreshold slope and low on-current. The high leakage current may be due to a poor interface between the i-nc-Si:H layer and the top a-SiN:H layer.

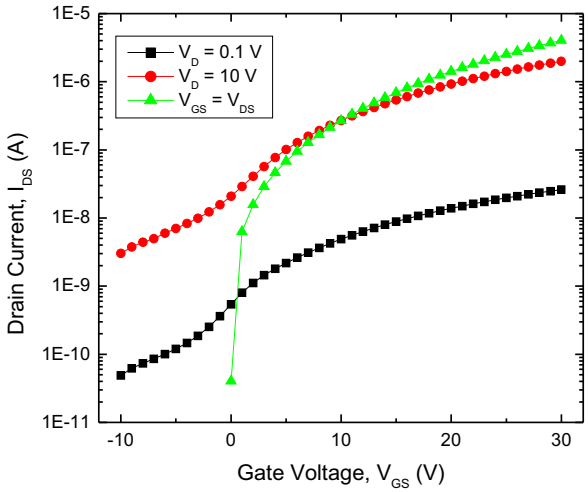

Figure 4.10: Transfer characteristics of one TFT from first set of TFTs with $W/L = 100/25$

4.3 Characterization of TFTs From Second Process Run

The second set of TFTs were fabricated with a 50 nm channel instead of a 140 nm channel because with the bottom-gate staggered style of TFT (see section §4) source and drain contact resistance increases with increasing channel thickness. This would lead to poor TFT characteristics. The 50 nm film channel layer is also less susceptible to light-induced effects leading to higher leakage currents. Although a thicker film would definitely show higher crystallinity, as discussed in Section §3.5, sufficient crystallinity was expected even with the thinner 50 nm channel layer.

Unlike the first set of TFTs, the second set of TFTs were much more successful. The annealing effect on the TFTs' performance is shown as well as their electrical characteristics, extracted parameters, and stability.

4.3.1 Annealing Effect on Performance

Prior to characterization, the TFT wafers were annealed at approximately 150 °C for two hours in a vacuum to improve the

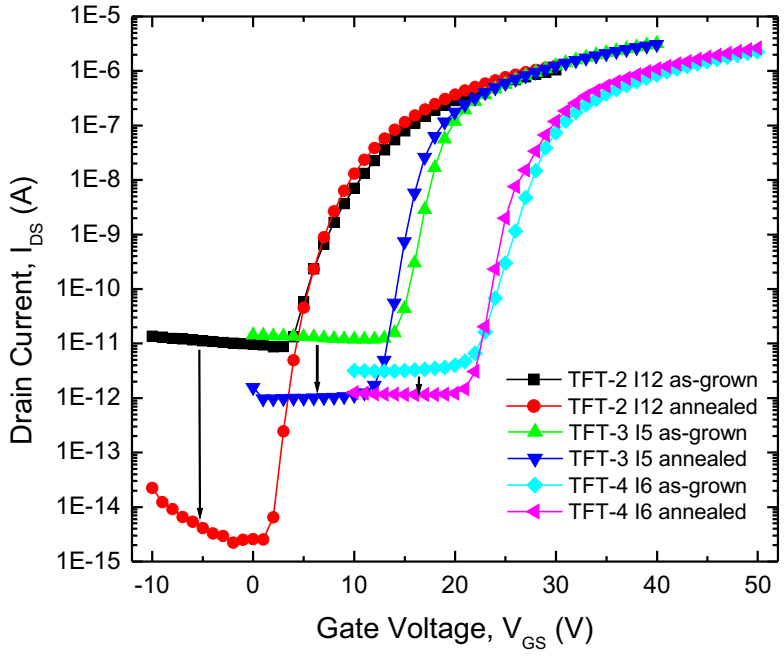

Figure 4.11: TFT characteristics before and after annealing with $W/L = 100/25$. The four right most curves were shifted for display purposes.

contact properties. Figure 4.11 shows the change in the TFTs' performance after annealing. The mobility and threshold voltage did change; however, the change was less than or close to the standard deviation of these parameters across five TFTs from each wafer TFT-2, TFT-3, and TFT-4 so this change is insignificant. The only parameters which changed considerably and consistently across all samples were the subthreshold slope, S, and the off-current, I_{off} (which will also cause the on-off current ratio, $I_{on/off}$ to change) and this change is clearly visible in Figure 4.11. There was no negative effect on the extracted parameters after annealing the samples. The improvement in the I_{off} can be attributed to both annealing of bulk metastable defect states at around 150 °C and annealing of interface defects at around 110 °C [78].

4.3.2 I-V Characterization

The TFTs have gate lengths (L) ranging from 25 μm to 200 μm, and the channel width (W) is a constant 100 μm. The TFTs are labelled TFT-1, TFT-2, TFT-3, TFT-4, where the suffix denotes the corresponding process condition as described in section §3.1. Transfer characteristics are measured by keeping the drain voltage constant at $V_{DS} = 0.1$, 1, and 10 V and sweeping the gate voltage from -10 to 30 V. Output characteristics are measured by keeping the gate voltage constant at $V_{GS} = 5$, 10, 15 V, etc . . . and sweeping the drain voltage between 0 and 30 V.

The I-V characteristics of selected 25 μm channel length TFTs from each of the wafers TFT-2, TFT-3, and TFT-4[2] are shown below. Uniformity on each wafer was fairly good ($\approx 10\,\%$ variation in the output current for TFT-2 and $\approx 20\,\%$ TFT-3 and TFT-4) so graphs of only one TFT from each wafer are shown. The die which was selected is denoted by a letter and a number (for example, I5), corresponding to the row and column location, respectively, on the TFT.

The transfer and output characteristics of a selected TFT from TFT-2 are shown in Figure 4.12 and Figure 4.13 respectively. This particular TFT, TFT-2 N11, shows extremely good saturation characteristics (as seen in Figure 4.13) and low off-current (as seen in Figure 4.12), as well as slightly lower on-current (due to a lower mobility) compared to TFT-3 and TFT-4. Recall from Chapter 3 that samples 50-2 and 300-2 appeared to be almost completely amorphous.

The transfer and output characteristics of a selected TFT from TFT-3 are shown in Figure 4.14 and Figure 4.15 respectively. This TFT, TFT-3 I5, shows poor saturation characteristics (as seen in Figure 4.15) although the mobility is higher than in TFT-2 N11.

The transfer and output characteristics of a selected TFT from TFT-4 are shown in Figure 4.16 and Figure 4.17 below. This TFT, TFT-4 I6, shows similar characteristics to TFT-3 I5 although it

[2]Unfortunately, TFT-1 which had an amorphous channel layer (it was deposited with no hydrogen dilution in the plasma) did not survive the processing.

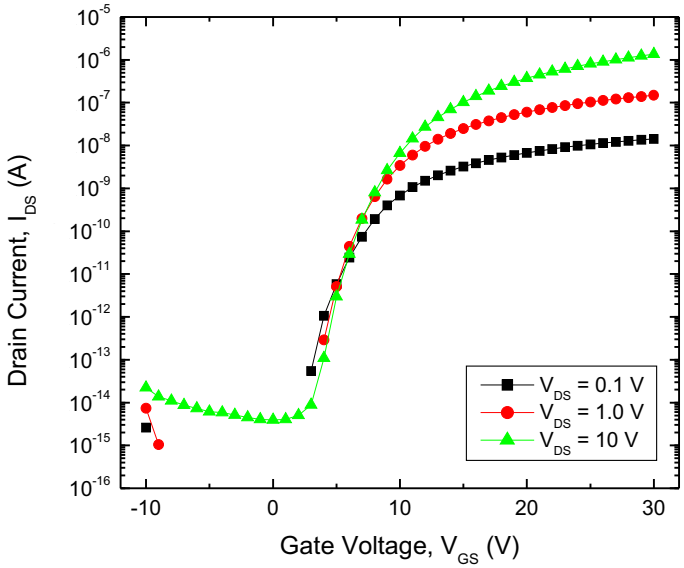

Figure 4.12: TFT-2 N11 transfer characteristics

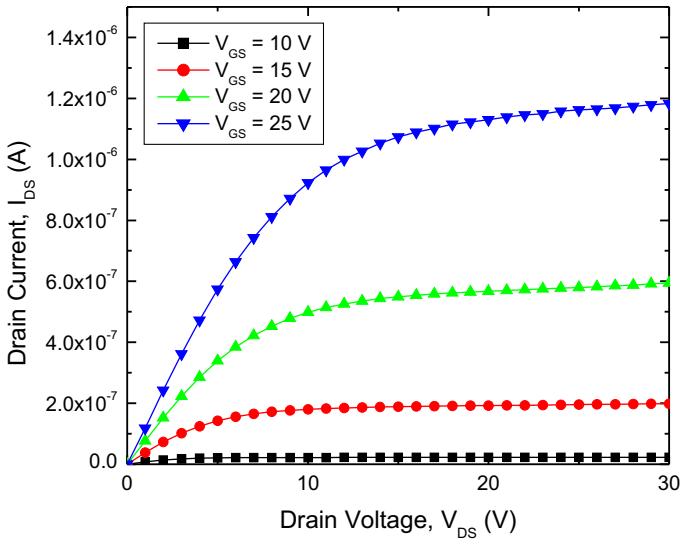

Figure 4.13: TFT-2 N11 output characteristics

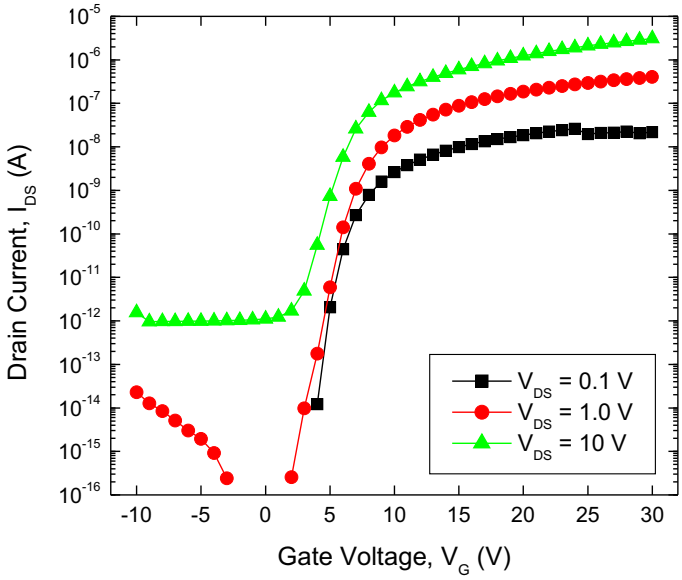

Figure 4.14: TFT-3 I5 transfer characteristics

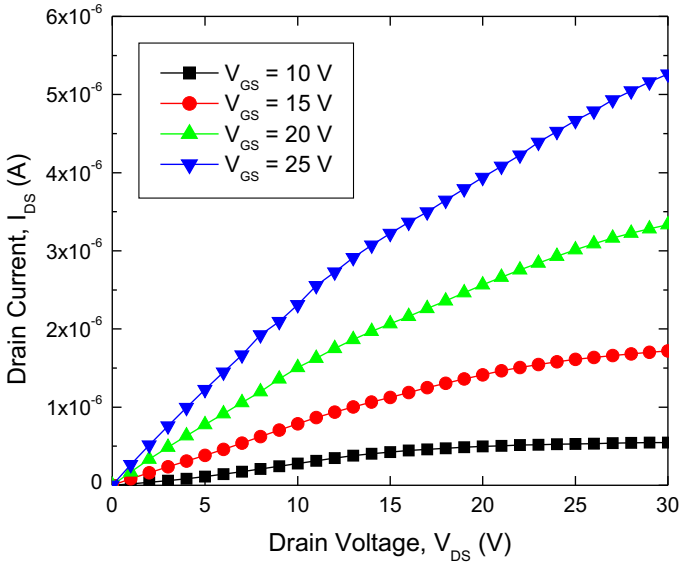

Figure 4.15: TFT-3 I5 output characteristics

has the highest threshold voltage compared to TFT-2 N11 and TFT-3 I5.

4.3.3 Extraction of TFT Parameters

Two different extraction methods were used. The first is used to get some basic device parameters based on a simple FET model. The second is a more complicated technique designed by Dr. Peyman Servati based on his physical model [79].

4.3.3.1 Simple Method

Values for linear and saturated mobility (μ_{lin} and μ_{sat}) and linear and saturated threshold voltage ($V_{t,lin}$ and $V_{t,sat}$) were extracted using simple equations as described in [80]. Using this model the drain current in the linear regime is given by,

$$I_{DS,lin} = \mu_{lin} C_i \frac{W}{L}(V_G - V_{t,lin}) \cdot V_{DS}, \tag{4.1}$$

and in the saturation regime,

$$\begin{aligned} I_{DS,sat} &= \frac{1}{2}\mu_{sat} C_i \frac{W}{L}(V_G - V_{t,sat})^2 \\ (I_{DS,sat})^{1/2} &= \left(\frac{1}{2}\mu_{sat} C_i \frac{W}{L}\right)^{1/2} (V_G - V_{t,sat}), \end{aligned} \tag{4.2}$$

where C_i is the gate capacitance per unit area of the TFT, W is the TFT's channel width, L is the TFT's channel length, V_G is the gate-source voltage, V_{DS} is the drain-source voltage, and μ_{lin} and μ_{sat} are the linear and saturation mobilities respectively. By fitting a line to the linear above-threshold portion of the curve and taking the slope and the x-axis intercepts for the I_{DS} vs. V_{GS} curves in the linear ($V_{DS} = 0.1\,\mathrm{V}$) and saturation ($V_{DS} = V_{GS}$) region we can determine the mobility and threshold voltage. In the linear regime,

$$\mu_{lin} = m \frac{1}{C} \frac{L}{W} \frac{1}{V_{DS}}, \tag{4.3}$$

and in the saturation regime,

$$\mu_{sat} = 2m^2 \frac{1}{C} \frac{L}{W} \tag{4.4}$$

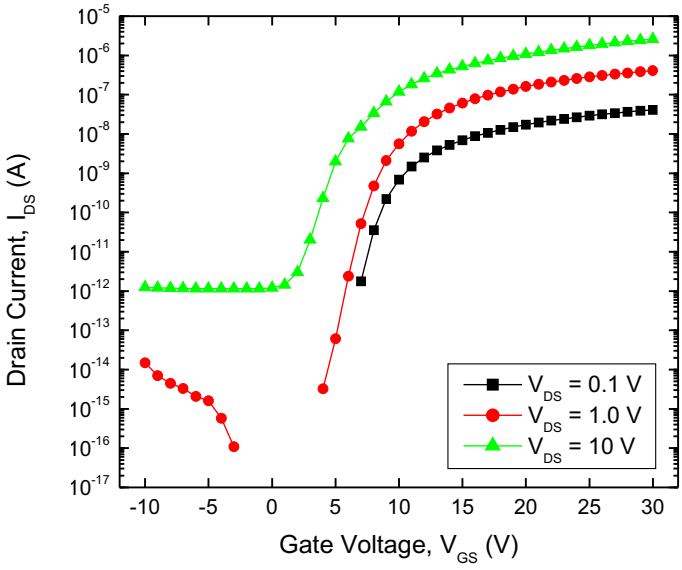

Figure 4.16: TFT-4 I6 transfer characteristics

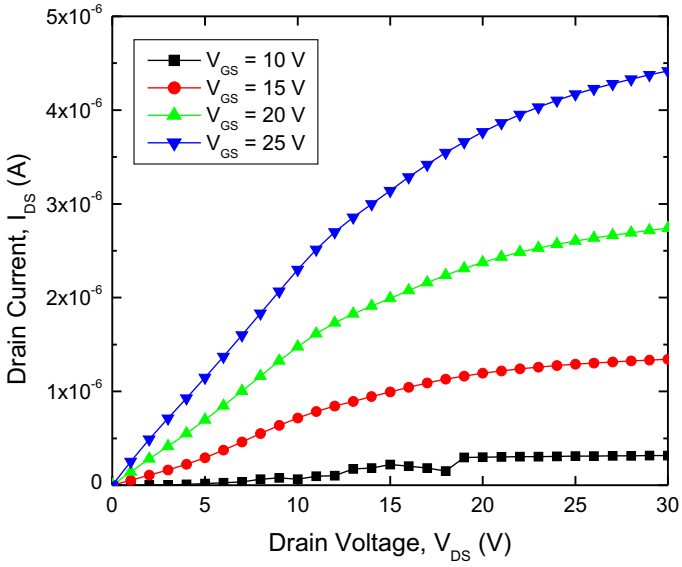

Figure 4.17: TFT-4 I6 output characteristics

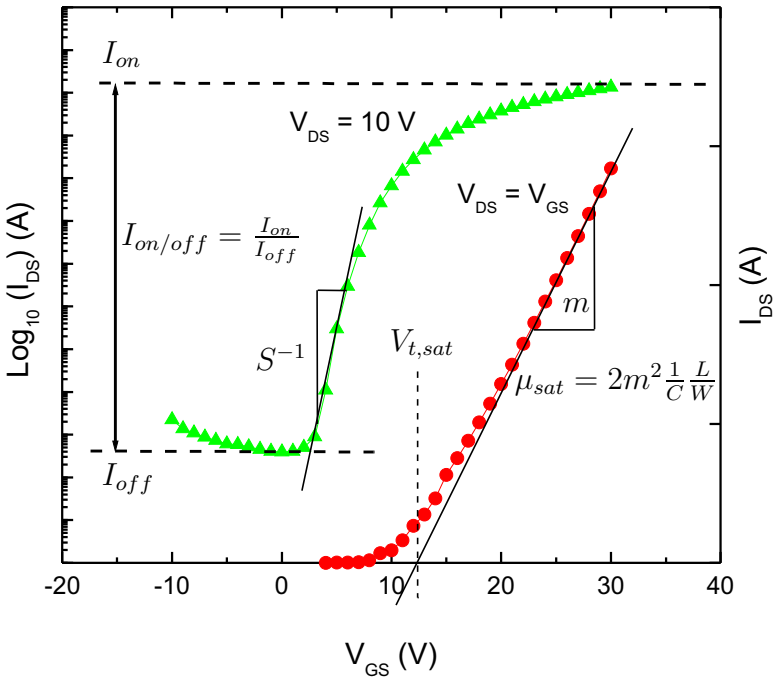

Figure 4.18: Graph of TFT transfer characteristics for an example TFT showing how extraction of parameters is performed using the simple method

where m is the slope of the fit line. The threshold voltage in the linear and saturation regime is just given by the x-axis intercept in both cases. The right-hand side of Figure 4.18 shows an example extraction of a TFT's saturation threshold voltage and mobility, The above extractions using the simple model are performed semi-automatically using Python scripts which are provided in Appendix B.

The extracted parameters from the linear and saturation transfer characteristics are summarized in Table 4.1.

From the transfer characteristics with $V_{DS} = 10\,\mathrm{V}$, the off-current, I_{off}, (also known as the "leakage current") and the on-current, I_{on}, are defined as the minimum and maximum current respectively. The on-off ratio, $I_{on/off}$, is given by I_{on}/I_{off} and the subthreshold slope, S, is defined as the inverse maximum slope in the sub-threshold region. This is demonstrated on the left-hand

Table 4.1: Extracted mobility and threshold voltage for TFTs with $L = 25,\ 50,\ 75,\ 100,\ 200\,\mu$m and $W = 100\,\mu$m from linear and saturation transfer characteristics

TFT	$\mu_{lin}\left(\frac{\text{cm}^2}{\text{V}\cdot\text{s}}\right)$	$\mu_{sat}\left(\frac{\text{cm}^2}{\text{V}\cdot\text{s}}\right)$	$V_{t,lin}$ (V)	$V_{t,sat}$ (V)
TFT-2	0.02-0.10	0.12-0.17	9.9-12.4	11.6-13.6
TFT-3	0.23-0.27	0.34-0.38	9.6-11.3	7.5-9.6
TFT-4	0.28-0.30	0.34-0.46	11.8-13.0	7.3-9.5

Table 4.2: Extracted sub-threshold slope, on/off current ratio, and off current for TFTs with $L = 25,\ 50,\ 75,\ 100,\ 200\,\mu$m and $W = 100\,\mu$m from logarithmic transfer characteristics with $V_{GS} = 10\,$V

TFT	$S\left(\frac{\text{V}}{\text{decade}}\right)$	$I_{on/off}$	I_{off}(A)
TFT-2	0.46-0.81	$> 10^7$	$< 10^{-14}$
TFT-3	0.76-0.95	$> 10^6$	$< 10^{-12}$
TFT-4	0.76-1.20	$> 10^6$	$\leq 10^{-12}$

side of Figure 4.18. The extracted TFT parameters from the logarithmic transfer characteristics with $V_{GS} = 10\,$V are summarized in Table 4.2.

From Table 4.1 and Table 4.2 we see that all of the TFTs show a high V_t and S. Interestingly, for TFT-2 $V_{t,sat} > V_{t,lin}$ whereas for TFT-3 and TFT-4, $V_{t,sat} < V_{t,lin}$. TFT-3 and TFT-4 display better threshold voltage and field-effect mobility compared to TFT-2; however, TFT-2 shows slightly improved sub-threshold slope and extremely low leakage ($I_{off} < 10^{-14}$). The values of μ_{sat} for TFT-4 are similar to the mobility measured by the Hall effect ($0.27\,\text{cm}^2/(\text{V}\cdot\text{s})$) in sample 300-4 (see section §3.4.2.2). The on/off current ratio is more than suitable for AMLCD applications [11]. The gate leakage (I_G) was measured during the transfer characteristics measurements and was consistently $\approx 10^{-13} - 10^{-12}\,$A for all TFTs.

4.3.3.2 Servati Extraction

The Servati extraction method is based on the model given in [81, 82]. The equations look very similar to (4.1) and 4.2 above.

For the linear regime, the above-threshold current is given by

$$I_{DS,lin} = \mu_{eff}\zeta C_i^{\alpha-1}\frac{W}{L_{eff}}(V_{GS} - V_T - 0.5V_{DS})^{\alpha-1}(V_{DS} - R_{DS}I_{DS}), \tag{4.5}$$

where $L_{eff} = L + \Delta L$, where ΔL is the channel enlargement factor, due to the source and drain resistance R_{DS} which is equal to $R_S + R_D$. μ_{eff} is the effect field-effect mobility, ζ is the unit-matching parameter, α is the power parameter, and all the other variables have the same meanings as above in Section 4.3.3.1. In the saturation regime the current is given by

$$I_{DS,sat} = \frac{\mu_{eff}}{\alpha}\zeta C_i^{\alpha-1}\frac{W}{L_{eff}}\gamma_{sat}\left(V_{GS} - \frac{R_{DS}}{2}I_{DS} - V_T\right)^{\alpha} x_{cm}, \tag{4.6}$$

where x_{cm} is $1 + \lambda V_{DS}/L_{eff}$ where λ is the usual channel length modulation parameter. We now proceed as in [81, 82] to extract all relevant device parameters for a set of TFT from the TFT-3 wafer. The TFT-2 and TFT-4 wafers did not provide a complete set of good TFTs of varying channel length compared with TFT-3 where the curves for all the TFTs lengths were acceptable as shown in Figure 4.19.

Extraction of R_{DS} The measured resistance for the shortest and longest TFTs is calculated from $R_m = V_{DS}/I_{DS}$ for the linear transfer characteristics ($V_{DS} = 0.1\,\mathrm{V}$). The resistance of the longest TFT is then scaled by the lengths (in this case, a factor of 8 since the longest TFT has $L = 200\,\mu\mathrm{m}$ and the shortest TFT has $L = 25\,\mu\mathrm{m}$. This scaled resistance of the longest TFT is substracted from the resistance of the shortest TFT and the left-over resistance is approximately equal to the parasitic source and drain resistance, at high voltages. From Figure 4.20 we find that $R_{25} - R_{200}/8$ approaches $1.78\,\mathrm{M\Omega}$ at high voltages. This is usually multiplied by $W = 100\,\mu\mathrm{m}$ and expressed as $R_{DS}W = 17.8\,\mathrm{k\Omega{\cdot}cm}$. In the above calculations, it was important to use the effective gate length as opposed to the actual width of the metallic gate. The effective gate length in our case was only $15\,\mu m$ whereas the actual gate length was $25\,\mu m$ due to a large source/drain-gate overlap.

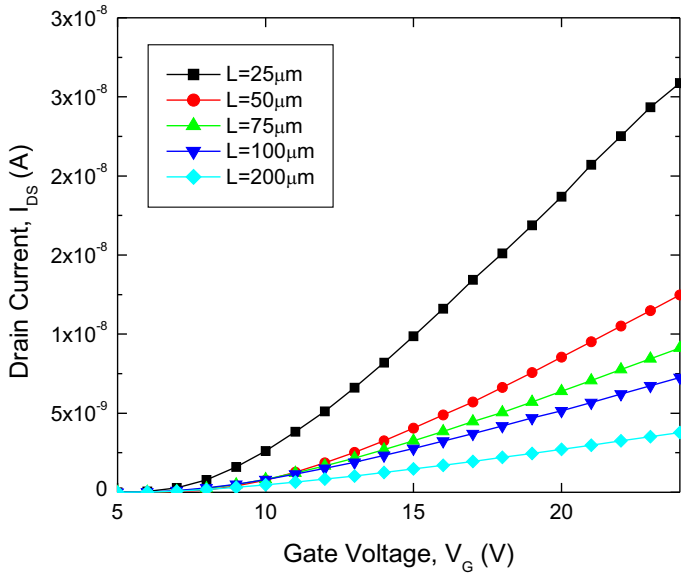

Figure 4.19: TFT-3 I5 transfer characteristics for all TFT channel lengths

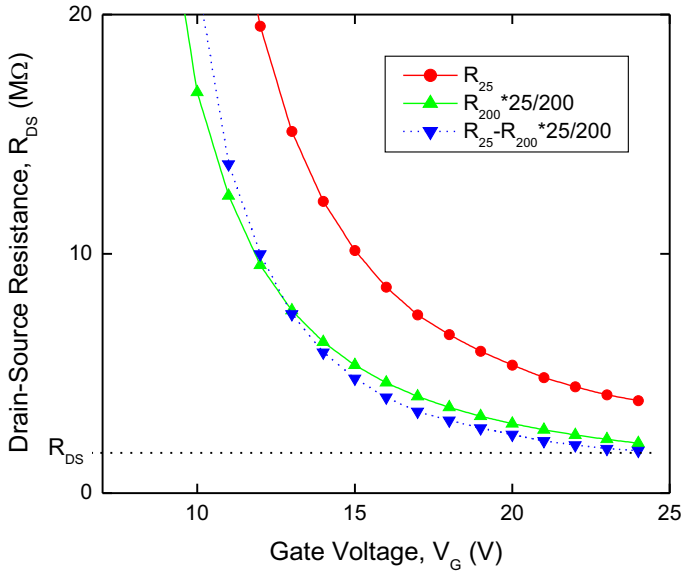

Figure 4.20: Measured resistance as a function of gate voltage for shortest (25 μm) and longest (200 μm) channel length TFTs. The dashed line represents is the extracted R_{DS} value.

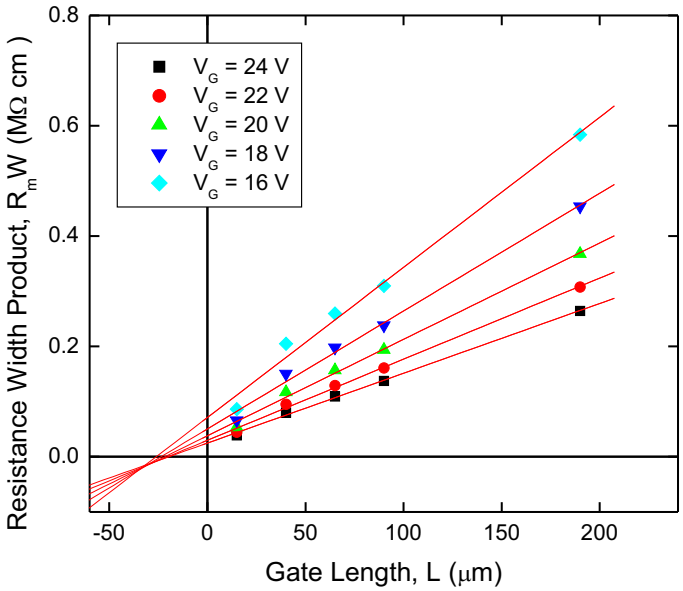

Figure 4.21: Plot of $R_m W$ as a function of the channel length L for different values of V_{GS}

Extraction ΔL Normally this is straightforward, however, in our case we see a negative value of R_{DS} when extrapolating the resistance as in [81, 82] using the method which is also used to extract ΔL. Figure 4.21 shows $R_m = V_{DS}/I_{DS}$ plotted as a function of the channel length L for different values of V_{GS}. Normally, the intersection point of the lines is at the point $(-\Delta L, R_{DS}W)$, however in our case, this would yield a negative value for R_{DS} which does make physical sense. The most likely reason for the extrapolated lines meeting in the lower-left quadrant instead of the upper-left quadrant of the graph is that these points were not plotted at constant $V_{GS} - V_T$ but against constant V_{GS} only. Since V_T varies for each TFT, in order to do this graph properly it is necessary to extract V_T for each TFT and plot curves for constant values of $V_{GS} - V_T$. Another possibility is that the data for the shortest channel length TFT is causing the best fit line's slope to increase. This can be seen qualitatively from Figure 4.21. Discarding these data points may help.

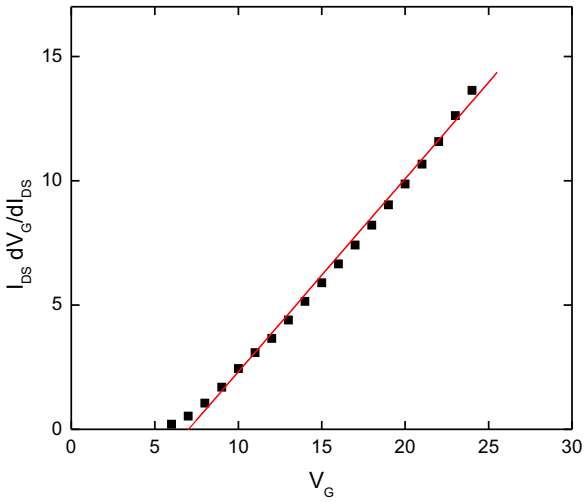

Figure 4.22: Extraction of α and V_T from the slope and intercept of a best fit line of $I_{DS,lin}\frac{\partial V_G}{\partial I_{DS,lin}}\frac{V_{DS}-R_{DS}I_{DS,lin}}{V_{DS}}$ versus V_{GS}

Extraction of V_T and α To extract V_T and α the left-hand side of the following equation is plotted versus V_{GS}:

$$I_{DS,lin}\frac{\partial V_G}{\partial I_{DS,lin}}\frac{V_{DS}-R_{DS}I_{DS,lin}}{V_{DS}} = \frac{V_{GS}-V_T-0.5V_{DS}}{\alpha-1}, \qquad (4.7)$$

where $\partial I_{DS,lin}/\partial V_G$ was calculated from a discrete derivative of the curves shown in Figure 4.19 and the value of R_{DS} is that which was calculated previously to be 1.78 MΩ. This plot is shown in Figure 4.22, and a straight line fit to the graph with slope m and intercept b will yield the α parameter and the threshold voltage, according to (4.7),

$$\begin{aligned} \alpha &= \frac{1}{m}+1 \\ V_T &= -b(\alpha-1)-0.5V_{DS}. \end{aligned} \qquad (4.8)$$

Figure 4.22 and (4.8) yields $\alpha = 2.28$ and $V_T = 7.22$ V. Extracting α and V_T from the other, shorter channel length TFTs yields α in the range of 2.28–2.36 and V_T in the range of 7.30–8.03 V.

Attempting to extract the saturation parameters α_{sat} and γ_{sat} did not yield correct results so these results will not be quoted here.

Calculating ζ, V_{nt} The scaling parameter ζ is found from

$$\zeta = \frac{(q\epsilon\alpha V_T N_0)^{1-\alpha/2}}{\alpha - 1} = \frac{(4.1 \times 10^{-16}\alpha)^{1-\alpha/2}}{\alpha - 1}, \tag{4.9}$$

and V_{nt}, the charateristic slope of the band tail is calculated from

$$\alpha = \frac{2V_{nt}}{V_T}, \tag{4.10}$$

where $V_T = kT/q$ (thermal voltage). For the present TFTs, $\zeta = 106\,(\mathrm{C/cm^2})^{\alpha-2}$ and $V_{nt} = 29.3\,\mathrm{mV}$.

Extraction of Effective Mobility μ_{eff} The effective mobility is found from the plot of $(I_{DS,lin}/V_{DS})^{1/(\alpha-1)}$ versus V_{GS} [81]. Doing so for the long channel TFT and finding the slope of the best fit line, m, one uses the following

$$\mu_{eff} = \frac{L_{eff}}{\zeta W}\left(\frac{m}{C_i}\right)^{\alpha-1}. \tag{4.11}$$

The long channel TFT on wafer 300-3 is found to have an effective mobility of $0.23\,\mathrm{cm^2\ V^{-1}\ s^{-1}}$. This is a bit lower than the value of $\mu_H = 0.27\,\mathrm{cm^2\ V^{-1}\ s^{-1}}$ obtained from Hall effect measurements on sample 300-4 in section §3.4.2.2 but it is reassuring that these values are both on the same order. This method of finding μ_{eff} does not compensate for R_{DS}, however, it has been extracted using the data for the longest TFT therefore the effects of the drain and source resistance should be minimal.

Summary The results of the extraction of TFT-3 by the Servati method is summarized in Table 4.3. The value obtained for the effective mobility of $\mu_{eff} = 0.23\,\mathrm{cm^2\ V^{-1}\ s^{-1}}$ is similar to that obtained via the simple extraction method in section §4.3.3.1 for TFT-3 and TFT-4 ($\mu_{lin} = 0.23$–$0.30\,\mathrm{cm^2\ V^{-1}\ s^{-1}}$ and $\mu_{sat} = 0.34$–$0.46\,\mathrm{cm^2\ V^{-1}\ s^{-1}}$) and that obtained from Hall measurements in Section §3.4.2.2 ($\mu_H = 0.27\,\mathrm{cm^2\ V^{-1}\ s^{-1}}$) for sample 300-4 (note: this sample was highly crystalline, however). The lower mobility in the field effect device using the Servati method may be explained

Table 4.3: Summary of extracted parameters for TFT-3 I5 using Servati method

Extracted Parameter	Value
μ_{eff}	$0.23\,\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$
V_T	$7.22\,\mathrm{V}$
α	2.28
$R_{DS}W$	$17.8\,\mathrm{k\Omega{\cdot}cm}$
ΔL	not extractable
ζ	$106\,(\mathrm{C/cm}^2)^{\alpha-2}$
V_{nt}	$29.3\,\mathrm{mV}$
α_{sat}	not extractable
γ_{sat}	not extractable

by the interfacial nature of the electron transport through a highly defective interfacial region, compared to the Hall effect, where transport through the interface region is not so highly favoured, due to the lack of vertical electric fields.

One of the most glaring problems with these TFT results is the high threshold voltage upwards of 7 V. This is high for a-Si:H TFTs and is highly related to the density of band tail states or a high density of trapped charge at the a-SiN:H/channel interface or in the a-SiN:H bulk. The power parameter is also much higher than usual at 2.28 and this leads to a high V_{nt} of 29.3 mV which is clear evidence for a large conduction band tail density of states. $R_{DS}W$ is also a bit high at 17.8 kΩ·cm. Other TFTs show contact resistance as low as $\approx 0.2\,\mathrm{k\Omega{\cdot}cm}$ [82] when extracted by the Servati method, thus the contact resistance in the present case is two orders of magnitude higher than it could be.

4.3.4 Stability of TFTs

The stability of the TFT was measured by stressing the TFT with $V_G = 30\,\mathrm{V}$ and $V_D = V_S = 0\,\mathrm{V}$, then measuring the linear ($V_{DS} = 0.1\,\mathrm{V}$) and saturation ($V_{DS} = V_G$) transfer characteristics either every five minutes for up to 30 minutes (this was done for three TFTs) or every 60 minutes for up to 2 hours (this was done for three different TFTs).

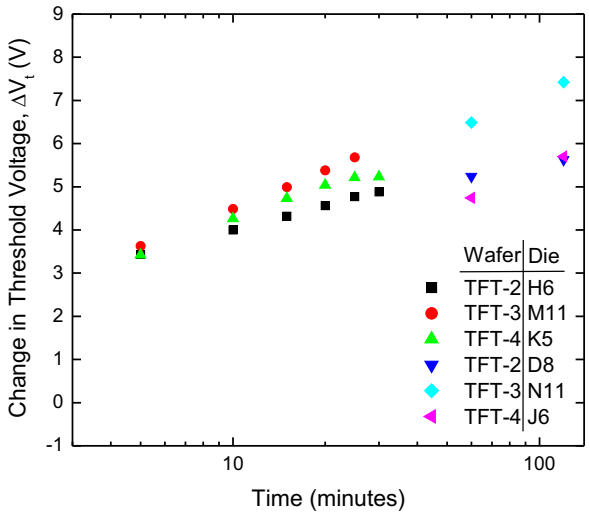

Figure 4.23: Threshold voltage shift measured every 5 minutes and every 60 minutes for six different TFTs.

Figure 4.23 shows the change in the threshold voltage over time, beginning with the first measurement, which was done before any stress was applied. The V_t shift in these TFTs is very high, and after two hours still no saturation is observed. This may be due to a a-SiN:H layer which is not optimized for TFT fabrication. The two main causes for threshold voltage shift is defect state creation at the interface and charge trapping in the a-SiN:H gate dielectric [83]. Since the change in V_t observed here occurs on such a short time scale, it is most likely due to charge trapping in the a-SiN:H layer, as opposed to defect state creation which is a much slower process. Further measurements need to be performed on different time scales and with different bias voltages, to determine the exact mechanism for this V_t shift. This stability problem is a serious one, and at these magnitudes of voltage shift would surely make this device unusable for driver circuits, but perhaps also unusable as a pixel switch TFT.

4.4 Discussion

It is clear from the material characterization studies that the TFT channel layer is not made up of nc-Si:H but rather a-Si:H. The electrical performance of the TFTs (see Table 4.1, Table 4.2, and Table 4.3) is comparable to previous pulsed PECVD TFT work [84] and other low temperature a-Si:H TFTs [85]. The off-current and on-off ratio are more than acceptable for pixel switching applications, and the mobility is acceptable; however, the threshold voltage (V_t) is high, which is most likely due to charge trapping at the interface or in the dielectric. The high threshold voltage shift of the TFT seen in Figure 4.23 supports this claim as it is widely known that V_t shift is related to defects at the a-SiN:H/channel interface and/or a-SiN:H bulk. The power parameter α is also high, which indicates a high density of band tail states due to a defective channel layer.

The TFTs could be made more crystalline using pulsed PECVD by reducing the incubation layer thickness and improving the quality of the a-SiN:H layer. The quality of the TFTs would thus improve and with increased crystallinity the mobility and stability of the TFTs should also increase.

It is believed that these TFTs are just the second attempt ever at fabricating TFTs using the pulsed PECVD technique. The crystallinity of the 50 nm layers is not as high as expected, based on previous data [4, see Figure 5 in ref.]. In that process, the onset of crystallization occured at a thickness much less than 50 nm. In order to have sufficient crystallinity in the channel layer, the deposition conditions should be optimized to minimize the amorphous incubation layer to ensure that it is thinner than the channel thickness. Oxygenation of the film as in 300-3 and 300-4 also needs to be reduced to avoid high TFT leakage current.

Crystallinity is also affected by the substrate [4], and in the case of a bottom-gate TFT, the active layer is deposited on top of an a-SiN:H layer which delayed the onset of crystal growth. In [4] an Asahi TCO substrate was used which may have caused increased nucleation during film growth. Alternatively, top-gate TFTs may be preferred for nc-Si:H TFTs, because in this case the channel layer would be formed in the highly crystalline part of the

film.

During the growth of nc-Si:H, the initial growth phase is normally amorphous. This amorphous phase can be in the range of tens of nanometres for films grown using Electron Cyclotron Resonance Chemical Vapour Deposition (ECR-CVD) [86], and similarily for PECVD and Hot-wire Chemical Vapour Deposition (HWCVD). This is most common with deposition on glass substrates (as opposed to deposition on a nc-Si:H seed layer or other advanced deposition techniques), due to the amorphous nature of the glass, but also because of the low temperatures normally used in deposition on glass, which favours the amorphous phase [87]; however, the incubation layer is an intrinsic property of nc-Si:H growth and is present even with deposition of nc-Si:H on a c-Si substrate. Small crystallites will form near the growing surface and during film growth, the crystals can grow upwards and laterally, sometimes forming columnar-like or cone-like grains. It has been proven experimentally that in all cases, crystallinity, and hence mobility, free carrier density, and conductivity of the nc-Si:H film usually increases as the film becomes thicker [10, 88]. For TFTs, this fact has been exploited by Cheng and Wagner [22] by growing a thick "seed" layer on top of their substrate first, and then growing the active TFT active layer on top of this seed layer after source/drain patterning to avoid the initial amorphous growth regime in the active layer. Usually, nc-Si:H TFTs are fabricated in a top-gate configuration, like that shown in Figure 4.24 so that the channel is formed at the top of the nc-Si:H film, where the crystallinity is highest. Bottom-gate TFTs have an active channel formed near the bottom of the nc-Si:H film. Since this channel is almost invariably of low crystallinity and in most cases purely amorphous, it is almost never considered.

There are many research groups who use a bottom-gate technique for nc-Si:H TFTs. These devices almost invariably lead to very low mobility devices, with $1\,\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$ at most, which is comparable to the best a-Si:H devices. This is a direct result of the fact that the initial nc-Si:H film growth is almost always amorphous, so in these bottom-gate devices, the channel is formed in a a-Si:H material which has the low mobility due to the high density of band tail states.

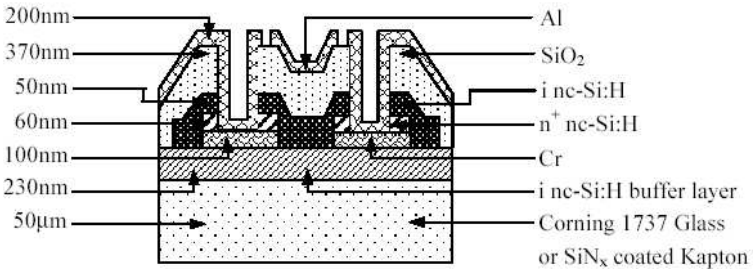

Figure 4.24: Top-gate TFT structure with bottom source and drain and seed layer. From [89].

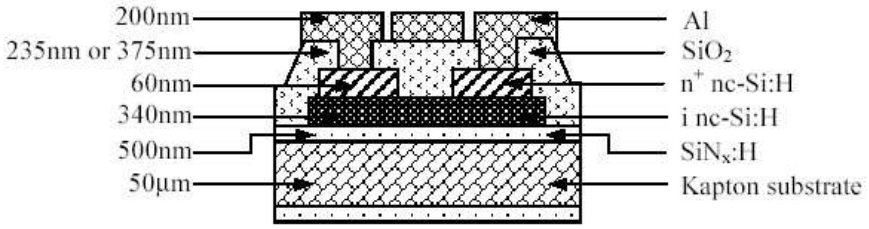

Figure 4.25: Top-gate TFT structure with top source and drain. From [89].

There are several different top-gate structures which can be fabricated to avoid this problem. Some examples of the types of structures being used in research are: staggered top-gate with a bottom source/drain [22] (see Figure 4.24) and coplanar top-gate with a top source/drain [10] (see Figure 4.25). The bottom source/drain structure can be made with or without the intrinsic seed layer. The top source/drain method has a small processing problem, whereby the active channel can easily be over-etched during the patterning of the source and drain contacts. The bottom source/drain does not have this problem since it is never in contact with the etching chemicals.

Chapter 5

Conclusion, Summary, and Recommendations

In this thesis pulsed PECVD was used to deposit the active layer and dielectric for bottom-gate TFTs. The characteristics of the TFTs such as its DC static electrical characteristics were measured and discussed, as well as its long-term stability, where the shift in the threshold voltage, V_t with time was measured. Important device parameters such as field-effect mobility, threshold voltage, sub-threshold slope, and on-off ratio were measured using a simple FET model and these basic parameters along with the α power law parameter was extracted according to a more complicated physical model.

Material characterization (structural and electrical) was performed on individual films 50 nm and 300 nm thick. Electrical properties, such as the dark and photo conductivity and Hall mobility were measured, as well as the optical band gap and the stability of the conductivity against light-soaking. The structural measurements include using Raman spectroscopy, XRD, and AFM to determine crystal grain structure (crystalline orientation and crystal size) and crystal fraction.

Pulsed PECVD has demonstrated that it can produce a highly crystalline material. Further optimization of the deposition conditions is needed to reduce the incubation layer and oxygen contamination. The TFT results are promising and could easily be improved through further optimization of the a-SiN:H and chan-

nel layers which would enable nc-Si:H TFTs on flexible substrates using pulsed PECVD.

5.1 Main Results

5.1.1 Structural

Individual 300 nm films show a high crystallinity, while 50 nm films are mostly made up of an amorphous incubation layer according to the Raman data. The thinner samples deposited with hydrogen dilution (50-2, 50-3, and 50-4) showed higher bonding order in the films, compared to the purely a-Si:H film 50-1. Clearly these films deposited by pulsed PECVD show a high dependency on the thickness of the grown films.

The XRD data showed that the 300 nm are mostly $\langle 111 \rangle$ oriented but with some $\langle 220 \rangle$ crystalline orientation as well. The crystalline grain size is small and less than 7.1 nm.

The AFM data shows that the even sample 300-2 which appeared amorphous in the Raman and XRD data looks drastically different from the a-Si:H sample 300-1. The AFM roughness measurements confirm the crystallite size in the thicker films to be around 6–7 nm.

5.1.2 Electrical

The 300 nm films 300-3 and 300-4 were most likely doped with oxygen as they showed high conductivity and high carrier concentration as determined by Hall effect measurements. The 50 nm showed high photo conductivity and low dark conductivity in the same range one would observe for a-Si:H. The conductivity did not vary much after one-month exposure to air and the crystalline samples 300-3 and 300-4 showed better stability under light-soaking.

The Hall mobility was measured to be $0.27\,\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$ and the carrier concentration was calculated to be $n = 1.1 \times 10^{17}\,\mathrm{cm}^{-3}$. The optical band gap was measured and the thin films had an optical gap of around 2–2.2 eV and the thick films had an optical gap of around 1.7–2 eV.

5.1.3 TFTs

A typical TFT showed the following characteristics: $\mu_{sat} < 0.38\,\mathrm{cm}^2$ V^{-1} s^{-1}, $V_{t,sat} \geq 7.3\,\mathrm{V}$, $I_{on/off} \geq 10^6$, S <1 V/decade, and a high V_t shift under gate bias stress. Using the Servati model for TFT-3, we obtained a high α parameter of 2.28, a threshold voltage of $V_T = 7.22\,\mathrm{V}$, a somewhat high source/drain resistance of $R_{DS}W = 17.8\,\mathrm{k\Omega{\cdot}cm}$, and an effective mobility of $0.23\,\mathrm{cm}^2$ V^{-1} s^{-1}. The high V_t may be due to charge trapped in the a-SiN:H layer and the high α may be due to a high trap density or possibly a defective a-SiN:H/channel interface. A very high theshold voltage shift was also observed which, like V_t, is probably also related to charge trapping in the a-SiN:H layer.

5.2 Recommendations

There are several recommendations for further research the area of pulsed PECVD TFTs, and namely, nc-Si:H TFTs. They are as follows:

- Oxygen concentration was high in samples 300-3 and 300-4 even though these samples were coated with an insulating a-SiN:H cap layer prior to shipping from MVSystems to the University of Waterloo. This indicates that oxygen most likely came from the inlet gases or from outgassing from the chamber. This two sources need to be reduced to ensure good low-conductivity films.

- The substrate may have some effect on the crystallinity of the film, as evidenced by the 50 nm films studied in this thesis, which did not have a visible crystalline structure as expected. Material characterization wafers in the future should always be deposited on the same layer structure as it would be in the TFT. For the bottom-gate staggered TFT case, this would mean deposition on a-SiN:H on top of glass.

- Each film material should be completely re-optimized for TFTs performance, this means the channel layer and the a-SiN:H should both be optimized.

- Instead of developing a process from scratch, a well-developed, reliable nc-Si:H process should be ported to a pulsed PECVD process. Parameters such as pulsing frequency, RF power, and duty cycle should be varied to observe effect on film quality, crystallinity, and TFT performance.

- The stability needs to be improved and the mechanisms of the metastability in this material need to be better understood in order to reduce it. This may be fixed once the optimized a-SiN:H layers are used. For bottom gate TFTs, it may not be possible to take advantage of higher mobility in nc-Si:H since conduction occurs in the bottom part of the film, however, it should be possible to take advantage of nc-Si:H's theoretically higher stability.

- A different TFT structure altogether can be used (see section §4.4), or a TFT structure with an increased channel thickness but without the increased source/drain resistance which usually accompanies an increase in channel thickness for staggered TFTs.

Appendix A

LCD Model

This following describes the equations used in this LCD model. This model is very simple, but some complicated back end functions were required to be able to solve the system simultaneously and also to be able to alter which variables to keep constant and which to vary, during the simulation.

A.1 Equations for LCD Model

The following equations (A.1)–(A.6) are all geometrical,

$$pixelArea = pixelWidth \times pixelHeight \tag{A.1}$$

$$pixelSkew = \frac{pixelWidth}{pixelHeight} \tag{A.2}$$

$$displayWidth = numWidth \times pixelWidth \tag{A.3}$$

$$displayHeight = numHeight \times pixelHeight \tag{A.4}$$

$$displayArea = displayWidth \times displayHeight \tag{A.5}$$

$$aspectRatio = \frac{displayWidth}{displayHeight} \tag{A.6}$$

Most of the above are important except for *pixelSkew* which could be used for non-square pixels, however, this would probably never be used.

Equations (A.7)–(A.9) relate the refresh rate, an important parameter for display performance to the line rate and the number of rows in the display.

$$refreshRate = \frac{1}{refreshTime} \tag{A.7}$$

$$lineRate = \frac{1}{lineTime} \tag{A.8}$$

$$refreshTime = lineTime \times numHeight \tag{A.9}$$

The *chargeRatio* is an important parameter, and must be sufficiently high to ensure that the pixel is fully charged during charging cycles. Anywhere where the gate length L would normally appear, *designRule* is used instead to represent the minimum feature size in the process.

$$\begin{aligned} chargeRatio &= \frac{1 - ae^{(-(lineTime-gateDelay)/\tau)}}{1 - be^{(-(lineTime-gateDelay)/\tau)}}, \quad \text{where} \\ \tau &= \frac{C_{px} \times fillFactor \times pixelArea}{\beta(V_g - V_t - V_d)}, \\ \beta &= \mu C_i \frac{tftWidth}{designRule}, \\ a &= \frac{V_d - V_{n0}}{V_d} \cdot \frac{2(V_g - V_t - V_d) + V_d}{2(V_g - V_T - V_d) + V_d - V_{n0}}, \quad \text{and} \\ b &= \frac{V_d - V_{n0}}{2(V_g - V_t - V_d) + V_d - V_{n0}} \end{aligned} \tag{A.10}$$

The *resolution* is an important metric in displays. It is a measure of the density of pixels and how finely spaced they are.

$$resolution = \frac{numWidth \times numHeight}{displayArea} \tag{A.11}$$

The *diagonal* is what is usually used to differentiate display sizes, as opposed to the horizontal or vertical dimensions. Common

diagonals include 10.4″, 14″, 17″, 19″, etc. ...

$$displayWidth^2 + displayHeight^2 = diagonal^2 \tag{A.12}$$

The gate delay is a time constant which is for charging the gate of a TFT due to the capacitance and resistance of the gate lines themselves.

$$gateDelay = \epsilon_{SiN} \times \rho_{gate} \times \frac{2 \times displayWidth^2}{t_{gate} \times t_{SiN}} \tag{A.13}$$

The fill factor is another important design parameter which must be kept at least above 0.5, preferably higher to have a high quality display.

$$\begin{aligned} fillFactor = 1 - \frac{unlitArea}{pixelArea}, \quad \text{where} \\ unlitArea = 3 \times tftWidth \times designRule + \\ designRule \times (pixelWidth + pixelHeight) \end{aligned} \tag{A.14}$$

In (A.14) the first term is the area of the source and drain (estimated) and the second and third terms are the area of the gate and data lines, respectively.

A.2 Source Code

The following code is written in Python and is used to calculate LCD parameters using a model described in section §A.1.

A.2.1 lcdModel.py

lcdModel.py is a class which represents a model a real LCD display. It stores the variables and constants and all their values as well as the equations used in the model.

```
import fpformat
from Numeric import *

#VARIABLES format: name, units, default value, pretty print units
    , conversion factor for pretty print
VARIABLES = [
    ["Pixel Area","m^2","2500.0e-12","um^2",1.e12], #0
```

```
    ["Pixel Width","m","50.0e-6","um",1.e6], #1
    ["Pixel Height","m","50.0e-6","um",1.e6], #2
    ["Pixel Skew","","1.0","",1.], #3
    ["# Width","pixels","800.","pixels",1.], #4
    ["# Height","pixels","600.","pixels",1.], #5
    ["Display Width","m","0.055","inches",1.e2/2.54], #6
    ["Display Height","m","0.041","inches",1.e2/2.54], #7
    ["Display Area","m^2","0.002","cm^2",1.e4], #8
    ["Aspect Ratio","","1.333","",1.], #9
    ["Refresh Rate","Hz","24.9","Hz",1.], #10
    ["Refresh Time","s","0.04","ms",1.e3], #11
    ["Line Rate","Hz","6.4e4","kHz",1.e-3], #12
    ["Line Time","s","1.6e-5","us",1.e6], #13
    ["Charge ratio","fraction","0.9","percent",1.e2], #14
    ["Resolution","pixels/m^2","2.2e9","pixels/cm^2",1.e-4], #15
    ["Diagonal","m","0.43","inches",39.37], #16
    ["mu","cm^2/Vs","1.0","V/cm^2*s",1.], #17
    ["TFT W","m","50.e-6","um",1.e6], #18
    ["Design Rule","m","50.e-6","um",1.e6], #19
    ["Cpix","F/m^2","10.**(-4)","pF",1.], #20
    ["Ci","F/m^2","2.0e-8","pF/um^2",1.], #21
    ["Gate resistivity","ohm-m","5.e-8","u-ohm-cm",1.e8], #22
    ["Gate delay","s","1.e-6","us",1.e6],#23
    ["Fill factor","no units","","",1.] #24
]

pixelArea = 0
pixelWidth = 1
pixelHeight = 2
pixelSkew = 3
numWidth = 4
numHeight = 5
displayWidth = 6
displayHeight = 7
displayArea = 8
aspectRatio = 9
refreshRate = 10
refreshTime = 11
lineRate = 12
lineTime = 13
chargeRatio = 14
resolution = 15
diagonal = 16
mu = 17
tftWidth = 18
designRule = 19
Cpix = 20
Ci = 21
gateResistivity = 22
gateDelay = 23
fillFactor = 24

class lcdModel:
#-----------------------------------------------------------------
    #for pixel area (total pixel area)
    def f0(self,x): return x[pixelArea] - x[pixelWidth]*x[
        pixelHeight]
```

```
#-------------------------------------------------------------
    #for pixel skew ratio
    def f1(self,x): return x[pixelSkew]*x[pixelHeight] - x[
        pixelWidth]
#-------------------------------------------------------------
    #for display width
    def f2(self,x): return x[displayWidth] - x[numWidth]*x[
        pixelWidth]
#-------------------------------------------------------------
    #for display height
    def f3(self,x): return x[displayHeight] - x[numHeight]*x[
        pixelHeight]
#-------------------------------------------------------------
    #for display area
    def f4(self,x): return x[displayArea] - x[displayWidth]*x[
        displayHeight]
#-------------------------------------------------------------
    #for aspect ratio
    def f5(self,x): return x[aspectRatio]*x[displayHeight] - x[
        displayWidth]
#-------------------------------------------------------------
    #for refresh rate
    def f6(self,x): return x[refreshRate]*x[refreshTime] - 1.0
#-------------------------------------------------------------
    #for line time
    def f7(self,x): return x[lineRate]*x[lineTime] - 1.0
#-------------------------------------------------------------
    #relate line time to frame time
    def f8(self,x): return x[refreshTime] - x[lineTime]*x[
        numHeight]
#-------------------------------------------------------------
    #charge time on pixel
    def f9(self,x):
        Vd = 12.
        Vn0 = 0.
        Vg = 24.
        Vt = 2.
        den = 2.*(Vg - Vt - Vd) + Vd - Vn0
        b = (Vd - Vn0)/den
        a = b*(2.*(Vg-Vt-Vd)+Vd)/Vd
        beta = x[mu]*x[Ci]*x[tftWidth]/x[designRule]
        tau = x[Cpix]*x[fillFactor]*x[pixelArea]/(beta*(Vg-Vt-Vd)
            )
        return log(1-x[chargeRatio])-log(a-b*x[chargeRatio])+(x[
            lineTime]-x[gateDelay])/tau
#-------------------------------------------------------------
    #resolution formula
    def f10(self,x): return x[resolution]*x[displayArea] - x[
        numWidth]*x[numHeight]
#-------------------------------------------------------------
    #diagonal formula
    def f11(self,x): return x[displayWidth]**2 + x[displayHeight
        ]**2 - x[diagonal]**2
#-------------------------------------------------------------
    #gate delay
    def f12(self,x):
        gateThickness = 100.e-9
```

```
        SiN_thickness = 250.e-9
        epsilon_SiN = 8.85e-14*6.9
        return x[gateDelay] - 2*x[displayWidth]*x[displayWidth]*
            epsilon_SiN*x[gateResistivity]/(gateThickness*
            SiN_thickness)
#-------------------------------------------------------------------
    #fill factor
    def f13(self,x):
        unlitArea = 3*x[tftWidth]*x[designRule] + x[designRule]*(
            x[pixelWidth]+x[pixelHeight])#factor of 3 is for
            Source/Drain
        return x[fillFactor] - 1 + (unlitArea/x[pixelArea])
#-------------------------------------------------------------------

    def __str__(self):
        """
        Print out objects
        """
        result = ""
        for i in range(len(self.x)):
            temp = 0.
            if abs(self.x[i]) < 10000. and abs(self.x[i])
                 > 0.001:
                number = fpformat.fix(self.x[i],3)
            else:
                number = fpformat.sci(self.x[i],3)
            result = result + VARIABLES[i][0] + ": " + number + "
                 " + VARIABLES[i][1] + "\n"
        return result

    def printOut(self,constants,pretty=0):
        """
        Print out objects in nice form, with or without units
            conversion to nice units

        pretty - if 1, converts to nice units, if 0, uses SI
            units

        return string
        """

        result = ""
        for i in range(len(self.x)):
            temp = 0.
            if pretty is 1:
                temp = self.x[i]*VARIABLES[i][4]
            else:
                temp = self.x[i]
            if abs(temp) < 10000. and abs(temp) > 0.001:
                number = fpformat.fix(temp,3)
            else:
                number = fpformat.sci(temp,3)
            for j in constants:
                if j == i:
                    temp = " "
                    break
                else:
```

```
                temp = "*"
            result = result + temp + VARIABLES[i][0] + ": " +
                number + " "
            if pretty is 1:
                result = result + VARIABLES[i][3] + "\n"
            else:
                result = result + VARIABLES[i][1] + "\n"
        return result

    def setX(self,x): self.x = x
    def getX(self): return self.x

    def __init__(self,x):
        """
        Initialization function
        """
        self.variables = VARIABLES
        self.funcs = [self.f0,self.f1,self.f2,self.f3,self.f4,
            self.f5,self.f6,self.f7,
                    self.f8,self.f9,self.f10,self.f11,self.f12,
                        self.f13]
        if len(x) != len(VARIABLES):
            print "Check the length of the x array."
        else:
            self.x = x
```

A.2.1.1 10inch.txt

The 10.4″display model is used in testLCD.py and is an approximation to a 640 × 480 PLANAR EL640×480-AM 10.4″display.

```
#640 x 480 PLANAR EL640x480-AM 10.4" display for military
    applications
    xs = range(len(VARIABLES))
    xs[pixelArea] = 1.0e-7
    xs[pixelWidth] = 330.0e-6
    xs[pixelHeight] = 330.0e-6
    xs[pixelSkew] = 1.0
    xs[numWidth] = 640.0
    xs[numHeight] = 480.0
    xs[displayWidth] = 0.210
    xs[displayHeight] = 0.158
    xs[displayArea] = 0.033
    xs[aspectRatio] = 1.3333
    xs[refreshRate] = 120.
    xs[refreshTime] = 0.008
    xs[lineRate] = 5.7e4
    xs[lineTime] = 1.7e-5
    xs[chargeRatio] = 0.95
    xs[resolution] = 10.e6
    xs[diagonal] = 0.26416
    xs[mu] = 1.
    xs[tftWidth] = 126.e-6
    xs[designRule] = 50.e-6
    xs[Cpix] = 6.e-5
```

```
    xs[Ci] = 2.0e-8
    xs[gateResistivity] = 5.e-8
    xs[gateDelay] = 1.e-7
    xs[fillFactor] = 0.523
```

A.2.1.2 21inch.txt

The 21″display model is used in testLCD.py and is an approximation to a 1600 × 1200 Samsung 213T 21″display.

```
#1600x1200 display, Samsung 213T 21" display
    xs = range(len(VARIABLES))
    xs[pixelArea] = 5.0e-8
    xs[pixelWidth] = 216.0e-6
    xs[pixelHeight] = 216.0e-6
    xs[pixelSkew] = 1.0
    xs[numWidth] = 1600.0
    xs[numHeight] = 1200.0
    xs[displayWidth] = 0.345
    xs[displayHeight] = 0.259
    xs[displayArea] = 0.089
    xs[aspectRatio] = 1.3333
    xs[refreshRate] = 75.
    xs[refreshTime] = 0.012
    xs[lineRate] = 1.e5
    xs[lineTime] = 1.e-5
    xs[chargeRatio] = 0.95
    xs[resolution] = 2.e7
    xs[diagonal] = 0.5334
    xs[mu] = 1.
    xs[tftWidth] = 63.e-6
    xs[designRule] = 25.e-6
    xs[Cpix] = 6.e-5
    xs[Ci] = 2.0e-8
    xs[gateResistivity] = 5.e-8
    xs[gateDelay] = 3.e-7
    xs[fillFactor] = 0.716
```

A.2.1.3 37inch.txt

The 37″display model is used in testLCD.py and is an approximation to a 1366 × 768 Sharp LC-37G4U 37″TV.

```
1366x768 Sharp LC-37G4U TV
    xs = range(len(VARIABLES))
    xs[pixelArea] = 5.0e-8
    xs[pixelWidth] = 216.0e-6
    xs[pixelHeight] = 216.0e-6
    xs[pixelSkew] = 1.0
    xs[numWidth] = 1366.0
    xs[numHeight] = 768.0
    xs[displayWidth] = 0.345
```

```
    xs[displayHeight] = 0.259
    xs[displayArea] = 0.089
    xs[aspectRatio] = 1.3333
    xs[refreshRate] = 75.
    xs[refreshTime] = 0.012
    xs[lineRate] = 1.e5
    xs[lineTime] = 1.e-5
    xs[chargeRatio] = 0.95
    xs[resolution] = 2.e7
    xs[diagonal] = 0.9398
    xs[mu] = 8.
    xs[tftWidth] = 63.e-6
    xs[designRule] = 25.e-6
    xs[Cpix] = 6.e-5
    xs[Ci] = 2.0e-8
    xs[gateResistivity] = 5.e-8
    xs[gateDelay] = 3.e-7
    xs[fillFactor] = 0.84
```

A.2.2 testLCD.py

testLCD.py is the script where all the initial conditions are defined and which calls to the functions which solve the model are made.

```
from dmath.newtonraphson import *
from Numeric import *
from lcdModel import *
from dmath.matrix import *
from scipy import gplt

def testlcdNewton():
    '''
    This is the main script to run to solve the model based on
        the
    initial guesses
    '''

    print "Starting LCD panel simulator"

    #set all variables/constants to initial guesses
    #1366x768 Sharp LC-37G4U TV
    xs = range(len(VARIABLES))
    xs[pixelArea] = 5.0e-8
    xs[pixelWidth] = 216.0e-6
    xs[pixelHeight] = 216.0e-6
    xs[pixelSkew] = 1.0
    xs[numWidth] = 1366.0
    xs[numHeight] = 768.0
    xs[displayWidth] = 0.345
    xs[displayHeight] = 0.259
    xs[displayArea] = 0.089
    xs[aspectRatio] = 1.3333
    xs[refreshRate] = 75.
    xs[refreshTime] = 0.012
```

```
xs[lineRate] = 1.e5
xs[lineTime] = 1.e-5
xs[chargeRatio] = 0.95
xs[resolution] = 2.e7
xs[diagonal] = 0.9398
xs[mu] = 8.
xs[tftWidth] = 63.e-6
xs[designRule] = 25.e-6
xs[Cpix] = 6.e-5
xs[Ci] = 2.0e-8
xs[gateResistivity] = 5.e-8
xs[gateDelay] = 3.e-7
xs[fillFactor] = 0.84

#make the model
theModel = lcdModel(xs)

#Set which variables are constant in the model

#To find fill factor, also set fill factor artificially low
    and uncomment the following
#constants = [pixelSkew,numWidth,numHeight,refreshRate,
    chargeRatio,diagonal,
#             mu,designRule,Cpix,Ci,gateResistivity]
#To find display size/resolution possible and uncomment the
    following
#constants = [pixelSkew,numWidth,numHeight,refreshRate,
    chargeRatio,
#             mu,designRule,Cpix,Ci,gateResistivity,
    fillFactor]


#Set up the variables that we want to solve for, based
#on what the user set as the "constants"
vars = []
j = 0
for i in range(len(theModel.funcs)+len(constants)):
    if j != len(constants) and constants[j] == i:
        j = j + 1
    else:
        vars.append(i)

#Error checking for incorrect number of unknowns/constants
if (len(vars) > len(theModel.funcs)):
    print "An incorrect number of unknowns/constants have
        been specified."
    print "You need to specify ", len(vars) - len(theModel.
        funcs), " variables as constant."
elif len(vars) < len(theModel.funcs):
    print "An incorrect number of unknowns/constants have
        been specified."
    print "You have specified too many variables as a
        constant.  Make ", len(theModel.funcs) - len(vars), "
         more variables unknown."
elif len(VARIABLES) != len(theModel.funcs) + len(constants):
    print "There is a problem with the model specification.
         Check it."
```

```
        print "The number of unknowns for this model should be "
            , len(theModel.funcs)
        print "and the number of constants should be ", len(
            VARIABLES)-len(theModel.funcs)

    #Actually solve the model
    else:
        newton2(theModel,vars,debug=0,iterations=10)
        print "Variables with * next to them were solved for"
        print theModel.printOut(constants,pretty=1)

def constants2var(model,constants):
    vars = []
    j = 0
    for i in range(len(model.funcs)+len(constants)):
        if j != len(constants) and constants[j] == i:
            j = j + 1
        else:
            vars.append(i)
    return vars

print "What do you want to do?"
print "(a) test the model"
char = raw_input("? ")
print char
if char == "a" or char == "a":
    testlcdNewton()
```

A.2.3 newtonraphon.py

newtonraphson.py is a solver for multiple non-linear equations. This function has been modified to handle varying constants/variable assignents.

```
from dmath.matrix import *
from dmath.linearsys import *
from Scientific.Functions.FirstDerivatives import *

def jacobian2(x, funcs, whichVars):
    """
    This one calculates the Jacobian based on some functions it
        is given
    and finds derivatives automatically
    funcs: a list of functions to find the first-order derivative
         of
    """
    jMatrix = mat0(len(whichVars), len(whichVars))
    for i in range(len(whichVars)):
        for j in range(len(whichVars)):
            func = funcs[i]
            temp = x[whichVars[j]]
            x[whichVars[j]] = DerivVar(temp)
            derivative = func(x)
            if isDerivVar(derivative):
```

```
                jMatrix[i][j] = float(derivative[1][0])
            else:
                jMatrix[i][j] = 0.0
            x[whichVars[j]] = temp
    return jMatrix

def makeF(x, funcs, whichVars):
    """
    This puts together the F function for the newton-raphson
    solver
    """
    fMatrix = vec0(len(whichVars))
    for i in range(len(whichVars)):
        func = funcs[i]
        fMatrix[i] = func(x)
    return vec2Col(fMatrix)

def newton2(model,whichVars,debug=0,iterations=20,TOL=1.0e-9):
    """
    multivariable newton's method given functions for f and j
    and an initial guess x, all matrices. Does n steps
    As warned in the text, keep n small and check frequently
    iterations is the maximum iterations
    This one uses jacobian2 and hence doesn't require any
    pre-defined derivative functions
    """
    flag = 0
    error = vec0(len(whichVars))
    for i in range(iterations):
        deltax=gausssolve(jacobian2(model.x,model.funcs,whichVars
            ),
                          makeF(model.x,model.funcs,whichVars))
                              #or do lu factor-solve
        for var in range(len(whichVars)):
            if debug == 1:
                print "var: ",var
                print "x[whichVars[var]]: ", "%.4e" % model.x[
                    whichVars[var]]
            error[var] = abs(deltax[var][0]/model.x[whichVars[var
                ]])
            model.x[whichVars[var]] = model.x[whichVars[var]] -
                deltax[var][0]
        if debug == 1:
            print "Iteration #:", i, " x:", vecOut(model.x)
            print "max error: ", max(error)
        else:
            print ".",
        if max(error) < TOL:
            print "\nNewton's Method succeeded in",i,"iterations
                .  Error is within",TOL*100,"% tolerance\n"
            return model.x
    print "reached maximum number of newton iterations: ",
        iterations
    return model.x
```

Appendix B

TFT Parameter Extraction Scripts Source Code

The following code is written in Python and is used to extract various parameters using a simple model from TFT transfer characteristics curves.

B.1 extract.py

extract.py contains the back-end functions which perform the extraction the curves.

```
##############################################################################

# extract.py - All functions to do actual extraction from IDS vs
    . VGS/VDS
#                curves
# @author: David J. Grant
# @copyright: 2003 David J. Grant
# @license: GPL (details at http://www.gnu.org)
# @dependencies: Numeric, Scipy, and David's dmath libraries
#
##############################################################################


from Numeric import *
from MLab import *
from scipy import gplt
from dmath.discreteDeriv import *
from dmath.dmath_util import *
from dmath.bestFitLine import *
from util.plot_util import *
from extraction.TFT import *
```

```
import sys,string
import re

def forwardCurrent(VGS,a,VDS,L,errorFactor=0.):
    """
    Useful for generating forward current curves from a TFT model

    This returns the forward current as a function of:
    VGS - the array of VGS values to calculate current for
    a - a TFT object instance, which contains all the parameters
    VDS - The voltage from drain to source that is applied
    L - the physical gate length
    errorFactor - a factor for some error when creating fake data
        . Make large for no error, small for lots of error
    """
    y = []
    x = []
    temp = 0.
    for i in range(len(VGS)):
        if VGS[i] > a.Vt+0.5*VDS:
            #forward regime
            temp = a.mu*a.zeta*(a.Ci**(a.alpha-1))*(a.W/(L+a.
                delta_L))*((VGS[i]-a.Vt-0.5*VDS)**(a.alpha-1))
            I = (temp*VDS)/(1+temp*(a.RDSW/(a.W*1.e-6)))
            if errorFactor != 0.:
                I = (1+rand()/errorFactor)*I
            y.append(I)
            x.append(VGS[i])
    return x,y

def extractSOnOff(Vgs, Ids):
    """
    This extracts the subthreshold slope and the on-off ratio
        given:

    Vgs = The gate source voltage data from the TFT
    Ids = The drain source current data from the TFT

    returns S, logionoff, lowIds
    """

    #Convert to Numeric array
    Ids = array(Ids)
    Vgs = array(Vgs)

    #Check for negative values of current which will screw things
        up
    firstNonNegativeIndex = 0
    for i in range(len(Ids)):
        if Ids[i] < 0.:
            Ids[i] = abs(Ids[i])
            print "warning: current at VGS = ",Vgs[i],"is
                negative"
            firstNonNegativeIndex = i+1

    #Find the slope of the curve using a 5-point discrete
        derivative algorithm
```

```
    logIds = log10(Ids)
    dlogIds = derivVecX(logIds[firstNonNegativeIndex:],Vgs[
        firstNonNegativeIndex:])

    #Plot data
    plotter(Vgs,logIds,new=1)
    if sys.platform != 'win32':
        plotter(Vgs[firstNonNegativeIndex:],dlogIds,new=1)

    #Ask user where to measure S from, enter 99 for the point
        where the slope S is maximum
    Spoint = input("Enter point to measure S from (enter 99 for
        max): ")

    #Calculate S
    if Spoint == 99:
        S = 1./max(dlogIds)
    else:
        S = 1./dlogIds[searchsorted(Vgs[firstNonNegativeIndex:],
            Spoint)]

    #Ask user where to take min/max current from
    lowVgs = input("Enter low Vgs for lowest current point (enter
         99 for minimum): ")
    highVgs = input("Enter high Vgs for highest current point (
        enter 99 for maximum): ")

    #Calculate min/max current and Ion/Ioff
    if lowVgs == 99:
        lowIds = min(Ids)
    else:
        lowIds = Ids[searchsorted(Vgs,lowVgs)]
    if highVgs == 99:
        highIds = max(Ids)
    else:
        highIds = Ids[searchsorted(Vgs,highVgs)]
    ionoff = highIds/lowIds
    log10ionoff = log10(ionoff)

    return S, log10ionoff, lowIds

def extractVtMu(Vgs,Ids,C,W,L,sat=1,Vds=0.1):
    """
    This extracts the field-effect mobility and the threshold
        voltage Vt, given:

    Vgs - An array of VGS values
    Ids - An array of IDS values
    C - The capacitance per unit cm^2 of the gate dielectric
    W - The width of the channel in any units
    L - The length of the channel in any units
    sat - If 1, extract for saturation regime, if 0, extract for
        linear regime
    Vds - The drain-to-source voltage

    returns mu,Vt
    """
```

```
    #Plot a graph of the data
    if sat is 0:
        plotter(Vgs,Ids,new=1)
        dIds = derivVecX(Ids,Vgs)
        plotter(Vgs,dIds/max(dIds)*max(Ids))
    else:
        Ids = Ids**(0.5)
        plotter(Vgs,Ids,new=1)
        dIds = derivVecX(Ids,Vgs)
        plotter(Vgs,dIds/max(dIds)*max(Ids))

    #Ask use for range
    lowVgs = input("Enter low Vgs to start from for extraction of
         mu and Vt:")
    highVgs = input("Enter high end of VGS for extraction of
        alpha and Vt:")
    lowVgs_index = searchsorted(Vgs,lowVgs)
    highVgs_index = searchsorted(Vgs,highVgs)

    #Extract alpha and threshold voltage
    I_fit = []
    V_fit = []

    for i in range(lowVgs_index,highVgs_index+1):
        I_fit.append(Ids[i])
        V_fit.append(Vgs[i])

    #Do fitting
    V_fit = array(V_fit)
    I_fit = array(I_fit)

    #Plot fit data
    plotter(V_fit,I_fit,title="graph for fitting alpha and Vt")
    fitted_data,slope,intercept,chi = bestFitLine(V_fit,I_fit)
    plotter(V_fit,fitted_data)

    #Calculate mu and Vt
    if sat is 0:
        mu = (slope*L)/(C*W*Vds)
    else:
        mu = (slope**2*2*L)/(C*W)
    Vt = -intercept/slope

    return mu,Vt

def generateData(baseFileName = "Peyman2_VGS_",errorFactor
     = 10000000.,VDS = 0.1,Vmax = 21.0):
    '''
    Just run this once to create some Ids vs. Vgs data for
        different L
    Then after that, use the files in the directory to do test
        extractions

    baseFileName - the base filename to use
    errorFactor - some random error added to the data
    VDS = the drain source voltage to apply
```

```
    Vmax = what gate voltage you want to measure up to
    '''

    #Define a TFT
    aTFT = TFT_peyman(2.085,3.9,4.03,0.94,2.3,5.4,100.,1.3e-8)

    #For generated data, this is the different lengths to use, in
        metres
    L = [25.,50.,75.,100.,200.]

    #This is the array of IDS vs. VGS for varying L
    #The format is this: IS_L[Leff][Vgs_index]
    IDS_L = []
    VGS_L = []

    #Make some fake data and write it to a file
    for i in range(len(L)):
        fileName = baseFileName+"L"+repr(L[i])+".csv"
        VGS = arange(0,Vmax,0.2)
        x,IDS = forwardCurrent(VGS,aTFT,VDS,L[i],errorFactor)
        #For generating fake reverse current
        for i in range(len(VGS)-len(x)):
            IDS.insert(0,IDS[0]/(10.*(i+1)))
        IDS_L.append(IDS)
        VGS_L.append(VGS)

        gplt.plot(VGS,IDS)

        f=open(fileName,'w')
        f.write("VGS,IDS\n")
        for j in range(len(VGS)):
            f.write(repr(VGS[j])+","+repr(IDS[j])+"\n")
        f.close()

    #Plot output data using Biggles
    bigglesPlotter(VGS_L[0],IDS_L,title="IDS vs. VGS",xtitle="x",
        lines=1,points=0,color=1,filename="test")

if __name__ == "__main__":
    generateData()
```

B.2 runExtract.py

runExtract.py implements a simple console UI for interaction with the program.

```
##############################################################################

# runExtract.py - This script runs the command-line user
    interface, opens
#                 files, and then runs functions in the extract.
    py module.
# @author: David J. Grant
```

```
# @copyright: 2003-2004 David J. Grant
# @license: GPL (details at http://www.gnu.org)
# @dependencies: Numeric, Scipy, David's dmath libraries, and
    extract.py
#
###############################################################################


from extraction.extract import *
from Numeric import *
from extraction.TFT import *
from string import *
from util import csv_util
import Tkinter
import tkFileDialog
import os.path
import sys


def main_loop():
    """
    This is the main loop.  Runs infinitely, showing the menu for
        the user
    until he/she quits.
    """
    char = ''
    fileindex = 0
    filenames = []

    while char != 'q':
        print "Welcome to David's TFT extraction utility"
        print "What do you want to do?\n"

        print "File operations:"
        print "(o)pen files\n"

        if len(filenames) == 0:
            print "***No files loaded***"
            print "Press 'o' to load comma-delimited file"
        else:
            if fileindex == len(filenames):
                print "No more files to process!"
                print "Restarting..."
                fileindex = 0
                filenames = []
            else:
                print "Current working files:"
                for i in range(len(filenames)):
                    print os.path.basename(filenames[i]), #
                    if i == fileindex:
                        print "<-------current working file", #
                    print ''
                print fileindex + 1, "of",len(filenames),"files"


        print "\nExtract:"
```

```
print "(a) Extract Vt, mu, from a single transfer
    characteristic"
print "(b) Extract S and Ion/off from a single transfer
    characteristic"

print "Other:"
print "(q)uit\n"
char = raw_input("? ")

#if user typed 'o', open file open... dialog
if char is "o":
    if len(filenames) != 0:
        append = raw_input("Do you want to (a)ppend or (s
            )tart from scratch")
    else:
        append = 's'
    root = Tkinter.Tk()
    root.withdraw()
    if append is 'a':
        if sys.platform == 'win32':
            filenames.append(tkFileDialog.askopenfilename
                (filetypes=[("comma-delimited","*.CSV"),(
                "comma-delimited","*.csv"),("All files","
                *.*")]))
        else:
            filenames.extend(tkFileDialog.askopenfilename
                (filetypes=[("comma-delimited","*.CSV"),(
                "comma-delimited","*.csv"),("All files","
                *.*")],multiple=1))
    elif append is 's':
        if sys.platform == 'win32':
            filenames = [tkFileDialog.askopenfilename(
                filetypes=[("comma-delimited","*.CSV"),("
                comma-delimited","*.csv"),("All files","
                *.*")])]
        else:
            filenames = tkFileDialog.askopenfilename(
                filetypes=[("comma-delimited","*.CSV"),("
                comma-delimited","*.csv"),("All files","
                *.*")],multiple=1)
    filecounter = len(filenames)

#if user typed 'a', extract Vt and mu, from either linear
     or saturation curves
elif char == "a":
    if len(filenames) is 0:
        print "You have not opened any files yet!"
        continue

    file = filenames[fileindex]
    print "Now processing file:", os.path.basename(file)
    print csv_util.csv2matrix(file)[1]
    x_name = raw_input("What is the name of the X column
        ? ")
    y_name = raw_input("What is the name of the Y column
        ? ")
```

```
            isSat = raw_input("Is this saturation data (y or n)?
                ")

            VGS,IDS,L,header = readDataFromFile([file],x_name,
                y_name)
            print "L = %.1f um" % L[0]
            if isSat is 'n':
                mu,Vt = extractVtMu(VGS[0],IDS[0],2.e-8,100.,L
                    [0],sat=0)
            else:
                mu,Vt = extractVtMu(VGS[0],IDS[0],2.e-8,100.,L
                    [0],sat=1)
            print "mu = %.4f cm^2/V*s" % mu
            print "Vt = %.2f V" % Vt

            done = raw_input("Are you done with this file (y or n
                )? ")
            if done is 'y':
                fileindex = fileindex + 1

        #if user typed 'b', extract S and Ion/off from V=10V
            curve
        elif char == 'b':
            if len(filenames) is 0:
                print "You have not opened any files yet!"
                continue

            file = filenames[fileindex]
            print "Now processing file:", os.path.basename(file)
            print csv_util.csv2matrix(file)[1]
            x_name = raw_input("What is the name of the X column
                ? ")
            y_name = raw_input("What is the name of the Y column
                ? ")

            VGS,IDS,L,header = readDataFromFile([file],x_name,
                y_name)
            S,Ionoff,Ioff = extractSOnOff(VGS[0],IDS[0])
            print "S = %.2f" % S
            print "Ionoff = 10^%.2f OR Ionoff > 10^%d" % (Ionoff
                , floor(Ionoff))
            print "Ioff = %.2e" % Ioff
            done = raw_input("Are you done with this file (y or n
                )? ")
            if done is 'y':
                fileindex = fileindex + 1

        elif char == "d":
            print "do nothing"


if __name__ == "__main__":
    main_loop()
```

B.3 TFT.py

TFT.py provides a TFT object which is used to store all TFT parameters.

```
class TFT_peyman:
    def __init__(self,alpha,Vt,zeta,mu,RDSW,delta_L,W,Ci):
        #unitless
        self.alpha = alpha
        #stored in volts
        self.Vt = Vt
        #stored in (C/cm**2)**(alpha-2)
        self.zeta = zeta
        #stored in cm^2/Vs
        self.mu = mu
        #stored in ohm*m
        self.RDSW = RDSW
        #stored in microns
        self.delta_L = delta_L
        #stored in microns
        self.W = W
        #stored in F/cm**2
        self.Ci = Ci

    def printAll(self):
        print "Alpha = ",self.alpha
        print "Vt = ",self.Vt, "V"
        print "Zeta = ",self.zeta,"(C/cm**2)**(alpha-2)"
        print "mu = ",self.mu,"cm^2/Vs"
        print "RDSW = ", self.RDSW/10.,"kohm*cm"
        print "RDS=",self.RDSW/(self.W*1.e-6),"ohms"
        print "delta_L = ", self.delta_L, "um"
        print "W = ", self.W, "um"

if __name__ == "__main__":
    myTFT = TFTobject(2.,1.,1.,1.,1000.,1.e6,1.,10.)
    myTFT.printAll()
```

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Glossary

AFM Atomic Force Microscope - A microscope used to capture information about the atomic structure on the surface of a sample.

AMLCD Active-Matrix Liquid Crystal Display - A liquid crystal display whose pixels are turned on and off usually by a TFT

a-Si amorphous silicon - Disordered silicon, usually formed by PECVD deposition at low temperature or by sputtering from a silicon target.

a-Si:H hydrogenated amorphous silicon - Amorphous silicon which has some hydrogen incorporated within its structure which can help to passivate defects

Al aluminium - Metal which is commonly used in the top metallization of a TFT process, deposited by sputtering or evaporation.

Ar argon - Argon is an inert gas which is commonly ionized for use as a bombardment ion in sputtering systems.

BHF Buffered Hydrofluoric Acid - A strong acid, buffered with Ammonium Fluoride, its primary use in thin-film fabrication is for etching silicon nitride (SiN)

CdS cadmium sulfide - Light-sensitive amorphous semiconductor

c-Si crystalline silicon - Pure crystalline silicon with a single crystallographic orientation.

CMOS Complementary Metal Oxide Silicon - A CMOS device normally consists of n-type and p-type MOS devices.

σ_d dark conductivity - The conductivity of a sample when it is not exposed to light.

σ_p photo conductivity - The conductivity of a sample when it is exposed to light.

CRT Cathode Ray Tube - It is the display device used in most computer displays, video monitors, televisions and oscilloscopes[1].

Cu copper

CW Continuous Wave - Unmodulated; DC - Water that has had all or most of the dissolved ions removed.

DOS Density of States - The number of available and occupied states per unit energy.

ECR-CVD Electron Cyclotron Resonance Chemical Vapour Deposition - A "remote" CVD technique, where the reaction does not occur directly near the substrate, reducing ion bombardment.

FET Field-Effect Transistor - A transistor which operates via the field-effect, modulating the current in one direction by control of an electric field in another.

FPD Flat-Panel Display - Displays which are flat unlike CRT, such as LCDs and Organic Light-Emitting Diode (OLED) displays

FWHM Full-Width Half Maximum - The width of a Gaussian peak (typically) at the point where the intensity is half that at the peak.

GaAs gallium arsenide

[1] From `http://en.wikipedia.org/wiki/Cathode_ray_tube`

GXRD Grazing-incidence XRD - Method for determining the crystallographic planes of a thin film material using x-rays.

H_2 hydrogen gas

HRTEM High Resolution Transmission Electron Microscopy -

HWCVD Hot-wire Chemical Vapour Deposition - CVD performed by using high temperature filaments to thermally "crack" the source gas into radicals and ions.

IR Infrared

KOH potassium hydroxide - Potassium hydroxide is a base, which etches silicon. - A technique of growing nc-Si:H a layer at a time.

LCD Liquid Crystal Display - Display where a "liquid crystal" can either block or allow a back-light to pass through, depending on the voltage applied across the crystals.

LPCVD Low Pressure Chemical Vapour Deposition - At high temperature and low pressure, silane gas (SiH_4) can be separated into silicon and hydrogen atoms, which leads to subsequent deposition of silicon atoms on the substrate.

Mo molybdenum - A metal which is frequently used as the bottom-gate metallization in TFT processes.

i-nc-Si:H intrinsic nanocrystalline silicon - An undoped, intrinsic nc-Si:H layer. [2]

MOSFET Metal Oxide Semiconductor Field-Effect Transistor - A field-effect transistor made of a metal/polysilicon gate, an oxide dielectric, and a semiconductor active layer.

n^+-nc-Si:H n^+ doped nanocrystalline silicon - Silicon with some some crystalline fraction embedded in an amorphous phase and doped with a donor element, typically phosphorous

[2] In many cases this material is never totally undoped as it easily absorbs oxygen during and after deposition. Oxygen acts as an n-type donor in nc-Si:H.

nc-Si:H nanocrystalline silicon - Silicon which is made up of amorphous silicon and embedded crystallites of crystalline silicon

OLED Organic Light Emitting Diode

R_a mean roughness - Arithmetic average of the deviations from the centre plane. - A cleaning process developed at RCA for cleaning wafers for semiconductor processes.

R_q RMS roughness - Standard deviation of the Z (height) values within a given area in an AFM measurement

PAN Phosphoric Acetic Nitric acid - PAN is an etchant made up of phosphoric acid, acetic acid, nitric acid, and water.

PECVD Plasma-Enhanced Chemical Vapour Deposition - CVD in which radicals are formed from the gas phase by the creation of a plasma due to a high capacitive or inductive electric field.

poly-Si polycrystalline silicon - A type of crystalline silicon with no continuous crystalline orientation, but many crystalline grains

RF Radio Frequency - A range of frequencies in the electromagnetic spectrum from about 100 kHz–1 GHz.

RMS Root Mean Square - Equivalent to standard deviation

SE Spectroscopic Ellipsometry - A technique used for measuring thin film thickness and optical constants.

Si silicon

SiH_4 silane - Gas from which a-Si:H and nc-Si:H films are normally grown.

a-SiN:H amorphous silicon nitride - A dielectric material, similar to silicon oxide, only it contains silicon, nitrogen, as well as hydrogen and other contaminants.

SiO silicon oxide - A dielectric material, used as the dielectric in c-Si and poly-Si TFTs.

SPM Scanning Probe Microscopy - Microscopic technique which involve scanning a probe across a surface.

TCO Transparent Conductive Oxide - These include ZnO and ITO (Indium Tin Oxide) used extensively in thin film solar cell fabrication.

TFT Thin-Film Transistor - A transistor which made by deposited and etching subsequent layers, normally made with amorphous semiconductors.

μc-Si microcrystalline silicon - Microcrystalline silicon is similar to nc-Si:H, only the grain size is on the order of microns, instead of nanometres [3].

UV Ultra Violet - Part of the electromagnetic spectrum at energies higher than the highest energies in the visible spectrum. - UV reflectance measures the light reflected by the material for band gap analysis.

VHF Very-High Frequency - In terms of PECVD it refers to frequencies.

X_c crystalline fraction - Defined as $\gamma_c/(\gamma_c+\gamma_a)$, the percentage of nanocrystalline silicon which is crystalline.

XRD X-Ray Diffraction - Method for determining the crystallographic planes using x-rays.

[3]The terms nc-Si:H and μc-Si are sometimes used interchangeably.