Amorphous Silicon Thin Film Transistor Models and Pixel Circuits for AMOLED Displays

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

Hydrogenated amorphous Silicon (a-Si:H) Thin Film Transistor (TFT) has many advantages and is one of the suitable choices to implement Active Matrix Organic Light-Emitting Diode (AMOLED) displays. However, the aging of a-Si:H TFT caused by electrical stress affects the stability of pixel performance. To solve this problem, following aspects are important: (1) compact device models and parameter extraction methods for TFT characterization and circuit simulation; (2) a method to simulate TFT aging by using circuit simulator so that its impact on circuit performance can be investigated by using circuit simulation; and (3) novel pixel circuits to compensate the impact of TFT aging on circuit performance. These challenges are addressed in this thesis.

A compact device model to describe the static and dynamic behaviors of a-Si:H TFT is presented. Several improvements were made for better accuracy, scalability, and convergence of TFT model. New parameter extraction methods with improved accuracy and consistency were also developed. The improved compact TFT model and new parameter extraction methods are verified by measurement results.

Threshold voltage shift (ΔV_T) over stress time is the primary aging behavior of a-Si:H TFT under voltage stress. Circuit-level aging simulation is very useful in investigating and optimizing circuit stability. Therefore, a simulation method was developed for circuit-level ΔV_T simulation. Besides, a ΔV_T model which is compatible to circuit simulator was developed. The proposed method and model are verified by measurement results.

A novel pixel circuit using a-Si:H TFTs was developed to improve the stability of OLED drive current over stress time. The ΔV_T of drive TFT caused by voltage stress is compensated by an incremental gate voltage generated by utilizing a ΔV_T-dependent charge transfer from drive TFT to a TFT-based Metal-Insulator-Semiconductor (MIS) capacitor. A second MIS capacitor is used to inject positive charge to the gate of drive TFT to improve OLED drive current. The effectiveness of the proposed pixel circuit is verified by simulation and measurement results. The proposed pixel circuit is also compared to several conventional pixel circuits.

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Dedication

To my lovely wife and kind parents.

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Chapter 1

Introduction

1.1 OLED for Flat-Panel Displays

The fast progress of Organic Light-Emitting Diodes (OLED) has led to the development of flat-panel display technology based on OLED. Novel OLED display technology is superior to traditional Active Matrix Liquid Crystal Display (AMLCD) technology in terms of view angle, response speed, contrast, weight, power consumption, and cost [1]. Besides, it can be fabricated onto flexible substrates [1]. OLED technology is used in some small-size displays and is expected to be widely used in large-size displays.

1.2 OLED Display Architectures

OLED flat-panel displays can be implemented by using passive or active driving architectures. Passive Matrix OLED (PMOLED) architecture is shown in Figure 1.1 [2]. The array is addressed row by row by a row driver. When a row of OLEDs is addressed, the row line is connected to ground. Then, a column driver provides driving currents, which represent image information, through column lines to the OLEDs in the addressed row. Since there is no component used on display panel to store image information, when the OLEDs in one row are addressed, the OLEDs in other rows are turned OFF.

In PMOLED architecture, OLEDs are ON to emit light only when they are addressed by a row driver. Therefore, to achieve the average light energy for a required apparent brightness in a refresh cycle, OLEDs must be driven with high instant current density

during their short ON time in a refresh cycle. Although PMOLED architecture is advantageous in terms of simplicity, it is not suitable for large-size high-resolution flat-panel displays because of the problems summarized as follows [1–7]. Primarily, the high instant OLED current density associated to PMOLED architecture causes some problems:

- The power efficiency of OLED is high when current density is low or medium, but low when current density is high. To compensate the reduced power efficiency at high current density, an extra OLED current has to be supplied, so the advantage of OLED in reducing power consumption is compromised by the high instant OLED current density associated to PMOLED architecture.
- The aging of an OLED is dependent on the total charge injected to the OLED, so an extra current supplied to an OLED reduces its lifetime.
- A higher power consumption also causes heat-induced degradation.
- Because of high instant OLED current density, OLED pulse voltage has a large swing, resulting in a significant dynamic power consumption due to OLED capacitance.
- The large swing of OLED pulse voltage also makes it difficult to implement a column driver (essentially a current source) by using inexpensive CMOS technology.
- The column lines in PMOLED display are typically made of Indium Tin Oxide (ITO), which is OLED anode material and much more resistive than metal. Therefore, high OLED currents lead to significant voltage drops across column lines, resulting in a considerable power consumption and image non-uniformity.

In addition, PMOLED architecture also has the crosstalk problem caused by the leakage currents of reversely biased OLEDs. When display size is increased, the aforementioned problems become more serious. Therefore, the application of PMOLED architecture is limited to small-size displays (*e.g.*, less than 180 lines [1]).

Because of the problems of PMOLED architecture, Active Matrix OLED (AMOLED) architecture was developed and has been widely used [1–7]. AMOLED architecture is shown in Figure 1.2 [2]. Thin Film Transistors (TFTs) are used in each pixel on AMOLED display panel. When the pixels in a row are addressed by a row driver, they are put into programming phase. The switch TFTs in the pixels in the row are turned ON by the row driver, connecting a column driver to the internal nodes of the pixels in the row. The column driver provides data voltages or currents, which represent image information, to the pixels in the addressed row. At the end of programming phase, the row driver turns

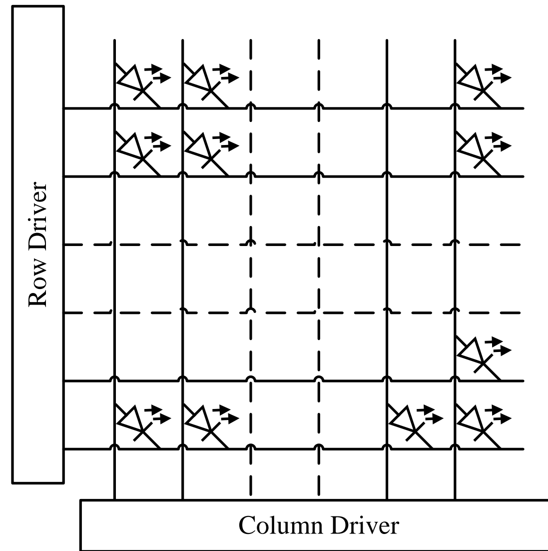


Figure 1.1: Passive matrix OLED display architecture.

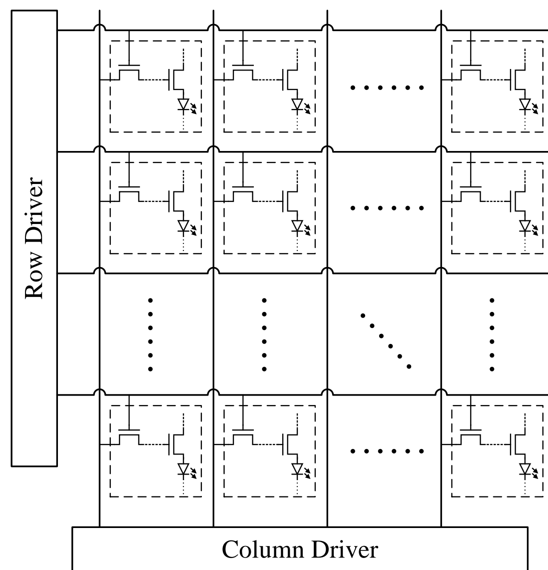


Figure 1.2: Active matrix OLED display architecture.

OFF the switch TFTs in the pixels in the row, so that the pixels are put into driving phase, holding the image information inside themselves. Programming operation is carried out row by row through out the whole panel. A typical frame refresh frequency is 60 Hz.

In driving phase, the image information stored in a pixel is used by the drive TFT in the pixel to modulate OLED current. Since the OLEDs used in AMOLED architecture continuously emit light throughout driving phase, peak OLED currents in AMOLED architecture are much lower in than those in PMOLED architecture. Besides, all global interconnection lines can be made of metal instead of ITO, so the resistivity of these lines is significantly reduced. In addition, unlike PMOLED architecture, AMOLED architecture does not have the crosstalk problem caused by OLED leakage currents. Since AMOLED architecture has these advantages, it is widely used in OLED-based flat-panel displays.

1.3 TFT for AMOLED Displays

Although researches so far have covered various materials as the active layer of TFT, polycrystalline-Silicon (poly-Si) TFT and Hydrogenated amorphous Silicon (a-Si:H) TFT are two main types which are used in AMOLED displays.

Poly-Si TFT has higher field mobilities (up to 100 $\mathrm{cm^2/(Vs)}$) and complementary types (*i.e.*, n-channel and p-channel [4]). Besides, the stability of I-V characteristics of poly-Si TFT under voltage stress over time is much better than that of a-Si:H TFT. However, the characteristics of poly-Si TFT have large spatial variations (especially threshold voltage V_T) due to the non-uniformity of crystallization during laser annealing of poly-Si [8, 9]. These spatial variations lead to significant non-uniformities of pixel performance and image quality across display panel. Besides, poly-Si TFT technology has a higher fabrication cost, because extra process steps must be used for the crystallization of poly-Si.

Although the field mobility of a-Si:H TFT (typically $\leqslant 1$ $\mathrm{cm^2/(Vs)}$) is much lower than that of poly-Si TFT, it is adequate for a-Si:H TFT to drive OLED [6, 10]. Besides, a-Si:H TFT has good spatial uniformity, which is important for large-area electronics. Since it has been widely used in AMLCD display for many years, its fabrication process is mature, readily available, and inexpensive. Finally, since its fabrication temperature is relatively low, its can be fabricated on flexible substrates (*e.g.*, plastic). Therefore, a-Si:H TFT is one of the suitable types of TFTs to be used in AMOLED displays.

Although a-Si:H TFT has many advantages, it has a major drawback in terms of temporal instability caused by voltage stress [4]. When a-Si:H TFT is stressed by gate voltage, its threshold voltage (V_T) shifts over stress time. The TFTs in AMLCD displays

are used simply as switch transistors, which are ON only during short programming phase, so their aging is not significant. In contrast, the TFTs in AMOLED displays are used as drive TFTs (*i.e.*, the transistors to drive OLEDs) as well as switch transistors. Since drive TFTs are always ON during driving phase, which is much longer than programming phase, they have significant aging over stress time. The aging of a-Si:H TFT is typically characterized as threshold voltage shift (ΔV_T). If not compensated, the ΔV_T of drive TFT leads to unstable OLED current and brightness over stress time.

1.4 Outline

The ΔV_T of a-Si:H TFT caused by voltage stress has a significant impact on the stability of performance of AMOLED displays. Several aspects are very important when developing the pixel circuits with improved performance and stability. These aspects are addressed in this thesis in following chapters.

Chapter 2 provides the reviews of widely used compact models and parameter extraction methods of a-Si:H TFT, and presents the improvements and innovations made on the compact models and parameter extraction methods. The improved a-Si:H TFT models and parameter extraction methods are verified by measurement results.

Chapter 3 provides a review of the ΔV_T models of a-Si:H TFT for different stress conditions, and then presents a novel simulation method developed for the circuit-level simulation of ΔV_T. The developed ΔV_T simulation method is verified by the comparison between simulation results and the measurement data obtained from literatures.

Chapter 4 provides a brief review of conventional pixel circuits of AMOLED displays, and then presents a novel voltage-programmed pixel circuit which uses a novel ΔV_T-compensation mechanism to improve the stability of OLED drive current for AMOLED displays. The effectiveness of the proposed pixel circuit is verified by simulation and measurement results. Besides, the proposed pixel circuit is compared to some conventional voltage-programmed and current-programmed pixel circuits.

Chapter 5 concludes the whole thesis, and provides insights for future work.

Chapter 2

Compact Device Modeling of a-Si:H TFT

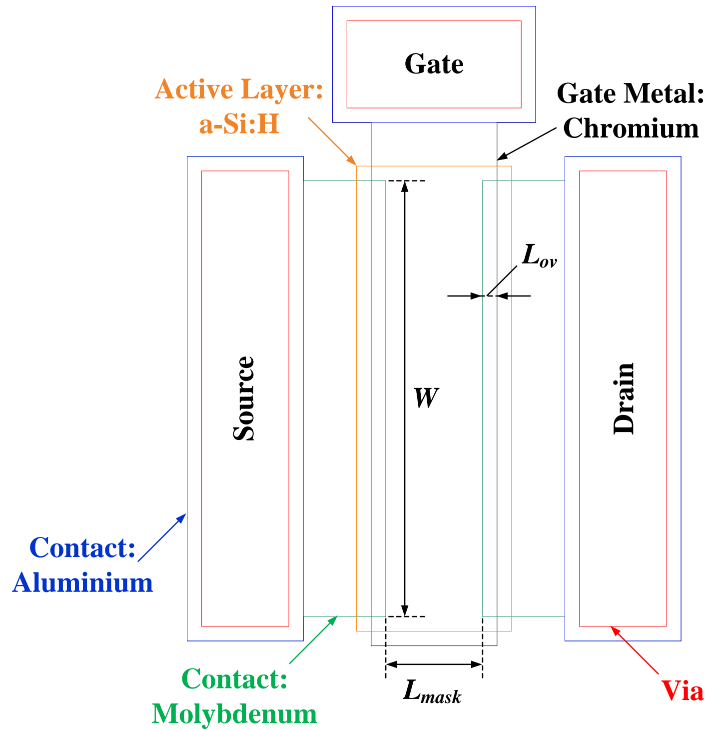
The compact device modeling of a-Si:H TFT is very important and useful for device characterization as well as circuit design, analysis, and simulation. In this chapter, the compact models and parameter extraction methods of a-Si:H TFT for both static and dynamic characterises are discussed. Then, the improvements and innovations made on a-Si:H TFT models and parameter extraction methods are presented.

2.1 Background

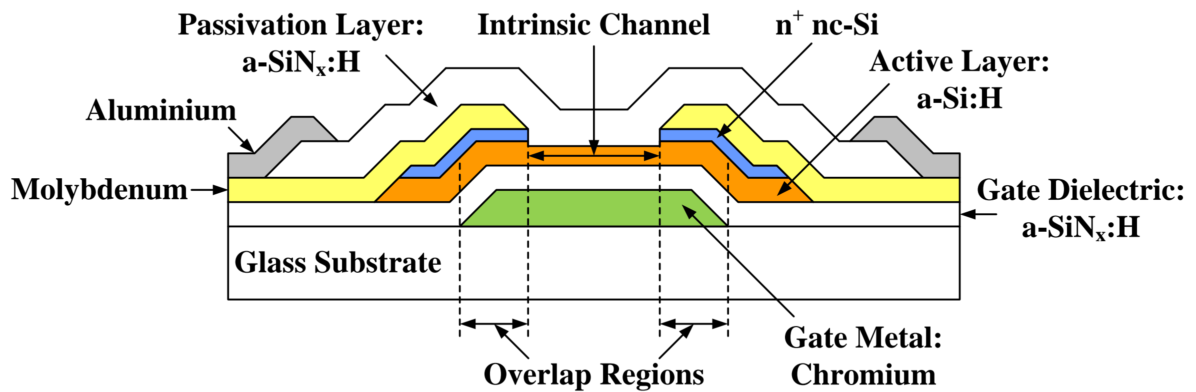
2.1.1 Device Structure

Hydrogenated amorphous Silicon (a-Si:H) TFT consists of several layers: gate metal, gate dielectric, active layer (a-Si:H), and n^+ contact and metal at source and drain. The material of gate dielectric is typically Hydrogenated amorphous Silicon Nitride (a-SiN$_x$:H).

In terms of structure, TFTs can be divided into a few types [11]. In a staggered TFT, gate terminal and drain/source terminals are on the different sides of active layer, while in a coplanar TFT, they are on the same side of active layer. The gate of an inverted (*i.e.*, bottom-gated) TFT is between substrate and active layer, while the gate of a non-inverted (*i.e.*, top-gated) TFT is on top of active layer. Inverted-staggered TFT is the most popular type used in flat-panel displays [11].



(a)



(b)

Figure 2.1: Inverted staggered BCE a-Si:H TFT: (a) layout; (b) cross-section.

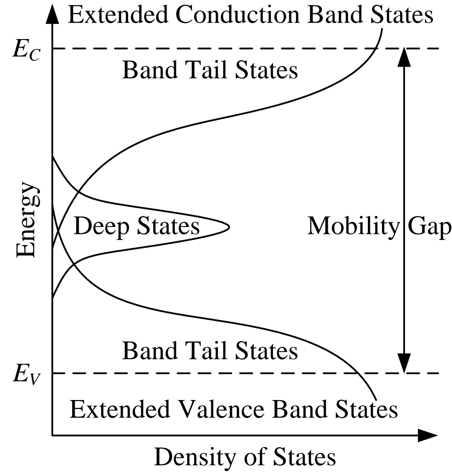
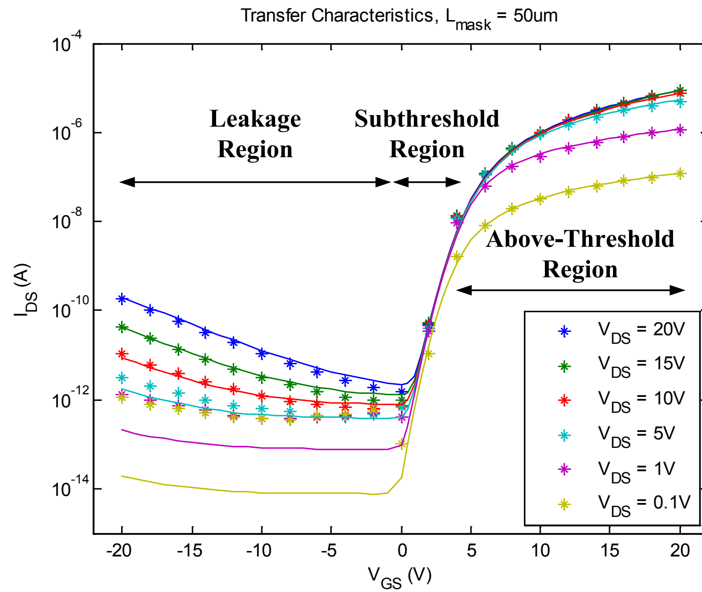


Figure 2.2: Density of states in a-Si:H material. E_C and E_V are the edges of conduction band and valence band, respectively.

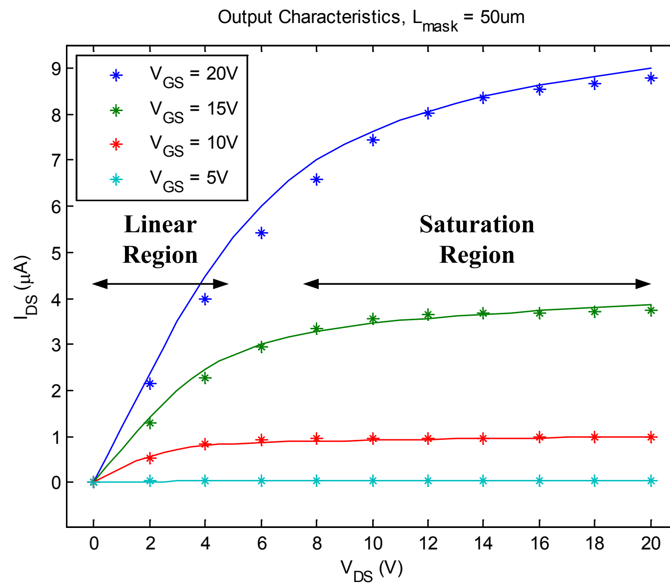
Inverted staggered TFTs can be further divided into two types: back-channel etched (BCE) type and back-channel passivated (BCP) type [12]. The difference between them is that a back-channel passivation layer is used in BCP type to cover a-Si:H layer before the deposition of source/drain n^+ contact and metal. In BCE type, because of the lack of the protection of passivation layer on top of a-Si:H layer, a-Si:H layer is subject to damage during processing [13]. However, BCE type is popular in LCD industry because it requires fewer masks and processing steps [14]. For illustration, the layout and cross-section of inverted staggered BCE a-Si:H TFT are shown in Figure 2.1. More details about the samples of a-Si:H TFT used in this research are described in section 2.3.2.

2.1.2 Device Operation

The behaviors and characteristics of a-Si:H TFT are fundamentally dependent on the distribution of density of states in the energy band diagram of a-Si:H material, which is illustrated in Figure 2.2 [13,15]. Because of the long-range disorder atomic lattice in a-Si:H material, band tail states extend from the edges of conduction band and valence band into forbidden band [13, 16]. This is significantly different from crystalline silicon. Besides, the dangling bonds in a-Si:H induce localized deep states around the center of forbidden band [13,16]. The high density of states in the band gap of a-Si:H results in high trapping rate of carriers, and therefore low carrier mobility.



(a)



(b)

Figure 2.3: Measurement data (symbols) and simulation results (curves) of typical I-V characteristics of n-channel a-Si:H TFT. $W/L = 500\ \mu\text{m}\ /\ 50\ \mu\text{m}$. (a) Transfer characteristics. (b) Output characteristics.

A n-channel a-Si:H TFT has three operation regions: above-threshold region, subthreshold region, and leakage region, as illustrated in Figure 2.3. Above-threshold region is divided into linear region and saturation region [13]. Subthreshold region can be divided into forward subthreshold region and reverse subthreshold region [17]. The operations of n-channel a-Si:H TFT in different regions are briefly described as follows [13, 17].

When gate voltage is negative and high, a-Si:H TFT is in leakage region. Fermi level is far away from the edge of conduction band. The equivalent diode formed by the n^+ contact layer and intrinsic a-Si:H layer in gate-to-drain overlap region is reversely biased and thus blocks drain-to-source current (I_{DS}). Therefore, leakage I_{DS} is limited at low levels. It is attributed to the hole conduction at front a-Si:H/a-SiN$_x$:H interface (*i.e.*, the interface closer to gate), and increases exponentially when V_{GS} is negatively increased. It is mainly controlled by Pool-Frenkel mechanism in gate-to-drain overlap region.

When gate voltage is positively increased, Fermi level is closer to the edge of conduction band. A-Si:H TFT enters subthreshold region when gate voltage begins to induce charge at front a-Si:H/a-SiN$_x$:H interface. In a crystalline-silicon MOSFET, almost the entire induced charge is available (*i.e.*, free) for current conduction. However, in a-Si:H TFT, a major part of induced charge is trapped in localized states, so the current conduction of a-Si:H is much weaker than that of crystalline-silicon MOSFET.

When gate voltage is further positively increased, Fermi level enters the tail states of conduction band, and the induced charge is in conduction band states and tail states. At this point, a-Si:H TFT enters above-threshold region. For a typical a-Si:H TFT applied with a gate voltage in a typical range, Fermi level cannot enter conduction band because of the high density of tail states. Comparing to crystalline-silicon MOSFET, the turn-ON transition of a-Si:H TFT is much more gradual, because carrier movement is limited by the trapping of localized states and the scattering of disorder lattice. As a result, the band mobility of a-Si:H is lower than that of crystalline silicon by orders of magnitude.

Besides, in above-threshold region, I_{DS} increases proportionally with V_{DS} until V_{DS} is comparable to V_{GS}. At this point, channel pinches off on drain side. Further increasing V_{DS} makes a-Si:H TFT enter saturation region, as illustrated in Figure 2.3.

2.2 Review of Static Models

2.2.1 Linear Region

The I-V characteristics of a-Si:H TFT in above-threshold region are illustrated in Figure 2.3. The device model of a-Si:H TFT in above-threshold region can be derived in a way similar to the models of crystalline-silicon MOSFET. However, a-Si:H TFT also has several important differences from crystalline-silicon MOSFET, reviewed as follows [13, 17].

The channel material of an enhancement-mode n-channel crystalline-silicon MOSFET is p-type. When an above-threshold gate voltage is applied, minority carriers accumulate and eventually inverse the type of the channel region near the interface of gate dielectric and channel region, so a conductive channel is formed. In contrast, the active layer of n-channel a-Si:H TFT is intrinsic. When a positive gate voltage is applied, electrons are attracted from n^+ nc-Si contacts. They transport through intrinsic a-Si:H layer and accumulate at the interface of gate dielectric and active layer, so that a channel is formed in active layer near the interface. Therefore, unlike crystalline-silicon MOSFET, there is no depletion charge in a-Si:H TFT [13]. When a-Si:H TFT operates in above-threshold region, a major part of total induced charge is trapped in localized states. Therefore, only a fraction of total induced charge is free charge, which contributes to current conduction. The total induced charge per unit area (*i.e.*, sheet density of total induced charge) in the active layer of a-Si:H TFT is $qn_{ind} = qn_{sa} + qn_{loc}$, where qn_{sa} is the sheet density of free charge, and qn_{loc} is the sheet density of the charge trapped in localized states [13]. Fermi level shifts with gate voltage, so does the occupancy of localized states. Therefore, qn_{loc} and qn_{sa} are strongly dependent on gate voltage.

Classical square-law above-threshold I_{DS} model of crystalline-silicon MOSFET is

$$I_{DS} = \mu_{FET}\,\frac{W}{L}\,C_i\left[(V_{GS} - V_T)\,V_{DS} - \frac{V_{DS}^2}{2}\right], \tag{2.1}$$

where μ_{FET} is field effective mobility, W is channel width, L is channel length, C_i is gate dielectric capacitance per unit area, V_{GS} is gate-to-source voltage, V_{DS} is drain-to-source voltage, and V_T is threshold voltage. For a low V_{DS}, MOSFET is in linear region, so Eq. (2.1) can be approximated as

$$I_{DS} = \mu_{FET}\,\frac{W}{L}\,C_i\,(V_{GS} - V_T)\,V_{DS}. \tag{2.2}$$

The sheet density of the total charge induced by gate voltage is

$$qn_{ind} = C_i\,(V_{GS} - V_T)\,, \tag{2.3}$$

so the formula of I_{DS} in linear region becomes

$$I_{DS} = \mu_{FET} \, \frac{W}{L} \, qn_{ind} V_{DS}. \tag{2.4}$$

Since these formulas are for crystalline-silicon MOSFET, the μ_{FET} used above is constant.

A widely used a-Si:H TFT model is RPI model [13]. In this model, the impact of the charge trapping at localized states on I_{DS} is described by empirically modeling field effect mobility as a function of gate voltage:

$$\mu_{FET} = \mu_n \left(\frac{n_{sa}}{n_{ind}} \right) = \mu_n \left(\frac{V_{GS} - V_T}{V_{AA}} \right)^{\gamma}, \tag{2.5}$$

where γ and V_{AA} are empirical parameters [13]. Therefore, Eq. (2.2) becomes

$$I_{DS} = C_i \frac{W}{L} \mu_n \left(\frac{V_{GS} - V_T}{V_{AA}} \right)^{\gamma} (V_{GS} - V_T) \, V_{DS}, \tag{2.6}$$

which is the I_{DS} model of a-Si:H TFT in linear region.

2.2.2 Saturation Region

In crystalline-silicon MOSFET, if V_{GD} is not high enough to induce strong inversion on drain side (*i.e.*, when $V_{DS} \geqslant V_{GS} - V_T$), channel pinches off on drain side, and no free charge exists in the part of channel between pinch-off point and drain. Since crystalline-silicon MOSFET has velocity saturation mechanism in the high-field region near drain, it actually enters saturation region at a V_{DS} which is lower than $(V_{GS} - V_T)$.

The V_{DS} at which a-Si:H TFT enters saturation region is also lower than $(V_{GS} - V_T)$. However, this is caused by the gradual distribution of the density of states in the energy band diagram of a-Si:H, instead of velocity saturation [13]. The μ_{FET} on drain side can be estimated by using Eq. (2.5) with V_{GS} being replaced by V_{GD}. When drain voltage is increased toward $(V_{GS} - V_T)$, V_{GD} decreases toward V_T, and μ_{FET} on drain side becomes negligible well before V_{GD} achieves V_T. This is because, when V_{GD} is decreased, qn_{sa} reduces much faster than qn_{ind} [13]. Therefore, a-Si:H TFT enters saturation region at a V_{DS} which is lower than $(V_{GS} - V_T)$. The author of [13] uses an universal approach introduced from the modeling of crystalline-silicon MOSFET [18] to model the behavior of a-Si:H TFT in saturation region. In this approach, saturation voltage V_{sat} is defined as

$$V_{sat} = \alpha_{sat} \, (V_{GS} - V_T) \, , \tag{2.7}$$

where $\alpha_{sat} \in (0, 1)$. Besides, in saturation region, when V_{DS} is increased, the pinch-off point in channel moves toward source, so effective channel length reduces. This is well known as channel length modulation (CLM) effect, which can be modeled by adding term $(1 + \lambda V_{DS})$ into the expression of I_{DS} in saturation region [13]. Therefore, the I_{DS} in saturation region can be expressed as

$$I_{DS} = C_i \frac{W}{L} \mu_n \left(\frac{V_{GS} - V_T}{V_{AA}} \right)^{\gamma} (V_{GS} - V_T) V_{sat} (1 + \lambda V_{DS}) \tag{2.8}$$

$$= C_i \frac{W}{L} \mu_n \left(\frac{V_{GS} - V_T}{V_{AA}} \right)^{\gamma} (V_{GS} - V_T)^2 \alpha_{sat} (1 + \lambda V_{DS}) . \tag{2.9}$$

In the model file of a-Si:H TFT to be used for circuit simulation, the V_{sat} in Eq. (2.8) should be replace by V_{DS}^{eff}, which is an effective voltage defined to provide a continuous and smooth transition between linear region and saturation region:

$$V_{DS}^{eff} = \frac{V_{DS}}{\left[1 + \left(\frac{V_{DS}}{V_{sat}} \right)^{m_{sat}} \right]^{\frac{1}{m_{sat}}}}, \tag{2.10}$$

where m_{sat} is smoothness parameter [13]. In linear region, $V_{DS} \ll V_{sat}$, so $V_{DS}^{eff} \approx V_{DS}$. In saturation region, $V_{DS} \gg V_{sat}$, so $V_{DS}^{eff} \approx V_{sat}$.

2.2.3 Subthreshold Region

In subthreshold region, Fermi level is in deep localized states, being far away from the edge of conduction band. Almost the entire charge induced by gate voltage is trapped in deep states, so Fermi level position depends on the density of deep states. By analyzing Fermi level position as a function of gate voltage and the density of deep states, the sheet density of free charge can be modeled as a power-law function of gate voltage [13]:

$$n_{sb} = n_{so} \left[\left(\frac{t_m}{d_i} \right) \left(\frac{V_{GS} - V_{FB}}{V_0} \right) \left(\frac{\varepsilon_i}{\varepsilon_s} \right) \right]^{\frac{2V_0}{V_e}} , \tag{2.11}$$

where

$$V_e = \frac{2V_0 V_{th}}{2V_0 - V_{th}}, \tag{2.12}$$

t_m is the thickness of the channel charge at the interface:

$$t_m = \sqrt{\frac{\varepsilon_s \varepsilon_0}{2qg_0}}, \tag{2.13}$$

and n_{so} is the sheet density of free charge when $V_{GS} = V_{FB}$:

$$n_{so} = N_C t_m \left(\frac{V_e}{V_0}\right) \exp\left(\frac{-dE_{F0}}{qV_{th}}\right). \tag{2.14}$$

2.2.4 Leakage Region

In leakage region, three components contribute to leakage current [13]: hole-injection-limited current, hole-conduction current, and electron-limited current. Total leakage current can be any combination of these current components, so it is difficult to build a precise model [13]. Therefore, an empirical model is used to describe leakage current:

$$I_{leak} = I_{0L}\left[\exp\left(\frac{V_{DS}}{V_{DSL}}\right) - 1\right] \exp\left(\frac{-V_{GS}}{V_{GSL}}\right) + \sigma_0 V_{DS}, \tag{2.15}$$

where I_{0L} is zero-bias leakage current, V_{DSL} and V_{GSL} are characteristic voltages, and σ_0 is minimum-current scaling parameter to take into account the minimum resolution of measurement instrument [13]. Note that, in [13], I_{0L} and σ_0 are defined as independent from TFT geometry. However, it is presented in [17] that for relatively high $V_{GS} < 0$ V and $V_{DS} > 0$ V, leakage current is proportional to the area of the contact overlap region on drain side. Therefore, in this thesis, I_{0L}^u and σ_0^u are introduced respectively as the values of I_{0L} and σ_0 per unit area of the contact overlap region on drain side. Correspondingly, the model of leakage current is modified in this thesis as

$$I_{leak} = WL_{ov,D}\left\{I_{0L}^u\left[\exp\left(\frac{V_{DS}}{V_{DSL}}\right) - 1\right] \exp\left(\frac{-V_{GS}}{V_{GSL}}\right) + \sigma_0^u V_{DS}\right\}, \tag{2.16}$$

where $L_{ov,D}$ is the overlap length on drain side.

2.2.5 Model Unification

To improve the convergence of circuit simulation, model formulas should be continuous and smooth. A universal approach is used in [13] to unify the models of a-Si:H TFT in different operation regions. The sheet density of free charge is defined as:

$$n_s = \frac{n_{sa} n_{sb}}{n_{sa} + n_{sb}}, \tag{2.17}$$

which reduces to n_{sa} in above-threshold region and to n_{sb} in subthreshold region, providing a smooth transition between regions. The formula of n_{sb} is presented in Eq. (2.11). The formula of n_{sa} can be derived from Eq. (2.3) and (2.5) as

$$n_{sa} = \frac{C_i\left(V_{GS} - V_T\right)}{q}\left(\frac{V_{GS} - V_T}{V_{AA}}\right)^{\gamma}. \tag{2.18}$$

The channel conductance when $V_{GS} = V_{GD}$ is defined as

$$g_{ch} = q\ n_s\ \mu_n\ W/L_{eff}^{IV}, \tag{2.19}$$

where $L_{eff}^{IV} = L_{mask} + \Delta L_S + \Delta L_D$ is effective channel length, taking into account the channel length defined on mask layout L_{mask} and the channel length extension on source (drain) side $\Delta L_{S(D)}$. The formula of drain-to-source current to unify the currents in above-threshold region and subthreshold region is defined as

$$I_{ab} = g_{ch} V_{DS}^{eff}\left(1 + \lambda V_{DS}\right), \tag{2.20}$$

where V_{DS}^{eff} is defined in Eq. (2.10). To incorporate the drain-to-source current in leakage region, an unified formula of drain-to-source current for all regions is defined as

$$I_{DS} = I_{leak} + I_{ab}. \tag{2.21}$$

In either above-threshold region or subthreshold region, $I_{ab} \gg I_{leak}$, so $I_{DS} \approx I_{ab}$. In leakage region, $I_{ab} \ll I_{leak}$, so $I_{DS} \approx I_{leak}$.

Besides, note that if V_{GS} is low or negative, $V_{GS,T} = (V_{GS} - V_T)$ and $V_{GS,FB} = (V_{GS} - V_{FB})$ can be negative, invalidating the relevant formulas presented above. To avoid this problem, effective voltages

$$V_{GS,T}^{eff} = \frac{V_{min}}{2}\left\{1 + \frac{V_{GS,T}}{V_{min}} + \left[\delta^2 + \left(\frac{V_{GS,T}}{V_{min}} - 1\right)^2\right]^{\frac{1}{2}}\right\} \tag{2.22}$$

and

$$V_{GS,FB}^{eff} = \frac{V_{min}}{2}\left\{1 + \frac{V_{GS,FB}}{V_{min}} + \left[\delta^2 + \left(\frac{V_{GS,FB}}{V_{min}} - 1\right)^2\right]^{\frac{1}{2}}\right\} \tag{2.23}$$

are defined in [13] to replace $(V_{GS} - V_T)$ and $(V_{GS} - V_{FB})$, respectively, in relevant aforementioned formulas. V_{min} is minimum effective voltage, and δ is smoothness parameter.

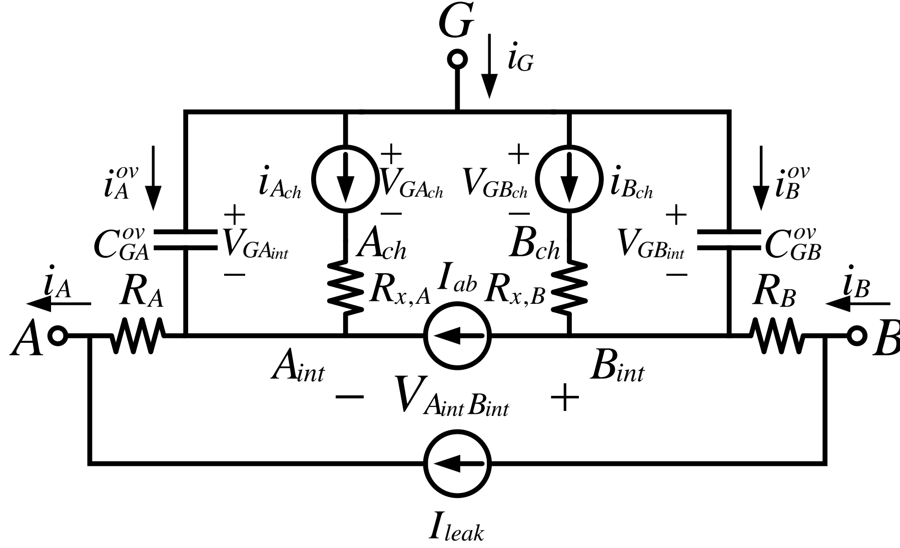


Figure 2.4: Compact device model of a-Si:H TFT. A and B can be either source (S) or drain (D), respectively, depending on specific bias condition.

The schematic of the entire compact device model of a-Si:H TFT is presented in Figure 2.4, illustrating the implementation of I_{ab} and I_{leak}. Other components used in the model are explained as follows. Note that A and B can be either source (S) or drain (D), respectively, depending on specific bias condition. Current sources $i_{A_{ch}}$ and $i_{B_{ch}}$ describe transient currents when channel is being charged/discharged. C_{GA}^{ov} and C_{GB}^{ov} represent overlap capacitances. Access resistors $R_{x,A}$ and $R_{x,B}$ model the delays caused by channel resistance. R_A and R_B represent contact resistances.

Define $V_{GS_{int}}$ as the voltage differences between gate (G) and internal source node (S_{int}), and $V_{D_{int}S_{int}}$ as the voltage differences between internal drain node (D_{int}) and source node (S_{int}). Since I_{ab} belongs to intrinsic channel, which is directly controlled by $V_{GS_{int}}$ and $V_{D_{int}S_{int}}$, $V_{GS_{int}}$ and $V_{D_{int}S_{int}}$ should be used to replace V_{GS} and V_{DS}, respectively, in relevant aforementioned formulas when implementing the device model into a model file (*e.g.*, by using Verilog-A Hardware Description Language) for circuit simulation.

2.3 Improved Static Model and Parameter Extraction Methods

2.3.1 Motivations

Compact device models and parameter extraction methods are needed by device characterization and circuit simulation. A desirable compact device model should be accurate in describing device behavior and scalable with device geometry (*i.e.*, correctly describe the dependence of device characteristics on channel width and length by using the same group of parameters values). A desirable parameter extraction method should yield accurate and consistent parameter values.

RPI compact device model of a-Si:H TFT [13] is widely used. Several parameter extraction methods were developed for this model [13, 19, 20]. The dependence of contact resistance and channel length extension on gate voltage is not taken into account in them. As a result, the extracted values of γ, V_T, and V_{AA} have apparent dependence on channel length. However, from the perspective of device physics, these parameters describe the property of a-Si:H material, so their values should be independent from channel length. The incorrect apparent dependence of the extracted values of parameters on channel length is misleading for the characterization a-Si:H TFT. Therefore, the dependence of contact resistance and channel length extension on gate voltage must be taken into account in the model and parameter extraction methods of a-Si:H TFT. An improved static model and innovated parameter extraction methods are presented in this section.

2.3.2 TFT Samples and Measurement Setup

The inverted staggered BCE a-Si:H TFT samples used in this research were fabricated in Giga-to-Nanoelectronics (G2N) Centre in the University of Waterloo. Depositing and patterning material layers on a glass substrate were carried sequentially: gate metal (70 nm chromium), gate dielectric (350 nm a-SiN$_x$:H), active layer (150 nm a-Si:H), and source and drain contacts (50 nm n$^+$ nc-Si and 100 nm molybdenum). After patterning source and drain metal, back channel etching was used to remove the n$^+$ nc-Si on top of active layer in intrinsic channel region. Then, passivation layer (350 nm a-SiN$_x$:H), contact window opening, contact metal (300 nm aluminium) deposition/pattering were conducted.

For illustration, the layout and cross-section of inverted staggered BCE a-Si:H TFT are shown in Figure 2.1. Nominal channel width is $W = 500$ μm. The nominal channel

lengthes defined on mask are $L_{mask} = 100$, 50, 20, 10, and 5 μm. The nominal overlap length between gate and source (drain) is $L_{ov,S(D)} = 5$ μm. Transfer and output characteristics were measured from a-Si:H TFT samples by using Agilent® 4155C Semiconductor Parameter Analyzer and a Cascade® Summit® 12000 probe station. Measurements were carried at room temperature (23 °C).

2.3.3 Contact Resistance and Channel Length Extension

The total resistance between source and drain is the sum of three components: intrinsic channel resistance (R_{ch}), contact resistance at source (R_S), and the one at drain (R_D):

$$R_{DS} = R_{ch} + R_S + R_D. \tag{2.24}$$

To simplify parameter extraction, a low V_{DS} (*e.g.*, 0.1 V) can be used in *I*-*V* measurements so that the source side of a TFT sample is approximately symmetrical to its drain side. In this case, since $R_S \approx R_D$, Eq. (2.24) yields

$$R_{DS} \approx R_{ch} + 2R_S. \tag{2.25}$$

The values of R_{DS} can be obtained from measurement data by using formula $R_{DS} = V_{DS}/I_{DS}$. Total contact resistance ($R_S + R_D \approx 2R_S$) can be extracted by plotting R_{DS} *vs.* L_{mask}, as shown in Figure 2.5(a)). Assuming $R_{ch} = r_{ch} \cdot L_{mask}$, where r_{ch} is intrinsic channel resistance per unit channel length, Eq. (2.25) becomes

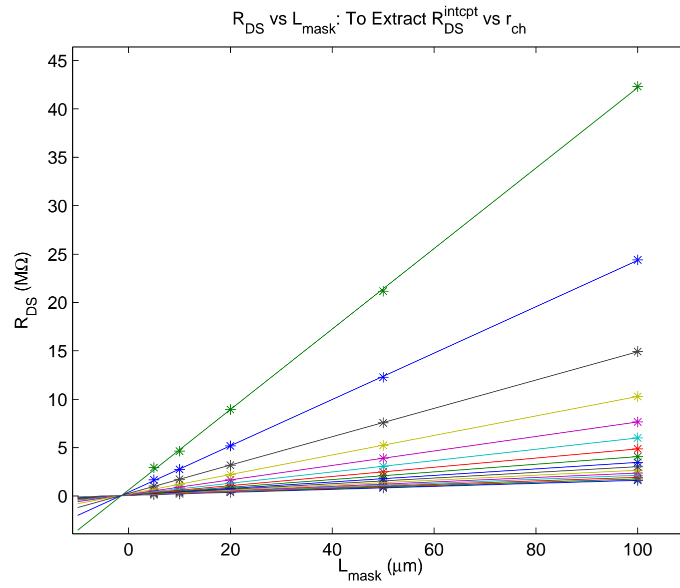
$$R_{DS} = r_{ch} \cdot L_{mask} + 2R_S. \tag{2.26}$$

If R_S is assumed as a constant, the lines of R_{DS} *vs.* L_{mask} for different V_{GS} should intersect at the same point: $(L_{mask}, R_{DS}) = (0, 2R_S)$. However, Figure 2.5(b) indicates that this is not the case, implying that R_S is dependent on V_{GS} and/or that a V_{GS}-dependent total channel length extension ΔL_{tot}^{IV} should be added to L_{mask}. The superscript "IV" in a item indicates that the item is associated to *I*-*V* characteristics and is used in static model. Therefore, Eq. (2.26) is modified as

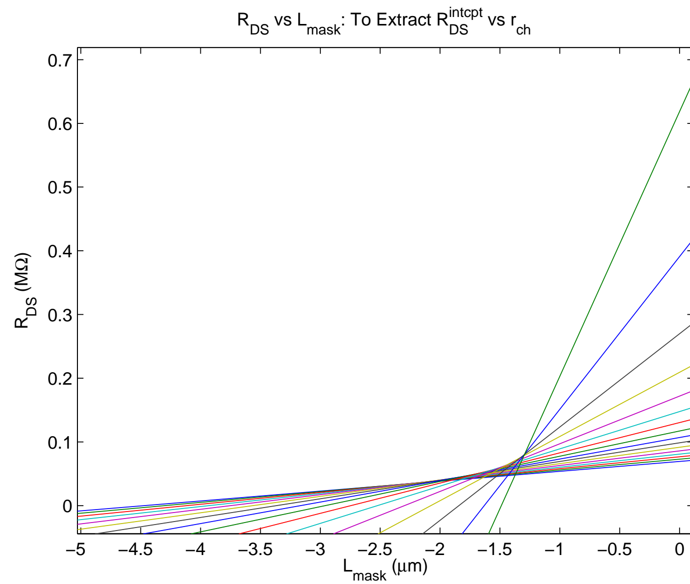
$$R_{DS} = r_{ch} \cdot \left(L_{mask} + \Delta L_{tot}^{IV}\right) + 2R_S. \tag{2.27}$$

At $L_{mask} = 0$, a line of R_{DS} *vs.* L_{mask} intercepts R_{DS}-axis, so

$$R_{DS}^{intcpt} = r_{ch} \cdot \Delta L_{tot}^{IV} + 2R_S. \tag{2.28}$$



(a)



(b)

Figure 2.5: Measurement results (symbols) and fitted model (lines) of (a) R_{DS} *vs.* L_{mask} (bottom to top: V_{GS} = 20, 19, ..., 5 V) and (b) the zoom-in plot of (a).

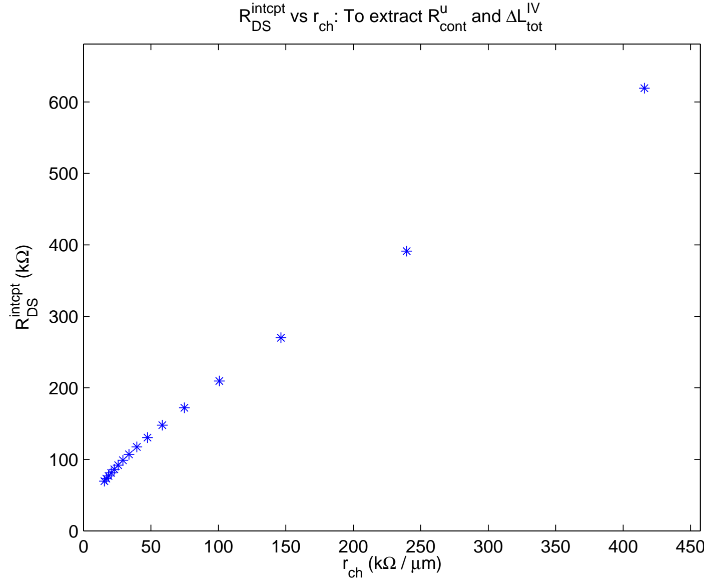
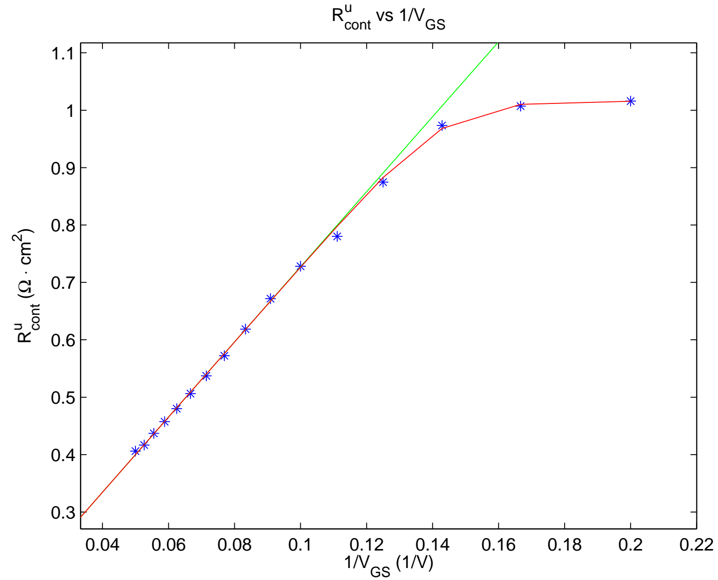


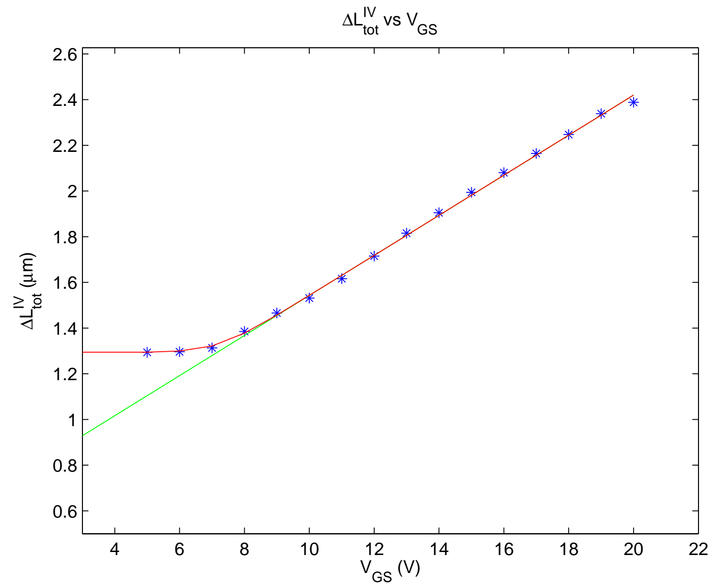
Figure 2.6: Extracted values of R_{DS}^{intcpt} *vs.* r_{ch}. Data points (left to right) are corresponding to V_{GS} = 20, 19, ..., 5 V.

For a given V_{GS}, the data of R_{DS}^{intcpt} and r_{ch} can be extracted by fitting Eq. (2.27) to measurement data, as illustrated in Figure 2.5(a). The extracted data of R_{DS}^{intcpt} *vs.* r_{ch} is shown in Figure 2.6. Note that the data points in Figure 2.6 are corresponding to the values of V_{GS} used in Figure 2.5. Figure 2.6 indicates that the slope of R_{DS}^{intcpt} *vs.* r_{ch} is not constant. Therefore, in this research, Eq. (2.28) was fitted locally to the data points around each data point in Figure 2.6 to extract the local values of r_{ch} and $2R_S$. The data of the contact resistance per unit overlap area R_{cont}^{u} was calculated by using $R_{cont}^{u} = R_S W L_{ov}$.

The extracted values of R_{cont}^{u} and ΔL_{tot}^{IV} *vs.* V_{GS} are presented in Figure 2.7(a) and 2.7(b), respectively. The dependence of R_{cont}^{u} and ΔL_{tot}^{IV} on V_{GS} can be explained by investigating the two-dimensional current distribution in overlap region [21, 22]. The overlap region on source side is analyzed as follows. The one on drain side can be analyzed in the same way. In the overlap region on source side, currents flow distributively from the edge of intrinsic channel to source metal contact. The currents flowing along parasitic channel are lower at locations farther away from the edge of intrinsic channel. When gate voltage is increased, parasitic channel has a lower resistivity, so currents flow along parasitic channel for longer distances before they turn vertically and flow toward source metal contact. Therefore, ΔL_{tot}^{IV} increases with gate voltage. Since a larger area of overlap region con-



(a)



(b)

Figure 2.7: Measurement results (symbols) and fitted models (lines and curves) of (a) R^u_{cont} *vs.* $1/V_{GS}$ and (b) ΔL^{IV}_{tot} *vs.* V_{GS}.

tributes to current conduction, the total resistance from parasitic channel to source metal contact is smaller. Therefore, R_S reduces when V_{GS} is increased, so does R^u_{cont}.

Besides, Figure 2.7(a) and 2.7(b) also indicate that when V_{GS} is decreased, R^u_{cont} and ΔL^{IV}_{tot} eventually become relatively constant. This is because, when V_{GS} is decreased, the resistivity of parasitic channel can become so large that the major part of total current does not go along parasitic channel in overlap region, but goes from the edge of intrinsic channel directly though intrinsic a-Si:H layer toward source metal contact. Therefore, the observed R^u_{cont} and ΔL^{IV}_{tot} are relatively independent from gate voltage. The constant level of ΔL^{IV}_{tot} is attributed to the fixed channel length extension due to the lateral etching of n^+ nc-Si layer and contact metal layer during fabrication.

As shown in Figure 2.7(a), when V_{GS} is relatively high, R^u_{cont} is observed as approximately linearly dependent on $1/V_{GS}$, so a linear model is used to describe the relationship:

$$R^{u,linear}_{cont} = S_{R^u_{cont}}/V^{R^u_{cont}}_{GS,eff} + R^{u,intcpt}_{cont}, \tag{2.29}$$

where $S_{R^u_{cont}}$ and $R^{u,intcpt}_{cont}$ are slope and intercept, respectively. $V^{R^u_{cont}}_{GS,eff}$ is so defined that it prevents a negative value of V_{GS} from invalidating Eq. (2.29):

$$V^{R^u_{cont}}_{GS,eff} = F^{R^u_{cont}}_{V_{GS,eff}} \ln\left[1 + \exp\left(\frac{V_{GS}}{F^{R^u_{cont}}_{V_{GS,eff}}}\right)\right], \tag{2.30}$$

where $F^{R^u_{cont}}_{V_{GS,eff}}$ is smoothness parameter. If $V_{GS} > 0$ V, $V^{R^u_{cont}}_{GS,eff} \approx V_{GS}$. If $V_{GS} < 0$ V, $V^{R^u_{cont}}_{GS,eff} \to 0^+$. The model in Eq. (2.29) was fitted as the straight line shown in Figure 2.7(a). The extracted values of parameters are $S_{R^u_{cont}} = 6.54$ V·Ω·cm^2, $R^{u,intcpt}_{cont} = 0.073$ Ω·cm^2, and $F^{R^u_{cont}}_{V_{GS,eff}} = 1$ V. Figure 2.7(a) also indicates that, when V_{GS} is decreased toward V_T, R^u_{cont} gradually saturates at a constant level $R^{u,const}_{cont}$, so the following formula is used to make a smooth transition between $R^{u,linear}_{cont}$ and $R^{u,const}_{cont}$:

$$R^u_{cont} = R^{u,const}_{cont} - F_{R^u_{cont}} \ln\left\{1 + \exp\left[\frac{-\left(R^{u,linear}_{cont} - R^{u,const}_{cont}\right)}{F_{R^u_{cont}}}\right]\right\}, \tag{2.31}$$

where $F_{R^u_{cont}}$ is smoothness parameter. If $R^{u,linear}_{cont} < R^{u,const}_{cont}$, $R^u_{cont} \approx R^{u,linear}_{cont}$. If $R^{u,linear}_{cont} > R^{u,const}_{cont}$, $R^u_{cont} \approx R^{u,const}_{cont}$. Eq. (2.31) is fitted as the curve in Figure 2.7(a). The extracted values of parameters are $F_{R^u_{cont}} = 0.0625$ Ω·cm^2 and $R^{u,const}_{cont} = 1.02$ Ω·cm^2.

As shown in Figure 2.7(b), when V_{GS} is relatively high, ΔL_{tot}^{IV} is observed as approximately linearly dependent on V_{GS}, so a linear model is used to describe the dependence of the variable component of ΔL_{tot}^{IV} on V_{GS}:

$$\Delta L_{var}^{IV,linear} = S_{\Delta L}^{IV} \cdot V_{GS} + \Delta L_{var}^{IV,intcpt}, \tag{2.32}$$

where $S_{\Delta L}^{IV}$ and $\Delta L_{var}^{IV,intcpt}$ are slope and intercept, respectively. Eq. (2.32) is fitted as the straight line shown in Figure 2.7(b) to extract parameter values: $S_{\Delta L}^{IV} = 0.0877$ μm/V, $\Delta L_{var}^{IV,intcpt} = 0.67$ μm. Figure 2.7(b) also indicates that, when V_{GS} is decreased, ΔL_{tot}^{IV} eventually saturates at a constant level ΔL_{const}^{IV}, so ΔL_{tot}^{IV} is expressed as

$$\Delta L_{tot}^{IV} = \Delta L_{const}^{IV} + \Delta L_{var}^{IV}, \tag{2.33}$$

where

$$\Delta L_{var}^{IV} = F_{\Delta L}^{IV} \ \ln \left[1 + \exp \left(\frac{\Delta L_{var}^{IV,linear} - \Delta L_{const}^{IV}}{F_{\Delta L}^{IV}} \right) \right]. \tag{2.34}$$

$F_{\Delta L}^{IV}$ is smoothness parameter. If $\Delta L_{var}^{IV,linear} > \Delta L_{const}^{IV}$, $\Delta L_{tot}^{IV} \approx \Delta L_{var}^{IV,linear}$. If $\Delta L_{var}^{IV,linear} < \Delta L_{const}^{IV}$, $\Delta L_{tot}^{IV} \approx \Delta L_{const}^{IV}$. The fitted model is shown as the curve in Figure 2.7(b). The extracted values of parameters are $F_{\Delta L}^{IV} = 0.05$ μm and $\Delta L_{const}^{IV} = 1.29$ μm.

Note that the above analysis is based on assumption $V_{GS} \approx V_{GD}$. For a high V_{DS}, since $V_{GS} \neq V_{GD}$, the value of the R_{cont}^{u} on source (drain) side (denoted as $R_{cont,S(D)}^{u}$) is calculated by using $V_{GS(D)}$ in Eq. (2.29)-(2.31). Besides, the value of the variable component of the channel length extension on source (drain) side (denoted as $\Delta L_{S(D),var}^{IV}$) is calculated as

$$\Delta L_{S(D),var}^{IV} = \frac{1}{2} \Delta L_{var}^{IV} \left(V_{GS(D)} \right), \tag{2.35}$$

where $\Delta L_{var}^{IV} \left(V_{GS(D)} \right)$ is the value of ΔL_{var}^{IV} calculated by using Eq. (2.34) when $V_{GS(D)}$ is used in Eq. (2.32). Therefore, Eq. (2.33) becomes

$$\Delta L_{tot}^{IV} = \Delta L_{const}^{IV} + \Delta L_{S,var}^{IV} + \Delta L_{D,var}^{IV}, \tag{2.36}$$

which was implemented in the Verilog-A model file of a-Si:H TFT.

2.3.4 γ, V_T, and V_{AA}

Taking into account contact resistance and channel length extension, Eq. (2.6) becomes

$$I_{DS} = C_i \frac{W}{(L_{mask} + \Delta L_{tot}^{IV})} \mu_n \frac{(V_{GS} - V_T - I_{DS} R_S)^{\gamma+1}}{V_{AA}^{\gamma}} (V_{DS} - 2 I_{DS} R_S). \tag{2.37}$$

The author of [13] extracted $(\gamma+1)$ simply as the slope of $\ln(I_{DS})$ *vs.* $\ln(V_{GS})$, without taking into account $(I_{DS}R_S)$, ΔL_{tot}^{IV}, and V_T. $(I_{DS}R_S)$ is the voltage drop across the contact region on one side of TFT when $V_{GS} \approx V_{GD}$. Neglecting $(I_{DS}R_S)$ and ΔL_{tot}^{IV} results in that the extracted value of γ decreases with L_{mask}. Besides, since typically $V_T > 0$ V, neglecting V_T results in that the extracted value of γ is larger than its true value. Since the extraction of V_{AA} uses the extracted value of γ, the extracted value of V_{AA} is also dependent on L_{mask}. However, γ and V_{AA} should be independent from L_{mask}, because they are material property parameters of a-Si:H, reflecting the impact of charge trapping in a-Si:H on current conduction (see Eq. (2.5)). Besides, since the extractions of V_T and α_{sat} in [13] use the extracted values of γ and V_{AA}, the errors of the extracted values of γ and V_{AA} cause the errors of the extracted values of V_T and α_{sat}. To avoid these problems, $(I_{DS}R_S)$, ΔL_{tot}^{IV}, and V_T must be taken into account during the extraction of γ so as to improve the accuracy and consistency of the extracted values of parameters.

Integral function method for parameter extraction was proposed by previous researchers in [19, 20]. In this method, R_S is taken into account, and γ and V_T are extracted at the same time. However, this method implicitly assumes that ΔL_{tot}^{IV} is zero, and that R_S is independent from V_{GS}. These two assumptions are not true (refer to section 2.3.3). Besides, this method requires the extraction of transconductance g_m. However, the numerical differentiation used to extract g_m amplifies measurement noise.

Therefore, in this thesis, a new parameter extraction method is proposed to take into account the impact of ΔL_{tot}^{IV} and $(I_{DS}R_S)$, which are dependent on V_{GS}. The value of γ is extracted first, then V_T and V_{AA} are extracted. When extracting γ, although V_T and V_{AA} are unknown, they do not affect the extraction of γ. The proposed parameter extraction method is detailed as follows. First, Eq. (2.37) is reformulated as

$$C^{\frac{1}{\gamma+1}} = A \cdot V_{GS_{init}} - B, \tag{2.38}$$

where

$$A = \left(C_i W \mu_n / V_{AA}^{\gamma}\right)^{\frac{1}{\gamma+1}}, \tag{2.39}$$
$$B = A \cdot V_T, \tag{2.40}$$
$$C = I_{DS}\left(L_{mask} + \Delta L_{tot}^{IV}\right) / V_{D_{int}S_{int}}, \tag{2.41}$$
$$V_{GS_{int}} = V_{GS} - I_{DS}R_S, \tag{2.42}$$

and

$$V_{D_{int}S_{int}} = V_{DS} - 2I_{DS}R_S. \tag{2.43}$$

The data of L_{mask}, I_{DS}, V_{GS}, and V_{DS} are available from I-V measurement data. The data of R_S $(= R^u_{cont}/(WL_{ov}))$ and ΔL^{IV}_{tot} can be obtained as presented in section 2.3.3 (see Figure 2.7(a) and 2.7(b)). So, the values of C, $V_{GS_{int}}$, and $V_{D_{int}S_{int}}$ can be obtained by using Eq. (2.41)-(2.43).

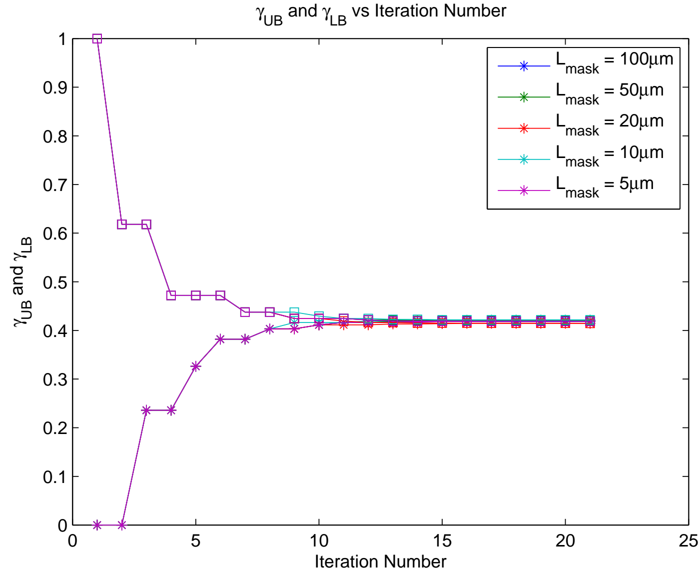
Therefore, Eq. (2.38), which is a linear model of $C^{\frac{1}{\gamma+1}}$ *vs.* $V_{GS_{int}}$, has three unknown parameters: γ, A, and B. The value of γ is extracted by using an iterative optimization method based on the principle described as follows. Assuming Eq. (2.37) exactly models measurement data, Eq. (2.38) implies that, if γ is equal to its true value, the data points of $C^{\frac{1}{\gamma+1}}$ *vs.* $V_{GS_{int}}$ should be exactly on a straight line, *i.e.*, they should have a perfect linearity. Their linearity can be measured by using $\rho_{data,\ model}$, *i.e.*, the correlation coefficient between measurement data points and the corresponding points on the fitted linear model. If measurement data points are identical to linear model points, the two groups of points are exactly positively linearly correlated, so $\rho_{data,\ model} = 1$. If not identical, $\rho_{data,\ model} < 1$. Therefore, the extraction of γ can be abstracted as an optimization task: search for the optimal value of γ to maximize $\rho_{data,\ model}$. In each step of optimization iterations, for a given value of γ, Eq. (2.38) is fitted to the data points of $C^{\frac{1}{\gamma+1}}$ *vs.* $V_{GS_{int}}$. Then, $\rho_{data,\ model}$ is calculated to evaluate the linearity of the data points of $C^{\frac{1}{\gamma+1}}$ *vs.* $V_{GS_{int}}$.

Golden Section Search method [23] was used to carry out the optimization task. In this method, an initial search range of γ must be set before optimization algorithm is started. Since γ is typically between zero and one, $\gamma_{UB} = 1$ and $\gamma_{LB} = 0$ are set to define the initial search range. When the algorithm iterates, γ_{UB} and γ_{LB} gradually converge toward each other, as illustrated in Figure 2.8(a). When $(\gamma_{UB} - \gamma_{LB})$ is smaller than a pre-defined error tolerance (*e.g.*, 10^{-4} is used here), $(\gamma_{UB} + \gamma_{LB})/2$ is used as the extracted value of γ, which is used to calculate $C^{\frac{1}{\gamma+1}}$. Then, Eq. (2.38) is fitted to the calculated data of $C^{\frac{1}{\gamma+1}}$ *vs.* $V_{GS_{int}}$ to extract A and B, as illustrated in Figure 2.8(b). The value of V_T is extracted by using $V_T = B/A$ (see Eq. (2.40)). The value of V_{AA} is extracted by using

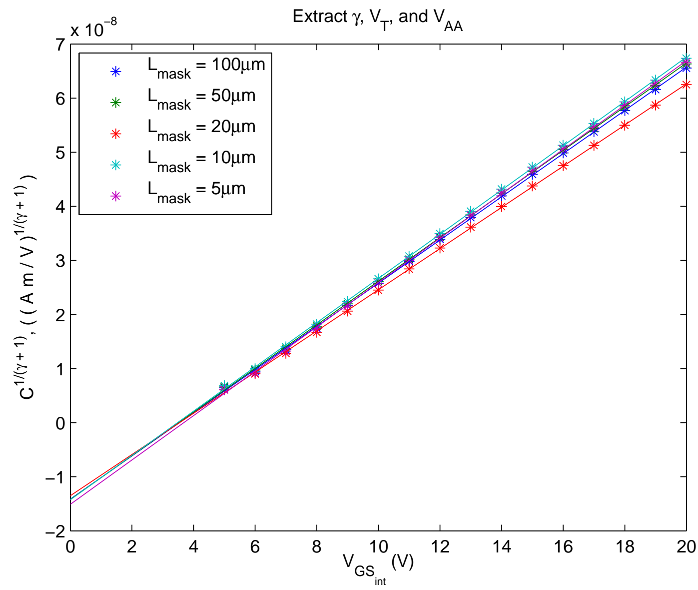
$$V_{AA} = \left(C_i W \mu_n / A^{\gamma+1}\right)^{1/\gamma}, \tag{2.44}$$

which was derived from Eq. (2.39). Note that C_i is channel capacitance per unit area, which can be determined by using C-V measurement data; μ_n is electron band mobility, which is a material parameter with a given constant value $\mu_n = 0.001\ \mathrm{m^2/(Vs)}$ [13].

The proposed parameter extraction method was run repeatedly to extract the values of γ, V_T, and V_{AA} for different L_{mask}. As shown in Figure 2.9(a), 2.9(b), and 2.10, the extracted values do not systematically depend on L_{mask}. The relative errors of the extracted values are 0.98% for γ, 3.58% for V_T, and 7.83% for V_{AA}. These results are consistent to

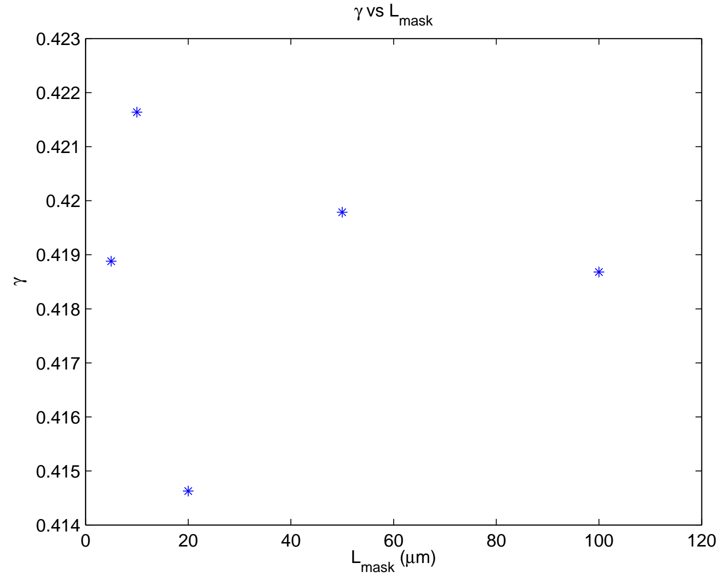


(a)

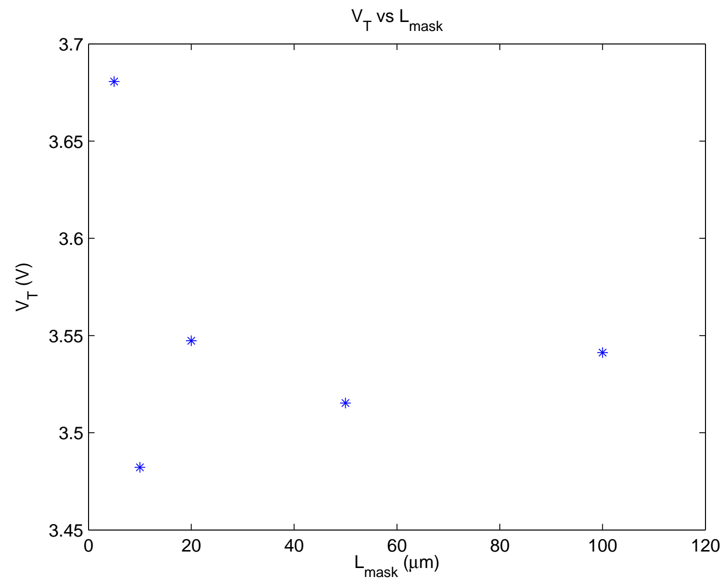


(b)

Figure 2.8: (a) γ_{UB} and γ_{LB} *vs.* Iteration Number (b) Extract γ, V_T, and V_{AA}.



(a)



(b)

Figure 2.9: Extracted values of (a) γ *vs.* L_{mask}, (b) V_T *vs.* L_{mask}.

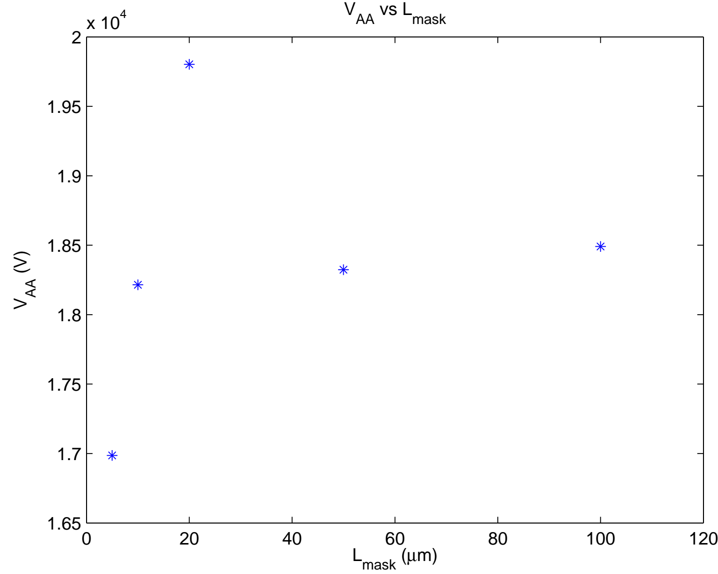


Figure 2.10: Extracted values of V_{AA} *vs.* L_{mask}.

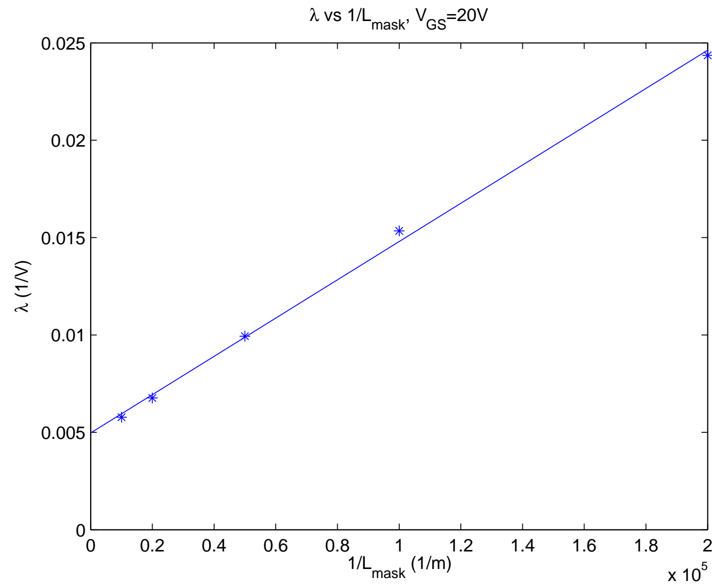
the device physics knowledge that those parameters should be independent from L_{mask}, because they are primarily determined by the property of a-Si:H material, especially when channel length is not very short (*i.e.*, longer than 5 μm). The averages of the extracted values of parameters are $\gamma = 0.419$, $V_T = 3.55$ V, and $V_{AA} = 18364$ V, respectively.

2.3.5 λ and m_{sat}

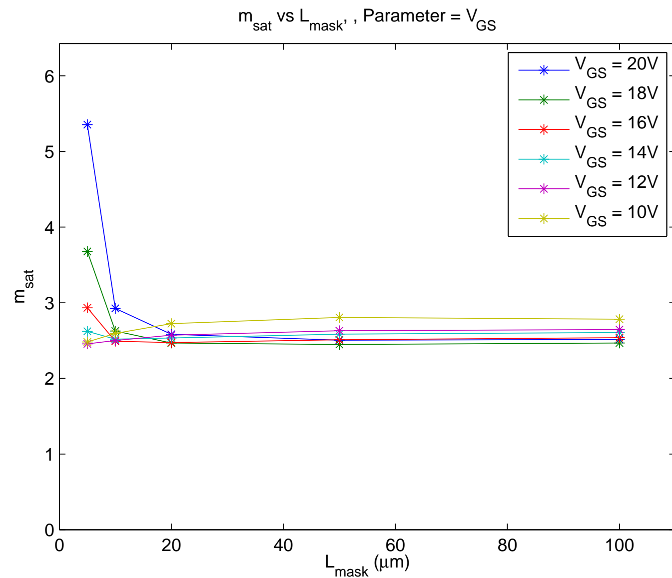
For a given L_{mask} and at a given V_{GS}, the values of λ and m_{sat} were extracted by using the method presented in [13]. To avoid the impact of contact resistance, the data of $V_{D_{int}S_{int}}$ (see Eq. (2.43)) instead of V_{DS} was used in parameter extraction. As shown in Figure 2.11(a), the extracted value of λ is proportional to $1/L_{mask}$. This behavior is similar to that of the λ of crystalline-silicon MOSFET. When L_{mask} is reduced, channel length modulation effect becomes relatively more significant, so λ increases. This dependence is described in this thesis by using an empirical model:

$$\lambda = S_\lambda / L_{mask} + \lambda_{intcpt}, \tag{2.45}$$

where S_λ and λ_{intcpt} are fitting parameters. Eq. (2.45) was fitted to the extracted values of λ *vs.* $1/L_{mask}$, as illustrated in Figure 2.11(a). The extracted values of parameters are



(a)



(b)

Figure 2.11: (a) Extracted values (symbols) and fitted model (line) of λ *vs.* $1/L_{mask}$ for $V_{GS} = 20$ V. (b) Extracted values of m_{sat} *vs.* L_{mask} for different V_{GS}.

$S_\lambda = 9.83 \times 10^{-8}$ m/V and $\lambda_{intcpt} = 4.97 \times 10^{-3}$ V^{-1}. Besides, the extracted m_{sat} *vs.* L_{mask} for different V_{GS} are shown in Figure 2.11(b). The extracted values of m_{sat} are fairly constant, expect for the ones for $L_{mask} = 5$ μm. The large variations of the extracted values of m_{sat} for $L_{mask} = 5$ μm could be attributed to some short channel effects which are not taken into account in RPI a-Si:H model [13]. The average of the extracted values of m_{sat}, excluding the ones for $L_{mask} = 5$ μm, is $m_{sat} = 2.59$.

2.3.6 α_{sat}

The author of [13] presented a method to extract α_{sat}. However, in this method, the impacts of contact resistance, channel length extension, and channel length modulation are not taken into account. To take into account these impacts, a new method to extract α_{sat} is presented as follows. First, Eq. (2.9) is reformulated as

$$I_{DS} = \alpha_{sat} \cdot D, \tag{2.46}$$

where

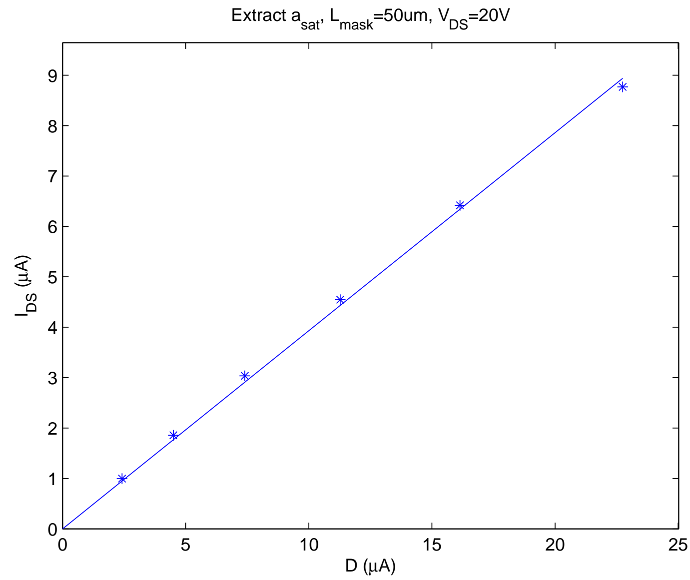
$$D = C_i \frac{W}{(L_{mask} + \Delta L_{tot}^{IV})} \mu_n \frac{(V_{GS_{int}} - V_T)^{\gamma+2}}{V_{AA}^{\gamma}} \left(1 + \lambda V_{D_{int}S_{int}}\right). \tag{2.47}$$

The parameter values extracted in previous sections and the *I*-*V* measurement data for $V_{DS} = 20$ V were used to calculate the values of D by using Eq. (2.47). Then, Eq. (2.46) was fitted to the data of I_{DS} *vs.* D to extract α_{sat}. For illustration, the data of I_{DS} *vs.* D for $L_{mask} = 50$ μm and the fitted line of the model in Eq. (2.46) are shown in Figure 2.12(a). The extracted values of α_{sat} for different L_{mask} are shown in Figure 2.12(b). The maximum relative error is only 2.64%. The average of the extracted values is $\alpha_{sat} = 0.395$.

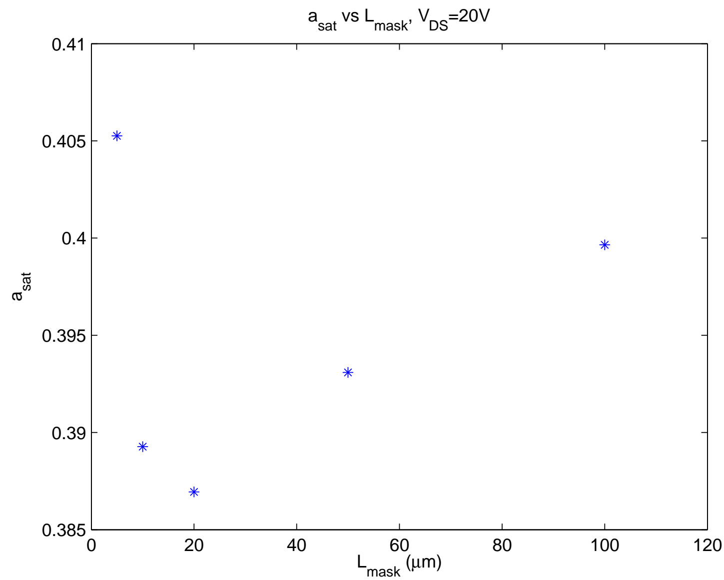
2.3.7 V_{GSL}, V_{DSL}, I_{0L}^u, and σ_0^u

In Eq. (2.16), $(\sigma_0^u V_{DS})$ and "-1" are negligible when $V_{DS} \gg 0$ and $V_{GS} \ll 0$. Therefore, by using the measurement data in this region, V_{GSL} and V_{DSL} can be extracted from the data of $\ln(I_{leak})$ *vs.* V_{GS} and $\ln(I_{leak})$ *vs.* V_{DS}, respectively [13]. For illustration, the extractions of V_{GSL} and V_{DSL} for $L_{mask} = 50$ μm are shown in Figure 2.13(a) and 2.13(b), respectively. Then, I_{0L}^u can be extracted by using a formula derived from Eq. (2.16):

$$I_{0L}^u = \exp\left[\ln\left(I_{leak}\right) - \frac{V_{DS}}{V_{DSL}} + \frac{V_{GS}}{V_{GSL}}\right] / \left(W L_{ov,D}\right) \tag{2.48}$$

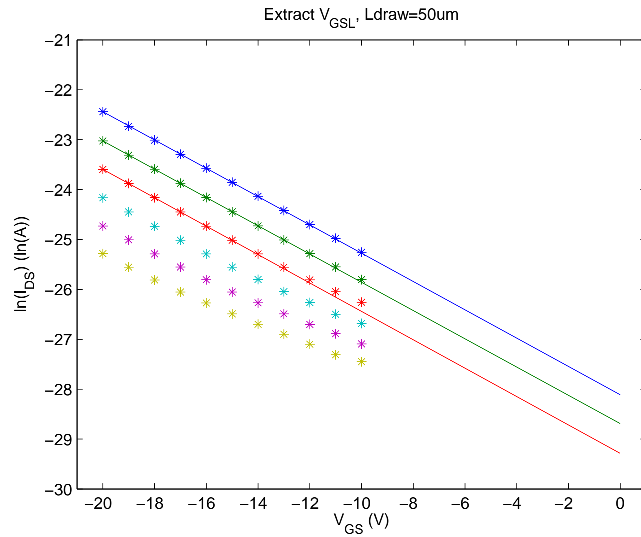


(a)

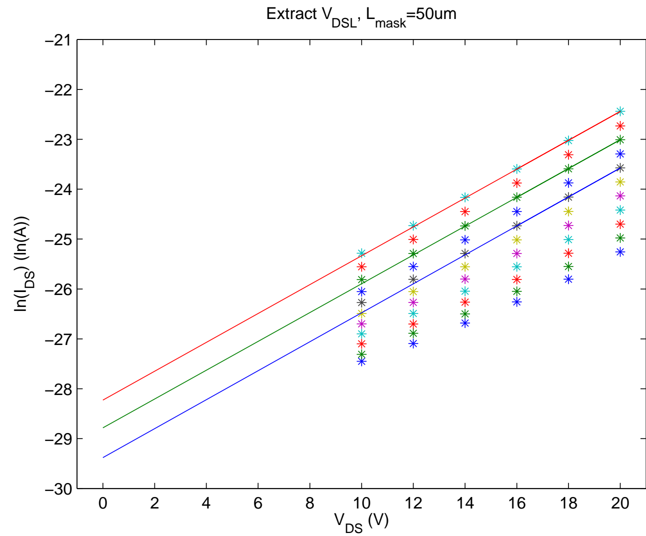


(b)

Figure 2.12: (a) Extract a_{sat} for V_{DS} = 20 V and L_{mask} = 50 μm. Data is indicated as symbols, and fitted model is line. (b) Extracted values of a_{sat} *vs.* L_{mask} for V_{DS} = 20 V.



(a)



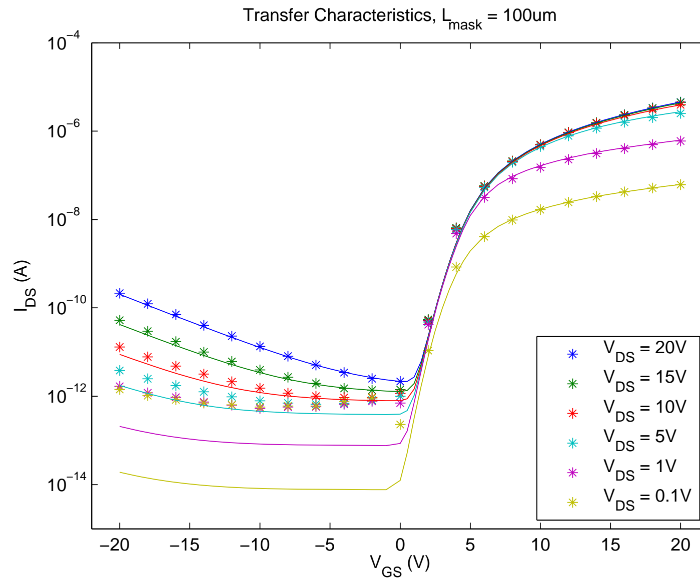
(b)

Figure 2.13: Extract leakage parameters for $L_{mask} = 50\ \mu$m. Data is indicated as symbols, and fitted models are lines. (a) Extract V_{GSL}. Bottom to top, measurement data: $V_{DS} =$ 10, 12, ..., 20 V; fitted model: $V_{DS} =$ 16, 18, 20 V. (b) Extract V_{DSL}. Bottom to top, measurement data: $V_{GS} = -10, -12, ..., -20$ V; fitted model: $V_{GS} = -16, -18, -20$ V.

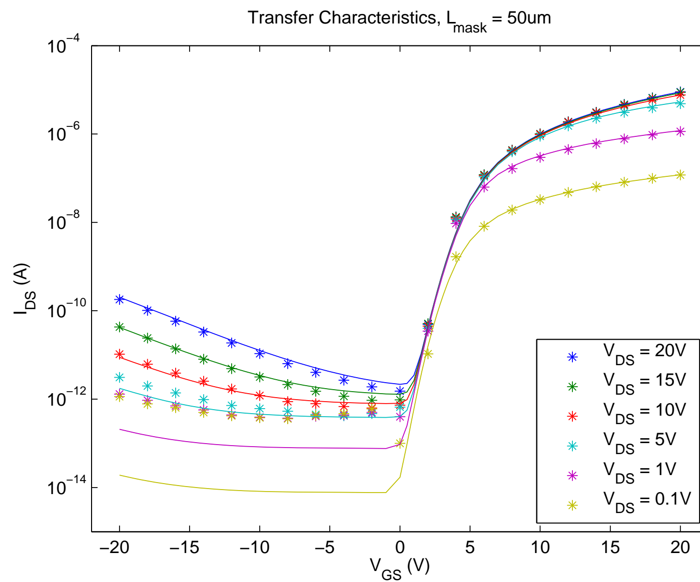
and the measurement data for $V_{DS} \gg 0$ V and $V_{GS} \ll 0$ V. Besides, σ_0^u can be extracted by using $\sigma_0^u = I_{min}^{V_{DS}^{max}} / V_{DS}^{max}$, where V_{DS}^{max} is the maximum V_{DS} used in measurement, and $I_{min}^{V_{DS}^{max}}$ is the minimum measured value of I_{DS} for V_{DS}^{max} [13]. The leakage current for $V_{GS} \ll 0$ V (*e.g.*, $V_{GS} < -8$ V) is primarily due to Poole-Frenkel effect, so the extracted values of parameters are essentially independent from channel length [17]. Therefore, it is reasonable to average the extracted parameter values for different channel lengthes. The averages of the extracted values of parameters are $V_{GSL} = 3.47$ V, $V_{DSL} = 3.16$ V, $I_{0L}^u = 5.42 \times 10^{-7}$ A/m^2, and $\sigma_0^u = 3.66 \times 10^{-5}$ A/(V·m^2). The leakage current for relatively low negative V_{GS} (*e.g.*, -8 V $< V_{GS} < 0$ V) is primarily due to back channel conduction, which is dependent on channel length [17], so the model in Eq. (2.16) is not suitable in this region. However, since the currents in this region are much lower than those in other regions by orders of magnitudes, the discrepancy of the model in Eq. (2.16) in this region may not be a major concern in practical circuit design.

2.3.8 Parameter Optimization and Model Verification

The a-Si:H TFT model presented in this section was implemented into a model file by using Verilog-A Hardware Description Language. The model file can be used with Cadence® Spectre® circuit simulator for circuit-level simulation. Besides, based on the parameter extraction methods presented in this section, a MATLAB® program was developed for parameter extraction and optimization. It controls the circuit simulator to simulate *I-V* characteristics. Simulation results were used by the program to automatically optimize the values of a group of selected parameters for the globally best fitting of simulation results to *I-V* measurement data for various L_{mask}. The selected parameters and their optimized values are: $V_{FB} = -1.981$ V, $V_0 = 0.1696$ V, $\alpha_{sat} = 0.3942$, $S_\lambda = 7.788 \times 10^{-8}$ m/V, $\lambda_{intcpt} = 6.325 \times 10^{-3}$ V^{-1}, $m_{sat} = 2.5896$, $\delta = 5.008$, $V_{min} = 0.3005$ V, $I_{0L}^u = 4.465 \times 10^{-7}$ A/m^2, and $\sigma_0^u = 3.037 \times 10^{-5}$ A/(V·m^2). The simulated transfer and output characteristics when using the optimized parameter values are verified by measurement data, as shown in Figure 2.14, 2.15, 2.16, and 2.17.

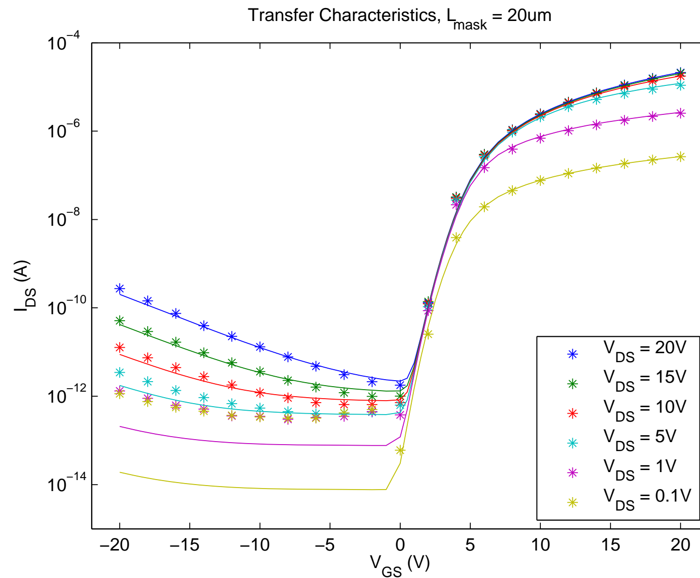


(a)

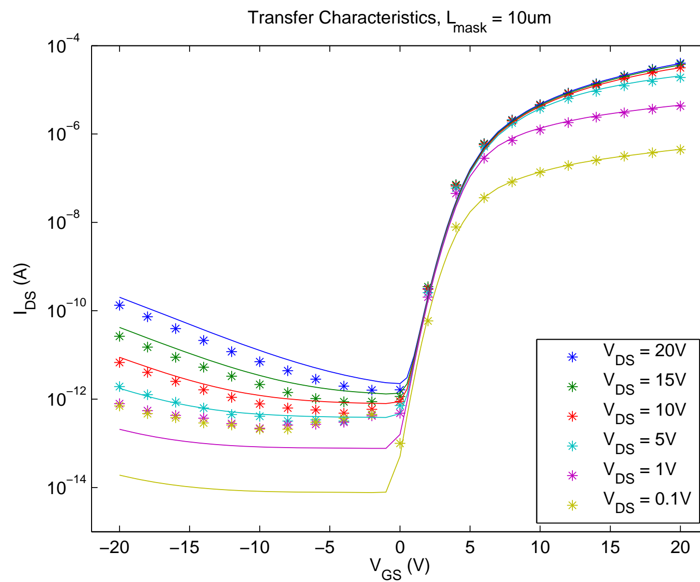


(b)

Figure 2.14: Comparison between measurement data (symbols) and simulation results (curves) of the transfer characteristics: (a) $L_{mask} = 100$ μm, and (b) $L_{mask} = 50$ μm.

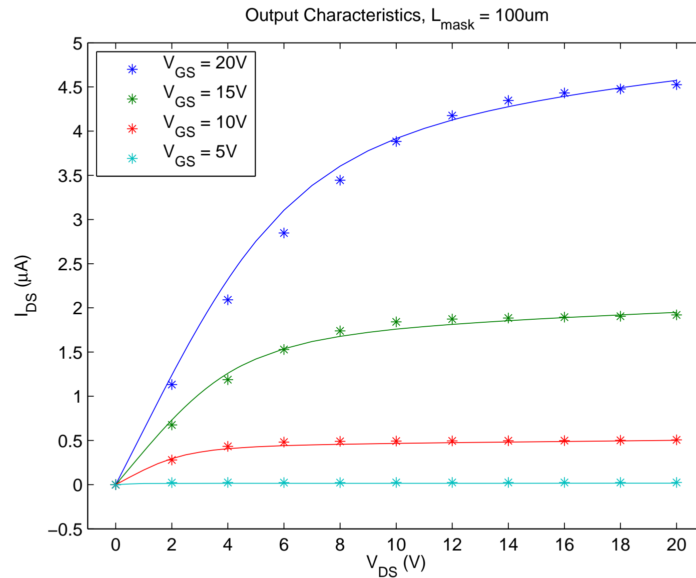


(a)

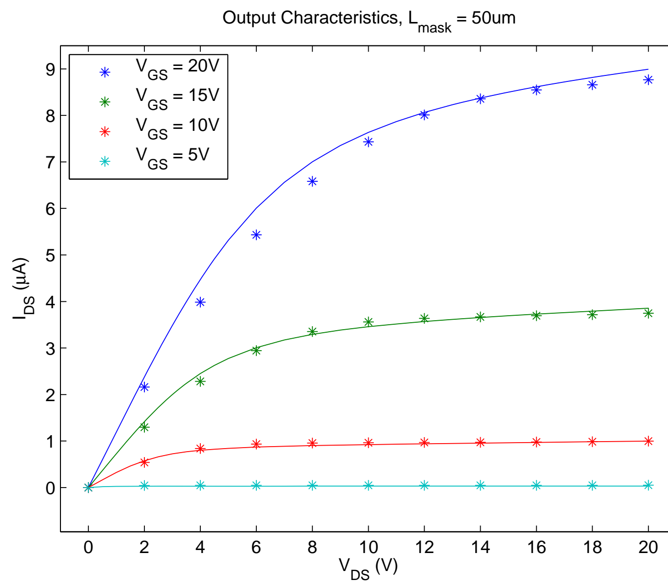


(b)

Figure 2.15: Comparison between measurement data (symbols) and simulation results (curves) of the transfer characteristics: (a) $L_{mask} = 20$ μm, and (a) $L_{mask} = 10$ μm.

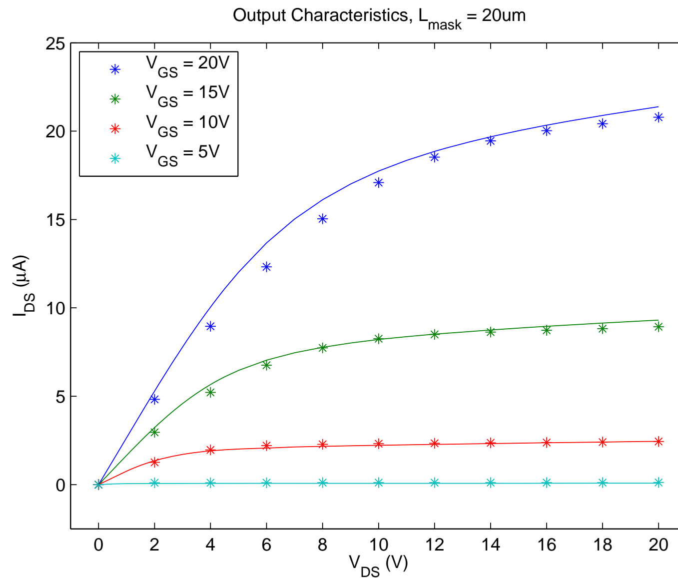


(a)

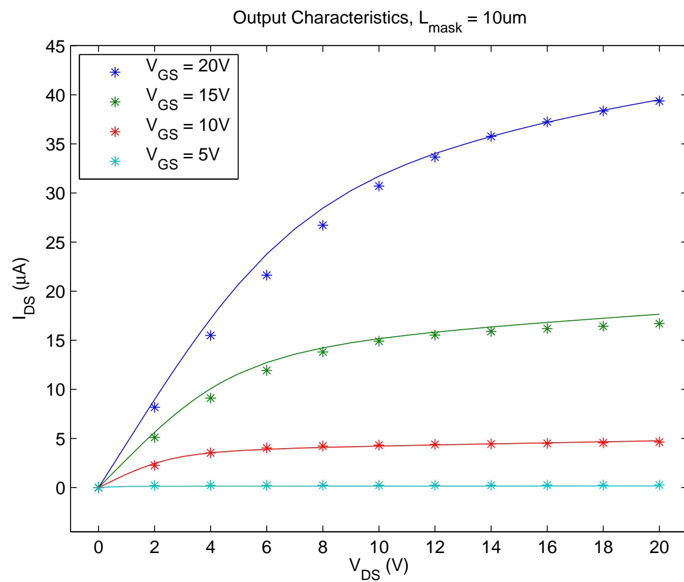


(b)

Figure 2.16: Comparison between measurement data (symbols) and simulation results (curves) of the output characteristics: (a) $L_{mask} = 100$ μm, and (b) $L_{mask} = 50$ μm.



(a)



(b)

Figure 2.17: Comparison between measurement data (symbols) and simulation results (curves) of the output characteristics: (a) $L_{mask} = 20\ \mu$m, and (b) $L_{mask} = 10\ \mu$m.

2.4 Review of Dynamic Models

Several dynamic models were proposed by previous researchers for a-Si:H TFTs. They can be divided into two categories: charge-based models and capacitance-based models.

2.4.1 Charge-Based Dynamic Models

Some charge-based dynamic models were proposed by previous researchers for a-Si:H TFT [17, 24–27]. These models are similar to the ones of crystalline-silicon MOSFET [28, 29]. In [24], the channel charges associated to source and drain are expressed as

$$Q_S = \int_0^L W C_{i,eff} V_{GC}(x) \left(1 - \frac{x}{L}\right) dx \tag{2.49}$$

and

$$Q_D = \int_0^L W C_{i,eff} V_{GC}(x) \left(\frac{x}{L}\right) dx, \tag{2.50}$$

respectively, where

$$C_{i,eff} = \begin{cases} C_i, & \text{if } V_{GS} \geqslant V_T, \\ 0, & \text{if } V_{GS} < V_T. \end{cases} \tag{2.51}$$

$V_{GC}(x)$ is defined as follows. Assuming source as the origin of x-axis, source-to-drain as the direction of x-axis, and source voltage as reference voltage level, $V_{GC}(x)$ is the difference between gate voltage and the voltage at a-Si:H/a-SiN$_x$:H interface at location x:

$$V_{GC}(x) = \left\{ \left[(V_{GD} - V_T)^{\frac{2}{\alpha}} - (V_{GS} - V_T)^{\frac{2}{\alpha}} \right] \frac{x}{L} + (V_{GS} - V_T)^{\frac{2}{\alpha}} \right\}^{\frac{\alpha}{2}}, \tag{2.52}$$

where $\alpha = 1$, if $T > T_c$; $\alpha = T/T_c$, if $T < T_c$; and $T_c = 300$ K [24]. Since the TFTs used in AMOLED displays normally operate under room temperature or higher, $\alpha = 1$ is assumed in the following derivation. Substituting Eq. (2.52) into Eq. (2.49) and (2.50) yields the channel charges respectively associated to source (Q_S), drain (Q_D), and gate (Q_G):

$$Q_S = Q_G|_{V_{GS}=V_{GD}} \left(\frac{4}{15}\right) \left(\frac{\beta_v^3 + 2\beta_v^2 + 3\beta_v + \frac{3}{2}}{(\beta_v + 1)^2}\right) \cdot (-1), \tag{2.53}$$

$$Q_D = Q_G|_{V_{GS}=V_{GD}} \left(\frac{4}{15}\right) \left(\frac{1 + 2\beta_v + 3\beta_v^2 + \frac{3}{2}\beta_v^3}{(\beta_v + 1)^2}\right) \cdot (-1), \tag{2.54}$$

$$Q_G = Q_G|_{V_{GS}=V_{GD}} \left(\frac{2}{3}\right) \left(\frac{\beta_v^2 + \beta_v + 1}{\beta_v + 1}\right) = -(Q_S + Q_D), \tag{2.55}$$

where

$$\beta_v = (V_{GD} - V_T) / (V_{GS} - V_T), \tag{2.56}$$

$$Q_G|_{V_{GS}=V_{GD}} = C_{G,DC}|_{V_{GS}=V_{GD}} \ (V_{GS} - V_T), \tag{2.57}$$

and

$$C_{G,DC}|_{V_{GS}=V_{GD}} = C_{i,eff} W L. \tag{2.58}$$

$C_{G,DC}|_{V_{GS}=V_{GD}}$ is the total gate-to-channel capacitance for $V_{DS} = 0$ V. Note that Q_S, Q_D, and Q_G are modeled as directly related to V_{GS} and V_{GD}. Besides, note that Eq. (2.53)-(2.55) are valid only for $V_{GS} \geqslant V_{GD} \geqslant V_T$ (*i.e.*, linear region). To guarantee the validity in other conditions, if $V_{GS} \geqslant V_T > V_{GD}$ (*i.e.*, saturation region), $(V_{GD} - V_T)$ should be fixed at zero; if $V_T > V_{GS} \geqslant V_{GD}$ (*i.e.*, subthreshold region and leakage region), both $(V_{GS} - V_T)$ and $(V_{GD} - V_T)$ should be fixed at zero, and β_v can be fixed at zero. Also note that, as indicated in Eq. (2.51), $C_{i,eff}$ is a piecewise function of V_{GS}. Therefore, the models of Q_S, Q_D, and Q_G respectively in Eq. (2.53)-(2.55) are piecewise functions of V_{GS} and V_{GD}.

It is proved in [24] that the transient currents at source and drain should be calculated respectively by using the following two formulas

$$i_S = dQ_S/dt, \tag{2.59}$$

$$i_D = dQ_D/dt. \tag{2.60}$$

The advantage of charge-based dynamic model is that it guarantees charge conservation, and therefore, simulation accuracy, because transient current is directly calculated from the change of charge with time: $i = dQ/dt$ [29, 30]. Nevertheless, conventional charge-based dynamic models still have a major drawback: since the model of $Q_{S(D)}$ is piecewise and has a corner at $V_{GS(D)} = V_T$, its first-order derivative (*i.e.*, capacitance) at $V_{GS(D)} = V_T$ is not continuous. This may result in convergence problems in transient simulation, especially for practical circuits where multiple TFTs are simultaneously involved in circuit simulation.

2.4.2 Capacitance-Based Dynamic Models

Capacitance-based dynamic TFT models [13, 31] were developed based on Meyer's capacitance model [32]. The formula of total gate charge Q_G in Eq. (2.55) is used to define the

small-signal channel capacitance between gate and source (drain) ($C_{GS(D)}$) [13]:

$$C_{GS} \triangleq \left.\frac{\partial Q_G}{\partial V_{GS}}\right|_{\overline{V_{GD}}} = \frac{2}{3}\, C_{G,DC}|_{V_{GS}=V_{GD}} \left(1 - \frac{(V_{GD}-V_T)^2}{(V_{GS}+V_{GD}-2V_T)^2}\right), \tag{2.61}$$

$$C_{GD} \triangleq \left.\frac{\partial Q_G}{\partial V_{GD}}\right|_{\overline{V_{GS}}} = \frac{2}{3}\, C_{G,DC}|_{V_{GS}=V_{GD}} \left(1 - \frac{(V_{GS}-V_T)^2}{(V_{GS}+V_{GD}-2V_T)^2}\right), \tag{2.62}$$

where $C_{G,DC}|_{V_{GS}=V_{GD}}$ is defined in Eq. (2.58). The author of [13] proposed to use

$$C_{i,eff} = \frac{C_i}{1 + 2\exp\left[\frac{-(V_{GS}-V_T)}{\eta_0 V_{th}}\right]} \tag{2.63}$$

as the formula of $C_{i,eff}$. Eq. (2.63) is based on Unified Charge Control Model [18], which takes into account the total induced charge in channel. It is valid for both above-threshold and below-threshold regions. Eq. (2.63) and its derivatives are continues with respect to V_{GS}. This is a desirable property for a better convergence of circuit simulation.

The transient currents at source and drain are defined respectively as [13]:

$$i_S \triangleq i_{GS} = C_{GS} \cdot dV_{GS}/dt, \tag{2.64}$$

$$i_D \triangleq i_{GD} = C_{GD} \cdot dV_{GD}/dt. \tag{2.65}$$

A major problem of this model is the inaccuracy caused by the definition of transient currents in Eq. (2.64) and (2.65). This problem is analyzed as follows. First, by using the definition of C_{GS} in Eq. (2.61) and C_{GD} in (2.62), expanding Eq. (2.64) and (2.65) yields

$$i_S = \frac{\partial Q_G}{\partial V_{GS}}\frac{dV_{GS}}{dt} = \left(\frac{\partial Q_S}{\partial V_{GS}}\frac{dV_{GS}}{dt}\right) + \left(\frac{\partial Q_D}{\partial V_{GS}}\frac{dV_{GS}}{dt}\right), \tag{2.66}$$

$$i_D = \frac{\partial Q_G}{\partial V_{GD}}\frac{dV_{GD}}{dt} = \left(\frac{\partial Q_S}{\partial V_{GD}}\frac{dV_{GD}}{dt}\right) + \left(\frac{\partial Q_D}{\partial V_{GD}}\frac{dV_{GD}}{dt}\right). \tag{2.67}$$

For comparison, expanding Eq. (2.59) and (2.60) yields

$$i_S = \frac{dQ_S}{dt} = \left(\frac{\partial Q_S}{\partial V_{GS}}\frac{dV_{GS}}{dt}\right) + \left(\frac{\partial Q_S}{\partial V_{GD}}\frac{dV_{GD}}{dt}\right), \tag{2.68}$$

$$i_D = \frac{dQ_D}{dt} = \left(\frac{\partial Q_D}{\partial V_{GS}}\frac{dV_{GS}}{dt}\right) + \left(\frac{\partial Q_D}{\partial V_{GD}}\frac{dV_{GD}}{dt}\right). \tag{2.69}$$

The i_S in Eq. (2.66) includes component $\left(\frac{\partial Q_D}{\partial V_{GS}}\frac{dV_{GS}}{dt}\right)$, which should not be a component of i_S, as indicated in Eq. (2.68). It is actually a component of i_D, as indicated in Eq. (2.69). Besides, the i_S in Eq. (2.66) does not include component $\left(\frac{\partial Q_S}{\partial V_{GD}}\frac{dV_{GD}}{dt}\right)$, which should be included in i_S, as shown in Eq. (2.68). Similar analysis applies to i_D. Therefore, the definitions of i_S and i_D respectively in Eq. (2.64) and (2.65) are inappropriate.

Besides, capacitance-based dynamic model has charge non-conservation problem [28–30]. It occurs when using $i_C = C(V) \cdot \frac{dV}{dt}$ (see Eq. (2.64) and (2.65)) in numerical computation (*e.g.*, in circuit simulation) to calculate transient current acrose a voltage-dependent nonlinear capacitor. More detailed analysis can be found in [28–30].

The capacitance-based dynamic model shown above is also not smooth. If $V_{GS(D)} < V_T$, term $\left(V_{GS(D)} - V_T\right)$ in the bracket of Eq. (2.61) ((2.62)) must be fixed at zero to guarantee the validity of the formulas. Therefore, Eq. (2.61) ((2.62)) is a piecewise function and has a corner at $V_{GS(D)} = V_T$. At this corner, the discontinuity of the first-order derivative of Eq. (2.61) ((2.62)) may result in convergence problem in circuit simulation.

2.4.3 Frequency Dispersion Effect

The C-V measurement results of a-Si:H TFT are dependent on measurement frequency. The apparent capacitance observed from measurement data decreases when frequency is increased. This is called frequency dispersion effect [13]. It is caused by the resistances of channel and contact and the finite carrier trapping/detrapping speed of a-Si:H. It can be modeled by adding equivalent access resistors in series with transient current sources [30] or channel capacitors [13]. Access resistor is modeled as a fraction of channel resistance:

$$R_{x,S} = \left.\frac{R_{ch}}{K_{SS}}\right|_{V_{DS}=0}, R_{x,D} = \left.\frac{R_{ch}}{K_{SS}}\right|_{V_{DS}}, \tag{2.70}$$

where

$$R_{ch} = \left.\left(\frac{dI_{DS}}{dV_{DS}}\right)^{-1}\right|_{V_{GS},V_{DS}} \tag{2.71}$$

is the small-signal resistance of entire channel, and K_{SS} is an empirical parameter, which can be extracted from C-V measurement data [13].

2.5 Improved Charge-Based Dynamic Model

2.5.1 Motivations

As discussed in section 2.4.2, capacitance-based dynamic models of a-Si:H TFT have drawbacks including: (1) inaccuracy problems caused by the inappropriate definitions of transient currents; (2) charge non-conservation problem; and (3) convergence problem in circuit simulation. A charge-based dynamic model is more preferable because it does not have the first two problems. However, as mentioned at the end of section 2.4.1, conventional charge-based dynamic models are not smooth, resulting in convergence problem in circuit simulation. Besides, conventional dynamic models assume a fixed channel length and a fixed K_{SS}. However, C-V measurement results indicate that they are dependent on gate voltage. Therefore, an improved charge-based dynamic model was developed in this research. It is smooth with respect to bias voltages so as to improve simulation convergence. Besides, it takes into account the dependence of channel length and K_{SS} on gate voltage.

2.5.2 Channel Length Extension

By carefully comparing Figure 2.21(a), 2.22(a), 2.23(a), and 2.24(a), one can see that under the same measurement condition, channel capacitance is not strictly proportional to L_{mask}. When L_{mask} is reduced, the observed channel capacitance is larger than the one estimated by assuming channel capacitance is strictly proportional to L_{mask}. This discrepancy is relatively more significant when L_{mask} is shorter. The extra channel capacitance can be explained by taking into account effective channel length extension ΔL_{tot}^{CV}:

$$L_{tot}^{CV} = L_{mask} + \Delta L_{tot}^{CV}, \tag{2.72}$$

where

$$\Delta L_{tot}^{CV} = \Delta L_{const}^{CV} + \Delta L_{S,var}^{CV} + \Delta L_{D,var}^{CV}. \tag{2.73}$$

ΔL_{const}^{CV} is independent from bias condition, and $\Delta L_{S(D),var}^{CV}$ is dependent on $V_{GS(D)}$ on source (drain) side. The superscript "CV" in a item indicates that the item is associated to C-V characteristics and is used in dynamic model. As a first-order estimation, assuming $\Delta L_{tot}^{CV} = \text{Ratio}_{CV/IV}^{\Delta L} \cdot \Delta L_{tot}^{IV}$, where $\text{Ratio}_{CV/IV}^{\Delta L}$ is an empirical parameter, Eq. (2.36) yields

$$\Delta L_{tot}^{CV} = \text{Ratio}_{CV/IV}^{\Delta L} \cdot \left(\Delta L_{const}^{IV} + \Delta L_{S,var}^{IV} + \Delta L_{D,var}^{IV}\right). \tag{2.74}$$

$\text{Ratio}^{\Delta L}_{CV/IV}$ can be extracted from measurement results. Since L_{mask} and ΔL^{IV}_{const} are constant, the constant component of L^{CV}_{tot} is

$$L^{CV}_{const} = L_{mask} + \text{Ratio}^{\Delta L}_{CV/IV} \cdot \Delta L^{IV}_{const}. \tag{2.75}$$

Besides, the comparison between Eq. (2.73) and (2.74) indicates that

$$\Delta L^{CV}_{S(D),var} = \text{Ratio}^{\Delta L}_{CV/IV} \cdot \Delta L^{IV}_{S(D),var}. \tag{2.76}$$

Eq. (2.75) and (2.76) are used to calculate channel charges in the following section.

2.5.3 Channel Charge Components

As aforementioned, to avoid the convergence problem in circuit simulation, a desirable dynamic model should be continuous and smooth with respect to bias voltages. To obtain such a model, the formula of $V_{GC}(x)$ shown in Eq. (2.52) should be used to substitute the V_{GS} in the formula of $C_{i,eff}$ shown in Eq. (2.63). Then, the modified formula of $C_{i,eff}$ in Eq. (2.63) should be used to replace $C_{i,eff}$ in Eq. (2.49) and (2.50). However, the derived integrals are too complicated to be solved analytically. Therefore, an approximation method is used as follows. Note that, channel charges are directly controlled by $V_{GS_{ch}}$ and $V_{GD_{ch}}$ (indicated in Figure 2.4), instead of V_{GS} and V_{GD}.

Total channel charge has two parts: the part associated to L^{CV}_{const} and the part associated to $\Delta L^{CV}_{S(D),var}$. The first part is derived as follows. Denote $Q^{const}_G|_{V_{GS_{ch}}=V_{GD_{ch}}}$ as the gate-to-channel charge associated to L^{CV}_{const} when $V_{GS_{ch}} = V_{GD_{ch}}$. To derive a continuous and smooth formula of $Q^{const}_G|_{V_{GS_{ch}}=V_{GD_{ch}}}$, the formula of $C_{i,eff}$ in Eq. (2.63) is used in the following integral:

$$Q^{const}_G|_{V_{GS_{ch}}=V_{GD_{ch}}} = \int_{-\infty}^{V_{GS_{ch}}} C_{i,eff}\; W L^{CV}_{const}\; dV_{GS_{ch}} \tag{2.77}$$

$$= C_i\; W L^{CV}_{const}\; V^{eff,CV}_{GS_{ch},T}\,, \tag{2.78}$$

where

$$V^{eff,CV}_{GS_{ch},T} = \eta_0 V_{th} \ln\left[1 + \frac{1}{2}\exp\left(\frac{V_{GS_{ch}} - V_T}{\eta_0 V_{th}}\right)\right]. \tag{2.79}$$

Using $Q_G^{const}|_{V_{GS_{ch}}=V_{GD_{ch}}}$ derived in Eq. (2.78) to replace $Q_G|_{V_{GS}=V_{GD}}$ in Eq. (2.53)-(2.55) yields the formulas of the charge components associated to L_{const}^{CV}:

$$Q_S^{const} = Q_G^{const}|_{V_{GS_{ch}}=V_{GD_{ch}}} \left(\frac{4}{15}\right)\left(\frac{\beta_v^3+2\beta_v^2+3\beta_v+\frac{3}{2}}{(\beta_v+1)^2}\right)\cdot(-1)\,, \tag{2.80}$$

$$Q_D^{const} = Q_G^{const}|_{V_{GS_{ch}}=V_{GD_{ch}}} \left(\frac{4}{15}\right)\left(\frac{1+2\beta_v+3\beta_v^2+\frac{3}{2}\beta_v^3}{(\beta_v+1)^2}\right)\cdot(-1)\,, \tag{2.81}$$

$$Q_G^{const} = Q_G^{const}|_{V_{GS_{ch}}=V_{GD_{ch}}} \left(\frac{2}{3}\right)\left(\frac{\beta_v^2+\beta_v+1}{\beta_v+1}\right) = -\left(Q_S+Q_D\right)\,, \tag{2.82}$$

where

$$\beta_v = V_{GS_{ch},T}^{eff,CV}/V_{GD_{ch},T}^{eff,CV}\,, \tag{2.83}$$

and $V_{GD_{ch},T}^{eff,CV}$ is defined as

$$V_{GD_{ch},T}^{eff,CV} = \eta_0 V_{th}\ln\left[1+\frac{1}{2}\exp\left(\frac{V_{GD_{ch}}-V_T}{\eta_0 V_{th}}\right)\right]\,, \tag{2.84}$$

which prevents a negative $(V_{GD_{ch}}-V_T)$ from invaliding the above formulas.

The part of channel charge associated to $\Delta L_{S(D),var}^{CV}$ is estimated as follows. Denote $V_T^{\Delta L}$ as the value of $V_{GS_{ch}(D_{ch})}$ beyond which $\Delta L_{S(D),var}^{IV}$ starts to increase with $V_{GS_{ch}(D_{ch})}$. When $V_{GS_{ch}(D_{ch})} = V_T^{\Delta L}$, $\Delta L_{var}^{IV,linear} = \Delta L_{const}^{IV}$, so $V_T^{\Delta L} = \left(\Delta L_{const}^{IV} - \Delta L_{var}^{IV,intcpt}\right)/S_{\Delta L}^{IV}$. Therefore, the part of channel charge associated to $\Delta L_{S(D),var}^{CV}$ is expressed as

$$Q_{S(D)}^{var} = -\int_{V_T^{\Delta L}}^{V_{GS(D)}} C_i W \Delta L_{S(D),var}^{CV} dV_{GS_{ch}(D_{ch})} \tag{2.85}$$

$$\approx -\frac{1}{2}\,C_i W \Delta L_{S(D),var}^{CV}\cdot\left(V_{GS_{ch}(D_{ch})} - V_T^{\Delta L}\right). \tag{2.86}$$

Using Eq. (2.76), (2.35), and (2.34), it can be proved that $Q_{S(D)}^{var}\to 0$ when $V_{GS_{ch}(D_{ch})}\to -\infty$, so the approximation in Eq. (2.86) does not affect simulation convergence. The total transient current at source (drain) is calculated as

$$i_{S_{ch}(D_{ch})} = \frac{d\left(-Q_{S(D)}^{const} - Q_{S(D)}^{var}\right)}{dt} \tag{2.87}$$

and implemented as the current sources in device model, as illustrated in Figure 2.4.

2.5.4 Overlap Capacitance

As shown in Figure 2.4, a simple capacitor $C_{GS(D)}^{ov} = C_{ov}WL_{ov,S(D)}$ is used to model the overlap capacitance between gate and source (drain). C_{ov} is the effective capacitance per unit area in overlap region, and $L_{ov,S(D)}$ is the overlap length on source (drain) side. The transient current associated to source (drain) overlap capacitor is calculated as

$$i_{S(D)}^{ov} = C_{GS(D)}^{ov} \frac{dV_{GS_{int}(D_{int})}}{dt}, \tag{2.88}$$

where $V_{GS_{int}(D_{int})}$ is the voltage difference between gate (G) and internal node at source (drain), *i.e.*, S_{int} (D_{int}). Since $C_{GS(D)}^{ov}$ is independent from bias voltages, using Eq. (2.88) in dynamic model does not cause charge non-conservation problem.

2.5.5 Access Resistors

In this thesis, F_{SS} is defined as $F_{SS} = 1/K_{SS}$. F_{SS} is the ratio of access resistor to the resistance of intrinsic channel. The value of F_{SS} can be extracted from measurement data, as discussed in section 2.6.3. The extracted values of F_{SS} are dependent on gate voltage, as shown in Figure 2.20(a). If V_{GS} is lower than V_T, TFT is OFF, so a minimal part of channel is involved in dynamic operation. If V_{GS} is relatively high, TFT is ON, so a larger part of channel is involved in dynamic operation. Since the dependence of F_{SS} on V_{GS} is similar to that of channel capacitance on V_{GS} (*e.g.*, see Figure 2.19(b)), an empirical model, which is similar to Eq. (2.63), is defined for F_{SS} in this thesis:

$$\frac{1}{K_{SS}} \triangleq F_{SS} = \frac{F_{SS}^{\text{Max-Min}}}{\left(1 + F_{p1}\exp\left[\frac{-(V_{GS}-F_{p3})}{F_{p5}}\right] + F_{p2}\exp\left[\frac{-(V_{GS}-F_{p4})}{F_{p6}}\right]\right)} + F_{SS}^{\text{Min}}, \tag{2.89}$$

where $F_{p1,2,\ldots,6}$, $F_{SS}^{\text{Max-Min}}$, and F_{SS}^{Min} are empirical parameters. Then, access resistors $R_{x,S}$ and $R_{x,D}$ are calculated by using following formulas:

$$R_{ch}^{ab} = \left(\frac{dI_{ab}}{dV_{D_{int}S_{int}}}\right)^{-1}\Bigg|_{V_{GS_{int}},V_{D_{int}S_{int}}}, \tag{2.90}$$

$$R_{ch}^{leak} = \left(\frac{dI_{leak}}{dV_{DS}}\right)^{-1}\Bigg|_{V_{GS}=0,V_{DS}=0}, \tag{2.91}$$

$$R_{ch} = \frac{R_{ch}^{ab}R_{ch}^{leak}}{R_{ch}^{ab} + R_{ch}^{leak}}, \tag{2.92}$$

$$R_{x,S} = F_{ss} \cdot R_{ch}|_{V_{D_{int}S_{int}}=0}, \tag{2.93}$$

$$R_{x,D} = F_{ss} \cdot R_{ch}. \tag{2.94}$$

Note that $R_{ch}|_{V_{D_{int}S_{int}}=0}$ is the value of R_{ch} calculated by using R_{ch}^{leak} and $R_{ch}^{ab}|_{V_{D_{int}S_{int}=0}}$.

2.6 Parameter Extraction for Dynamic Model

2.6.1 TFT Samples and Measurement Setup

The a-Si:H TFT samples used in *C*-*V* measurements were the same ones used in *I*-*V* measurements (see section 2.3.2). The capacitance between the gate and source of a-Si:H TFT for $V_{DS} = 0$ V was measured by using various frequencies at room temperature (23 °C). Since $V_{DS} = 0$ V, the source side and drain side of TFT are symmetrical, so the investigation on only source side is sufficient. Besides, since there is no static current between source and drain, there is no voltage drop across R_S. Therefore, $V_{GS} = V_{GS_{int}}$.

The impendence between the gate and source of a-Si:H TFT was measured by using Agilent® 4284 LCR meter and a Cascade® Summit® 12000 probe station. During *C*-*V* measurements, LCR meter was set to "C_S-R_S" mode, in which it uses an equivalent capacitor (C_{GS}^{eq}) and an equivalent resistor (R_S^{eq}) connected in series to model the measured impendence between the gate and source of a-Si:H TFT, as illustrated in Figure 2.18(a).

Static voltage sweeping was carried out in *C*-*V* measurements. Gate voltage was set at virtual ground level. The static voltages at source and drain were kept equal to each other (*i.e.*, $V_{DS} = 0$ V) while they were being swept. After a static bias voltage was assigned to source and drain, LCR meter applied a sinusoidal voltage signal to source. By using the measured amplitude and phase angle of gate transient current and the equivalent model shown in Figure 2.18(a), LCR meter calculates and reports the values of C_{GS}^{eq} and R_S^{eq}.

2.6.2 C_{GS}^{ov}, $C_{GS_{ch}}$, and $R_{x,S}$

The source side of the a-Si:H TFT model improved in this research (see Figure 2.4) is redrawn in Figure 2.18(b). Note that transient current source $i_{S_{ch}}$ is replaced by $C_{GS_{ch}}$ for the convenience of following discussion. The model shown in Figure 2.18(b) is different from the one used inside LCR meter (see Figure 2.18(a)), so the data of C_{GS}^{eq} and R_S^{eq} obtained from LCR meter can not be directly used in the proposed model. Therefore, a

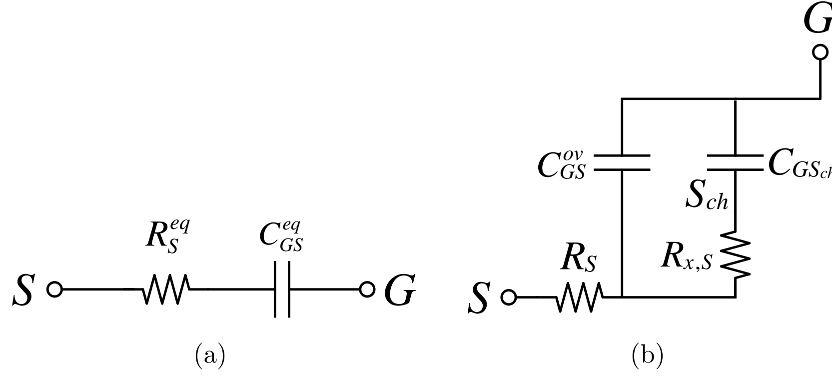


Figure 2.18: Dynamic models: (a) used in Agilent® 4284 LCR meter (C_S-R_S mode), and (b) used in this thesis for parameter extraction.

parameter extraction method was developed in this research by linking the proposed model to the one used in LCR meter. The impendence between G and S in Figure 2.18(b) is

$$Z_{GS} = \frac{[\,1/(sC_{GS_{ch}}) + R_{x,S}\,]\,/\,(sC_{GS}^{ov})}{[\,1/(sC_{GS_{ch}}) + R_{x,S}\,] + 1/(sC_{GS}^{ov})} + R_S \tag{2.95}$$

$$= \frac{R_{x,S}\;C_{GS_{ch}}^2}{(C_{GS}^{ov} + C_{GS_{ch}})^2 + (C_{GS}^{ov}\;C_{GS_{ch}}\;R_{x,S}\;\omega)^2} + R_S - j\frac{(C_{GS}^{ov} + C_{GS_{ch}}) + (C_{GS_{ch}}\;R_{x,S}\;\omega)^2 C_{GS}^{ov}}{\omega\left[(C_{GS}^{ov} + C_{GS_{ch}})^2 + (C_{GS_{ch}}\;R_{x,S}\;\omega)^2 C_{GS}^{ov\,2}\right]} \tag{2.96}$$

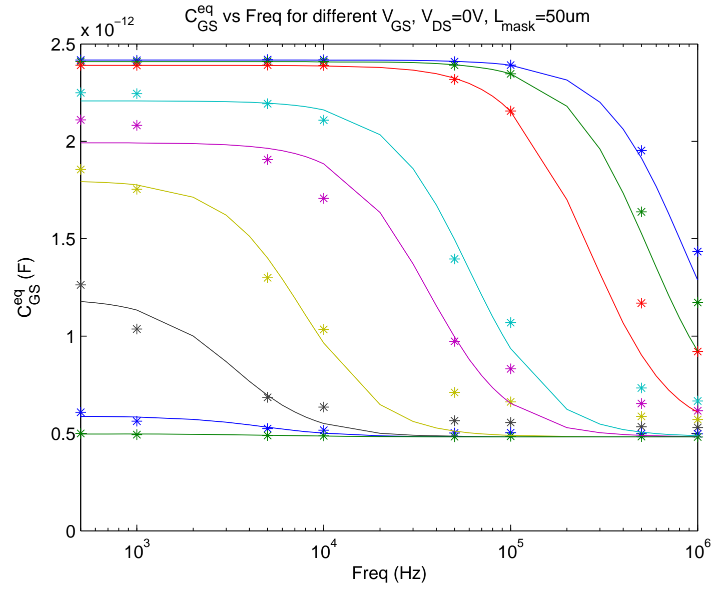
$$= R_S^{eq} - j\frac{1}{\omega C_{GS}^{eq}}. \tag{2.97}$$

Therefore, R_S^{eq} and C_{GS}^{eq} are the functions of ω $(= 2\pi f)$:

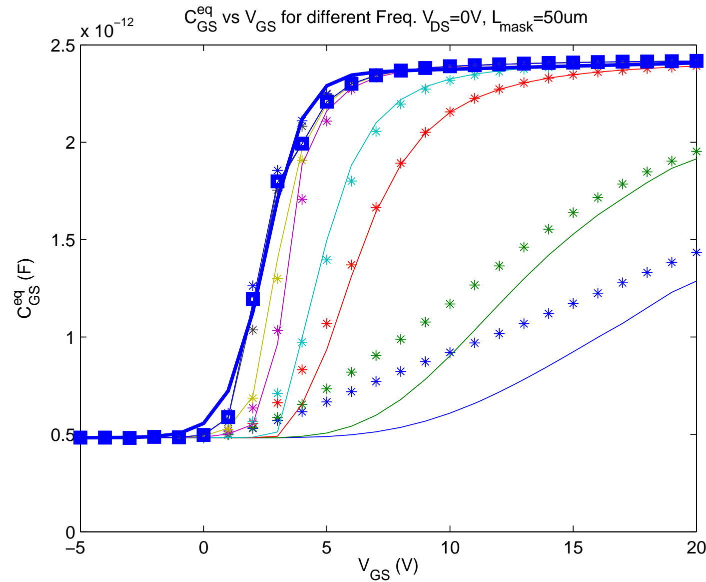
$$R_S^{eq} = \frac{R_{x,S} C_{GS_{ch}}^2}{(C_{GS}^{ov} + C_{GS_{ch}})^2 + (C_{GS}^{ov}\;C_{GS_{ch}}\;R_{x,S}\;\omega)^2} + R_S, \tag{2.98}$$

$$C_{GS}^{eq} = \frac{(C_{GS}^{ov} + C_{GS_{ch}})^2 + (C_{GS_{ch}}\;R_{x,S}\;\omega)^2 C_{GS}^{ov\,2}}{(C_{GS}^{ov} + C_{GS_{ch}}) + (C_{GS_{ch}}\;R_{x,S}\;\omega)^2 C_{GS}^{ov}}, \tag{2.99}$$

Parameters C_{GS}^{ov}, $C_{GS_{ch}}$, and $R_{x,S}$ were extracted from measurement data by using Eq. (2.99). First, since Eq. (2.99) reduces to $C_{GS}^{eq} = C_{GS}^{ov}$ if $C_{GS_{ch}}$ is zero, C_{GS}^{ov} was extracted as the average of the values of C_{GS}^{eq} when TFT is OFF, which is $C_{GS}^{ov} = 0.482$ pF. Since $C_{GS}^{ov} = C_{ov} W L_{ov,S}$ (see section 2.5.4), $C_{ov} = 19.3$ nF/cm^2. Then, for each given V_{GS},



(a)



(b)

Figure 2.19: Extracted data (symbols) and fitted model (curves) of (a) C_{GS}^{eq} *vs.* Frequency, top to bottom: $V_{GS} = 20$, 15, 10, 5, 4, ..., 0 V; (b) C_{GS}^{eq} (thin) and $(C_{GS_{ch}} + C_{GS}^{ov})$ (thick) *vs.* V_{GS}, top to bottom: Frequency = 500, 1 k, 5 k, ..., 1 MHz. $L_{mask} = 50\ \mu$m.

$C_{GS_{ch}}$ and $R_{x,S}$ were extracted by fitting Eq. (2.99) to the measurement data of C_{GS}^{eq} *vs.* Frequency. For illustration, the extraction of $C_{GS_{ch}}$ and $R_{x,S}$ for $L_{mask} = 50$ μm is presented in Figure 2.19(a). The plot is redrawn in Figure 2.19(b) as C_{GS}^{eq} *vs.* V_{GS}. The extracted values of $(C_{GS_{ch}} + C_{GS}^{ov})$ are indicated as the thick symbols in Figure 2.19(b).

2.6.3 F_{SS}

F_{SS} was calculated by using $F_{SS} = R_{x,S}/(R_{ch}|_{V_{D_{int}S_{int}}=0})$, which was derived from Eq. (2.93). The data of $R_{x,S}$ *vs.* V_{GS} was extracted as described in section 2.6.2. The data of $R_{ch}|_{V_{D_{int}S_{int}}=0}$ *vs.* V_{GS} was obtained by using Eq. (2.90)-(2.92). Eq. (2.89) was fitted to the calculated data of F_{SS} *vs.* V_{GS} to extract the parameters in Eq. (2.89). For illustration, the fitted model of F_{SS} for $L_{mask} = 50$ μm is presented as the curve in Figure 2.20(a), for which the extracted values are $F_{p1} = 11.83$, $F_{p2} = 0.717$, $F_{p3} = 2.33$ V, $F_{p4} = 0.127$ V, $F_{p5} = 1.15$ V, $F_{p6} = 24.39$ V, $F_{SS}^{\text{Max-Min}} = 0.353$, and $F_{SS}^{\text{Min}} = 7.20 \times 10^{-8}$.

2.6.4 C_i, η_0, V_T, and Ratio$_{CV/IV}^{\Delta L}$

The extracted data of $C_{GS_{ch}}$ *vs.* V_{GS} was used to extract C_i, η_0, V_T, and Ratio$_{CV/IV}^{\Delta L}$. $C_{GS_{ch}}$ is the sum of two capacitance components: (1) the part associated to $(L_{const}^{CV}/2)$, and (2) the part associated to $\Delta L_{S,var}^{CV}$. Therefore, the formula of $C_{GS_{ch}}$ was derived as follows:

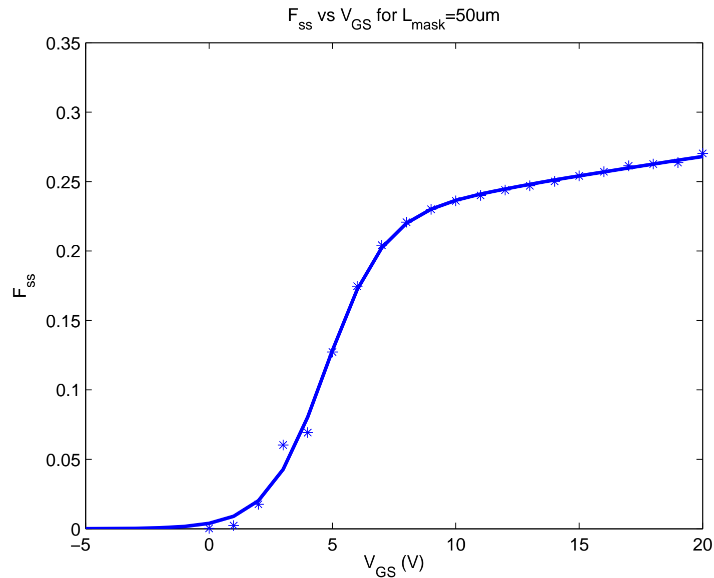
$$C_{GS_{ch}} = C_{i,eff} W L_{const}^{CV}/2 + C_i W \Delta L_{S,var}^{CV} \tag{2.100}$$

$$= \frac{C_i W \left(L_{mask} + \text{Ratio}_{CV/IV}^{\Delta L} \cdot \Delta L_{const}^{IV}\right)/2}{1 + 2\exp\left[\frac{-\left(V_{GS_{ch}} - V_T\right)}{\eta_0 V_{th}}\right]} + C_i W \left(\text{Ratio}_{CV/IV}^{\Delta L} \cdot \Delta L_{S,var}^{IV}\right). \tag{2.101}$$

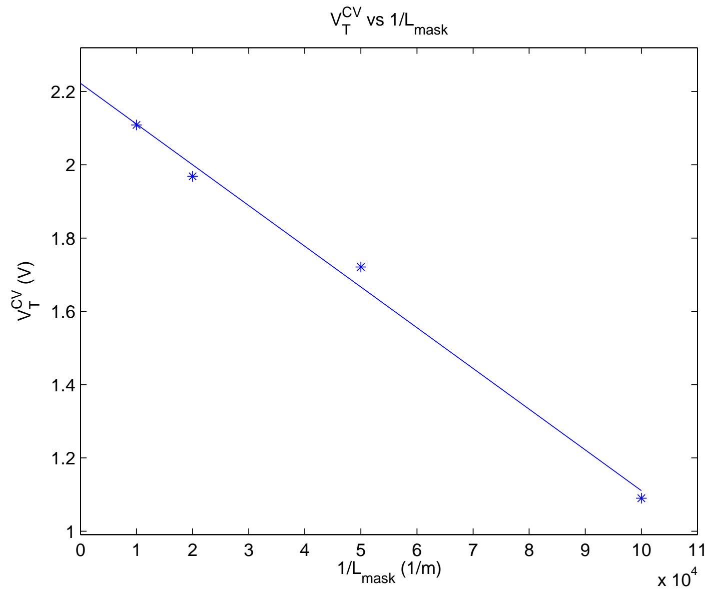
Note that the data of ΔL_{const}^{IV} and $\Delta L_{S,var}^{IV}$ *vs.* V_{GS} is already extracted in section 2.3.3. For a given L_{mask}, Eq. (2.101) is fitted to the extracted data of $C_{GS_{ch}}$ *vs.* V_{GS} to extract C_i, η_0, V_T, and Ratio$_{CV/IV}^{\Delta L}$. For illustration, the data and fitted model for $L_{mask} = 50$ μm are presented as the thick symbols and curve in Figure 2.19(b), for which the extracted values are $C_i = 14.7$ nF/cm^2, $\eta_0 = 30.93$, $V_T = 1.97$ V, and Ratio$_{CV/IV}^{\Delta L} = 1.001$.

2.6.5 Empirical Model of V_T^{CV}

The value of V_T extracted from *C-V* measurement data and used in dynamic model is denoted as V_T^{CV}. It may not be equal to V_T, which is the threshold voltage extracted from



(a)



(b)

Figure 2.20: Extracted data (symbols) and fitted model (curve or line) of (a) F_{SS} *vs.* V_{GS} for $L_{mask} = 50$ μm, and (b) V_T^{CV} *vs.* $1/L_{mask}$.

I-V measurement data (see section 2.3.4). V_T^{CV} is lower for a shorter L_{mask}, as shown in Figure 2.20(b). This dependence could be explained as follows. For a shorter L_{mask}, channel resistance is smaller, so $R_{x,S}$ is smaller. Therefore, when V_{GS} is close to V_T, the measured C_{GS}^{eq} is significantly larger (refer to Eq. (2.99)) than its expected value when assuming C_{GS}^{eq} is strictly proportional to L_{mask}. As a result, when L_{mask} is shorter, the measured C_{GS}^{eq} starts to increase with V_{GS} at a lower V_{GS}, so V_T^{CV} is lower. More in-depth investigations are need to further clarify the mechanism of this phenomenon. For practical consideration, to facilitate the usage of dynamic model in circuit simulation, the dependence of V_T^{CV} on L_{mask} is empirically modeled by using

$$V_T^{CV} = S_{V_T}/L_{mask} + V_T^{CV,intcpt}, \tag{2.102}$$

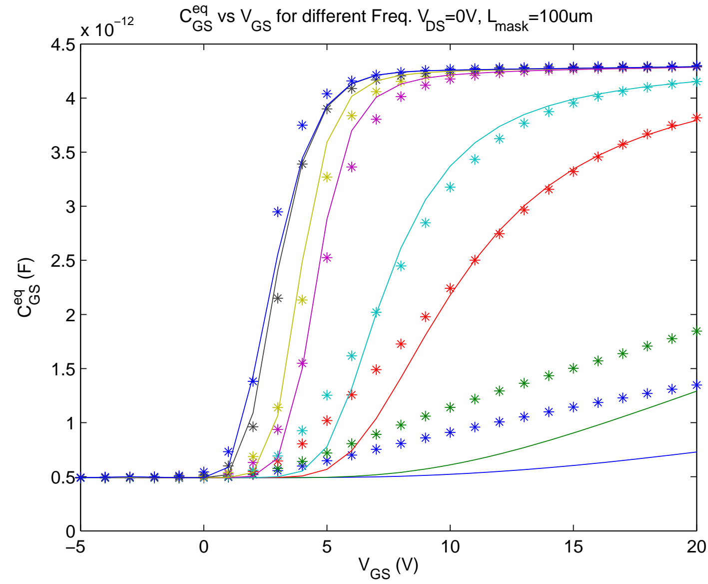
where S_{V_T} and $V_T^{CV,intcpt}$ are fitting parameters, whose values were extracted by fitting Eq. (2.102) to the data shown in Figure 2.20(b): $S_{V_T} = -1.11 \times 10^{-5}$ V/m, $V_T^{CV,intcpt} = 2.22$ V. V_T^{CV} is used to replace V_T in Eq. (2.79) and (2.84) when they are implemented in the model file of a-Si:H TFT for circuit simulation.

2.6.6 Parameter Optimization and Model Verification

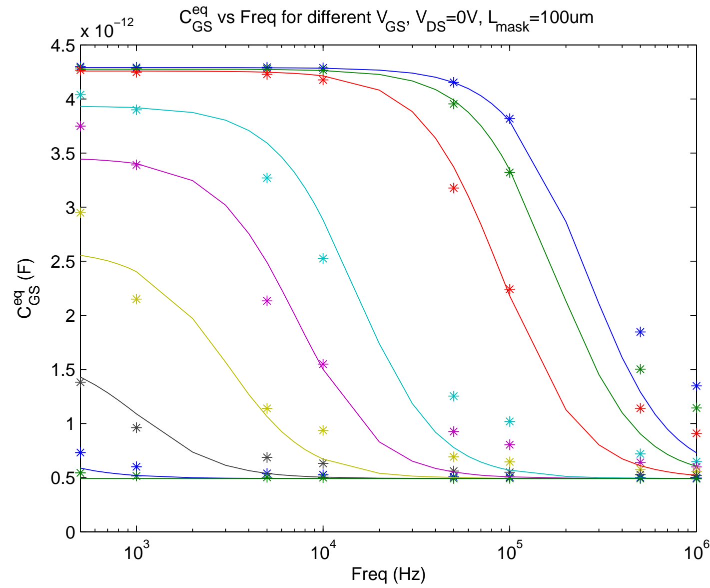
To further improve the accuracy of dynamic model, the values of the parameters used in dynamic model were optimized for the globally best fitting of dynamic model to C-V measurement data for various L_{mask}. The optimized values of parameters are C_i = 14.9 nF/cm^2, η_0 = 36.96, $\text{Ratio}_{CV/IV}^{\Delta L}$ = 0.892, F_{p1} = 12.02, F_{p2} = 1.90, F_{p3} = 2.48 V, F_{p4} = 0.0947 V, F_{p5} = 0.792 V, F_{p6} = 18.44 V, $F_{SS}^{\text{Max-Min}}$ = 0.5, $F_{SS}^{\text{Min}} = 5.41 \times 10^{-7}$, $S_{V_T} = -1.11 \times 10^{-5}$ V/m and $V_T^{CV,intcpt}$ = 2.22 V. For L_{mask} = 100, 50, 20, and 10 μm, the dynamic model improved in this research is verified by the comparison between the C-V measurement data and the fitted model when using the optimized parameter values, as shown in Figure 2.21, 2.22, 2.23, and 2.24, respectively.

2.7 Summary

For the static model and parameter extraction of a-Si:H TFT, the contributions made in this research are summarized as follows. (1) The gate-voltage dependence of contact resistance and channel length extension was extracted by using an improved method, described by using empirical models, and incorporated in static model. (2) A new method to extract γ, V_T, and V_{AA} was developed to correct the inaccuracy caused by gate-voltage-dependent

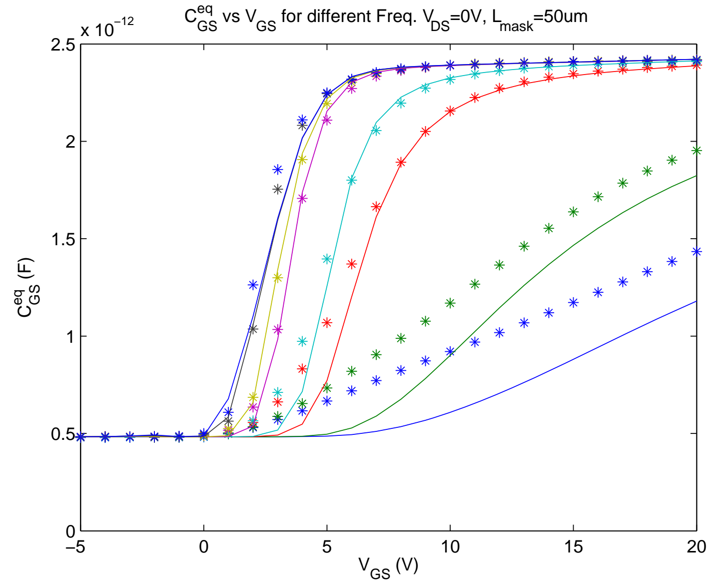


(a)

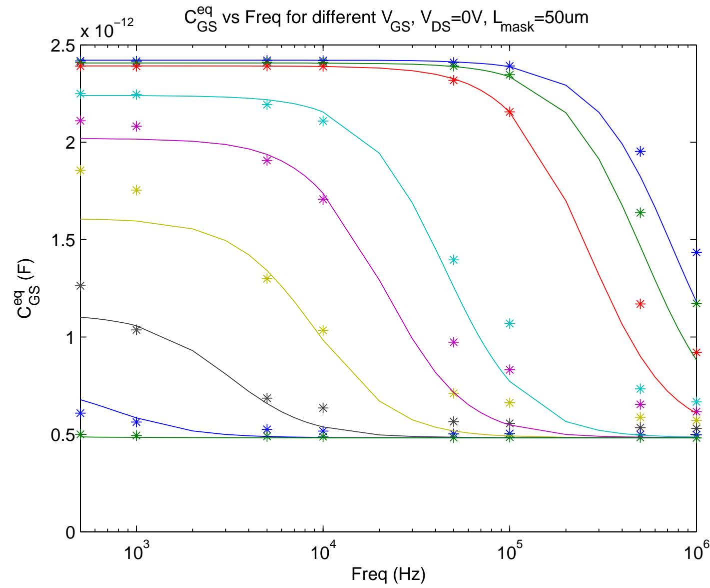


(b)

Figure 2.21: Measurement data (symbols) and fitted model (curves) of (a) C_{GS}^{eq} *vs.* V_{GS}, top to bottom: Frequency = 500, 1 k, 5 k, ..., 1 MHz; (b) C_{GS}^{eq} *vs.* Frequency, top to bottom: V_{GS} = 20, 15, 10, 5, 4, ..., 0 V. L_{mask} = 100 μm.

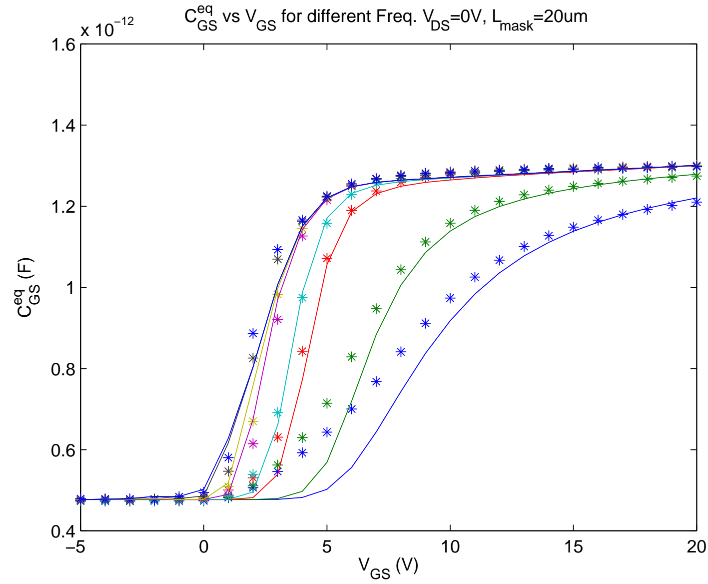


(a)

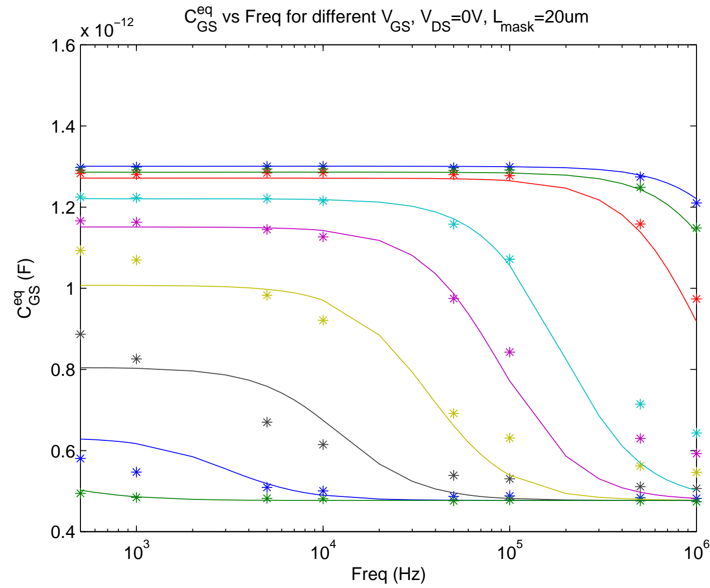


(b)

Figure 2.22: Measurement data (symbols) and fitted model (curves) of (a) C_{GS}^{eq} *vs.* V_{GS}, top to bottom: Frequency = 500, 1 k, 5 k, ..., 1 MHz; (b) C_{GS}^{eq} *vs.* Frequency, top to bottom: V_{GS} = 20, 15, 10, 5, 4, ..., 0 V. L_{mask} = 50 μm.

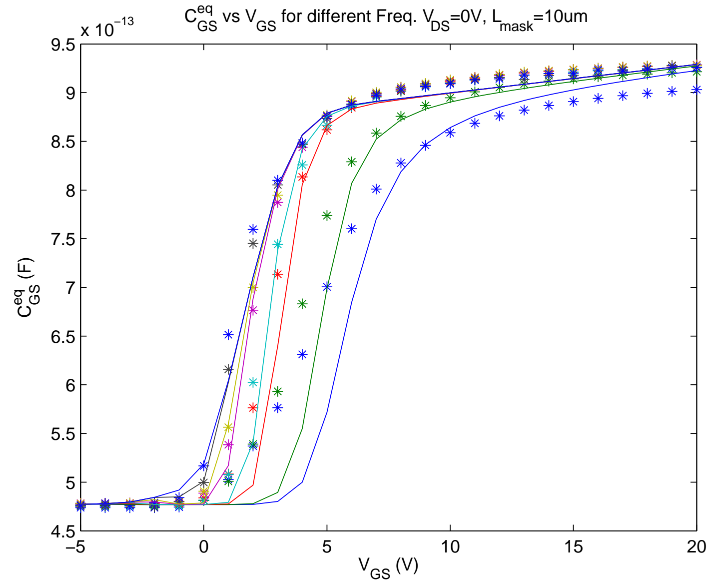


(a)

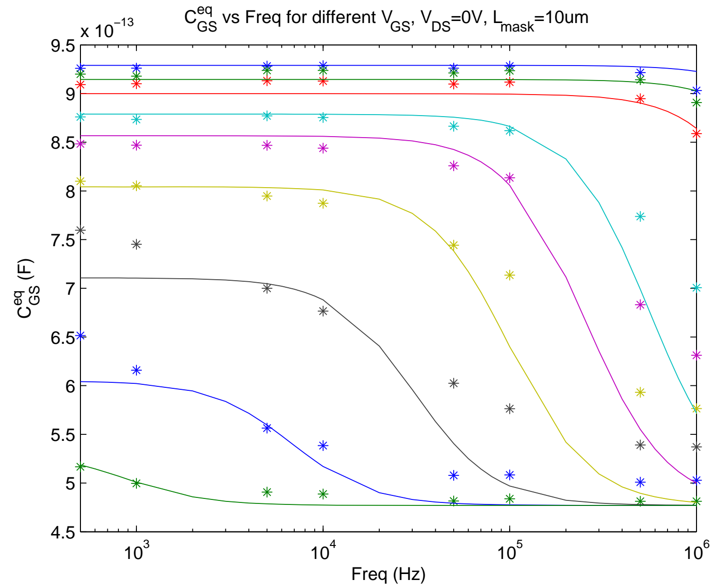


(b)

Figure 2.23: Measurement data (symbols) and fitted model (curves) of (a) C_{GS}^{eq} *vs.* V_{GS}, top to bottom: Frequency = 500, 1 k, 5 k, ..., 1 MHz; (b) C_{GS}^{eq} *vs.* Frequency, top to bottom: V_{GS} = 20, 15, 10, 5, 4, ..., 0 V. L_{mask} = 20 μm.



(a)



(b)

Figure 2.24: Measurement data (symbols) and fitted model (curves) of (a) C_{GS}^{eq} *vs.* V_{GS}, top to bottom: Frequency = 500, 1 k, 5 k, ..., 1 MHz; (b) C_{GS}^{eq} *vs.* Frequency, top to bottom: V_{GS} = 20, 15, 10, 5, 4, ..., 0 V. L_{mask} = 10 μm.

contact resistance and channel length extension. (3) The extractions of λ and m_{sat} were improved by taking into account contact resistance. (4) A new extraction method of α_{sat} was developed to correct the inaccuracy caused by gate-voltage-dependent contact resistance, channel length extension, and channel length modulation. (5) The dependence of λ on L_{mask} is described by using an empirical model.

For the dynamic model and parameter extraction of a-Si:H TFT, the contributions made in this research are summarized as follows. (1) Charge-based dynamic model was improved to improve its convergence in transient simulation. (2) Channel length extension is taken into account to improve model accuracy, especially for short-channel TFTs. (3) A method was developed to extract the parameter values needed in the improved dynamic model. (4) The dependence of F_{SS} on gate voltage is described by using an empirical model. (5) The dependence of V_T^{CV} on L_{mask} is described by using an empirical model.

The presented static model of a-Si:H TFT was implemented by using Verilog-A Hardware Description Language. The presented parameter extraction methods were implemented by using MATLAB® programming language. The accuracy of the model and parameter extraction methods is verified by measurement results. For above-threshold *I*-*V* characteristics, typical relative errors between simulation and measurement results are less than 5%. For *C*-*V* characteristics, when frequency is high (*i.e.*, $>$ 100 kHz) and V_{GS} is close to V_T, there are large relative errors between model and measurement data. However, this may not be a major concern in circuit design, since a-Si:H TFTs are not operated in this region in typical applications. In other cases, relative errors are typically less than 10%.

Chapter 3

Circuit-Level Aging Simulation of a-Si:H TFT

A method to simulate the aging of a-Si:H TFT by using circuit simulator is very helpful for the investigation of the impact of TFT aging on circuit performance and the improvement of circuit stability. A lot of previous researches were focused on the physical mechanism of the threshold voltage shift (ΔV_T) of a-Si:H TFT. Simple physical models were developed for some fixed stress conditions. However, in circuit operation, stress conditions may vary over stress time. Besides, conventional physical models use closed-form analytical formulas. However, the circuit-level simulation of ΔV_T requires transient simulation, which needs the differential equations of ΔV_T. These issues were addressed in this research.

In this chapter, conventional ΔV_T models of a-Si:H TFT are reviewed first. Then, the differential equations derived for the transient simulation of ΔV_T are presented. The influence of the finite response speed of a-Si:H TFT on ΔV_T is taken into account. The effectiveness of the proposed ΔV_T simulation method is verified by measurement results.

3.1 Review of ΔV_T Models

3.1.1 Constant Voltage Stress

The aging of a-Si:H TFT under gate voltage stress is a primary issue for its applications. Typically, it can be characterized as threshold voltage shift (ΔV_T), which can be attributed to two mechanisms: (1) the defect state creation in active layer and (2) the charge

trapping in gate dielectric [11, 12]. The dominance of these two mechanisms depends on stress condition. Charge trapping dominates under high gate voltage stress, while defect state creation dominates under low/medium gate voltage stress (*e.g.*, $|V_{GS}| < 30 \sim 50$ V, depending on gate dielectric quality) [11, 12, 33–37]. Since the gate voltages of the a-Si:H TFTs used in AMOLED displays are typically low/medium, defect state creation is the dominant ΔV_T mechanism of the a-Si:H TFTs used in AMOLED displays.

Positive (negative) gate stress voltage leads to positive (negative) ΔV_T and therefore decreased (increased) I_{DS} [38]. A-Si:H TFTs are used as switches in their conventional applications (*e.g.*, LCD displays). Comparing to total operation time, the time during which a switch TFT is ON (*i.e.*, being applied with an above-threshold gate voltage) is negligible, so the ΔV_T of a-Si:H TFT in those conventional applications is not significant. However, in AMOLED displays, a-Si:H TFTs are used as drive TFTs, which drive OLED currents, as well as switch TFTs. Drive TFTs are always or mostly ON when AMOLED display operates, so their aging is much more significant than that of switch TFTs. Besides, different stress histories result in different ΔV_T in different pixels, so the uniformity of pixel performance across a display panel may degrade over stress time.

Charge Trapping

The charge trapped in a-SiN$_x$:H gate dielectric causes ΔV_T. Charge trapping is dependent on N/Si ratio. A larger N/Si ratio results in less trapping states in a-SiN$_x$:H and thus a smaller ΔV_T caused by the charge trapped in a-SiN$_x$:H. Therefore, for a larger N/Si ratio, charge trapping dominates only under a higher gate voltage [36, 37, 39, 40].

Charge trapping occurs at a-SiN$_x$:H/a-Si:H interface and in the bulk of a-SiN$_x$:H near the interface [41]. a-SiN$_x$:H has a high defect density [38]. When a gate voltage is applied, the energy barrier between the charge in the states near the band edge of a-Si:H and the trapping states in a-SiN$_x$:H is lowered, so charge tunnels from a-Si:H into a-SiN$_x$:H. Tunneling charge is first trapped in the states at a-SiN$_x$:H/a-Si:H interface, and then moves to and is trapped in the states in the bulk of a-SiN$_x$:H for a longer stress time, a higher stress voltage, and/or a higher temperature [41].

Defect Creation/Removal

For a-Si:H TFT with nitride-rich a-SiN$_x$:H gate dielectric and low/medium gate voltage, defect state creation/removal in a-Si:H near a-Si:H/a-SiN$_x$:H interface is the dominant ΔV_T mechanism [11, 33–37, 42–44]. If a positive $V_{GS} > V_T$ is applied, electrons are accumulated

in a-Si:H near the interface. Some weak Si-Si bonds are broken by the accumulated electrons and become dangling bonds (*i.e.*, defects states) [12]. The created defect states are distributed in the lower part of the band gap of a-Si:H and trap the electrons from conduct band tail states. Since the density of electrons in conduction band tail states is reduced, there is a decrease of I_{DS}, which can be characterized as a positive ΔV_T. If a negative gate voltage is applied, holes are accumulated in a-Si:H near the interface, so some defect states are removed from the lower part of band gap [34, 35]. Since less electrons are trapped in defect states, there is a increase of I_{DS}, which can be characterized as a negative ΔV_T.

Several models were developed by previous researchers to describe the ΔV_T caused by the defect state creation/removal under constant voltage stress. A widely used ΔV_T model is stretched exponential model:

$$\Delta V_T = \left(V_{GS} - V_T^{init}\right) \left\{1 - \exp\left[-\left(\frac{t}{\tau_{st}}\right)^{\beta_{st}}\right]\right\}, \tag{3.1}$$

where V_T^{init} is the initial V_T of a fresh TFT before aging test, t is stress time, τ_{st} is characteristic time constant, and β_{st} is stretched exponential exponent. τ_{st} and β_{st} are dependent on gate voltage polarity, temperature, and process technology. The value of β_{st} is about 0.5 for above-threshold gate stress voltage, and 0.3 for negative gate stress voltage [38]. Eq. (3.1) can be approximated by a power-law ΔV_T model if $t \ll \tau_{st}$ [36, 38]:

$$\Delta V_T = \left(V_{GS} - V_T^{init}\right) \left(\frac{t}{\tau_{st}}\right)^{\beta_{st}}. \tag{3.2}$$

In addition, previous researchers also observed that ΔV_T has a power-law dependence on gate stress voltage [38, 45–55]. It can be modeled as

$$\mid \Delta V_T \mid = A \left|V_{GS} - V_T^{init}\right|^{\alpha_{st}} t^{\beta_{st}}, \tag{3.3}$$

where A, α_{st}, and β_{st} are dependent on gate voltage polarity [38]. For above-threshold gate voltage, the range of α_{st} is about $1 \sim 2$. For negative gate voltage, the range of α_{st} is about $3 \sim 4$ [45]. The comparison between Eq. (3.2) and Eq. (3.3) indicates that τ_{st} is dependent on $|V_{GS} - V_T^{init}|$ [38, 54]. The dependence can be expressed as

$$\tau_{st} = \frac{1}{A^{1/\beta}} \left|V_{GS} - V_T^{init}\right|^{\frac{1-\alpha_{st}}{\beta}}. \tag{3.4}$$

Effect of Drain Stress Voltage

The ΔV_T models discussed above are based on the assumption that $V_{DS} = 0$ V. This may be a reasonable assumption for the switch TFTs used in AMLCD and AMOLED displays. In contrast, the drive TFTs of OLEDs in AMOLED displays are biased in saturation region, where $V_{DS} \neq 0$ V. Therefore, the dependence of ΔV_T on V_{DS} is discussed as follows.

For low/medium above-threshold gate stress voltage, the dependence of ΔV_T on V_{DS} is explained by relating ΔV_T to the profile of local density of mobile electrons along the channel of a-Si:H TFT [27, 55–57]. When a n-channel a-Si:H TFT is ON, the local ΔV_T in channel is proportional to local defect density, and the increase rate of local defect density is proportional to the local density of mobile electrons. The ΔV_T extracted from *I*-*V* characteristics is an average of the ΔV_T profile along channel. The influence of different V_{DS} levels on ΔV_T is discussed as follows [27, 55–57].

- If $V_{GS} > V_T$ and $V_{DS} = 0$ V, mobile electron density, defection creation, and therefore ΔV_T, are uniform along channel, so the extracted ΔV_T has a maximum value.
- If V_{GS} is kept the same, but $V_{DS} > 0$ V, mobile electron density, defection creation, and therefore ΔV_T are reduced near drain, so the extracted ΔV_T is smaller.
- If V_{DS} is so high that TFT is in saturation region, the mobile electrons at a-Si:H/a-SiN_x:H interface exist in channel only between source and pinch-off point. From pinch-off point to drain, electrons are not concentrated at the interface. Therefore, defect creation is limited in the part of channel between source and pinch-off point.
- If V_{DS} is further increased, pinch-off point moves towards source, so defect creation is more limited toward the source side of channel. Besides, when TFT is in saturation region, pinch-off point location and channel electron density do not vary significantly with V_{DS}, so the extracted ΔV_T is not significantly dependent on V_{DS}.

To take into account the dependence of ΔV_T on V_{DS} for the a-Si:H TFT stressed by above-threshold gate voltage in linear region, the authors of [56] modified Eq. (3.3) as

$$\Delta V_T = A\left(V_{GS} - V_T^{init}\right) t^{\beta_{st}} \left(\frac{Q_G}{Q_{G,0}}\right), \tag{3.5}$$

where $\alpha_{st} = 1$ is assumed. In Eq. (3.5), $Q_{G,0}$ is the channel charge when $V_{DS} = 0$ V:

$$Q_{G,0} = C_i W L \left(V_{GS} - V_T\right), \tag{3.6}$$

which is the maximum channel charge for a given V_{GS}, because channel is uniform when $V_{DS} = 0$ V. Besides, Q_G is the channel charge when V_{GS} and V_{GD} are both higher than V_T:

$$Q_G = \frac{2}{3}\, C_i W L\, \frac{\left(V_{GS} - V_T\right)^3 - \left(V_{GD} - V_T\right)^3}{\left(V_{GS} - V_T\right)^2 - \left(V_{GD} - V_T\right)^2}, \tag{3.7}$$

where C_i is the gate dielectric capacitance per unit area, and W and L are channel width and length, respectively [58]. If $V_{GD} \to V_{GS}$, $Q_G/Q_{G,0} \to 1$, Eq. (3.5) reduces to Eq. (3.3). If $V_{GD} \to V_T$, $Q_G/Q_{G,0} \to 2/3$. If V_{GD} is further reduced beyond V_T, TFT is stressed in deeper saturation region, $Q_G/Q_{G,0}$ remains as 2/3 [56].

The dependence of ΔV_T on V_{DS} when n-channel a-Si:H TFT is stressed by negative gate voltage is mentioned in [50], but is not deeply investigated in literatures.

ΔV_T under Zero Voltage Stress

After gate stress voltage is removed, the density of defect states reduces, and the charge trapped in defect states de-traps [38, 59], so V_T recovers toward its initial value of fresh a-Si:H TFT. This behavior of V_T is described by using a stretched exponential model:

$$V_T = \left[V_T\left(0\right) - V_T\left(\infty\right)\right] \cdot \exp\left[-\left(\frac{t}{\tau_{rex}}\right)^{\beta_{rex}}\right] + V_T\left(\infty\right), \tag{3.8}$$

where $V_T\left(0\right)$ and $V_T(\infty)$ are the values of V_T at the beginning of relaxation phase and after infinite time, respectively, and β_{rex} and τ_{rex} are empirical parameters [59]. As presented in [59], at temperature 403 K and after long enough relaxation time, V_T eventually comes back to its initial value of fresh a-Si:H TFT, *i.e.*, $V_T(\infty) = V_T^{init}$.

3.1.2 Step-Increasing Voltage Stress

A step-increasing gate stress voltage is shown in Figure 3.1 [54]. A method to predict the ΔV_T for this stress condition is presented in [54]. Based on Eq. (3.1), $f\left(V_{GS}, t\right)$ is defined:

$$f\left(V_{GS}, t\right) = \Delta V_T = \left(V_{GS} - V_T^{init}\right)\left\{1 - \exp\left[-\left(\frac{t}{\tau_{st}}\right)^{\beta_{st}}\right]\right\}, \tag{3.9}$$

where τ_{st} is defined essentially the same to Eq. (3.4):

$$\tau_{st} = K_{st}\left|V_{GS} - V_T^{init}\right|^{\frac{1-\alpha_{st}}{\beta_{st}}}. \tag{3.10}$$

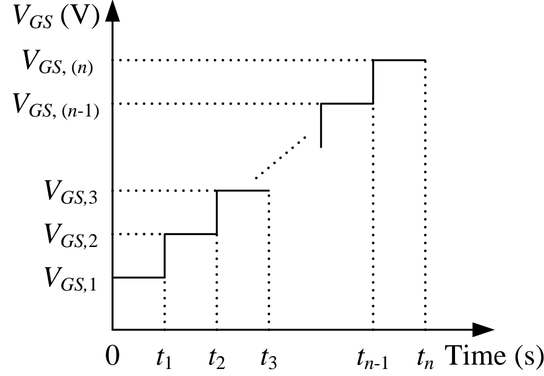


Figure 3.1: Diagram for a step-increasing gate stress voltage.

In this method, $\Delta V_{T,1}$, which is the ΔV_T at $t = t_1$, is calculated by using Eq. (3.9). When calculating $\Delta V_{T,2}$, which is the ΔV_T at $t = t_2$, t_1 is replaced by effective time $t^{eff}_{st,1}$, which is the t calculated by using $V_{GS,2}$ and $\Delta V_{T,1}$ in the inverse function of Eq. (3.9):

$$t^{eff}_{st,1} = f^{-1}\left(V_{GS,2},\ \Delta V_{T,1}\right). \tag{3.11}$$

Then, by using $t^{eff}_{st,1}$ and $V_{GS,2}$ in Eq. (3.9), $\Delta V_{T,2}$ is calculated as

$$\Delta V_{T,2} = f\left[V_{GS,2},\ t^{eff}_{st,1} + (t_2 - t_1)\right]. \tag{3.12}$$

Eq. (3.11) and (3.12) are generalized respectively as

$$t^{eff}_{st,(n-1)} = f^{-1}\left[V_{GS,(n)}, \Delta V_{T,(n-1)}\right], \tag{3.13}$$

$$\Delta V_{T,(n)} = f\left[V_{GS,(n)},\ t^{eff}_{st,(n-1)} + (t_n - t_{n-1})\right]. \tag{3.14}$$

which are used iteratively to calculate the ΔV_T at $t = t_n$ (*i.e.*, $\Delta V_{T,(n)}$) [54].

3.1.3 Regular Pulse Voltage Stress

Dependence on Frequency

In a period of unipolar pulse gate stress voltage applied to a-Si:H TFT, there are two phases: stress phase (*i.e.*, $V_{GS} \neq 0$ V) and relaxation phase (*i.e.*, $V_{GS} = 0$ V). The duration of stress

phase is pulse width. The ratio of the duration of stress phase to that of relaxation phase is duty ratio. For a given duty ratio, pulse width is inversely proportional to frequency. The dependence of the ΔV_T of a-Si:H TFT on frequency depends on the polarity of pulse gate stress voltage [38, 60]. If a-Si:T TFT is stressed by a positive pulse gate voltage, only if frequency is not too high, ΔV_T is essentially independent from frequency [38, 60]. In contrast, if it is stressed by a negative pulse gate voltage, $|\Delta V_T|$ decreases when frequency is increased, and vanishes when frequency is high enough [38].

The frequency-dependence of ΔV_T is due to RC-delay effect [38, 60]. This is because $|\Delta V_T|$ depends on the density of mobile charge in channel, and charging/discharging channel is not instantaneous. RC-delay effect can be modeled by an equivalent circuit proposed in [38], which yields the formula of the voltage across gate dielectric in stress phase:

$$V_i = V_G \left[1 - \frac{C_i}{C_s + C_i} \cdot \exp\left(\frac{-t}{\tau_{RC}} \right) \right], \tag{3.15}$$

where τ_{RC} is time constant:

$$\tau_{RC} = R_S \left(C_S + C_i \right), \tag{3.16}$$

V_G is gate voltage, C_i is gate dielectric capacitance, C_S and R_S are the capacitance and resistance between source and a-Si:H/a-SiN$_x$:H interface, and t is time [38].

When a positive pulse gate voltage is applied to a-Si:H TFT, since (1) contacts operate as ohmic resistors with relatively low resistance and (2) channel is formed and therefore its resistance is relatively low, R_S is small. Therefore, τ_{RC} is small (*e.g.*, τ_{RC} is around 1 μs for channel length 10 μm [38]), and electrons can rapidly charge/discharge channel. Only if frequency is not too high (*e.g.* below 100 kHz [60]) and duty ratio is not too small, the internal stress voltage across gate dielectric (*i.e.*, V_i) is approximately equal to external stress voltage (*i.e.*, V_G), so the density of electrons accumulated at a-Si:H/a-SiN$_x$:H interface in stress phase is not significantly dependent on pulse width. Therefore, ΔV_T is approximately independent from frequency [38, 60].

When a negative gate voltage is applied to a-Si:H TFT in stress phase, holes are attracted from contacts to channel. However, it is hard to collect holes from n$^+$ nc-Si contacts. Contacts act like reverse-biased diodes [17], preventing holes from rapidly charging channel. Therefore, in stress phase, the magnitude of V_i is much smaller than that of V_G. R_S is large, so is τ_{RC} (*e.g.*, τ_{RC} is on the order of 10^{-2} s in [38]). For a given duty ratio, when frequency is higher than a certain level (*e.g.* tens Hz in [38, 60]), pulse width is too short for enough holes to be collected at a-Si:H/a-SiN$_x$:H interface to cause a significant ΔV_T. In contrast, in relaxation phase, gate stress voltage is removed, and holes leave from

channel. In this case, it is easy to collect electrons from n^+ nc-Si layer. Contacts act like forwarded-biased diodes, allowing holes to rapidly leave from channel, so ΔV_T mechanism rapidly stops. Therefore, when a-Si:H TFT is stressed by a negative pulse gate voltage, it is hard for holes to enter channel to cause ΔV_T in stress phase, but easy to for them to leave from channel to stop ΔV_T in relaxation phase. As a result, a higher frequency (*i.e.*, short pulse width) leads to a smaller $|\Delta V_T|$.

Dependence on Duty Ratio

Under pulse voltage stress, the dependence of ΔV_T on duty-ratio is another important factor. For a given frequency, a smaller duty ratio results in a smaller ΔV_T because of (1) a shorter stress phase and therefore less time for $|\Delta V_T|$ to increase, and (2) a longer relaxation phase for ΔV_T to recover back toward zero [38, 61].

ΔV_T Model under Regular Pulse Voltage Stress

The ΔV_T of the a-Si:H TFT stressed by a bipolar pulse gate voltage is modeled in [50]:

$$\Delta V_T(t) = \Delta V_T^+ + \Delta V_T^- = \Delta V_T^+ - |\Delta V_T^-| \tag{3.17}$$

$$\begin{aligned} &= \left|V_{GS}^+ - V_T^{init}\right|^{\alpha_{st}^+} \left\{1 - \exp\left[-\left(\frac{t \cdot DR}{\tau_{st}^+}\right)^{\beta_{st}^+}\right]\right\} \cdot f^+(V_{DS}) \\ &- \left|V_{GS}^- - V_T^{init}\right|^{\alpha_{st}^-} \left\{1 - \exp\left[-\left(\frac{t \cdot (1-DR)}{\tau_{st}^-}\right)^{\beta_{st}^-}\right]\right\} \cdot f^-(V_{DS}) \cdot F_{PW}, \end{aligned} \tag{3.18}$$

where $\Delta V_T^{+(-)}$ is the ΔV_T under positive (negative) gate stress voltage, $V_{GS}^{+(-)}$ is the positive (negative) level of gate pulse voltage, t is total stress time, DR is the duty ratio of gate pulse voltage, $(t \cdot DR)$ is the effective stress time of above-threshold gate voltage, $t \cdot (1 - DR)$ is the effective stress time of negative gate voltage, and the minus between ΔV_T^+ and $|\Delta V_T^-|$ reflects the fact that V_T shifts in opposite directions under positive and negative gate stress voltages. Besides, $f^+(V_{DS})$ describes the dependence of ΔV_T^+ on V_{DS}:

$$f^+(V_{DS}) = \frac{2}{3} \cdot \frac{\left(V_{GS}^+ - V_T^{init}\right)^3 - \left(V_{GS}^+ - V_{DS} - V_T^{init}\right)^3}{\left(V_{GS}^+ - V_T^{init}\right)^2 - \left(V_{GS}^+ - V_{DS} - V_T^{init}\right)^2} \cdot \frac{1}{\left(V_{GS}^+ - V_T^{init}\right)}, \tag{3.19}$$

$f^-(V_{DS})$ describes the dependence of ΔV_T^- on V_{DS}:

$$f^-(V_{DS}) = 1 + \frac{V_{DS}}{2 \cdot \left(V_T^{init} - V_{GS}^-\right)}, \tag{3.20}$$

and F_{PW} describes the dependence of ΔV_T^- on pulse width PW:

$$F_{PW} = 1 - \frac{\tau_{RC}}{PW} + \frac{\tau_{RC}}{PW} \exp\left(-\frac{PW}{\tau_{RC}}\right). \tag{3.21}$$

Eq. (3.21) is based on the RC-delay model at Eq. (3.15) and (3.16) [38].

To take into account the recovery of ΔV_T when gate voltage is zero (*i.e.*, in relaxation phase), another modified stretched exponential model to describe ΔV_T is presented in [61]

$$\Delta V_T(t) = \left(V_{eff} - V_T^{init}\right)\left\{1 - \exp\left[-\left(\frac{t}{\tau_{st}}\right)^{\beta_{st}}\right]\right\}. \tag{3.22}$$

In this modified model, V_{GS} is replaced by V_{eff}. When total stress time is long enough, in a cycle of pulse gate voltage, the increase of V_T in stress phase is canceled by the decrease of V_T in relaxation phase, so V_T saturates at $V_{eff} = V_T^{sat} = (V_T^{init} + \Delta V_T^{sat})$. Defining T_1 and T_2 as the durations of stress phase and relaxation phase, respectively:

$$T_1 = 1/f \cdot DR, \tag{3.23}$$

$$T_2 = 1/f \cdot (1 - DR), \tag{3.24}$$

where f is the frequency of pulse gate voltage, the formula of ΔV_T^{sat} is derived in [61]:

$$\frac{\Delta V_T^{sat}}{V_{GS} - V_T^{init}} = \frac{T_1^{\beta_1}}{T_1^{\beta_1} + kT_2^{\beta_2}}, \tag{3.25}$$

where k, β_1, and β_2, are empirical parameters. Eq. (3.22) and (3.25) can be used together to describe the dependence of ΔV_T on the duty ratio of pulse gate stress voltage.

3.1.4 Variable Voltage Stress

In large signal operations (*e.g.* in AMOLED display), V_{GS} and V_{DS} of a TFT may vary over time. The authors of [51] developed a method to estimate ΔV_T under variable voltage stress. In this method, a parameter Age is defined as a linear function of stress time. Then, the increment of Age is calculated by using the following formula:

$$\Delta Age(\Delta t_i) = \int_{t_{i-1}}^{t_i} A^{1/\beta} \exp(-E_A/\beta kT) \left|V_{GS} - \eta V_{DS} - V_T^{init}\right|^{\alpha/\beta} dt, \tag{3.26}$$

where V_{GS} and V_{DS} are assumed as constant during $\Delta t_i = t_i - t_{i-1}$. Then, the values of ΔAge are summed together to obtain the total Age at the end of the stress time t_{stop}:

$$Age\left(t_{stop}\right) = \sum_{i=0}^{N} \Delta Age\left(\Delta t_i\right). \tag{3.27}$$

Finally, Age and ΔV_T are extrapolated to estimate the ΔV_T at a user-specified time (t_{age}):

$$\Delta V_T\left(t_{age}\right) = \left[\frac{t_{age}}{t_{stop}}\ Age\left(t_{stop}\right)\ \right]^{\beta}. \tag{3.28}$$

3.1.5 Summary of Conventional ΔV_T Models

Several conventional ΔV_T models of a-Si:H TFT for different stress conditions are reviewed in this section. However, these models are not suitable for circuit-level ΔV_T simulation:

- Some ΔV_T models can be used only for constant stress voltage. However, this stress condition may not be the case for practical circuits, because the ΔV_T of the TFTs in the circuit may change the stress conditions of those TFTs.

- When stress time goes to infinity, the ΔV_T of the TFT stressed by a constant V_{GS} eventually saturates at a constant level. However, some ΔV_T models assume a power-law or logarithmic dependence on stress time, so they predict that ΔV_T eventually goes to infinity. Therefore, they are not suitable for long-term ΔV_T estimation.

- Conventional ΔV_T models for pulse voltage stress assume that the magnitude, frequency, and duty ratio of pulse voltage are all fixed for the entire stress time. However, in a circuit, the ΔV_T of TFTs may cause the variations of the magnitude, frequency, and/or duty ratio of the stress voltages of the TFTs in the circuit, so those ΔV_T models may not be suitable for the simulation of ΔV_T in a circuit.

- The accuracy and computational cost of transient simulation depend on the size of time step. If voltage varies fast, time step should be smaller to guarantee simulation accuracy. If it varies slowly, time step should be larger to reduce computational cost. Modern commercial circuit simulators (*e.g.*, Cadence® Spectre®) can automatically adjust time step for an appropriate trade-off between accuracy and computational cost, so ΔV_T model should be made compatible to such a kind of circuit simulators.

- To maximize the applicability of the method of circuit-level ΔV_T simulation, the method should be based on a widely accepted physics-based ΔV_T model. Therefore, stretched exponential ΔV_T model should be used as the basis of ΔV_T simulation.

3.2 Circuit-Level ΔV_T Simulation

In this research, considering the aspects listed in section 3.1.5, differential equations of ΔV_T were derived and implemented in a model file of a-Si:H TFT, which was used with a circuit simulator to simulate the ΔV_T of a-Si:H TFT by using transient simulation.

3.2.1 Channel RC-Delay Effect

If external stress voltage varies so slow that the charge in the channel of a-Si:H TFT can fully follow up, external stress voltage is fully applied across gate dielectric, so the dV_T/dt at an arbitrary time instant can be calculated by directly using the formulas derived from the ΔV_T model for constant stress voltage. However, if external stress voltage varies so fast that channel charge can not fully follow up, the delay inside TFT affects ΔV_T.

The delay of the response of channel charge can be modeled by using a simple RC circuit illustrated in Figure 3.2(a) [38]. It describes the electron/hole accumulation/removal in channel. The channel charge on source side when TFT is ON is discussed as follows. The one on drain side can be analyzed in the same way. $R_{S,tot}$ is the total resistance from source terminal to a-Si:H/a-SiN$_x$:H interface. If TFT is ON, contact region acts like an ohmic resistor, and $R_{S,tot} = R_{S,tot}^{\mathrm{ON}}$. C_i^S and C_{Si}^S are the capacitances across dielectric and a-Si:H, respectively, on source side. The following differential equation was derived for V_i^S:

$$\frac{dV_i^S}{dt} = \frac{V_{GS} - V_i^S}{R_{S,tot}^{\mathrm{ON}}\left(C_i^S + C_{Si}^S\right)}. \tag{3.29}$$

When V_{GS} varies, at an arbitrary time instant t, the net charge at a-Si:H/a-SiN$_x$:H interface on source side ($i.e.$, on node A in Figure 3.2(a)) is

$$Q_A = -C_i^S V_i^S + C_{Si}^S\left(V_{GS} - V_i^S\right). \tag{3.30}$$

If V_{GS} is constant and equal to $\left(-Q_A/C_i^S\right)$, $V_{Si}^S = 0$ V, $V_i^S = V_{GS}$, so the net charge on node A is also Q_A. Therefore, the net charge on node A induced by variable V_{GS} is the same to the one induced by constant $V_{GS} = -Q_A/C_i^S$. So, V_{GS}^{eff} is defined so that

$$C_i^S V_{GS}^{eff} = -Q_A = C_i^S V_i^S - C_{Si}^S\left(V_{GS} - V_i^S\right). \tag{3.31}$$

Substituting the expression of V_i^S derived from Eq. (3.31) into (3.29) yields the differential equation to describe the dependence of V_{GS}^{eff} on V_{GS}

$$\frac{dV_{GS}^{eff}}{dt} \approx \frac{V_{GS} - V_{GS}^{eff}}{R_{S,tot}^{\mathrm{ON}}\left(C_i^S + C_{Si}^S\right)}. \tag{3.32}$$

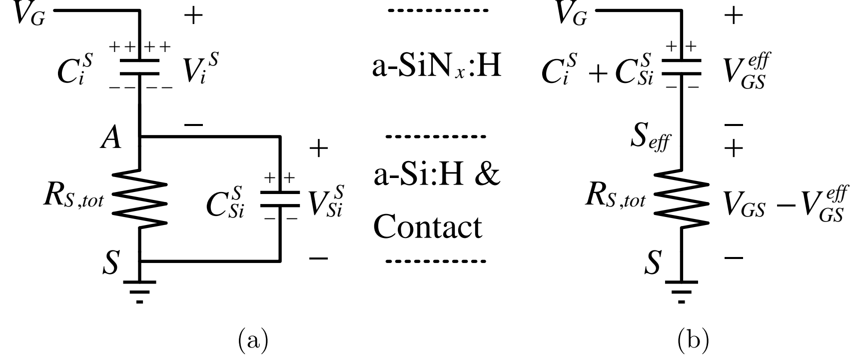


Figure 3.2: Model the influence of RC-delay (source side) on ΔV_T: (a) equivalent circuit and (b) simplified circuit.

Eq. (3.32) is valid when $V_{GS}^{eff} \geqslant V_T$. Note that $C_{Si}^S \ll C_i^S$ is assumed for simplicity when deriving Eq. (3.32). The equivalent circuit of Eq. (3.32) is shown in Figure 3.2(b).

The RC-delay effect when TFT is OFF is modeled in a similar way. Note that the behavior of contact region when TFT is OFF depends on the direction of transient current [17]. If transient current is flowing from contact to channel, contact acts like a reversely-biased diode, so $R_{S,tot}^{\text{OFF,rvs}}$ is relatively large. On contrary, if transient current is leaving from channel to contact, contact acts like a forwarded-biased diode, so $R_{S,tot}^{\text{OFF,fwd}}$ is relatively small. Therefore, the values of $R_{S,tot}$ for these two cases are significantly different.

The above discussions and formulas for different conditions are summarized as follows:

$$\frac{dV_{GS}^{eff}}{dt} \approx \frac{V_{GS} - V_{GS}^{eff}}{\tau_S}, \tag{3.33}$$

where

$$\tau_S = R_{S,tot}\left(C_i^S + C_{Si}^S\right) \tag{3.34}$$

and

$$R_{S,tot} = \begin{cases} R_{S,tot}^{\text{ON}} & V_{GS}^{eff} \geqslant V_T, \\ R_{S,tot}^{\text{OFF,rvs}} & V_{GS}^{eff} \leqslant V_T \text{ and } V_{GS} < V_{GS}^{eff}, \\ R_{S,tot}^{\text{OFF,fwd}} & V_{GS}^{eff} \leqslant V_T \text{ and } V_{GS} > V_{GS}^{eff}. \end{cases} \tag{3.35}$$

Note that $R_{S,tot}^{\text{OFF,fwd}} \ll R_{S,tot}^{\text{OFF,rvs}}$, because the equivalent resistance of a diode when it is forward-biased is much smaller than that when it is reverse-biased. In other words, when

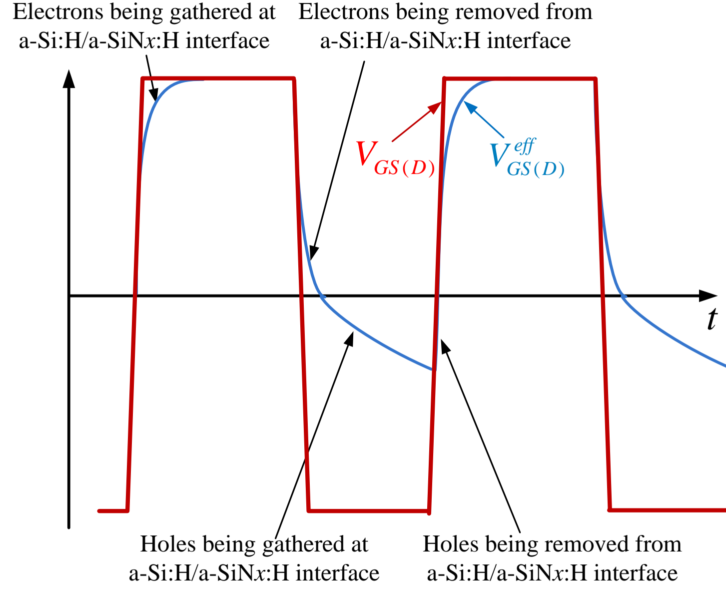


Figure 3.3: Bipolar pulse $V_{GS(D)}$ (red curve) and $V^{eff}_{GS(D)}$ (blue curve).

TFT is OFF, removing holes from channel is much easier than gathering them into channel. Figure 3.3 shows V_{GS} and V^{eff}_{GS} modeled by Eq. (3.33)-(3.35) when electrons/holes are being gathered/removed at a-Si:H/a-SiN$_x$:H interface.

The same model of RC-delay effect can be built on drain side:

$$\frac{dV^{eff}_{GD}}{dt} \approx \frac{V_{GD} - V^{eff}_{GD}}{\tau_D}, \tag{3.36}$$

where

$$\tau_D = R_{D,tot}\left(C^D_i + C^D_{Si}\right) \tag{3.37}$$

and

$$R_{D,tot} = \begin{cases} R^{\mathrm{ON}}_{D,tot} & V^{eff}_{GD} \geqslant V_T, \\ R^{\mathrm{OFF,rvs}}_{D,tot} & V^{eff}_{GD} \leqslant V_T \text{ and } V_{GD} < V^{eff}_{GD}, \\ R^{\mathrm{OFF,fwd}}_{D,tot} & V^{eff}_{GD} \leqslant V_T \text{ and } V_{GD} > V^{eff}_{GD}. \end{cases} \tag{3.38}$$

In short, given $V_{GS}(t)$, $V_{GD}(t)$, and parameter values, Eq. (3.33)-(3.38) are used to calculate $V^{eff}_{GS}(t)$ and $V^{eff}_{GD}(t)$, which are used in ΔV_T simulation.

3.2.2 Definitions of Stress Voltage

To take RC-delay into account, V_{GS}^{eff} and V_{GD}^{eff}, instead of V_{GS} and V_{GD}, are used in ΔV_T simulation. If condition $V_{GD}^{eff} \leqslant V_{GS}^{eff}$ is not satisfied, the values of V_{GS}^{eff} and V_{GD}^{eff} are interchanged before being used in ΔV_T simulation. For the convenience of the discussions in following sections, V_{st} is defined as

$$V_{st}(t) = \begin{cases} V_{GS}^{eff}(t), & V_{GS}^{eff} > \max\{V_T(t), V_T^{init}\}, \\ \left[V_{GS}^{eff}(t) + V_{GD}^{eff}(t)\right] \Big/ 2, & V_{GS}^{eff} \leqslant \max\{V_T(t), V_T^{init}\}. \end{cases} \tag{3.39}$$

Note that $V_{st} = (V_{GS}^{eff} + V_{GD}^{eff})/2$ is a simplistic approximation adapted from [50]. A device-physics-based ΔV_T model for $V_{GS}^{eff} \neq V_{GD}^{eff}$ when TFT is OFF is unavailable from literatures. However, simulation convergence requires a ΔV_T model to be defined for this condition. Since this research was focused on the simulation method instead of physical model of ΔV_T, that simplistic approximation of V_{st} adapted from [50] is used in Eq. (3.39).

3.2.3 Above-Threshold Gate Voltage Stress

When a-Si:H TFT is stressed by a low/medium gate voltage, defect creation/removal is dominant ΔV_T mechanism. It can be described by stretched exponential model (Eq. (3.1)) or power-law model (Eq. (3.2) or (3.3)). When stress time goes to infinity, all electrons in channel are trapped in defect states. Since no mobile electron remains in channel, no more defect is created, and ΔV_T saturates at $(V_{GS} - V_T^{init})$. Stretched exponential model is consistent to this trend. In contrast, power-law model predicts that ΔV_T goes to infinity. Since the prediction of stretched exponential model is more reasonable, it was used to derive the differential equations for ΔV_T simulation.

The following formulas were derived based on Eq. (3.1), (3.5)-(3.7), and (3.10) for the ΔV_T of the a-Si:H TFT stressed in above-threshold region:

$$\Delta V_T(t) = \left(V_{st} - V_T^{init}\right) \left\{1 - \exp\left[-\left(\frac{t}{\tau_{st}^{+}}\right)^{\beta_{st}^{+}}\right]\right\} \frac{Q_G}{Q_{G,0}}, \tag{3.40}$$

where

$$\tau_{st}^{+} = K_{st}^{+} \left|V_{st} - V_T^{init}\right|^{\frac{1-\alpha_{st}^{+}}{\beta_{st}^{+}}}, \tag{3.41}$$

$$\frac{Q_G}{Q_{G,0}} = \begin{cases} 1, & V_{GD}^{eff} = V_{st}; \\ \frac{2}{3} \cdot \frac{\left(V_{st}-V_T^{init}\right)^3-\left(V_{GD}^{eff}-V_T^{init}\right)^3}{\left(V_{st}-V_T^{init}\right)^2-\left(V_{GD}^{eff}-V_T^{init}\right)^2} \cdot \frac{1}{\left(V_{st}-V_T^{init}\right)}, & V_{GD}^{eff} \in [V_T^{init}, V_{st}); \\ 2/3, & V_{GD}^{eff} < V_T^{init} \end{cases} \tag{3.42}$$

describes the dependence of ΔV_T on drain voltage, and α_{st}^+, β_{st}^+, τ_{st}^+, and K_{st}^+ are the values of parameters for positive constant gate stress voltage. Differential equations of ΔV_T, which can be used by circuit simulator for ΔV_T simulation, were derived based on Eq. (3.40). As illustrated in Figure 3.4(a), assuming V_{st} switches from subthreshold region to above-threshold region (*i.e.* V_{st} crosses $\max\{V_T(t), V_T^{init}\}$) at time instant t_{switch}, the differential equations of ΔV_T for different initial conditions at t_{switch} are presented as follows.

If $\Delta V_T(t_{switch}) \geqslant 0$ V In this case, the following equation was derived from Eq. (3.40)

$$\Delta V_T(t) = \left(V_{st} - V_T^{init}\right)\left\{1 - \exp\left[-\left(\frac{t - \left(t_{switch} - t_{st}^{eff}\right)}{\tau_{st}^+}\right)^{\beta_{st}^+}\right]\right\}\frac{Q_G}{Q_{G,0}}, \tag{3.43}$$

where t_{st}^{eff} is the t solved from Eq. (3.40) after substituting $\Delta V_T(t)$ with $\Delta V_T(t_{switch})$. Treating V_{st} and V_{GD}^{eff} as constants at time instant t, differentiating Eq. (3.43) yields

$$\frac{d\Delta V_T}{dt} = \frac{\beta_{st}^+\left[\frac{Q_G}{Q_{G,0}}\left(V_{st} - V_T^{init}\right) - \Delta V_T\right]}{\tau_{st}^+}\left|\ln\left[1 - \frac{\Delta V_T}{\left(V_{st} - V_T^{init}\right)} \cdot \frac{Q_{G,0}}{Q_G}\right]\right|^{\frac{\beta_{st}^+ - 1}{\beta_{st}^+}}, \tag{3.44}$$

whose initial condition is $\Delta V_T(t_{switch}) = V_T(t_{switch}) - V_T^{init}$.

If $\Delta V_T(t_{switch}) < 0$ V The ΔV_T model of the a-Si:H TFT stressed by above-threshold gate voltage with negative initial ΔV_T (*i.e.* $\Delta V_T(t_{switch}) < 0$ V) is unavailable from literatures. However, simulation convergence requires a ΔV_T formula to be defined for this condition. Therefore, a simplistic approximate formula was derived by extending Eq. (3.40):

$$\Delta V_T(t) = V_{T,eff}^{init} + \left(V_{st} - V_{T,eff}^{init}\right)\left\{1 - \exp\left[-\left[\frac{t - \left(t_{switch} - t_{st}^{eff}\right)}{\tau_{st}^+}\right]^{\beta_{st}^+}\right]\right\}\frac{Q_G}{Q_{G,0}} - V_T^{init}, \tag{3.45}$$

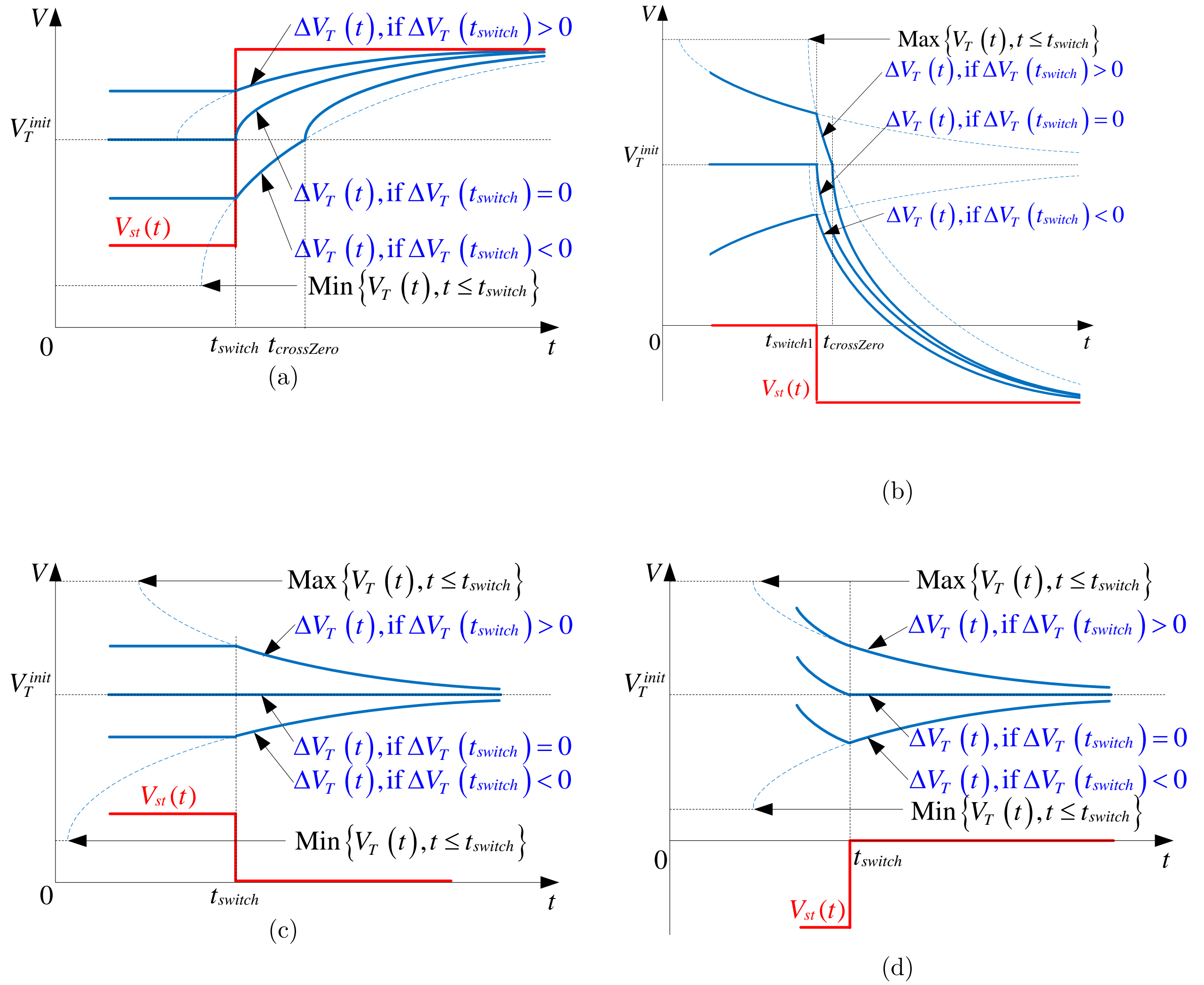


Figure 3.4: At t_{switch}, V_{st} switches from (a) subthreshold to above-threshold region; (b) zero to negative region; (c) subthreshold region to zero; (d) negative region to zero.

where $V_{T,eff}^{init} = \mathrm{Min}\left\{V_T\left(t\right), t \leqslant t_{switch}\right\}$, and t_{st}^{eff} is the t solved from

$$V_T\left(t_{switch}\right) - V_{T,eff}^{init} = \left(V_{st} - V_{T,eff}^{init}\right)\left\{1 - \exp\left[-\left(\frac{t}{\tau_{st}^{+}}\right)^{\beta_{st}^{+}}\right]\right\}\frac{Q_G}{Q_{G,0}}. \tag{3.46}$$

Treating V_{st} and V_{GD}^{eff} as constants at time instant t, differentiating Eq. (3.45) yields

$$\frac{d\Delta V_T}{dt} = \frac{\beta_{st}^{+}\left[\frac{Q_G}{Q_{G,0}}\left(V_{st} - V_{T,eff}^{init}\right) - \left(V_T - V_{T,eff}^{init}\right)\right]}{\tau_{st}^{+}}\left|\ln\left[1 - \frac{\left(V_T - V_{T,eff}^{init}\right)}{\left(V_{st} - V_{T,eff}^{init}\right)}\cdot\frac{Q_{G,0}}{Q_G}\right]\right|^{\frac{\beta_{st}^{+}-1}{\beta_{st}^{+}}}, \tag{3.47}$$

whose initial condition is $\Delta V_T\left(t_{switch}\right) = V_T\left(t_{switch}\right) - V_T^{init}$. Since TFT is stressed by an above-threshold gate voltage, ΔV_T increases and eventually comes across zero if stress time is long enough. Define $t_{crossZero}$ as the time instant at which ΔV_T increases across zero. After $t_{crossZero}$, $V_{T,eff}^{init}$ is replaced by V_T^{init}, and $d\Delta V_T/dt$ is calculated by using Eq. (3.44).

Summary Eq. (3.47) is a generalized formula of $d\Delta V_T/dt$. The values of $V_{T,eff}^{init}$ used in Eq. (3.47) for different conditions are summarized as

$$V_{T,eff}^{init} = \begin{cases} V_T^{init}, & \Delta V_T\left(t_{switch}\right) \geqslant 0 \text{ V or } t \geqslant t_{crossZero}; \\ \mathrm{Min}\left\{V_T\left(t\right), t \leqslant t_{switch}\right\}, & \Delta V_T\left(t_{switch}\right) < 0 \text{ V}. \end{cases} \tag{3.48}$$

3.2.4 Negative Gate Voltage Stress

For constant $V_{st} < 0$ V, the following equation is derived based on Eq. (3.1)

$$\Delta V_T\left(t\right) = \left(V_{st} - V_T^{init}\right)\left\{1 - \exp\left[-\left(\frac{t}{\tau_{st}^{-}}\right)^{\beta_{st}^{-}}\right]\right\}, \tag{3.49}$$

where V_{st} is defined in Eq. (3.39), time constant τ_{st}^{-} is

$$\tau_{st}^{-} = K_{st}^{-}\left|V_{st} - V_T^{init}\right|^{\frac{1-\alpha_{st}^{-}}{\beta_{st}^{-}}}, \tag{3.50}$$

and α_{st}^{-}, β_{st}^{-}, τ_{st}^{-}, and K_{st}^{-} are the values of parameters for negative constant gate stress voltage. Differential equations of ΔV_T, which can be used by circuit simulator for ΔV_T simulation, were derived based on Eq. (3.49). As illustrated in Figure 3.4(b), assuming V_{st} switches from zero to negative region at time instant t_{switch}, the formulas of ΔV_T for different initial conditions at t_{switch} are presented as follows.

If $\Delta V_T(t_{switch}) \leqslant 0$ V In this case, the following equation was derived from Eq. (3.49)

$$\Delta V_T(t) = \left(V_{st} - V_T^{init}\right)\left\{1 - \exp\left[-\left(\frac{t - \left(t_{switch} - t_{st}^{eff}\right)}{\tau_{st}^{-}}\right)^{\beta_{st}^{-}}\right]\right\}, \tag{3.51}$$

where t_{st}^{eff} is the t solved from Eq. (3.49) after substituting $\Delta V_T(t)$ with $\Delta V_T(t_{switch})$. Treating V_{st} as a constant at time instant t, differentiating Eq. (3.51) yields

$$\frac{d\Delta V_T}{dt} = \frac{\beta_{st}^{-}\left[\left(V_{st} - V_T^{init}\right) - \Delta V_T\right]}{\tau_{st}^{-}}\left|\ln\left[1 - \frac{\Delta V_T}{\left(V_{st} - V_T^{init}\right)}\right]\right|^{\frac{\beta_{st}^{-}-1}{\beta_{st}^{-}}}, \tag{3.52}$$

whose initial condition is $\Delta V_T(t_{switch}) = V_T(t_{switch}) - V_T^{init}$.

If $\Delta V_T(t_{switch}) > 0$ V The ΔV_T model of the a-Si:H TFT stressed by negative gate voltage with positive initial ΔV_T (*i.e.* $\Delta V_T(t_{switch}) > 0$ V) is unavailable from literatures. However, simulation convergence requires a ΔV_T formula to be defined for this condition. Therefore, a simplistic approximate formula was derived by extending Eq. (3.49):

$$\Delta V_T(t) = V_{T,eff}^{init} + \left(V_{st} - V_{T,eff}^{init}\right)\left\{1 - \exp\left[-\left(\frac{t - \left(t_{switch} - t_{st}^{eff}\right)}{\tau_{st}^{-}}\right)^{\beta_{st}^{-}}\right]\right\} - V_T^{init}, \tag{3.53}$$

where $V_{T,eff}^{init} = \mathrm{Max}\left\{V_T(t), t \leqslant t_{switch}\right\}$, and t_{st}^{eff} is the t solved from

$$V_T(t_{switch}) - V_{T,eff}^{init} = \left(V_{st} - V_{T,eff}^{init}\right)\left\{1 - \exp\left[-\left(\frac{t}{\tau_{st}^{-}}\right)^{\beta_{st}^{-}}\right]\right\}. \tag{3.54}$$

Treating V_{st} as a constant at time instant t, differentiating Eq. (3.53) yields

$$\frac{d\Delta V_T}{dt} = \frac{\beta_{st}^{-}\left[\left(V_{st} - V_{T,eff}^{init}\right) - \left(V_T - V_{T,eff}^{init}\right)\right]}{\tau_{st}^{-}}\left|\ln\left[1 - \frac{\left(V_T - V_{T,eff}^{init}\right)}{\left(V_{st} - V_{T,eff}^{init}\right)}\right]\right|^{\frac{\beta_{st}^{-}-1}{\beta_{st}^{-}}}, \tag{3.55}$$

whose initial condition is $\Delta V_T(t_{switch}) = V_T(t_{switch}) - V_T^{init}$. Since TFT is stressed by negative gate voltage, ΔV_T decrease and eventually come across zero if stress time is long enough. Define $t_{crossZero}$ as the time instant at which ΔV_T decreases across zero. After $t_{crossZero}$, $V_{T,eff}^{init}$ is replaced by V_T^{init}, and $d\Delta V_T/dt$ is calculated using Eq. (3.52).

Summary Eq. (3.55) is a generalized formula of $d\Delta V_T/dt$. The values of $V_{T,eff}^{init}$ used in Eq. (3.55) for different conditions are summarized as

$$V_{T,eff}^{init} = \begin{cases} V_T^{init}, & \Delta V_T\left(t_{switch}\right) \leqslant 0 \text{ V or } t \geqslant t_{crossZero}; \\ \text{Max}\left\{V_T\left(t\right), t \leqslant t_{switch}\right\}, & \Delta V_T\left(t_{switch}\right) > 0 \text{ V}. \end{cases} \tag{3.56}$$

3.2.5 Zero Gate Voltage

As illustrated in Figure 3.4(c) and 3.4(d), assume V_{st} is switched from subthreshold region or negative region to zero at t_{switch}. When V_{st} is zero, ΔV_T recovers toward zero due to the removal of defect states in a-Si:H material. Assuming eventually V_T fully comes back to V_T^{init}, *i.e.*, $V_T\left(\infty\right) = V_T^{init}$, the following formula was derived based on Eq. (3.8),

$$\Delta V_T\left(t\right) = \left(V_{T,eff}^{init} - V_T^{init}\right) \cdot \exp\left[-\left(\frac{t - \left(t_{switch} - t_{rex}^{eff}\right)}{\tau_{rex}^{+(-)}}\right)^{\beta_{rex}^{+(-)}}\right], \tag{3.57}$$

where $\beta_{rex}^{+(-)}$ and $\tau_{rex}^{+(-)}$ are relaxation parameters when $\Delta V_T\left(t_{switch}\right)$ is positive (negative). $V_{T,eff}^{init}$ is effective initial V_T before the beginning of relaxation phase, defined as

$$V_{T,eff}^{init} = \begin{cases} \text{Max}\left\{V_T\left(t\right), t \leqslant t_{switch}\right\}, & \Delta V_T\left(t_{switch}\right) > 0 \text{ V}; \\ V_T^{init}, & \Delta V_T\left(t_{switch}\right) = 0 \text{ V}; \\ \text{Min}\left\{V_T\left(t\right), t \leqslant t_{switch}\right\}, & \Delta V_T\left(t_{switch}\right) < 0 \text{ V}. \end{cases} \tag{3.58}$$

Besides, the larger ΔV_T before relaxation phase is, the faster ΔV_T recoveries toward zero in relaxation phase [61]. This dependence is described by defining a formula of $\tau_{rex}^{+(-)}$:

$$\tau_{rex}^{+(-)} = K_{rex}^{+(-)} \left|V_{T,eff}^{init} - V_T^{init}\right|^{\frac{1-\alpha_{rex}^{+(-)}}{\beta_{rex}^{+(-)}}}, \tag{3.59}$$

where $K_{rex}^{+(-)}$ and $\alpha_{rex}^{+(-)}$ are fitting parameters. t_{rex}^{eff} in Eq. (3.57) is the t solved from

$$\Delta V_T\left(t_{switch}\right) = \left(V_{T,eff}^{init} - V_T^{init}\right) \cdot \exp\left[-\left(\frac{t}{\tau_{rex}^{+(-)}}\right)^{\beta_{rex}^{+(-)}}\right]. \tag{3.60}$$

Differential equations of ΔV_T, which can be used by circuit simulator for ΔV_T simulation, were derived based on Eq. (3.57):

$$\frac{d\Delta V_T}{dt} = \begin{cases} \frac{-\beta_{rex}^{+(-)} \cdot \Delta V_T}{\tau_{rex}^{+(-)}} \left[-\ln\left(\frac{\Delta V_T}{V_{T,eff}^{init} - V_T^{init}}\right)\right]^{\frac{\beta_{rex}^{+(-)}-1}{\beta_{rex}^{+(-)}}}, & \Delta V_T\left(t_{switch}\right) \neq 0 \text{ V}, \\ 0, & \Delta V_T\left(t_{switch}\right) = 0 \text{ V}. \end{cases} \tag{3.61}$$

3.2.6 Subthreshold Gate Voltage Stress

The ΔV_T model of the a-Si:H TFT stressed by subthreshold gate voltage is unavailable from literatures. However, simulation convergence requires a ΔV_T formula to be defined for this condition. Since this research was primarily focused on the simulation method instead of physical model of ΔV_T, $d\Delta V_T/dt$ is assumed as zero in subthreshold region. In pixel circuits, TFTs are typically either not stressed in subthreshold region, or just quickly go across this region during their transitions between ON and OFF. Therefore, even if $d\Delta V_T/dt \neq 0$ in subthreshold region, it has only a minor contribution to ΔV_T.

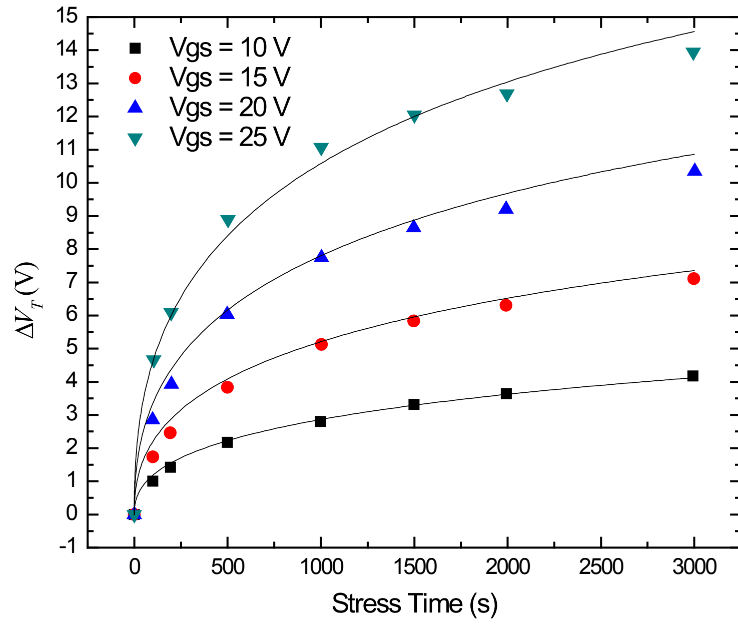
3.3 Implementation of ΔV_T Model and Simulation

Several examples are used in this section to demonstrate the applicability of the circuit-level simulation method of ΔV_T presented in section 3.2. The ΔV_T model presented in section 3.2 was implemented by using Verilog-A Hardware Description language, inserted into a Verilog-A TFT model file built by the author of [17], and run by using Cadence® Spectre® circuit simulator. The parameter values required by ΔV_T model were extracted from the measurement data obtained from literatures. The ΔV_T under various voltage stress conditions were simulated by using transient simulations. Simulation results are compared to the measurement data obtained from literatures.

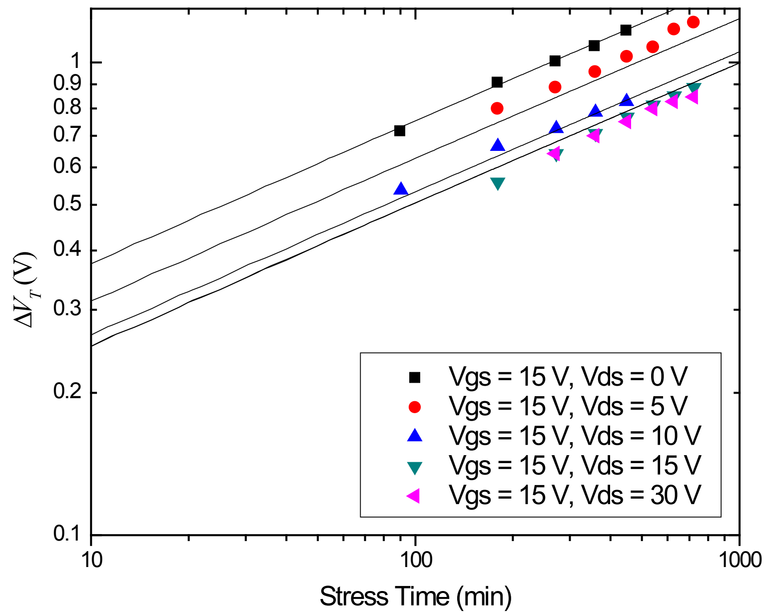
3.3.1 Above-Threshold Constant Gate Voltage Stress

Zero Drain Stress Voltage

The measurement data of the ΔV_T of the a-Si:H TFT stressed by above-threshold constant V_{GS} with $V_{DS} = 0$ V obtained from [54] are indicated as symbols in Figure 3.5(a). Since stress voltages are constant, $V_{GS}^{eff} = V_{GS}$, and $V_{GD}^{eff} = V_{GD}$. Since $V_{DS} = 0$ V, according to Eq. (3.39), $V_{st} = V_{GS}^{eff} = V_{GD}^{eff}$. Therefore, according to Eq. (3.42), $Q_G/Q_{G,0} = 1$. Parameter values can be extracted by fitting Eq. (3.40) to measurement data: $V_T^{init} = 0.942$ V, $\alpha_{st}^{+} = 1.37$, $\beta_{st}^{+} = 0.437$, and $K_{st}^{+} = 4.7 \times 10^4$ s/V$^{\left(1-\alpha_{st}^{+}\right)/\beta_{st}^{+}}$ [54]. As shown in Figure 3.5(a), simulation results (curves) match well to measurement data (symbols).



(a)



(b)

Figure 3.5: Measurement data (symbols) and simulation results (curves) of the ΔV_T of the a-Si:H TFT stressed by above-threshold constant V_{GS}. (a) $V_{DS} = 0$ V; and (b) $V_{DS} \geqslant 0$ V.

Non-Zero Drain Stress Voltage

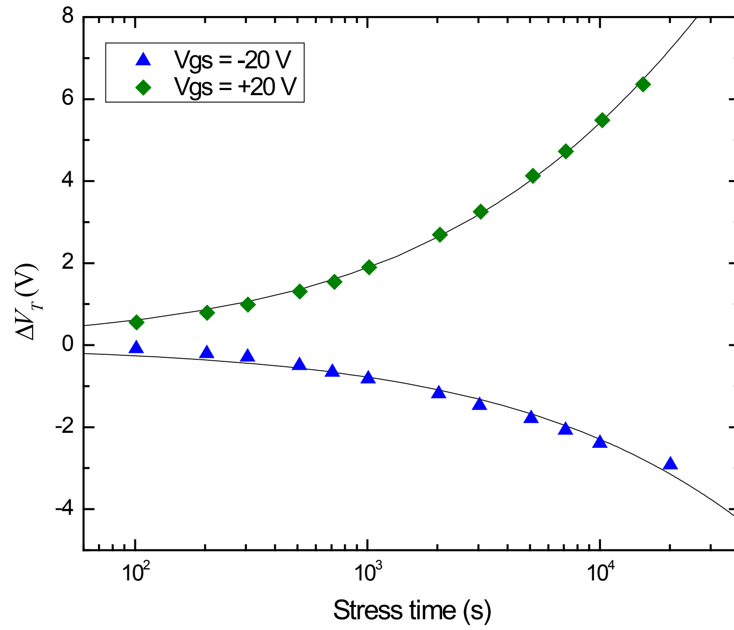
The measurement data of the ΔV_T of the a-Si:H TFT stressed by above-threshold constant V_{GS} with $V_{DS} \geqslant 0$ V obtained from [56] are indicated as symbols in Figure 3.5(b). Parameter values were extracted by fitting Eq. (3.40) to the measurement data for $V_{GS} = 15$ V and $V_{DS} = 0$ V. The extracted values of parameters are $V_T^{init} = 1.322$V, $\alpha_{st}^+ = 1.047$, $\beta_{st}^+ = 0.3084$, and $K_{st}^+ = 10^8$ s/V$^{\left(1-\alpha_{st}^+\right)/\beta_{st}^+}$. As shown in Figure 3.5(b), simulation results (curves) match well to measurement data (symbols).

3.3.2 Negative Constant Gate Voltage Stress

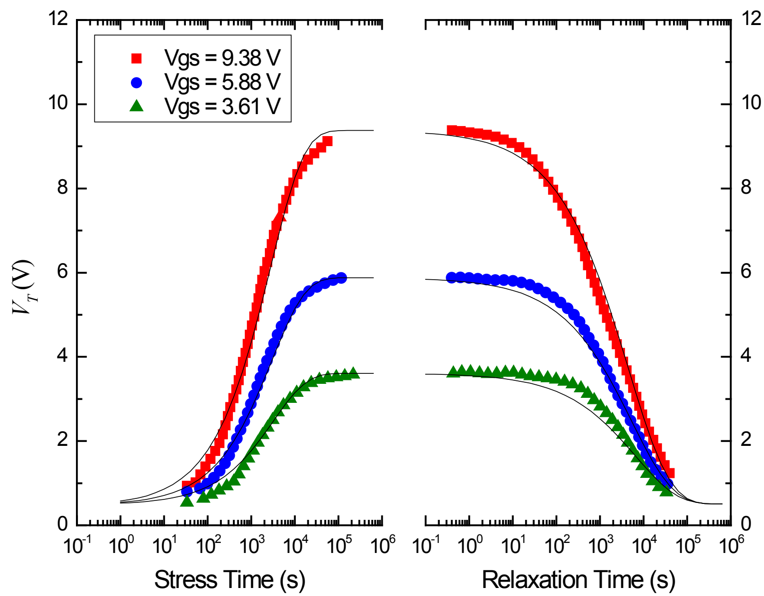
The measurement data of the ΔV_T of the a-Si:H TFT stressed by above-threshold and negative constant V_{GS} with $V_{DS} = 0$ V obtained from [38] are indicated as symbols in Figure 3.6(a). Parameter values were extracted by fitting Eq. (3.40) and (3.49) to the measurement data for positive and negative V_{GS}, respectively. V_T^{init} is 1 V [38]. The extracted values of parameters are listed as follows. For $V_{GS} = 20$ V, $\alpha_{st}^+ = 1.937$, $\beta_{st}^+ = 0.5067$, and $K_{st}^+ = 2 \times 10^7$ s/V$^{\left(1-\alpha_{st}^+\right)/\beta_{st}^+}$. For $V_{GS} = -20$ V, $\alpha_{st}^- = 2.388$, $\beta_{st}^- = 0.4856$, and $K_{st}^- = 5 \times 10^9$ s/V$^{\left(1-\alpha_{st}^-\right)/\beta_{st}^-}$. As shown in Figure 3.6(a), simulation results (curves) match well to measurement data (symbols).

3.3.3 Zero Gate Voltage

The measurement data of the ΔV_T of the a-Si:H TFT for above-threshold constant V_{GS} and then zero V_{GS} with $V_{DS} = 0$ V obtained from [59] are indicated as symbols in Figure 3.6(b). V_T^{init} is 0.5 V. The parameter values needed in the model of ΔV_T for above-threshold constant V_{GS} were extracted by fitting Eq. (3.40) to the measurement data on the left-hand side of Figure 3.6(b): $\alpha_{st}^+ = 1.077$, $\beta_{st}^+ = 0.5609$, and $K_{st}^+ = 3732$ s/V$^{\left(1-\alpha_{st}^+\right)/\beta_{st}^+}$. The parameter values needed in the model of ΔV_T for zero V_{GS} were extracted by fitting Eq. (3.57) to the measurement data on the right-hand side of Figure 3.6(b): $\alpha_{rex}^+ = 1.175$, $\beta_{rex}^+ = 0.4551$, and $K_{rex}^+ = 1.013 \times 10^4$ s/V$^{\left(1-\alpha_{rex}^+\right)/\beta_{rex}^+}$. As shown in Figure 3.6(a) and 3.6(b), simulation results (curves) match well to measurement data (symbols).

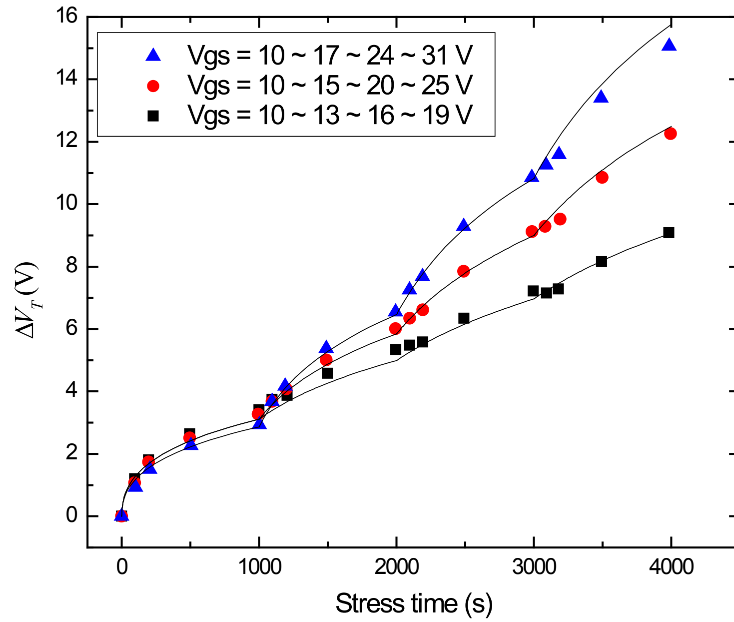


(a)

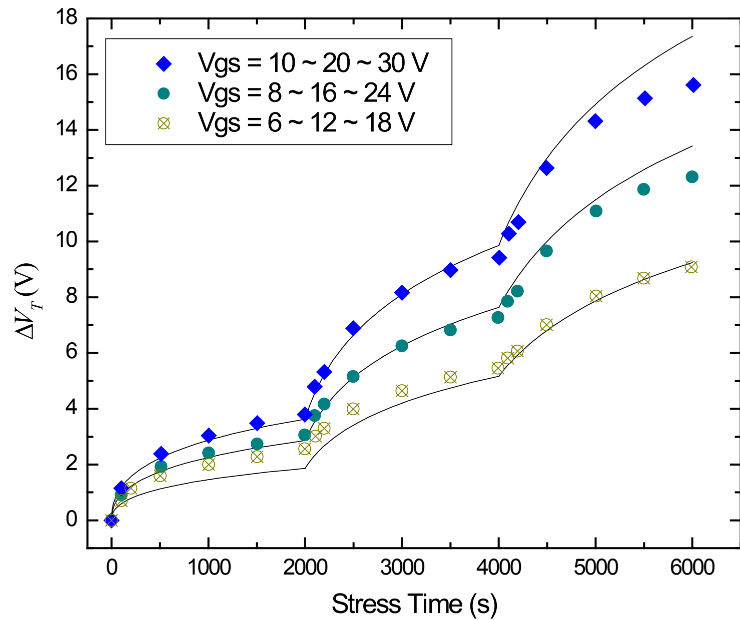


(b)

Figure 3.6: Measurement data (symbols) and simulation results (curves) of the ΔV_T of the a-Si:H TFT for: (a) above-threshold and negative constant V_{GS}; and (b) above-threshold constant (left-hand side) and then zero (right-hand side) V_{GS}.



(a)



(b)

Figure 3.7: Measurement data (symbols) and simulation results (curves) of the ΔV_T of the a-Si:H TFT stressed by above-threshold step-increasing V_{GS} with $V_{DS} = 0$ V when the duration of each stress voltage is (a) 1000 s and (b) 2000 s.

3.3.4 Step-Increasing Gate Voltage Stress

The measurement data of the ΔV_T of the a-Si:H TFT stressed by above-threshold step-increasing V_{GS} with $V_{DS} = 0$ V obtained from [54] are indicated as symbols in Figure 3.7. The parameter values extracted in section 3.3.1 are used in this section because the measurement data is from the same TFT samples used in the same literature. As shown in Figure 3.7, simulation results (curves) match well to measurement data (symbols).

3.3.5 Regular Pulse Gate Voltage Stress

Effect of Channel RC-Delay

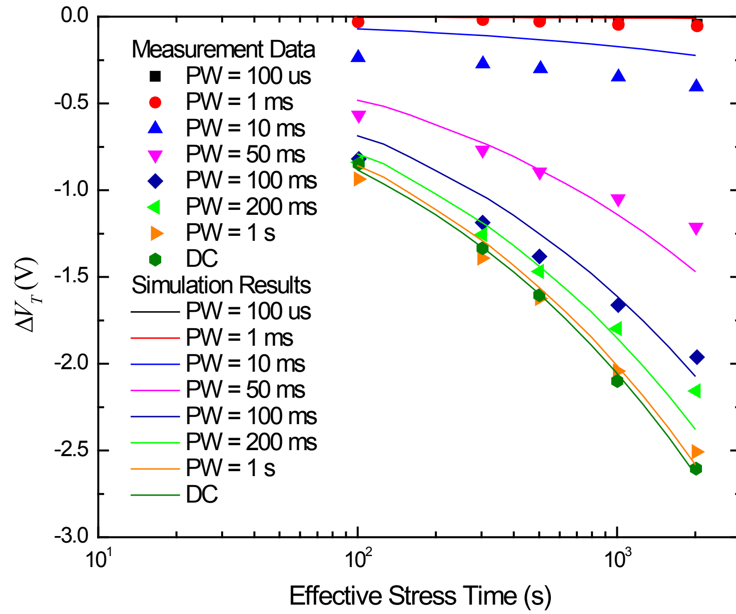
The measurement data of the ΔV_T of the a-Si:H TFT stressed by negative regular pulse V_{GS} (duty ratio is 50%) and constant V_{GS} with $V_{DS} = 0$ V obtained from [38] are indicated as symbols in Figure 3.8(a). The measurement data of the ratio of ΔV_T^{AC}, which is the ΔV_T for pulse V_{GS}, to ΔV_T^{DC}, which is the ΔV_T for constant V_{GS}, obtained from [38] is indicated as symbols in Figure 3.8(b). V_T^{init} is 1 V [38].

The swing of the negative pulse V_{GS} used in aging test was $(-20 \sim 0)$ V. The constant V_{GS} used in aging test was -20 V. The recovery of ΔV_T when V_{GS} is zero is neglected in [38], so the values of relaxation parameters (*i.e.*, α_{rex}^-, β_{rex}^-, and K_{rex}^-) are unavailable. The values of stress parameters for negative V_{GS} (*i.e.*, α_{st}^-, β_{st}^-, and K_{st}^-) were extracted by fitting Eq. (3.49) to the measurement data for constant $V_{GS} = -20$ V: $\alpha_{st}^- = 2.185$, $\beta_{st}^- = 0.3813$, and $K_{st}^- = 4.99 \times 10^9$ s/V$^{(1-\alpha_{st}^-)/\beta_{st}^-}$.

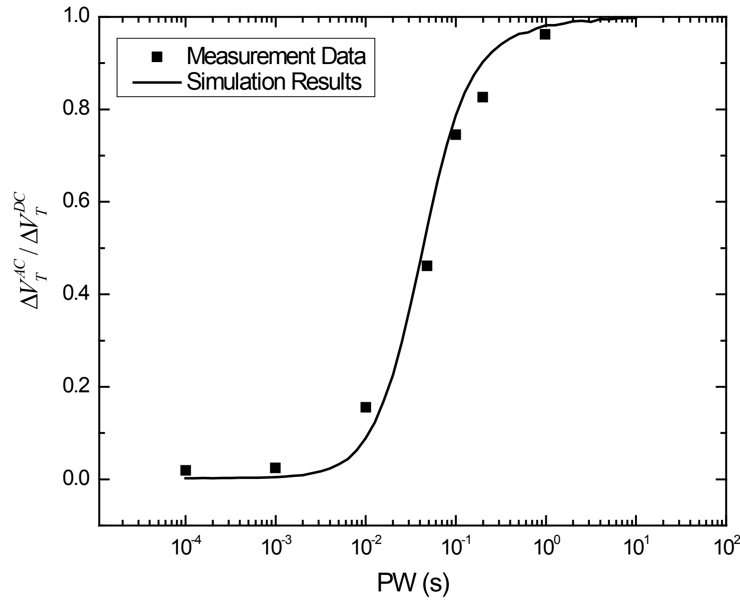
If many pulse cycles are involved in ΔV_T simulation, computational cost can be unaffordable. For the given duty ratio and total stress time, a simple technique to reduce computational cost is to use longer pulse width, so that less pulse cycles are involved in ΔV_T simulation. However, this technique has a problem. As discussed in section 3.1.3, the ΔV_T for negative pulse V_{GS} has a significant dependence on pulse width, so simply using longer pulse width may result in significant error in ΔV_T simulation. A solution of this problem is implied by Figure 3.3: if the time constant of RC-delay (*i.e.*, $\tau_{S(D)}$ in section 3.2.1) is increased proportionally with pulse width (PW), *i.e.*,

$$\tau'_{S(D)} \;/\; \tau_{S(D)} = PW' \;/\; PW, \tag{3.62}$$

the relationship between $V_{GS(D)}^{eff}$ and $V_{GS(D)}$ is not changed, so the accuracy of ΔV_T simulation is not significantly affected by the change of pulse width. In Eq. (3.62), $\tau_{S(D)}$ and PW



(a)



(b)

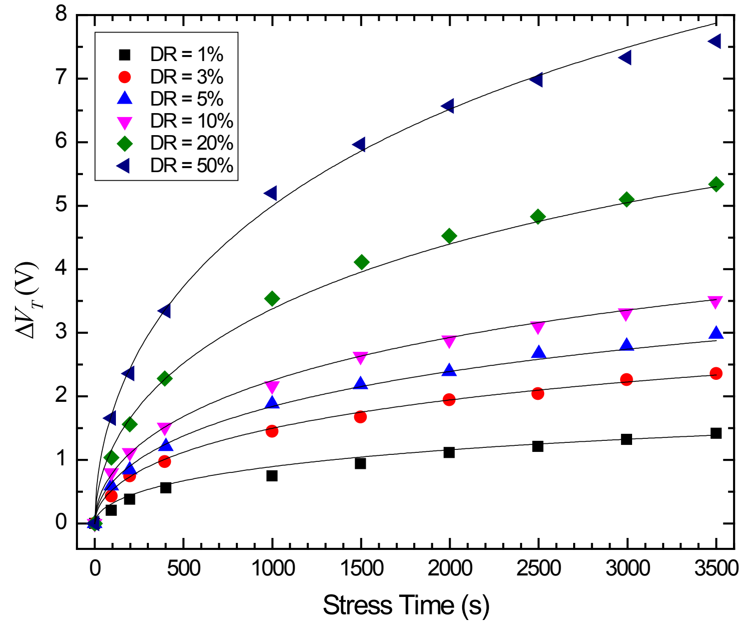
Figure 3.8: Measurement data (symbols) and simulation results of ΔV_T of the a-Si:H TFT stressed by negative pulse V_{GS} (duty ratio 50%) and constant V_{GS} with $V_{DS} = 0$ V. (a) For different effective stress time; (b) when effective stress time was 2000 s.

are original values, and $\tau'_{S(D)}$ and PW' are the changed values used in simulation. Since $V_{DS} = 0$ V, $\tau_S = \tau_D$. Denote $\tau_{S(D)}^{\text{OFF,fwd}}$ and $\tau_{S(D)}^{\text{OFF,rvs}}$ as the values of $\tau_{S(D)}$ when the equivalent diode in source (drain) contact region is forward-biased and reverse-biased, respectively. The value of $\tau_{S(D)}^{\text{OFF,rvs}}$ was extracted as 0.021 s, at which simulation results have the best fitting to measurement data. Since $R_{S(D),tot}^{\text{OFF,fwd}} \ll R_{S(D),tot}^{\text{OFF,rvs}}$, $\tau_{S(D)}^{\text{OFF,fwd}} \ll \tau_{S(D)}^{\text{OFF,rvs}}$. Therefore, for simplicity, $\tau_{S(D)}^{\text{OFF,fwd}}$ was neglected in simulation (*i.e.*, assigned with a very small value, *e.g.*, 10^{-10} s). When sweeping PW, PW' was set as 20 s, and ${\tau'}_{S(D)}^{\text{OFF,rvs}}$ was determined by using Eq. (3.62) and the extracted value of $\tau_{S(D)}^{\text{OFF,rvs}}$. As shown in Figure 3.8(a) and 3.8(b), simulation results (curves) match well to measurement data (symbols). The discrepancies between simulation results and measurement data could be attributed to the negligence of ΔV_T recovery when V_{GS} is zero, simplistic RC-delay model, approximations made in simulation, and/or measurement inaccuracy.

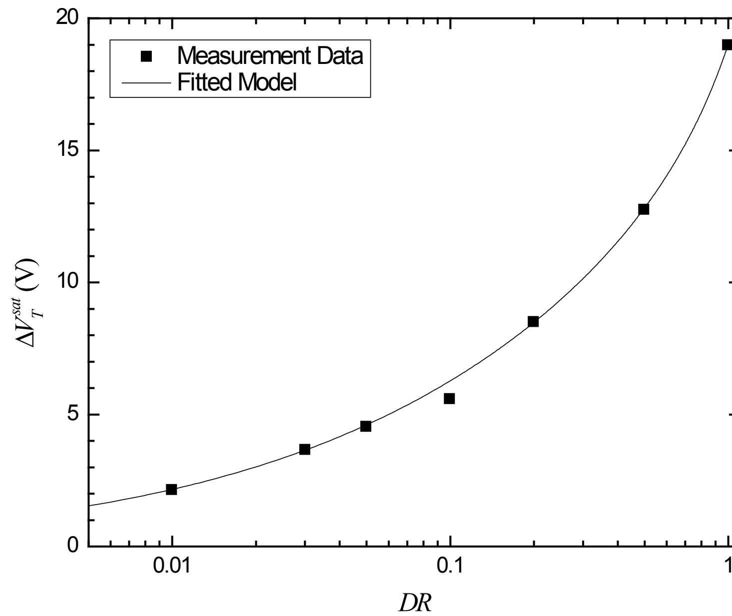
Effect of Duty Ratio

The measurement data of the ΔV_T of the a-Si:H TFT stressed by positive pulse gate voltage (60 Hz) with $V_{DS} = 0$ V and various duty ratios (DR) obtained from [61] is shown in Figure 3.9(a). V_T^{init} is 1 V. The data of saturated ΔV_T (denoted as ΔV_T^{sat}) after a long stress time for different duty ratios was extracted by the authors of [61], as shown in Figure 3.9(b). According to [61], ΔV_T under pulse gate voltage stress can be empirically described by using a modified stretched exponential model (see Eq. (3.22), where $V_{eff} = V_T^{sat}$). Therefore, by using the data of V_T^{sat} in Figure 3.9(b), Eq. (3.40) was fitted to the data in Figure 3.9(a) to extract stress parameter values: $\alpha_{st}^+ = 0.9574$, $\beta_{st}^+ = 0.526$, and $K_{st}^+ = 3086$ s/V$^{\left(1-\alpha_{st}^+\right)/\beta_{st}^+}$. The fitted model is shown as the curves in Figure 3.9(a).

In the simulation of the ΔV_T under positive pulse voltage stress, taking into account the recovery of ΔV_T in relaxation phase requires the values of relaxation parameters (*i.e.*, α_{rex}^+, β_{rex}^+ and K_{rex}^+). Unfortunately, the measurement data of the recovery of ΔV_T is not explicitly provided in [61]. Therefore, a technique was developed in this research to extract the values of relaxation parameters from the measurement data shown in Figure 3.9(b). As illustrated in Figure 3.10(a), when V_T achieves V_T^{sat}, the increase of V_T in stress phase is canceled by the decrease of V_T in relaxation phase [61]. Denote T_1 and T_2 as the durations of the stress phase and relaxation phase in a period of pulse voltage, respectively; f as the frequency of pulse voltage; and t_{st}^{eff} (illustrated in Figure 3.10(a)) as the t solved from Eq.

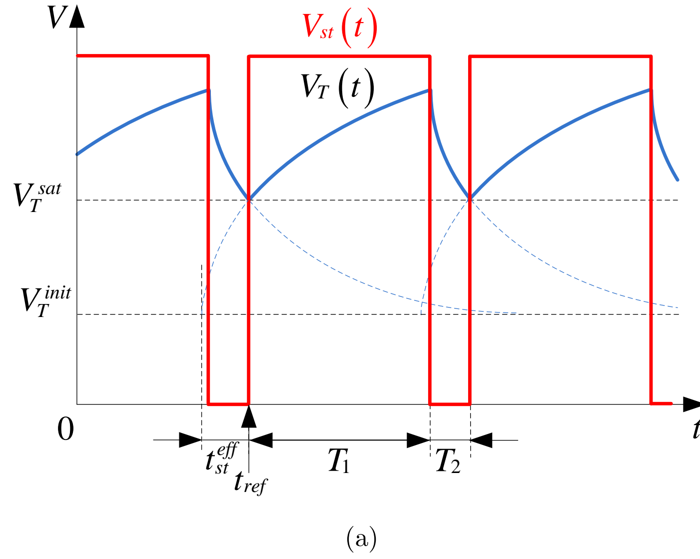


(a)

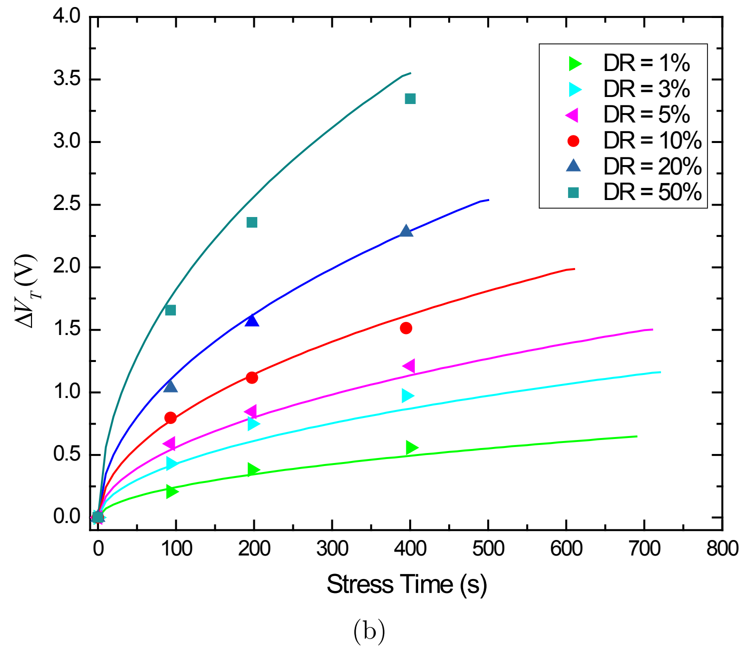


(b)

Figure 3.9: Measurement data (symbols) and models (curves) of (a) the ΔV_T of the a-Si:H TFT stressed by positive pulse gate voltages ($V_{DS} = 0$ V); (b) ΔV_T^{sat} *vs.* duty ratio (DR).



(a)



(b)

Figure 3.10: (a) After total stress time is long enough, the increase of V_T in stress phase (T_1) is canceled by the decrease of V_T in relaxation phase (T_2), so V_T saturates at V_T^{sat}. (b) Measurement data (symbols) and simulation results (curves) of the ΔV_T under positive pulse gate voltage stress with different duty ratios (DR) ($V_{DS} = 0$ V).

(3.40) after ΔV_T is substituted by ΔV_T^{sat}:

$$t_{st}^{eff} = \tau_{st}^{+} \left\{ -\ln \left[1 - \frac{\Delta V_T^{sat}}{V_{st} - V_T^{init}} \right] \right\}^{\frac{1}{\beta_{st}^{+}}}, \tag{3.63}$$

where τ_{st}^{+} is defined in Eq. (3.41). Based on Figure 3.10(a), Eq. (3.8) yields

$$\exp \left[-\left(\frac{T_2}{\tau_{rex}^{+}} \right)^{\beta_{rex}^{+}} \right] = \frac{\Delta V_T \left(t_{ref} \right)}{\Delta V_T \left(t_{ref} + T_1 \right)}, \tag{3.64}$$

where T_1 and T_2 are defined in Eq. (3.23) and (3.24), respectively;

$$\tau_{rex}^{+} = K_{rex}^{+} \left[\; \Delta V_T \left(t_{ref} + T_1 \right) \; \right]^{\frac{1-\alpha_{rex}^{+}}{\beta_{rex}^{+}}} \tag{3.65}$$

was derived from Eq. (3.59);

$$\Delta V_T \left(t_{ref} \right) = \Delta V_T^{sat}, \tag{3.66}$$

is indicated in Figure 3.10(a); and

$$\Delta V_T \left(t_{ref} + T_1 \right) = \left(V_{st} - V_T^{init} \right) \left\{ 1 - \exp \left[-\left(\frac{t_{st}^{eff} + T_1}{\tau_{st}^{+}} \right)^{\beta_{st}^{+}} \right] \right\}, \tag{3.67}$$

was derived from Eq. (3.43). Eq. (3.63)-(3.67) define an implicit function of ΔV_T^{sat} *vs.* DR with unknown relaxation parameters α_{rex}^{+}, β_{rex}^{+} and K_{rex}^{+}. To extract the values of relaxation parameters, this implicit function was fitted to the data of ΔV_T^{sat} *vs.* DR shown in Figure 3.9(b). The fitted model is indicated as the curve in Figure 3.9(b). Extracted parameter values are $\alpha_{rex}^{+} = 0.99972$, $\beta_{rex}^{+} = 1.2899$ and $K_{rex}^{+} = 654.55$ s/V$^{\left(1-\alpha_{rex}^{+}\right)/\beta_{rex}^{+}}$. By using the extracted values of stress and relaxation parameters, ΔV_T was simulated by using the formulas derived in section 3.2 under the same stress condition as in [61]. Since RC-delay effect does not have significant impact on ΔV_T when a-Si:H TFT is stressed by a positive pulse gate voltage with low frequency (*e.g.*, 60 Hz) (refer to [38,60] and section 3.1.3), it was neglected in simulation for simplicity. As shown in Figure 3.10(b), simulation results match well to the measurement data obtained from [61].

3.4 Summary

A circuit-level ΔV_T simulation method and a ΔV_T model which is compatible to a circuit simulator are presented in this chapter. The contributions made in this research are summarized as follows. (1) The differential equations required by the transient ΔV_T simulation for various voltage stress conditions were derived. (2) The impact of the finite response speed of a-Si:H TFT on ΔV_T is taken into account. (3) The derived differential equations and formulas were implemented by using Verilog-A Hardware Description Language into a compact device model file of a-Si:H TFT. (4) By using the device model file and Cadence® Spectre® circuit simulator, the ΔV_T under various voltage stress conditions were simulated. (5) The effectiveness of the proposed simulation method is verified by the measurement data obtained from literatures. The relative errors between simulation results and measurement data are typically less than 10%.

Chapter 4

Pixel Circuits to Improve Performance Stability of AMOLED Displays

Improving the performance stability of AMOLED displays requires the novel pixel circuits designed to compensate the impact of TFT aging on circuit performance. In this research, a novel voltage-programmed pixel circuit using a-Si:H TFTs was developed for AMOLED displays. To improve the stability of OLED current, the threshold voltage shift (ΔV_T) of drive TFT caused by voltage stress is compensated by an incremental gate-to-source voltage (ΔV_{GS}) generated by utilizing the ΔV_T-dependent charge transfer from drive TFT to a TFT-based Metal-Insulator-Semiconductor (MIS) capacitor. A second MIS capacitor is used to inject positive charge to the gate of drive TFT to improve OLED drive current. Besides, the non-ideality of ΔV_T-compensation, TFT overlap capacitance, programming speed, and OLED aging are discussed. The effectiveness of the proposed pixel circuit is verified by simulation and measurement results. The proposed pixel circuit is also compared to conventional voltage-programmed and current-programmed pixel circuits.

4.1 Introduction

The schematic and driving scheme of a conventional 2-TFT pixel circuit, which is the simplest pixel circuit of AMOLED displays, are shown in Figure 4.1 [4]. The a-Si:H TFTs used in the pixel circuit are n-channel. The pixel circuit consists of an OLED, a drive TFT

T_0, a switch TFT T_1, and a storage capacitor C_S. V_1 is shared by all the pixels in the same row. It controls the access from external programming voltage driver V_{prog} to the internal node A in the pixel circuit. V_{prog} is shared by all the pixels in the same column.

In programming phase, T_1 is turned ON by V_1^H, so V_{prog} programs a data voltage V_{data} onto node A. In driving phase, T_1 is turned OFF by V_1^L, so node A holds its voltage. Since T_0 has to be always ON to drive OLED current, the threshold voltage of T_0 ($V_{T,0}$) increases over stress time. Since the pixel circuit does not compensate the threshold voltage shift of T_0 ($\Delta V_{T,0}$), the increase of $V_{T,0}$ results in the decrease of the I_{OLED} in driving phase (I_{OLED}^{driv}), as demonstrated in Figure 4.2. Therefore, OLED brightness degrades. To improve the stability of OLED current in driving phase, various pixel circuits and driving schemes have been proposed to compensate the ΔV_T of the drive TFT of OLED current:

- Current-programmed pixel circuits (*e.g.*, [62]) can compensate not only the ΔV_T of drive TFT but also some other variations (*e.g.*, mobility, sizing, temperature, *etc.*). However, their programming speeds are relatively slow, especially for low programming currents and/or large-size displays [4]. Besides, two TFTs in series may need to be used in OLED current path. In this case, given the same gate voltage of drive TFT, a higher power supply voltage must be used to achieve the same OLED current, resulting in a higher power consumption.

- In conventional voltage-programmed pixel circuits, V_T-generation techniques are used to generate an incremental V_{GS} to compensate the ΔV_T of drive TFT [4]. However, their programming speeds are not fast because: (1) the speeds of V_T-generation techniques are limited, and (2) multiple sub-phases may be used in programming phase to implement V_T-generation techniques. Besides, two or more TFTs are typically used in series in OLED current path, resulting in a higher power consumption. Control signals are also typically complex, complicating external driver design.

- Optical feedback using a photo-sensor in pixel [63] complicates pixel circuit design. Besides, it takes up extra pixel area, resulting in lower aperture ratio and resolution. The instability of photo-sensor and the light interference from environment and neighboring pixels may cause error in feedback loop [64].

- Although external driver compensation [65] can compensate the aging of both OLED and TFT, the design of external driver is complicated and expensive. Besides, the number of the pixels that the external driver can monitor is limited.

A voltage-programmed pixel circuit using a novel ΔV_T-compensation mechanism was developed in this research [66–68] and is presented in this chapter. The ΔV_T of drive TFT is

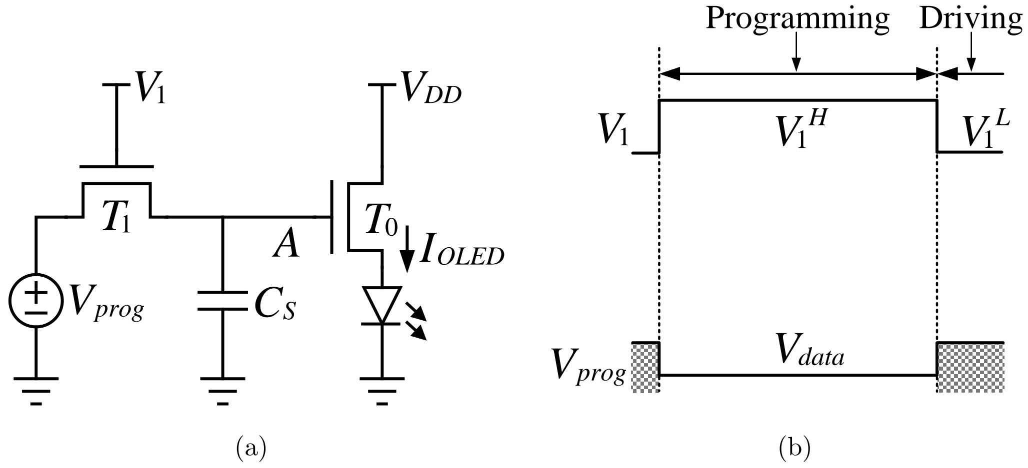


Figure 4.1: (a) Schematic and (b) driving scheme of conventional 2-TFT pixel circuit.

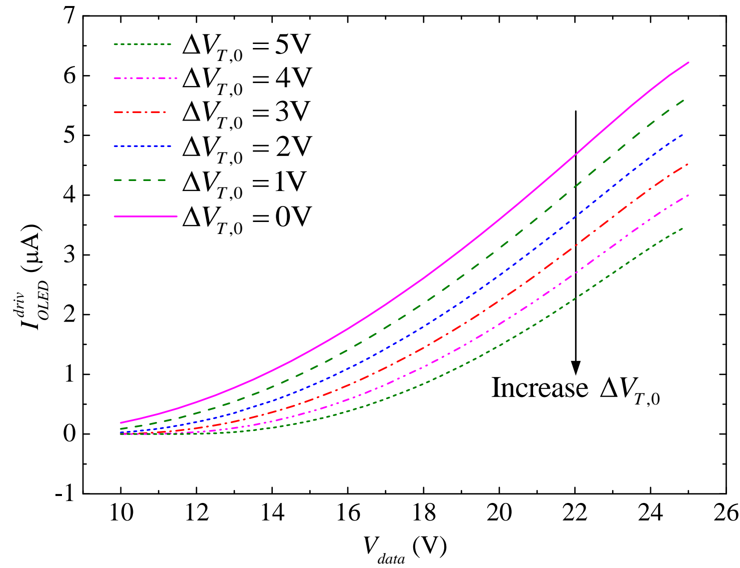


Figure 4.2: Simulated I_{OLED}^{driv} *vs.* V_{data} of a conventional 2-TFT pixel circuit [66].

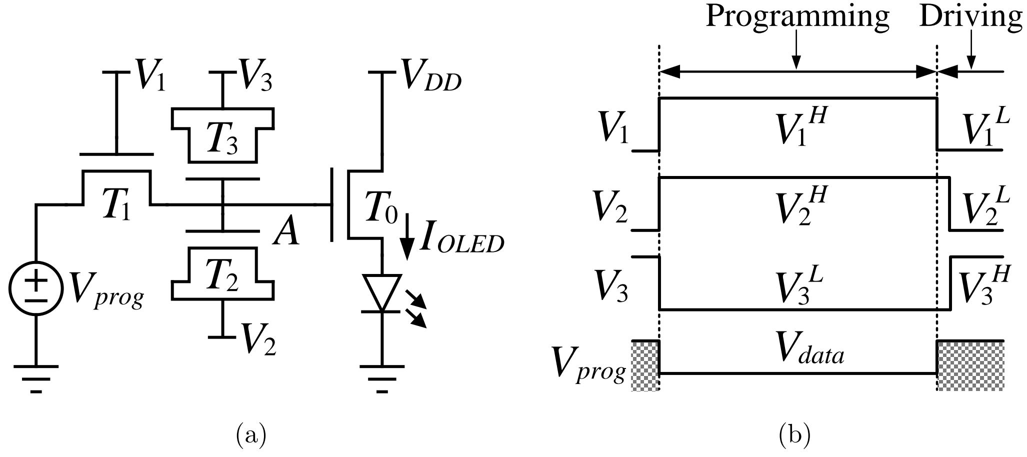


Figure 4.3: (a) Schematic and (b) driving scheme of the proposed pixel circuit [66–68].

compensated by the ΔV_{GS} generated by using a ΔV_T-dependent charge transfer from drive TFT to a TFT-based MIS capacitor. The proposed pixel circuit has a fast programming speed. Besides, only one TFT is in series with OLED, reducing power consumption. Control signals are also simple, reducing the complexity of external driver.

4.2 Pixel Circuit Structure

The proposed pixel circuit and driving scheme are shown in Figure 4.3. T_0 is drive TFT, which controls the OLED current in driving phase (I_{OLED}^{driv}). T_1 is switch TFT, which controls the access from external programming voltage driver (V_{prog}) to node A inside pixel. T_2 and T_3 are the TFTs used as MIS capacitors, because their drains and sources are shorted, respectively. In driving phase, T_2 provides the compensation of $\Delta V_{T,0}$, and T_3 injects positive charge onto the gate of T_0 to improve OLED drive current. When the voltage across a MIS capacitor is higher than V_T, the total capacitance of the capacitor is equal to channel capacitance plus contact overlap capacitance. When the voltage is lower than V_T, the total capacitance is equal to contact overlap capacitance [13].

In a pixel array, the bus lines of V_1, V_2, and V_3 are shared by the pixels in the same row and connected to a row driver. The bus line of V_{prog} is shared by the pixels in the same column and connected to a programming voltage driver (*i.e.*, column driver). Power supply V_{DD} and ground are shared by all pixels in array.

4.3 Pixel Circuit Operation

Each frame cycle has two phases: programming phase and driving phase. Driving phase is much longer than programming phase. For example, for a display array with N rows of pixels, if refresh rate is 60 Hz, programming phase is $(16.7/N)$ ms, while driving phase is 16.7 ms, which is N times longer than programming phase.

4.3.1 Programming Phase

At the beginning of programming phase, T_1 is turned ON by V_1^H, connecting node A to V_{prog}. T_2 is turned OFF by V_2^H, so mobile channel electrons are swept out from T_2, and the corresponding positive charge leaves from the gate of T_2. T_3 is turned ON by V_3^L and thus stores positive charge on its gate. The charge on the gate of a-Si:H TFT includes two pars: (1) Q_{ch}, the part of gate charge due to gate-to-channel capacitance; and (2) Q_{ov}, the part of gate charge due to overlap capacitance between gate and source/drain. After node voltages reaching set-points, T_0 is in saturation region, T_2 is OFF, T_1 and T_3 are in linear region. The Q_{ch} of T_0 is

$$Q_{ch,0}^{prog} \approx 2/3\ C_i W_0 L_0 \left(V_{data} - V_{OLED}^{prog} - V_{T,0}\right), \tag{4.1}$$

where C_i is gate-to-channel capacitance per unit area, W_0, L_0, and $V_{T,0}$ are the width, length, and threshold voltage of T_0, respectively, V_{OLED}^{prog} is set-point OLED voltage, and V_{data} is the data voltage provided by V_{prog}. For the same expected I_{OLED}^{driv}, V_{prog} provides the same V_{data} (*i.e.*, V_{data} is not changed with $\Delta V_{T,0}$). Coefficient 2/3 is used in Eq. (4.1) because T_0 is biased in saturation region [13,56].

In programming phase, T_2 is OFF, so its Q_{ch} is zero. Note that: (1) V_1^H, V_2^H, V_3^L, V_{data}, and V_{DD} do not change with $\Delta V_{T,0}$. (2) $\Delta V_{T,1}$ and $\Delta V_{T,3}$ are negligible when compared to $\Delta V_{T,0}$ (see section 4.5.2). (3) The ΔV_{OLED}^{prog} caused by $\Delta V_{T,0}$ is negligible (see section 4.5.1). Therefore, in programming phase, the Q_{ch} of T_1 and T_3 (*i.e.*, $Q_{ch,1}^{prog}$ and $Q_{ch,3}^{prog}$) as well as the Q_{ov} of all TFTs do not change with $\Delta V_{T,0}$, so they are not included in the analysis of the changes of charge components with $\Delta V_{T,0}$.

4.3.2 Driving Phase

In driving phase, T_1 is turned OFF by V_1^L to isolate node A from V_{prog}. T_2 is turned ON by V_2^L to provide $\Delta V_{T,0}$-compensation. T_3 is turned OFF by V_3^H to inject positive charge

onto node A so as to improve OLED drive current. To conserve the charge on node A, T_1 should be turned OFF before V_2 and V_3 are switched.

While T_1 is being turned OFF, a part of electrons in the channel of T_1 is injected onto node A. The injected charge is $Q_{Inj}^{T_1 \to A} \approx -\beta Q_{ch,1}^{prog}$. β is close to 1/2 if V_1 has a sharp falling edge [69]. Since $Q_{ch,1}^{prog}$ does not change with $\Delta V_{T,0}$ (see section 4.3.1), $Q_{Inj}^{T_1 \to A}$ is not included in the analysis of the changes of charge components with $\Delta V_{T,0}$. After node voltages settle down, T_0 is in saturation region, T_2 is in linear region, T_1 and T_3 are OFF. The values of the Q_{ch} of T_0 and T_2 are

$$Q_{ch,0}^{driv} \approx 2/3 C_i W_0 L_0 \left(V_{G,0}^{driv} - V_{OLED}^{driv} - V_{T,0}\right), \tag{4.2}$$

$$Q_{ch,2}^{driv} = C_i W_2 L_2 \left(V_{G,0}^{driv} - V_2^L - V_{T,2}\right), \tag{4.3}$$

where $V_{G,0}^{driv}$ is the set-point voltage on node A, and V_{OLED}^{driv} is the set-point voltage across OLED. Since T_1 and T_3 are OFF, their Q_{ch} values are zero. The Q_{ov} values of TFTs are

$$Q_{ov,0}^{driv} = C_{ov} W_0 L_{ov} (2V_{G,0}^{driv} - V_{OLED}^{driv} - V_{DD}), \tag{4.4}$$

$$Q_{ov \to A,1}^{driv} = -C_{ov} W_1 L_{ov} (V_{G,0}^{driv} - V_1^L), \tag{4.5}$$

$$Q_{ov,2}^{driv} = 2C_{ov} W_2 L_{ov} (V_{G,0}^{driv} - V_2^L), \tag{4.6}$$

$$Q_{ov,3}^{driv} = 2C_{ov} W_3 L_{ov} (V_{G,0}^{driv} - V_3^H), \tag{4.7}$$

where C_{ov} is source/drain overlap capacitance per unit overlap area, L_{ov} is the overlap length between gate and source/drain, and $Q_{ov \to A,1}^{driv}$ is the gate charge of T_1 due to the overlap capacitance on the side of node A.

4.4 Pixel Circuit Analysis, Design, and Simulation

4.4.1 ΔV_T and Charge Analysis

For the pixel circuit being switched from programming phase to driving phase, the following equation was derived based on the charge conservation on node A,

$$\frac{dQ_{ch,0}^{prog}}{dV_{T,0}} = \frac{dQ_{ch,0}^{driv}}{dV_{T,0}} + \frac{dQ_{ch,2}^{driv}}{dV_{T,0}} + \frac{dQ_{ov,Tot}^{driv}}{dV_{T,0}}, \tag{4.8}$$

where

$$Q_{ov,Tot}^{driv} = Q_{ov,0}^{driv} - Q_{ov \to A,1}^{driv} + Q_{ov,2}^{driv} + Q_{ov,3}^{driv}. \tag{4.9}$$

Note that, although other charge components also contribute to the charge conservation on node A, they do not vary with $\Delta V_{T,0}$. Therefore, they are not included in Eq. (4.8).

Neglecting CLM effect in Eq. (2.9), the I_{DS} of a-Si:H TFT in saturation region is

$$I_{DS} \approx \alpha_{sat}\ \mu_n C_i \frac{W}{L} \frac{(V_{GS} - V_T)^{\gamma+2}}{V_{AA}^{\gamma}}. \tag{4.10}$$

Therefore, when $V_{T,0}$ shifts, stabilizing I_{OLED}^{driv} requires

$$dV_{GS,0}^{driv}/dV_{T,0} = 1. \tag{4.11}$$

Since $V_{S,0} = V_{OLED}$ and $dV_{OLED}^{driv}/dV_{T,0} = 0$ (see Eq. (4.36)), Eq. (4.11) is equivalent to

$$dV_{G,0}^{driv}/dV_{T,0} = 1. \tag{4.12}$$

Substituting Eq. (4.12) and Eq. (4.36) into Eq. (4.2) yields

$$dQ_{ch,0}^{driv}/dV_{T,0} = 0, \tag{4.13}$$

so that if $\Delta V_{T,0}$ is fully compensated by $\Delta V_{GS,0}^{driv} = \Delta V_{T,0}$, the channel charge of T_0 in driving phase does not change with $\Delta V_{T,0}$. Substituting Eq. (4.13) into Eq. (4.8) yields

$$\frac{dQ_{ch,0}^{prog}}{dV_{T,0}} = \frac{dQ_{ch,2}^{driv}}{dV_{T,0}} + \frac{dQ_{ov,Tot}^{driv}}{dV_{T,0}}. \tag{4.14}$$

Substituting Eq. (4.1)-Eq. (4.7) and Eq. (4.9) into Eq. (4.14) and then using the relevant formulas presented in section 4.5 yield

$$W_2 = \frac{2/3 C_i W_0 L_0 + 2C_{ov,0} + C_{ov,1} + 2C_{ov,3}}{1/2 C_i L_2 - 2C_{ov} L_{ov}}, \tag{4.15}$$

where $C_{ov,n} = C_{ov} W_n L_{ov}$ $(n = 0, 1, 2, 3)$. The compensation of $\Delta V_{T,0}$ can be achieved by sizing T_2 as specified in Eq. (4.15). Note that, in circuit design practice, if coefficient values are different from the ones assumed in above procedures, one should accordingly adjust the coefficient values used in the formula of W_2.

4.4.2 $\Delta V_{T,0}$-Compensation Mechanism

The mechanism of the compensation of $\Delta V_{T,0}$ is explained by analyzing Eq. (4.8). Eq. (4.1) and (4.35) indicate that $Q_{ch,0}^{prog}$ reduces when $V_{T,0}$ increases, *i.e.*, the increase of $V_{T,0}$

results in less channel charge stored in T_0 in programming phase. To compensate $\Delta V_{T,0}$, $\Delta V_{G,0}^{driv}$ should be as large as $\Delta V_{T,0}$. Since $Q_{ov,Tot}^{driv}$ increases with $V_{G,0}^{driv}$, more positive charge must be provided to the source/drain overlap capacitances of the TFTs in the pixel circuit, otherwise $V_{G,0}^{driv}$ can not increase with $V_{T,0}$. Eq. (4.3) and (4.41) indicate that, since $V_{T,2}$ increases faster than $V_{GS,2}^{driv}$, $Q_{ch,2}^{driv}$ decreases when $V_{T,0}$ increases. Designing W_2 as specified in Eq. (4.15) validates Eq. (4.14). This means that, when $V_{T,0}$ increases, the decrease of $Q_{ch,2}^{driv}$ is so large that it not only cancels out the decrease of $Q_{ch,0}^{prog}$ but also provides the extra positive charge needed by the increase of $Q_{ov,Tot}^{driv}$. Therefore, $Q_{ch,0}^{driv}$ does not change with $V_{T,0}$ (see Eq. (4.13)), so $\Delta V_{GS,0}^{driv}$ is as large as $\Delta V_{T,0}$ (see Eq. (4.2)). Since $\Delta V_{T,0}$ is fully compensated by $\Delta V_{GS,0}^{driv}$, it does not affect I_{OLED}^{driv} (see Eq. (4.10)).

4.4.3 $\Delta V_{T,0}$-Compensation Effectiveness

Simulation Setup

To verify the proposed pixel circuit, circuit simulation was carried out by using Cadence® Spectre® circuit simulator and a Verilog-A model file of a-Si:H TFT. The model file was improved from the one built by the author of [17]. The parameter values used in circuit simulation are $\mu_{eff} = 0.3$ cm^2/(V·s), $V_T^{init} = 3$ V, $C_i = 19$ nF/cm^2, and $C_{ov} = 16$ nF/cm^2. μ_{eff} is effective mobility, and V_T^{init} is the initial V_T of a fresh TFT before it is stressed. Besides, a Verilog-A model file of OLED was used in circuit simulation. It was built by using the OLED model in [70] and *I-V* data in [71]. The size of OLED was assumed as 100×200 μm^2, and the capacitance per unit area of OLED was assumed as 25 nF/cm^2, so OLED capacitance used in circuit simulation was 5 pF [72].

The values of the design variables of the simulated pixel circuit are listed in Table 4.1. The minimum channel length was selected as 25 μm. It is within the range of $(23 \sim 130)$ μm, in which the TFT model was verified by measurement results [17,73]. Based on simulation results, $W_2 = 60$ μm was determined as the optimal value for $\Delta V_{T,0}$-compensation. Note that substituting the assumed parameter values into Eq. (4.15) yields $W_2 = 72.5$ μm instead of $W_2 = 60$ μm. This discrepancy is mainly caused by the rough approximation made in the coefficient 2/3 in Eq. (4.2). The specific formulas and parameter values relevant to that coefficient used in the TFT model file actually yield 0.413 as the exact value of that coefficient. Replacing 2/3 with 0.413 in Eq. (4.15) yields $W_2 = 57.2$ μm, which is very close to the optimal $W_2 = 60$ μm determined in simulations. TFT sizes can be scaled down along with the minimum channel length, so that the total area of TFTs can be significantly reduced. The typical minimum channel length used in industry is 5 μm.

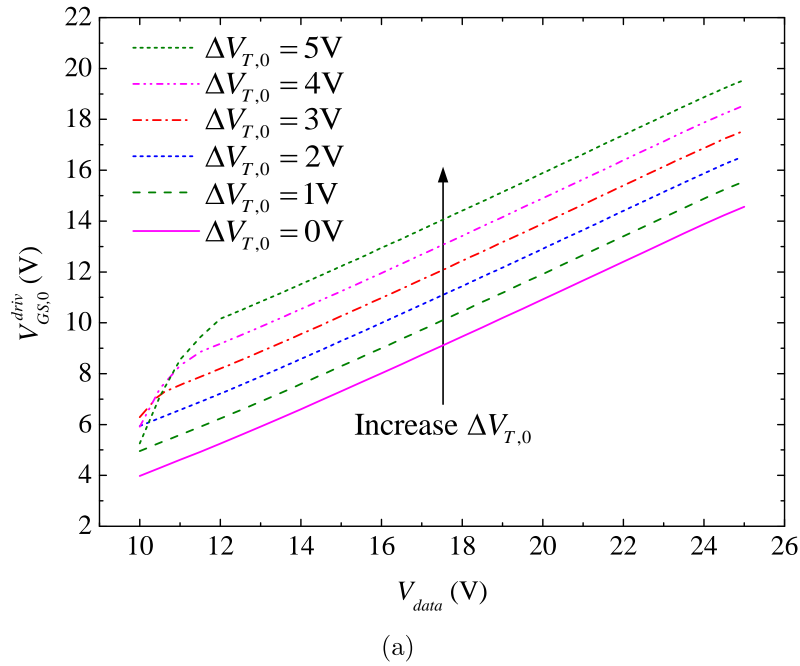
Table 4.1: Design Variables of Proposed Pixel Circuit used in Circuit Simulation [66]

Design Variable	Value	Design Variable	Value
Programming Phase (μs)	120	V_{data} (V)	$10 \sim 25$
W_0/L_0 (μm)	100/25	V_{DD} (V)	30
W_1/L_1 (μm)	50/25	V_1 (V)	$0 \sim 30$
W_2/L_2 (μm)	60/100	V_2 (V)	$2 \sim 30$
W_3/L_3 (μm)	35/100	V_3 (V)	$2 \sim 30$
L_{ov} (μm)	5	I_{OLED}^{driv} (μA)	$0 \sim 3$

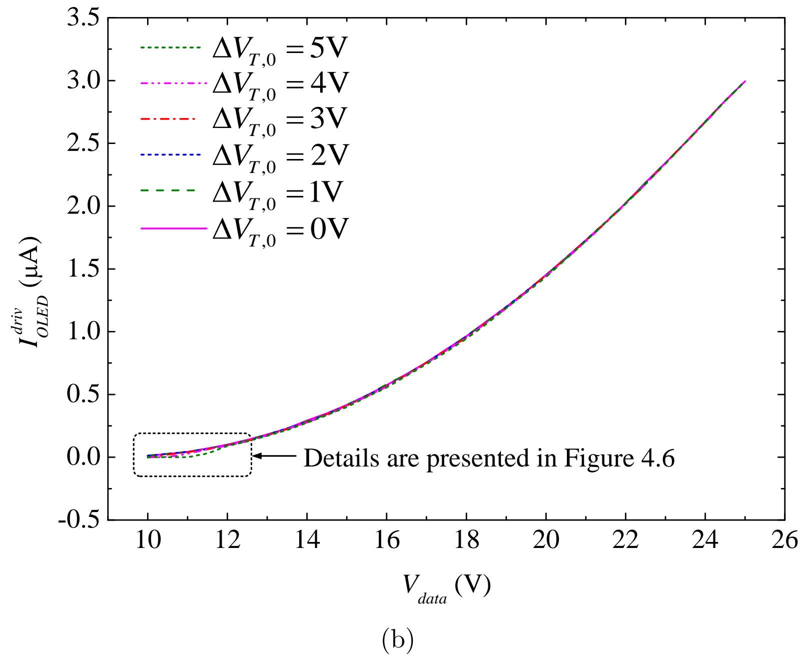
To verify the effectiveness of $\Delta V_{T,0}$-compensation, $\Delta V_{T,0}$ was swept in circuit simulation. When sweeping $\Delta V_{T,0}$, $\Delta V_{T,2}$ was set as $\Delta V_{T,2} = 3/2\Delta V_{T,0}$ (refer to section 4.5.4). The aging of T_1, T_3 and OLED was neglected (refer to section 4.5.1 and 4.5.2).

Charge Components and I_{OLED}^{driv} Stability

The $V_{GS,0}^{driv}$ and I_{OLED}^{driv} of the proposed pixel circuit were simulated for different V_{data} and $\Delta V_{T,0}$. Figure 4.4(a) shows that, for a relatively high V_{data}, $\Delta V_{GS,0}^{driv} = \Delta V_{T,0}$, so $\Delta V_{T,0}$ does not affect I_{OLED}^{driv}, as shown in Figure 4.4(b). For illustration, the simulation results of charge components included in Eq. (4.8) *vs.* $\Delta V_{T,0}$ for $V_{data} = 25$ V are shown in Figure 4.5(a). When $\Delta V_{T,0}$ increases, $\Delta Q_{ch,2}^{driv}$ is so large that it equals $(\Delta Q_{ch,0}^{prog} - \Delta Q_{ov,Tot}^{driv})$, so $Q_{ch,0}^{driv}$ does not change with $\Delta V_{T,0}$. This is already described in section 4.4.2. To make a comparison, the conventional 2-TFT pixel circuit illustrated in Figure 4.1 was also simulated. Since this circuit does not provide $\Delta V_{T,0}$-compensation, its I_{OLED}^{driv} drops significantly with the increase of $\Delta V_{T,0}$, as shown in Figure 4.2. The comparison between Figure 4.4(b) and Figure 4.2 demonstrates the effectiveness of the proposed pixel circuit in $\Delta V_{T,0}$-compensation. However, for a larger $\Delta V_{T,0}$ and the lowest levels of V_{data} and I_{OLED}^{driv}, Figure 4.4 also shows the under-compensation of $\Delta V_{T,0}$. This is discussed in section 4.4.4.

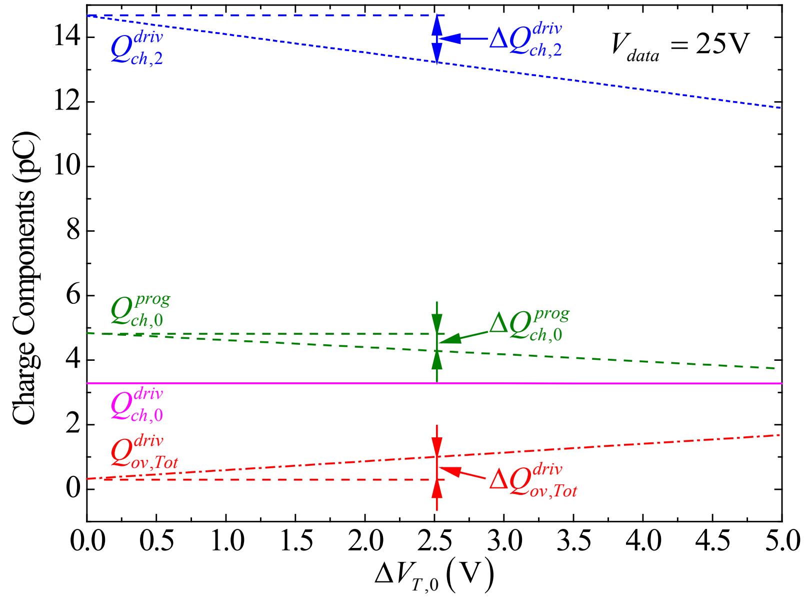


(a)

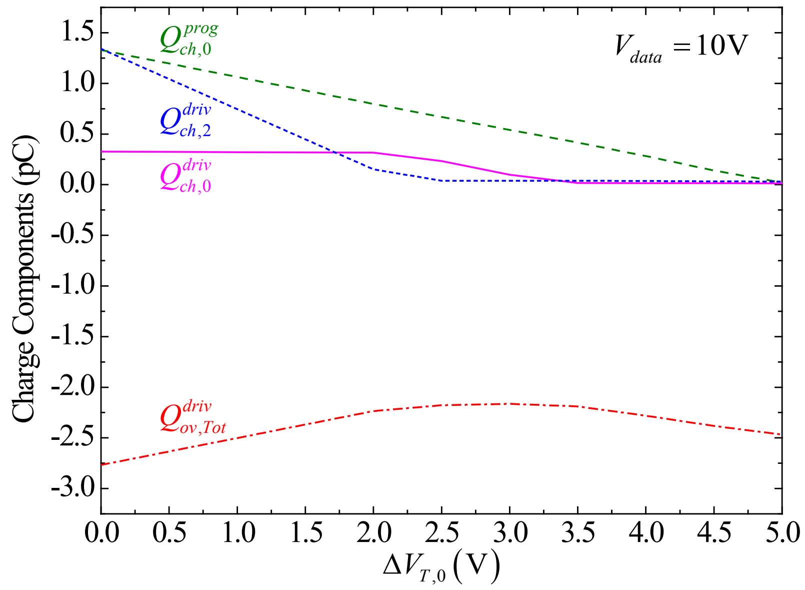


(b)

Figure 4.4: Simulation results of (a) $V_{GS,0}^{driv}$ *vs.* V_{data} and (b) I_{OLED}^{driv} *vs.* V_{data} of the proposed pixel circuit [66–68]. The zoomed-in part is shown in Figure 4.6.



(a)



(b)

Figure 4.5: Simulation results of charge components *vs.* $\Delta V_{T,0}$ of the proposed pixel circuit for (a) $V_{data} = 25$ V and (b) $V_{data} = 10$ V [66, 68].

4.4.4 $\Delta V_{T,0}$-Compensation Non-ideality

If $V_{T,2} > V_{GS,2}^{driv}$

For $V_{data} = 10$ V, Figure 4.5(b) shows that $\Delta V_{T,0}$ is not always fully compensated. For $\Delta V_{T,0} > 2.25$ V, $Q_{ch,0}^{driv}$ starts to drop with the increase of $\Delta V_{T,0}$. This means that $\Delta V_{GS,0}^{driv} < \Delta V_{T,0}$. This is referred to as the under-compensation of $\Delta V_{T,0}$. For a lower V_{data} and thus a lower I_{OLED}^{driv}, the under-compensation of $\Delta V_{T,0}$ appears at a smaller $\Delta V_{T,0}$, as shown in Figure 4.4 and 4.6. The under-compensation of $\Delta V_{T,0}$ is explained as follows.

Eq. (4.40) indicates that $V_{T,2}$ increases with $V_{T,0}$. For a lower V_{data}, $V_{GS,2}^{driv}$ is also lower, so the $\Delta V_{T,0}$ at which $V_{T,2}$ catches up $V_{GS,2}^{driv}$ is smaller. This mechanism is illustrated in Figure 4.7. Once $V_{T,2}$ catches up $V_{GS,2}^{driv}$, $Q_{ch,2}^{driv}$ becomes zero and thus stops decreasing with the increase of $\Delta V_{T,0}$, so $Q_{ch,0}^{driv}$ starts to drop with the increase of $\Delta V_{T,0}$, as illustrated in Figure 4.5(b). This means that $\Delta V_{GS,0}^{driv} < \Delta V_{T,0}$, so $\Delta V_{T,0}$ is under-compensated (see Figure 4.4(a)). Therefore, I_{OLED}^{driv} starts to drop with the increase of $\Delta V_{T,0}$ (see Figure 4.6).

If $\Delta V_{T,0}$ is not too large, the under-compensation of $\Delta V_{T,0}$ exists only at the lowest I_{OLED}^{driv} levels, so it does not significantly affect the overall stability of I_{OLED}^{driv} (see Figure 4.4). Define $I_{OLED}^{driv,Tol}$ as the level of I_{OLED}^{driv} beneath which the under-compensation of $\Delta V_{T,0}$ is allowed by design specification, $\Delta V_{T,0}^{Tol}$ as the maximum $\Delta V_{T,0}$ that can be fully compensated at $I_{OLED}^{driv,Tol}$, and $I_{OLED}^{driv,Max}$ as the maximum I_{OLED}^{driv} that the pixel circuit is designed to provide. $I_{OLED}^{driv,Tol}$ is normalized to $I_{OLED}^{driv,Max}$ to define a tolerance ratio Ratio_{tol}, which is used to measure the significance of the range of unstable I_{OLED}^{driv}:

$$\text{Ratio}_{tol} = \frac{I_{OLED}^{driv,Tol}}{I_{OLED}^{driv,Max}} = \left(\frac{\Delta V_{T,0}^{Tol}/2}{V_{ov,0}^{driv,Max}} \right)^{\gamma+2}, \tag{4.16}$$

where $V_{ov,0}^{driv,Max}$ is the overdrive voltage of T_0 for $I_{OLED}^{driv,Max}$. The derivation of Eq. (4.16) is shown in section 4.5.5. For $\Delta V_{T,0}^{Tol} = 5$ V, Ratio_{tol} is only 3.3% (refer to Figure 4.4(b) and 4.6), so the instability of I_{OLED}^{driv} at the levels below $I_{OLED}^{driv,Tol}$ does not significantly affect the overall stability of I_{OLED}^{driv}. If design specification requires $\text{Ratio}_{tol} \leqslant 3.3\%$, the proposed $\Delta V_{T,0}$-compensation technique works well until $\Delta V_{T,0}$ increases up to $\Delta V_{T,0}^{Tol} = 5$ V.

Discrepancy of $\Delta V_{T,2}/\Delta V_{T,0}$

As explained in section 4.5.4, $\Delta V_{T,2} \approx 3/2 \Delta V_{T,0}$ is assumed in pixel circuit design and analysis. This approximation may have a discrepancy up to 10% [56]. Define a discrepancy

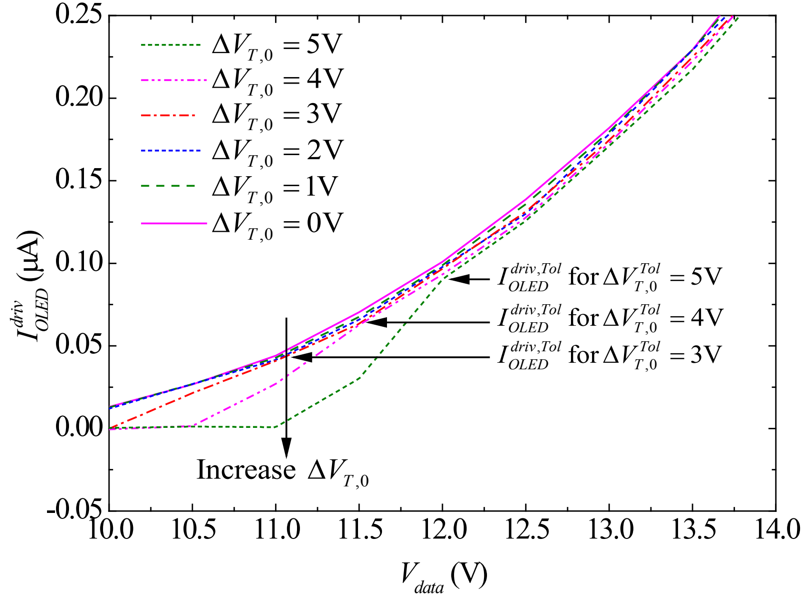


Figure 4.6: Simulated I_{OLED}^{driv} *vs.* V_{data} (the zoomed-in part of Figure 4.4(b)) [66].

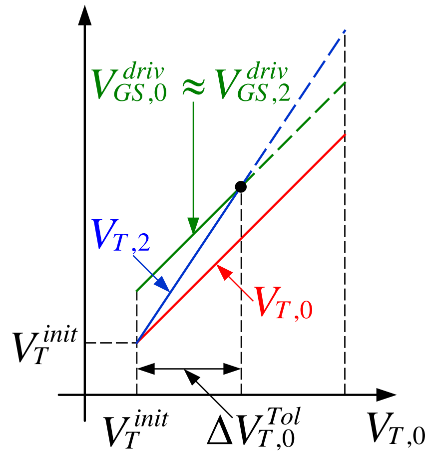


Figure 4.7: $V_{T,2}$ increases faster than $V_{T,0}$ and catches up $V_{GS,2}^{driv}$ at $V_{T,0}^{Tol}$ $(= V_T^{init} + \Delta V_{T,0}^{Tol})$.

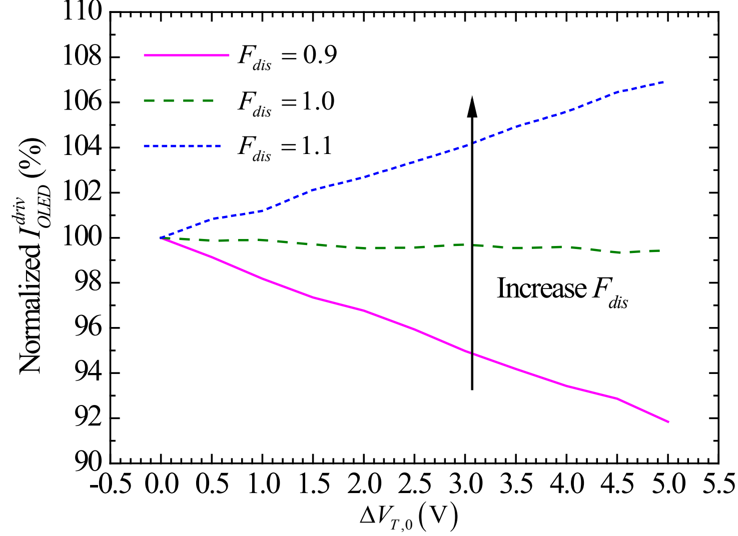


Figure 4.8: Normalized simulation results of I_{OLED}^{driv} *vs.* $\Delta V_{T,0}$ for different F_{dis} at $V_{data} = 25$ V [66]. W_2 is designed by using Eq. (4.17) and assuming $F_{dis} = 1$.

factor F_{dis} so that $\Delta V_{T,2} = (3/2\Delta V_{T,0})F_{dis}$, where $F_{dis} \in (0.9, 1.1)$, so Eq. (4.15) becomes

$$W_2 = \frac{2/3C_iW_0L_0 + 2C_{ov,0} + C_{ov,1} + 2C_{ov,3}}{(3/2F_{dis} - 1)C_iL_2 - 2C_{ov}L_{ov}}. \tag{4.17}$$

For the W_2 designed by assuming $F_{dis} = 1$, the impact of the variation of F_{dis} on the stability of I_{OLED}^{driv} was investigated by using circuit simulation. Simulation results are shown in Figure 4.8. For $F_{dis} > 1$, $\Delta V_{T,0}$ is over-compensated, so I_{OLED}^{driv} increases with $\Delta V_{T,0}$, vice versa. For $F_{dis} \in (0.9, 1.1)$, the instability of I_{OLED}^{dirv} is within 8%. In circuit design practice, the value of F_{dis} should be extracted from measurement results and used in Eq. (4.17) to achieve an accurate $\Delta V_{T,0}$-compensation.

4.4.5 Use T_3 to Improve OLED Drive Current

If T_3 is not used, since T_2 draws positive charge from node A in driving phase, $V_{G,0}^{driv}$ could be much lower than what is needed to achieve the I_{OLED}^{driv} levels required in practical designs. Therefore, T_3 is used to improve I_{OLED}^{driv} levels. In programming phase, T_3 is turned ON by V_3^L and stores positive charge on its gate. In driving phase, V_3 is switched to V_3^H to inject positive charge from the gate of T_3 onto node A, improving $V_{G,0}^{driv}$ and therefore I_{OLED}^{driv}. The improvement of I_{OLED}^{driv} can be adjusted by varying the size of T_3.

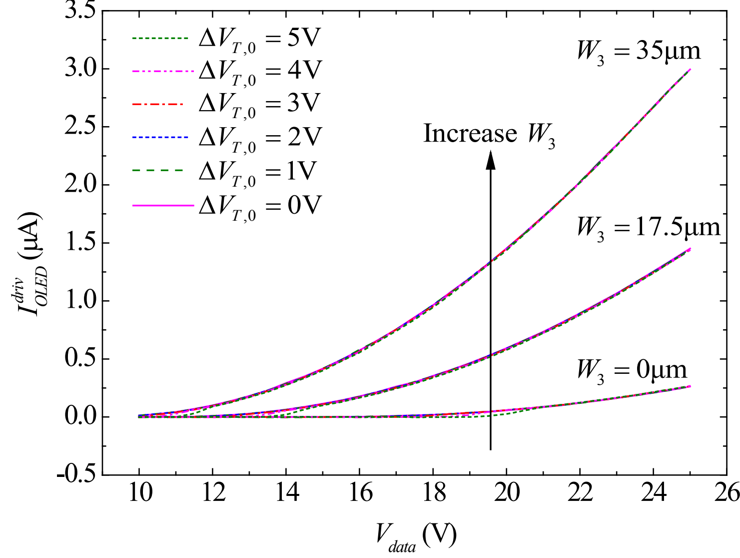


Figure 4.9: Simulated I_{OLED}^{driv} *vs.* V_{data} for different W_3 [66].

$Q_{ch,3}^{prog}$ is the part of the gate charge of T_3 associated to channel in programming phase. It is injected onto node A in driving phase. Since V_3^L is a fixed value shared by all pixels in the same row, $Q_{ch,3}^{prog}$ is determined by V_{data}. $Q_{ch,3}^{prog}$ does not change with $\Delta V_{T,0}$ (see section 4.3.1), so it does not affect $\Delta V_{T,0}$-compensation. The only impact of T_3 on $\Delta V_{T,0}$-compensation is due to $C_{ov,3}$ (refer to Eq. (4.15)). However, this impact is minor because $C_{ov,3}$ is a parasitic component. Assuming $C_{ov} = C_i$, based on the geometries listed in Table 4.1, it can be derived that $C_{ov,3}$ is only 3.55% of the total capacitance on node A in driving phase. The simulation results shown in Figure 4.9 confirm this analysis. Increasing the size of T_3 significantly improves I_{OLED}^{driv} without significantly affecting $\Delta V_{T,0}$-compensation.

4.4.6 Overlap Capacitance

Referring to Eq. (4.15), the channel area of T_2 (*i.e.*, $W_2 \times L_2$) required by $\Delta V_{T,0}$-compensation depends on not only the size of T_0 but also $C_{ov,n}$ ($n = 0, 1, 2, 3$). As shown in Figure 4.10, simulation results indicate that for a given $\Delta V_{T,0}$, a shorter L_{ov} (*i.e.*, smaller $C_{ov,n}$) leads to a higher I_{OLED}^{driv}. If L_{ov} is short enough, I_{OLED}^{driv} increases with $\Delta V_{T,0}$ (*i.e.*, $\Delta V_{T,0}$ is over-compensated). Therefore, for the same ($W_2 \times L_2$), reducing $C_{ov,n}$ ($n = 0, 1, 2, 3$) results in the over-compensation of $\Delta V_{T,0}$. Equivalently, if $C_{ov,n}$ ($n = 0, 1, 2, 3$) are reduced, the ($W_2 \times L_2$) needed by $\Delta V_{T,0}$-compensation can be smaller.

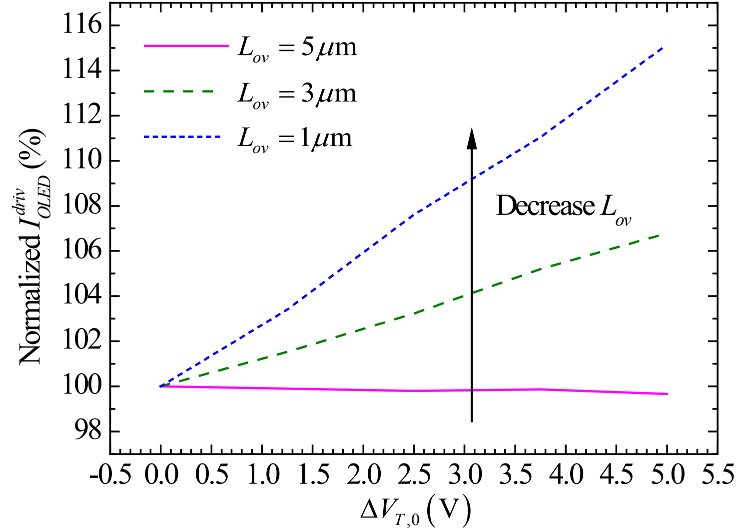


Figure 4.10: Normalized simulation results of I_{OLED}^{driv} *vs.* $\Delta V_{T,0}$ for different L_{ov} at $V_{data} = 25$ V in the proposed pixel circuit [66].

4.4.7 Programming Speed

Programming phase should be long enough for the gate voltage of drive TFT to settle down in programming phase. For the same refresh rate, the faster the gate voltage settles down, the shorter programming phase can be, and the more rows of pixels can be driven. In this section, the settling-down speeds of conventional current-programmed pixel circuit, voltage-programmed pixel circuit, and the proposed pixel circuit are analyzed and compared. The transient simulation results of the proposed pixel circuit are also presented.

Current-Programmed Pixel Circuit

An equivalent circuit of a current-programmed pixel circuit in programming phase is presented in Figure 4.11(a) [4]. I_{prog} is a programming current source shared by m pixels in the same column. In each pixel, T_0 is drive TFT, controlling OLED drive current. OLED is omitted to simplify analysis. C_A is the total equivalent capacitance on node A in programming phase. V_A is the voltage on node A. T_1 is switch TFT, controlling the access from I_{prog} to node A in the pixel. T_1 is controlled by V_1, which is shared by all the pixels in the same row. Each pixel has a $C_{ov,1}$, which is the overlap capacitance of T_1 on the side of I_{prog}. r_p is the resistance of column bus line between two neighboring pixels.

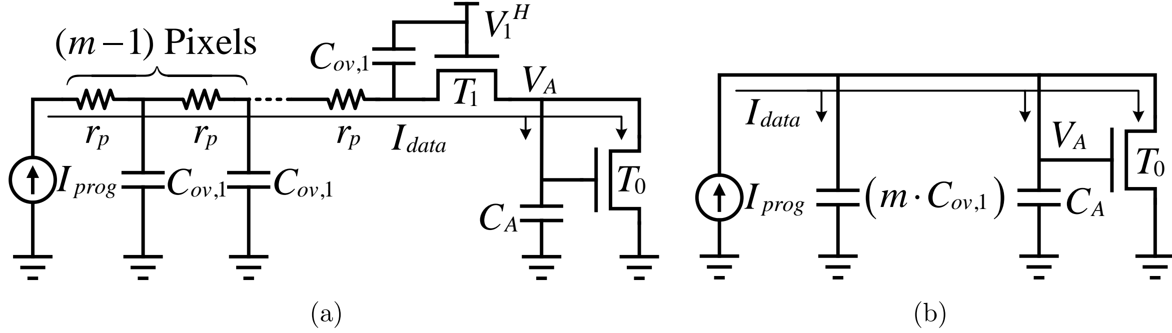


Figure 4.11: (a) Equivalent circuit to analyze the settling-down time of V_A in a conventional current-programmed pixel circuit, (b) simplified circuit.

In programming phase, I_{prog} provides I_{data} to the pixel being programmed. T_0 is diode-connected to I_{prog} through T_1. Since the total resistance on signal bus line is much smaller than the channel resistance of T_0 [4], it is neglected to simplify analysis. To get an analytical explicit solution, T_1 is omitted, and a simple square-law I_{DS} model is used in analysis. The simplified circuit is shown in Figure 4.11(b) [4]. The total capacitance on node A is

$$C_{tot} = m \cdot C_{ov,1} + C_A. \tag{4.18}$$

As shown in Figure 4.11(b), during programming phase, T_0 is diode-connected and operates in saturation region, so

$$I_{data} = C_{tot}\frac{dV_A}{dt} + \frac{K}{2}\left(V_A - V_T\right)^2, \tag{4.19}$$

where $K = \mu_n C_i \frac{W_0}{L_0}$ [4]. Assuming $V_A = V_T$ at the beginning of programming phase, Eq. (4.19) is solved for V_A:

$$\frac{V_A^{prog} - V_A}{V_A^{prog} - V_T} = \frac{2\exp\left(-\frac{t}{\tau}\right)}{1 + \exp\left(-\frac{t}{\tau}\right)}, \tag{4.20}$$

where V_A^{prog} is the value of V_A after it settles down in programming phase:

$$V_A^{prog} - V_T = \sqrt{2I_{data}/K}, \tag{4.21}$$

and τ is time constant [4]:

$$\tau = \frac{C_{tot}}{\sqrt{2KI_{data}}}. \tag{4.22}$$

Assuming V_A is considered as settled down when

$$\frac{V_A^{prog} - V_A}{V_A^{prog} - V_T} \leqslant \varepsilon, \tag{4.23}$$

where ε is a pre-defined error tolerance, Eq. (4.20) yields that settling-down time is

$$t_{settle} = \tau \ln\left(\frac{2}{\varepsilon} - 1\right) \approx \tau \ln(2/\varepsilon). \tag{4.24}$$

Conventional Voltage-Programmed Pixel Circuit using V_T-Generation

Conventional voltage-programmed pixel circuits typically use a V_T-generation sub-phase in programming phase to generate a gate voltage to compensate the ΔV_T of drive TFT. V_T-generation techniques have three types: stacked type, parallel-compensation type, and bootstrapping type [4]. The V_T-generation operations of these types are essentially the same. In stacked type, OLED capacitance, which is typically much larger than other capacitance components in a pixel circuit, is charged/discharged during V_T-generation, so settling-down speed is slow. In bootstrapping type, V_T-generation and V_{data}-inputting are carried out in two different sub-phases, so programming phase requires longer time. In parallel-compensation type, V_T-generation and V_{data}-inputting are carried out at the same time, so programming phase can be shorter. Parallel-compensation type is used in this section as an example to analyze the settling-down speed during V_T-generation.

A simplified equivalent pixel circuit in V_T-generation sub-phase is presented in Figure 4.12 [4]. Before the beginning of V_T-generation sub-phase, T_1 is OFF, and V_A is pre-charged by an external voltage source (not shown) to a certain high level V_A^{init}. During V_T-generation sub-phase, T_1 is turned ON by V_1^H. Since node A is discharged by a transient current going through T_1 and T_0 to V_{prog}, V_A decreases until it becomes $V_A = V_{data} + V_T$, where V_{data} is the data voltage provided by V_{prog}. The dynamic behavior of V_A is analyzed as follows. T_1 is omitted in analysis to achieve an analytical solution of V_A. The gate and drain of T_0 are shorted by T_1, so T_0 is biased in saturation region. Therefore,

$$i_0 = -C_A \frac{dV_A}{dt} = \frac{1}{2} K \left(V_A - V_{data} - V_T\right)^2, \tag{4.25}$$

where $K = \mu_n C_i \frac{W_0}{L_0}$. Solving Eq. (4.25) yields

$$\frac{V_A - (V_{data} + V_T)}{V_A^{init} - (V_{data} + V_T)} = \frac{1}{1 + \frac{t}{\tau}}, \tag{4.26}$$

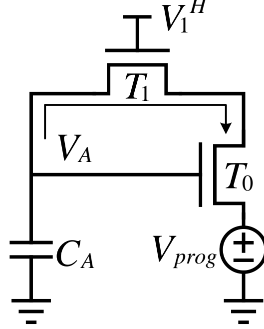


Figure 4.12: Equivalent circuit to analyze the settling-down time of V_A in a conventional voltage-programmed pixel circuit (parallel-compensation type) during V_T-generation.

where τ is time constant

$$\tau = \frac{2C_A}{K\left[\ V_A^{init} - (V_{data} + V_T)\ \right]}. \tag{4.27}$$

Assuming V_A is considered as settled down when

$$\frac{V_A - (V_{data} + V_T)}{V_A^{init} - (V_{data} + V_T)} \leqslant \varepsilon, \tag{4.28}$$

where ε is a pre-defined error tolerance, Eq. (4.26) yields that settling-down time is

$$t_{settle} = \tau\left(\frac{1}{\varepsilon} - 1\right) \approx \tau/\varepsilon. \tag{4.29}$$

The comparison between Eq. (4.29) and Eq. (4.24) indicates the difference of settling-down time between current-programmed pixel circuit and the voltage-programmed pixel circuit using V_T-generation techniques. When it comes to τ, assuming C_A has the same value in both circuits and it is much smaller than $(m \cdot C_{ov,1})$ (see Eq. (4.18)), C_{tot} in Eq. (4.22) is much larger than C_A in Eq. (4.27).[1] Besides, when a current-programmed pixel is expected to have a small brightness in driving phase, a low I_{data} is used. If the V_A of the current-programmed pixel circuit at the beginning of programming phase is lower than V_A^{prog}, the low I_{data} has to charge a large C_{tot} to raise V_A toward V_A^{prog}, so the settling-down

[1]For example, assuming the minimum channel length defined on mask of a pixel circuit is $L_{mask}^{min} = 25$ μm, a pixel circuit typically has $C_A = 2 \sim 3$ pF. Assuming $W_1 = 50$ μm, $L_{ov} = 5$ μm, $C_i = 14.9$ nF/cm^2, and 10^3 rows of pixels, $(m \cdot C_{ov,1}) = 37.18$ pF, so $C_A \ll C_{tot} = m \cdot C_{ov,1} + C_A$.

speed of V_A is very slow (refer to Eq. (4.22)). In contrast, for a conventional voltage-programmed pixel circuit, Eq. (4.27) indicates that τ is relatively small because (1) C_A is relatively small (since it is a capacitance inside pixel, instead of the capacitance of a whole signal bus line) and (2) appropriate values can be selected respectively for V_A^{init} and V_{data} to reduce τ. Therefore, although $\ln(2/\varepsilon)$ in Eq. (4.24) is smaller than $(1/\varepsilon)$ in Eq. (4.27),[2] the difference of τ dominates the difference of settling-down time, so conventional voltage-programmed pixel circuits are typically faster than current-programmed pixel circuits.

Proposed Voltage-Programmed Pixel Circuit with ΔV_T-Compensation

The simplified equivalent circuit of the proposed pixel circuit in programming phase is presented in Figure 4.13(a). Programming voltage source V_{prog} drives m pixels in the same column. T_1, V_1^H, $C_{ov,1}$, r_p, C_A, and V_A are the same to the ones presented in Figure 4.11(a). Since the total resistance of bus line is much smaller than the channel resistance of T_1, it is neglected to simplify analysis. The simplified circuit is shown in Figure 4.13(b).

In programming phase, if the initial value of V_A is lower than the V_{data} provided by V_{prog}, a transient current flows from V_{prog} to node A, so V_A increases toward V_{data}. Since V_A is the source voltage of T_1, an increasing V_A results in a decreased overdrive voltage of T_1, *i.e.*, $\left(V_1^H - V_A - V_{T,1}\right)$. This results in an increased channel resistance of T_1, and thus an increased time constant of V_A. In contrast, if the initial value of V_A is higher than V_{data}, a transient turret flows from node A to V_{prog}, and V_A decreases toward V_{data}. Since the source voltage of T_1 is fixed by V_{prog} at V_{data}, the overdrive voltage of T_1 is fixed at $\left(V_1^H - V_{data} - V_T\right)$, so the time constant of V_A does not significantly vary.[3] Therefore, charging node A is slower than discharging node A.

The worse case of the settling-down speed of V_A is when V_{data} is set at its highest level while the initial V_A is at its lowest level. The worse-case settling-down time is analyzed as follows. Based on Figure 4.13(b), the following differential equation is established:

$$i_1 = C_A \frac{dV_A}{dt} = K\left(V_1^H - V_A - V_T\right)\left(V_{data} - V_A\right), \tag{4.30}$$

where $K = \mu_n C_i \frac{W_1}{L_1}$. Assuming $V_A = V_T$ at the beginning of programming phase, solving Eq. (4.30) yields

$$\frac{V_{data} - V_A}{V_{data} - V_T} = \frac{V_1^H - V_T - V_{data}}{(V_1^H - 2V_T)\exp\left(\frac{t}{\tau}\right) - (V_{data} - V_T)}, \tag{4.31}$$

[2] Assuming $\varepsilon = 10\%$, $\ln(2/\varepsilon) \approx 3$, while $(2/\varepsilon) = 10$.

[3] Assuming T_1 is always in linear region.

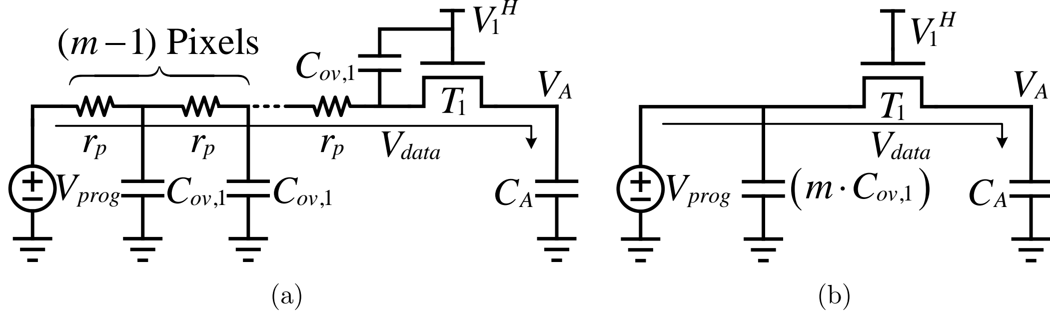


Figure 4.13: (a) Equivalent circuit to analyze the settling-down time of V_A in the proposed pixel circuit, (b) simplified circuit.

where τ is time constant

$$\tau = \frac{C_A}{K\left[\ V_1^H - (V_{data} + V_T)\ \right]}. \tag{4.32}$$

Assuming V_A is considered as settled down when

$$\frac{V_{data} - V_A}{V_{data} - V_T} \leqslant \varepsilon, \tag{4.33}$$

where ε is a pre-defined error tolerance, Eq. (4.31) yields the settling-down time of V_A:

$$t_{settle} = \tau \ln\left[\frac{V_{data} - V_T + \left(V_1^H - V_T - V_{data}\right)/\varepsilon}{V_1^H - 2V_T}\right] \approx \tau \ln\left(F_V/\varepsilon\right), \tag{4.34}$$

where $F_V = \left(V_1^H - V_T - V_{data}\right) / \left(V_1^H - 2V_T\right)$. The approximation in Eq. (4.34) is valid if $\left(V_1^H - V_T - V_{data}\right)/\varepsilon \gg (V_{data} - V_T)$, which is a typical case.

The settling-down time of V_A in the proposed pixel circuit and that in the conventional voltage-programmed pixel circuit are investigated by comparing Eq. (4.34) to Eq. (4.29). Assuming the C_A in Eq. (4.32) is equal to the $2C_A$ in Eq. (4.27), K has the same value in both equations, and V_1^H in Eq. (4.32) and V_A^{init} in Eq. (4.27) are equal to V_{DD}, these two pixel circuits have the same τ. Besides, $V_{data} \geqslant V_T$, so $F_V \leqslant 1$, and thus $\ln\left(F_V/\varepsilon\right) < 1/\varepsilon$. Therefore, the t_{settle} of the proposed pixel circuit is shorter than that of conventional voltage-programmed pixel circuit.

Besides theoretical analysis, transient simulation was also used to investigate the programming speed of the proposed pixel circuit. Simulation results of $V_{G,0}(t)$ in programming

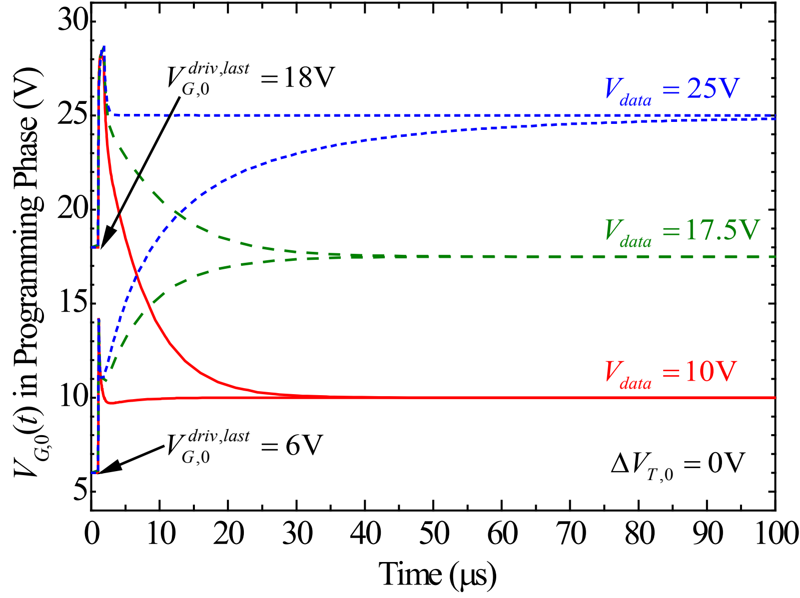


Figure 4.14: Simulation results of $V_{G,0}(t)$ in the proposed pixel circuit for $\Delta V_{T,0} = 0$ V and different initial values of $V_{G,0}(t)$ in programming phase [66].

phase are shown in Figure 4.14. The waveform of $V_{G,0}(t)$ depends on its initial value in programming phase, which is the value of $V_{G,0}(t)$ after it settling down in the last driving phase (denoted as $V_{G,0}^{driv,last}$). For $\Delta V_{T,0} = 0$ V, since $V_{G,0}^{driv}$ ranges from 6 V to 18 V (see Figure 4.17(a)), the waveforms of $V_{G,0}(t)$ were simulated for $V_{G,0}^{driv,last} = 6$ V and 18 V, respectively. Figure 4.14 shows that $V_{G,0}(t)$ settles down within 99% of V_{data} in 90 μs. For another corner $\Delta V_{T,0} = 5$ V, simulation results (not shown) verify the same conclusion.

As explained in Section 4.4.3, the minimum channel length L_{mask}^{min} was selected as 25 μm. Assuming TFT sizes are scaled down by 5 times so that L_{mask}^{min} becomes 5 μm, which is typically used in industry, the capacitance on node A is reduced by 25 times, while TFT driving strengths are kept the same. Therefore, neglecting the influence of contact resistance, the worse-case programming time can be reduced from 90 μs to 3.6 μs. If taking into account contact resistance, since it increases when contact area is reduced, the actual reduction of programming time should be less than 25 times.

In section 4.7, the programming speed of the proposed pixel circuit is further compared to those of some examples of conventional pixel circuits from literatures.

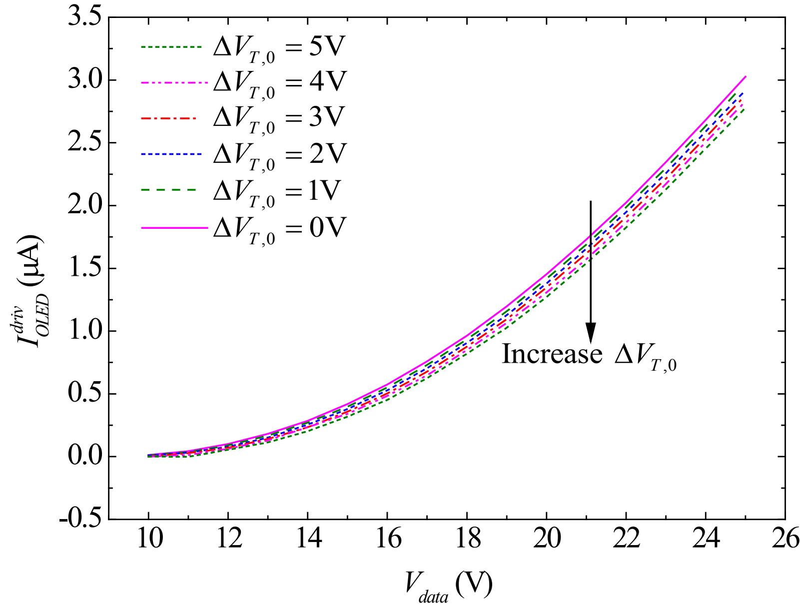


Figure 4.15: Simulated I_{OLED}^{driv} *vs.* V_{data} assuming $\Delta V_{OLED} = \Delta V_{T,0}/10$ [66].

4.4.8 OLED Aging

In previous sections, OLED aging is neglected. OLED actually ages over stress time. Its aging can be characterized as the increase of OLED voltage (ΔV_{OLED}) for a given OLED current density [74]. The impact of ΔV_{OLED} on I_{OLED}^{driv} was investigated by using circuit simulation. As an example, assuming $\Delta V_{OLED} = \Delta V_{T,0}/10$, Figure 4.15 shows that for $\Delta V_{T,0} = 5$ V, $\Delta I_{OLED}^{driv}/I_{OLED}^{driv}$ at $V_{data} = 25$ V is only 7.7%.

4.5 Justify Approximations and Assumptions

In previous sections, some approximations and assumptions are used in the analysis and design of the proposed pixel circuit. They are justified and discussed in this section.

4.5.1 OLED Aging and Voltage Shift

Assuming a drive TFT (T_0) and an OLED have typical sizes and the same stress condition in terms of current and temperature, referring to their aging models and data respectively

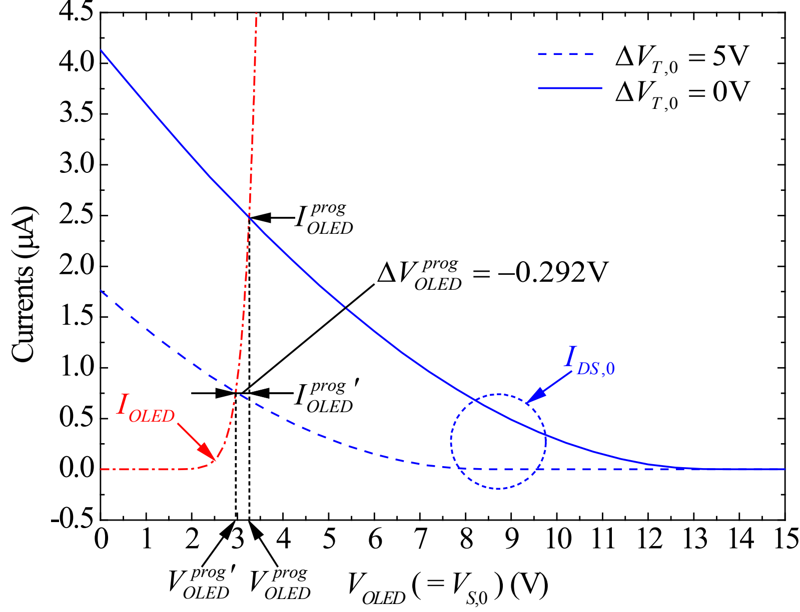


Figure 4.16: A significant $\Delta V_{T,0}$ leads to a small ΔV_{OLED}^{prog} due to the steep OLED *I*-*V* characteristic (for $V_{G,0}^{prog} = 16.7$ V) [66].

in [74] and [75], one can see that ΔV_{OLED} is much smaller than $\Delta V_{T,0}$. Based on this observation, several approximations are made as follows.

Since OLED *I*-*V* characteristic is steep, the ΔV_{OLED}^{prog} caused by $\Delta V_{T,0}$ is negligible:

$$dV_{OLED}^{prog}/dV_{T,0} \approx 0. \tag{4.35}$$

This is illustrated in Figure 4.16. V_{OLED}^{prog} (I_{OLED}^{prog}) and $V_{OLED}^{prog}{}'$ ($I_{OLED}^{prog}{}'$) are the OLED voltages (currents) in programming phase for $\Delta V_{T,0} = 0$ V and 5 V, respectively. Besides, $\Delta V_{OLED}^{prog} = (V_{OLED}^{prog}{}' - V_{OLED}^{prog})$. For $\Delta V_{T,0} = 5$ V, Figure 4.16 shows that $|\Delta V_{OLED}^{prog}| = 0.292$ V, which is only 5.84% of $\Delta V_{T,0}$, so Eq. (4.35) is reasonable.

In driving phase, assuming $\Delta V_{T,0}$ is fully compensated and OLED aging is negligible, I_{OLED}^{driv} does not change with $\Delta V_{T,0}$, so V_{OLED}^{driv} does not change with $V_{T,0}$:

$$dV_{OLED}^{driv}/dV_{T,0} \approx 0. \tag{4.36}$$

4.5.2 $\Delta V_{T,1}$ and $\Delta V_{T,3}$

Two observations about ΔV_T of TFTs are useful for circuit analysis. First, for a practical display with N rows of pixels, the total stress time spent in programming phases is only $1/N$ of that spent in driving phases. Second, for a typical refresh rate (*e.g.*, 60 Hz), the effect of negative pulse gate stress voltage on ΔV_T is much less significant than that of positive pulse gate stress voltage [38]. These two observations imply that only the ΔV_T of the TFTs stressed by positive gate voltages in driving phase are considerable. Therefore, $\Delta V_{T,1}$ and $\Delta V_{T,3}$ can be considered as negligible when compared to $\Delta V_{T,0}$ and $\Delta V_{T,2}$:

$$dV_{T,1}/dV_{T,0} \approx 0, \tag{4.37}$$

$$dV_{T,3}/dV_{T,0} \approx 0. \tag{4.38}$$

4.5.3 $V_{GS,0}^{driv}$ and $V_{GS,2}^{driv}$

Since the gates of T_0 and T_2 are connected, their gate voltages are the same. Their source voltages in driving phase can be made approximately the same. V_2^L is a fixed value provided by a row driver. V_{OLED}^{driv} is not fixed because it depends on V_{data}. However, since OLED has a steep I-V characteristic, the variation range of V_{OLED}^{driv} is much narrower than that of $V_{G,0}^{driv}$. If V_2^L is selected close to V_{OLED}^{driv}, since $V_{GS,0}^{driv} = \left(V_{G,0}^{driv} - V_{OLED}^{driv}\right)$ and $V_{GS,2}^{driv} = \left(V_{G,0}^{driv} - V_2^L\right)$,

$$V_{GS,0}^{driv} \approx V_{GS,2}^{driv}. \tag{4.39}$$

As indicated in Figure 4.17(a), V_2^L is selected as 2 V so that it is lower than but still close V_{OLED}^{driv}. This guarantees $\Delta V_{T,2} > \Delta V_{T,0}$ to enable $\Delta V_{T,0}$-compensation (refer to Eq. (4.17)). Figure 4.17(b) shows that $\left(V_{GS,2}^{driv}/V_{GS,0}^{driv}\right) \in (1,\ 1.1)$, so Eq. (4.39) is justified.

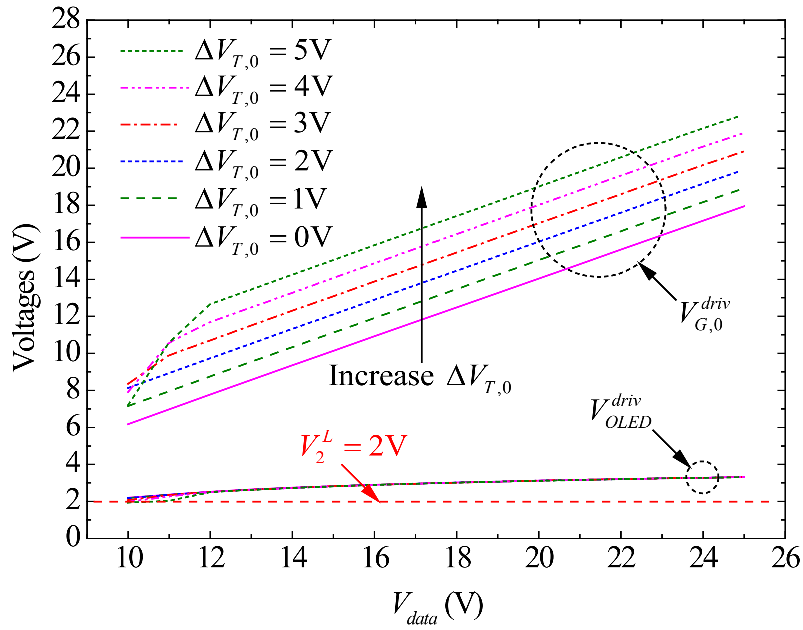
4.5.4 $\Delta V_{T,0}$ and $\Delta V_{T,2}$

$\Delta V_{T,0}$ and $\Delta V_{T,2}$ depend on the voltage stress history of T_0 and T_2. The parts of $\Delta V_{T,0}$ and $\Delta V_{T,2}$ caused by the voltage stress in programming phase are negligible because programming phase is much shorter than driving phase. In driving phase, T_0 is stressed in saturation region, but T_2 is stressed in linear region. Since $V_{GS,0}^{driv} \approx V_{GS,2}^{driv}$ (see Eq. (4.39)),

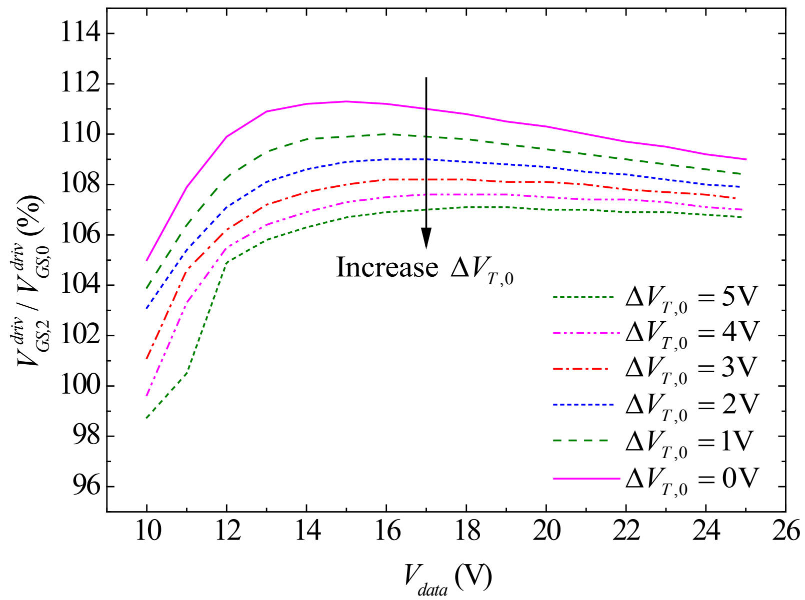
$$dV_{T,0}/dV_{T,2} \approx 2/3, \tag{4.40}$$

as discussed in [56]. Substituting Eq. (4.39) and Eq. (4.40) into Eq. (4.11) yields

$$dV_{GS,2}^{driv}/dV_{T,2} \approx 2/3. \tag{4.41}$$



(a)



(b)

Figure 4.17: Simulation results of (a) $V_{G,0}^{driv}$ and V_{OLED}^{driv} *vs.* V_{data}, (b) $(V_{GS,2}^{driv}/V_{GS,0}^{driv})$ *vs.* V_{data} in the proposed pixel circuit [66].

4.5.5 Estimating $\Delta V_{T,0}^{Tol}$ for a Given $I_{OLED}^{driv,Tol}$

As defined in section 4.4.4, for a given $I_{OLED}^{driv,Tol}$, $\Delta V_{T,0}^{Tol}$ is the boundary of $\Delta V_{T,0}$ between being fully-compensated and under-compensated. If $\Delta V_{T,0} = \Delta V_{T,0}^{Tol}$, T_2 in driving phase is at the boundary between ON and OFF, so $V_{GS,2}^{driv} = V_{T,2} = \left(V_T^{init} + 3/2\Delta V_{T,0}^{Tol}\right)$ (refer to Eq. (4.40)). Substituting this formula and Eq. (4.39) into Eq. (4.10) yields

$$I_{OLED}^{driv,Tol} = \alpha_{sat}\ \mu_n C_i \frac{W}{L} \frac{\left(\Delta V_{T,0}^{Tol}/2\right)^{\gamma+2}}{V_{AA}^{\gamma}}. \tag{4.42}$$

Then, normalizing Eq. (4.42) against Eq. (4.10) yields Eq. (4.16).

4.6 Measurement Results

4.6.1 Circuit Samples and Measurement Setup

The samples of the proposed pixel circuit were fabricated on glass substrate by using an in-house BCE a-Si:H technology in Giga-to-Nanoelectronics (G2N) Centre in the University of Waterloo. The minimum channel length in circuit samples was selected as 25 μm to guarantee yield. The values of the design variables used in the circuit samples are listed in Table 4.2. Figure 4.18 is the optical microphotograph of a fabricated sample of the proposed pixel circuit on glass substrate.

The schematic of the setup of aging test is presented in Figure 4.19(a). A photograph of instruments and a Cascade® Summit® 12000 probe station is shown in Figure 4.19(b). Layouts were so designed that the samples can be tested by using either regular probe needles or an advanced probe card, as illustrated in Figure 4.20(a) and 4.20(b), respectively.

The samples of the proposed pixel circuit were driven by the driving scheme presented in Figure 4.3(b). As shown in Figure 4.19(a), to generate the pulse voltage signals required by the driving scheme, Fluke® 294 Arbitrary Waveform Generator was used as the function generator, whose pulse voltage was shifted up from $(0 \sim 10)$ V to $(0 \sim 20)$ V by off-the-shelf voltage level shifters. Two groups of diodes, capacitors, and potentiometers were used to set the delays of the edges of V_2 and V_3 with respect to that of V_1 at the end of programming phase. An off-the-shelf Op-Amp was used as a current-to-voltage converter to convert I_{OLED} to V_{out}, which was monitored by using a LeCroy® WaveRunner® 6100A oscilloscope. BNC and tri-axial cables were used for shielding and guarding. An off-the-shelf Op-Amp was used as a voltage follower to drive the guarding layer of tri-axial cable.

Table 4.2: Design Variables of Proposed Pixel Circuit used in Tape-Out

Design Variable	Value	Design Variable	Value
W_0/L_0 (μm)	100/25	V_{DD} (V)	20
W_1/L_1 (μm)	50/25	$V_{1,2,3}$ (V)	$0 \sim 20$
W_2/L_2 (μm)	$75/(50, 75, 100)$	I_{OLED}^{driv} (μA)	$0 \sim 1.4$
W_3/L_3 (μm)	50/75	L_{ov} (μm)	5

The $\Delta V_{T,0}$-compensation of the proposed pixel circuit was verified by aging tests. $V_{DD} = 20$ V and $V_{data} = 15$ V were used. The low and high levels of V_1, V_2, and V_3 were zero and 20 V, respectively. Since the primary purpose of aging test was to verify $\Delta V_{T,0}$-compensation, OLED mimic (*i.e.*, diode-connected TFT) was excluded by setting V_{SS} as open-circuit. $I_{DS,0}^{driv}$ was measured from pad $V_{S,0}$, which was set at virtual ground.

4.6.2 $\Delta V_{T,0}$-Compensation

At the beginning of aging test, the measured $I_{DS,0}^{driv}$ of the sample of the proposed pixel circuit with $L_2 = 100$ μm was $I_{DS,0}^{driv} = 1.05$ μA. For comparison, an aging test was carried out on another sample whose $\Delta V_{T,0}$-compensation was disabled by fixing V_2 and V_3 at 20 V, so that this sample is equivalent to a conventional 2-TFT voltage-programmed pixel circuit (see Figure 4.1). To make it also have $I_{DS,0}^{driv} = 1.05$ μA at the beginning of aging test, its V_{data} was adjusted to 15.5 V. The measurement results shown in Figure 4.21(a) verify that the overall variation of the $I_{DS,0}^{driv}$ of the proposed pixel circuit in a 240-hour aging test is less than 9%. In contrast, the overall variation of $I_{DS,0}^{driv}$ of conventional 2-TFT pixel circuit, which does not provide $\Delta V_{T,0}$-compensation, is larger than 35% in 130 hours. Therefore, the stability of the proposed pixel circuit under voltage stress is much better than that of conventional 2-TFT pixel circuit.

Note that Figure 4.21(a) also indicates that, although $\Delta V_{T,0}$ is compensated, $I_{DS,0}^{driv}$ still has residual instability. It could be caused by some second-order effects, including non-zero $\Delta V_{T,1}$ and $\Delta V_{T,3}$, and/or variations of F_{dis} during aging test. To remove the over-compensation at the early stage of aging test, the size of T_2 can be decreased to reduce compensation strength. As shown in Figure 4.21(b), the aging test result of another sample

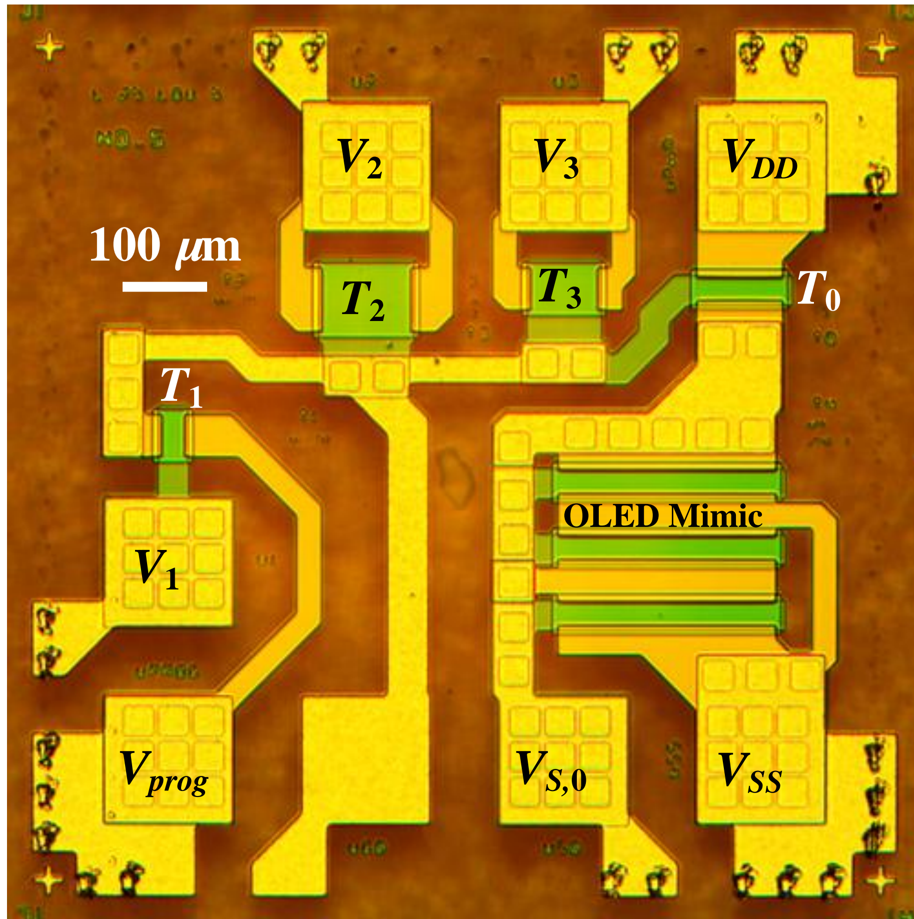
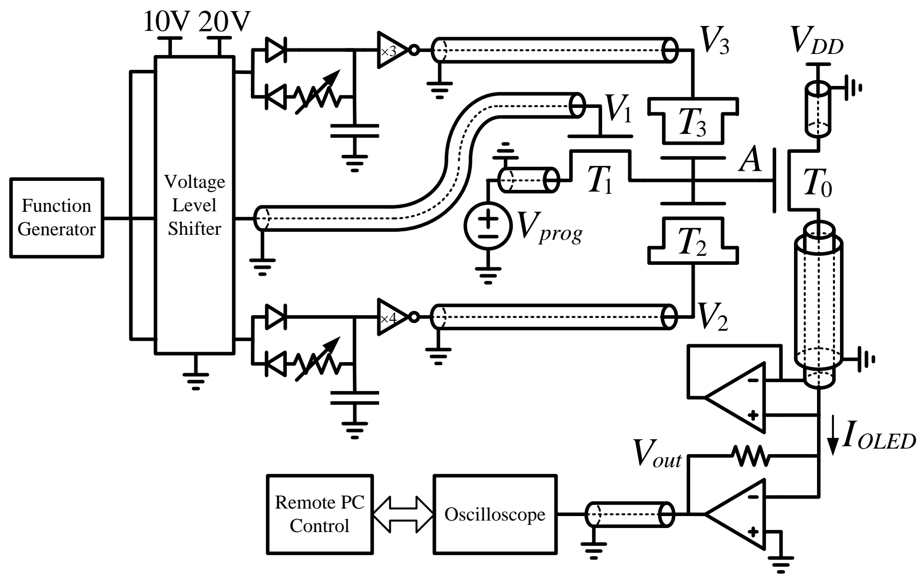
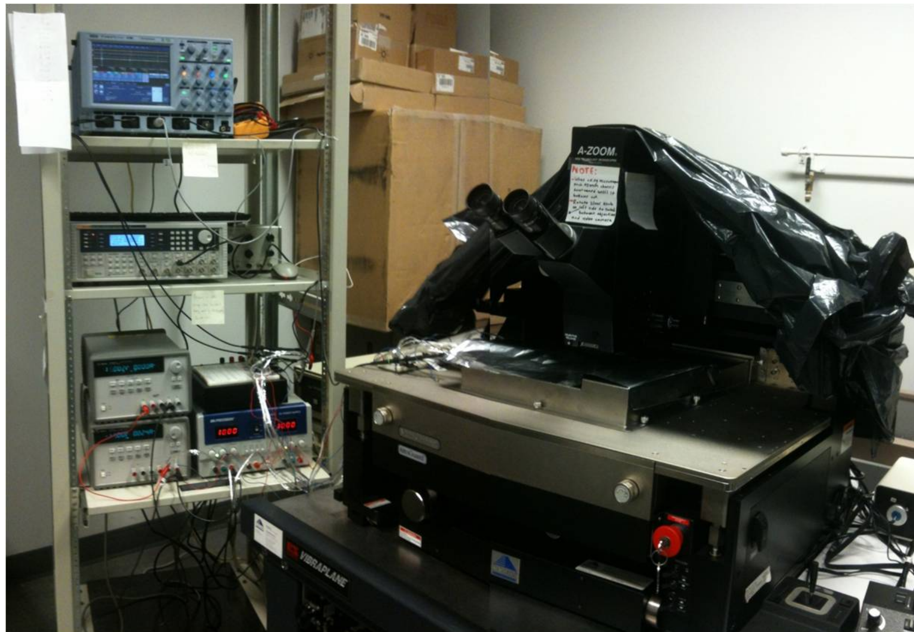


Figure 4.18: Sample of the proposed pixel circuit fabricated on glass substrate [68].

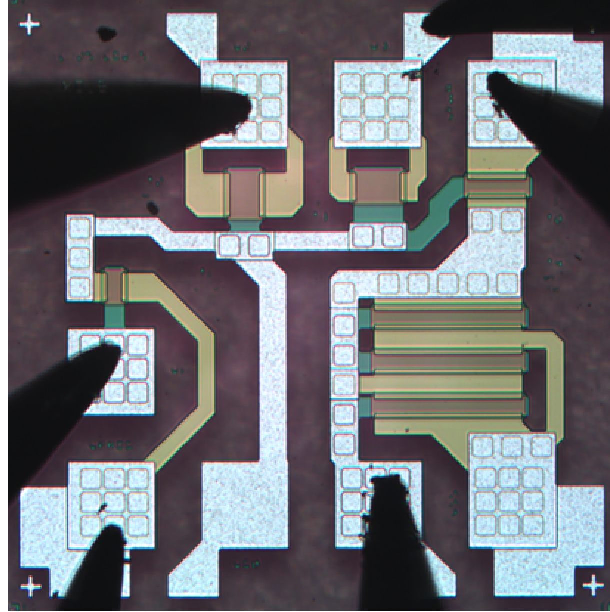


(a)

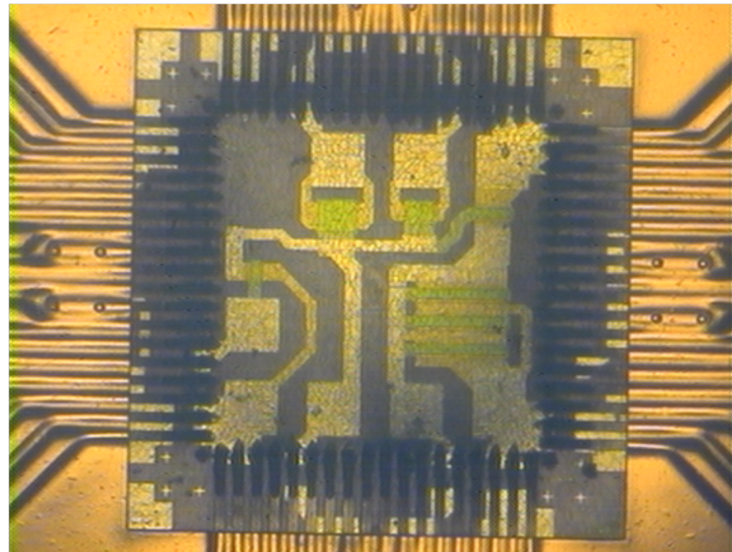


(b)

Figure 4.19: The setup of the aging test of the proposed pixel circuit by using a Cascade® Summit® 12000 probe station: (a) schematic and (b) photograph.



(a)



(b)

Figure 4.20: Test the samples of the proposed pixel circuit by using (a) probe needles and (b) a probe card installed on a Cascade® Summit® 12000 probe station.

of the proposed pixel circuit with $L_2 = 75$ μm indicates that the over-compensation at the early stage of aging test was removed by reducing the size of T_2.

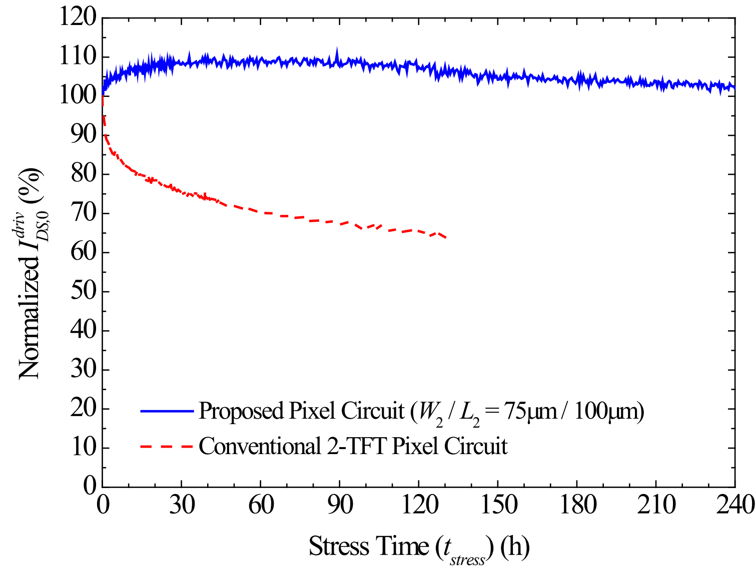
Figure 4.22(a) shows the measured transfer characteristics of T_0 in the sample of the proposed pixel circuit before and after the 240-hour aging test. The extracted $\Delta V_{T,0} \approx 2$ V is close to the result extracted from C-V measurements (see Figure 4.23). Figure 4.22(a) indicates that $\Delta V_{T,0}$ would have caused significant reduction of $I_{DS,0}^{driv}$ if $\Delta V_{T,0}$-compensation had not been used during the 240-hour aging test. In contrast, Figure 4.22(b) shows that, since $\Delta V_{T,0}$-compensation was used in the 240-hour aging test, except for the lowest $I_{DS,0}^{driv}$ levels, the variations of $I_{DS,0}^{driv}$ caused by $\Delta V_{T,0}$ were not significant. The under-compensation of $\Delta V_{T,0}$ at the lowest $I_{DS,0}^{driv}$ levels (zero to 0.15 μA) is discussed in section 4.4.4.

4.6.3 TFT V_T-Shifts

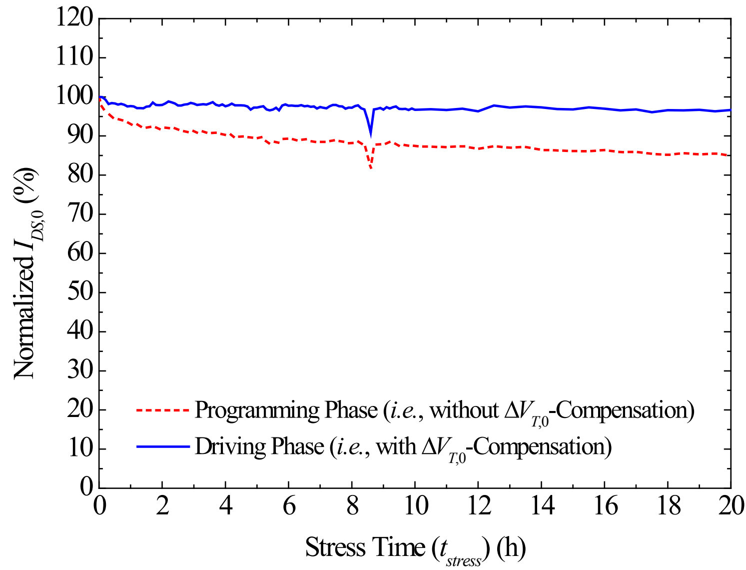
The assumptions about the ΔV_T of TFTs (refer to section 4.5.2 and 4.5.4) used in circuit analysis are verified by the C-V measurements on the TFTs in the sample of the proposed pixel circuit used in the 240-hour aging test. As shown in Figure 4.23, after the 240-hour aging test, $\Delta V_{T,0} \approx 2.15$ V and $\Delta V_{T,0} \approx 3.15$ V, so their ratio is close to the assumed 2/3 (see Eq. (4.40)). Besides, $\Delta V_{T,1}$ and $\Delta V_{T,3}$ are much smaller than $\Delta V_{T,0}$ and $\Delta V_{T,2}$, so it is fine to neglect $\Delta V_{T,1}$ and $\Delta V_{T,3}$ in first-order analysis (see Eq. (4.37) and (4.38)).

4.6.4 Settling-Down Time in Programming Phase

As shown in Figure 4.24, the programming speeds of the proposed pixel circuit were measured before and after the 240-hour aging test for V_{prog} switching from 5 V to 15 V (V_{prog}: $L \rightarrow H$) and from 15 V to 5 V (V_{prog}: $H \rightarrow L$). In this test, a FPGA card was used to generate control signals ($V_{1,2,3}$) and input signal (V_{prog}). In the worse case of settling-down time, $I_{DS,0}$ in programming phase settled down within 95% of its final value in 250 μs. If the minimum channel length of the TFTs used in the proposed pixel circuit is reduced to 5 μm (which is typically used in industry), programming speed should be even faster.

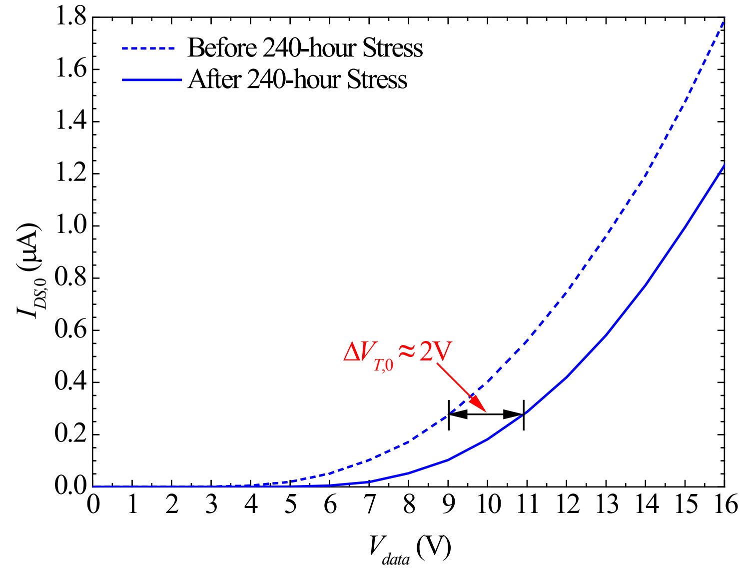


(a)

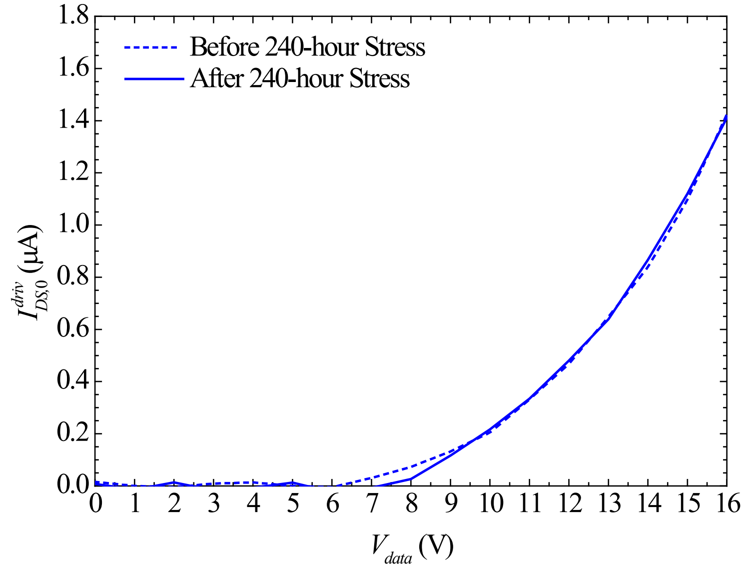


(b)

Figure 4.21: Aging test results. (a) Normalized $I_{DS,0}^{driv}$ *vs.* stress time. Temperature = 40 °C, programming time = 40 μs, $I_{DS,0}^{driv}$ (t_{stress} = 0) = 1.05 μA [68]. (b) Normalized $I_{DS,0}^{prog}$ and $I_{DS,0}^{driv}$ *vs.* stress time measured from a sample of the proposed pixel circuit with L_2 = 75 μm. Temperature = 23 °C, programming time = 800 μs, $I_{DS,0}^{driv}$ (t_{stress} = 0) = 0.66 μA.



(a)



(b)

Figure 4.22: Measurement results from a sample of the proposed pixel circuit with $L_2 = 100$ μm [68]. (a) The transfer characteristics of T_0 (measurement temperature = 23 °C), (b) $I_{DS,0}^{driv}$ *vs.* V_{data} of the proposed pixel circuit (measurement temperature = 40 °C).

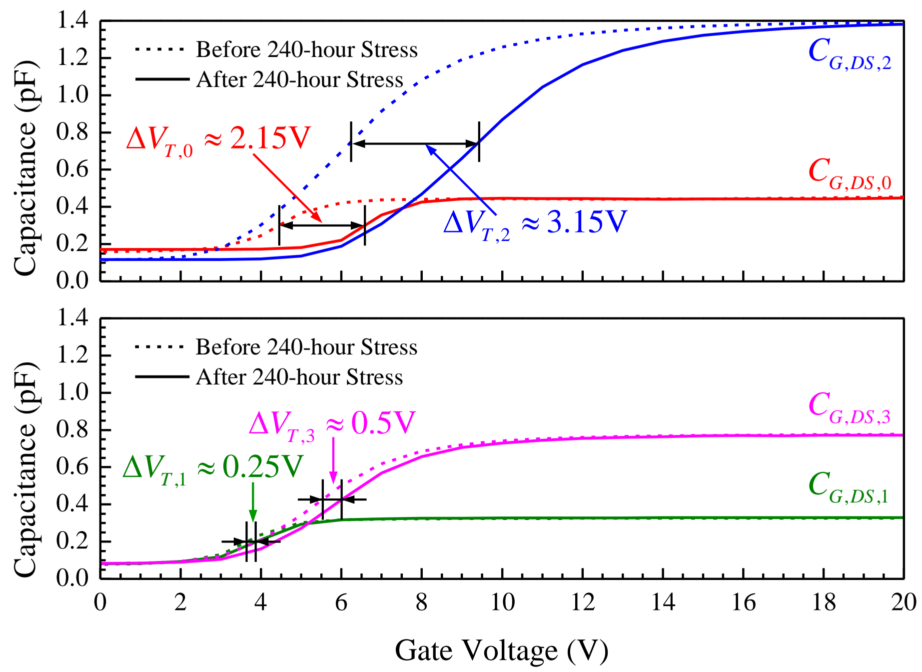


Figure 4.23: C-V measurement results of the TFTs in the sample of the proposed pixel circuit with $L_2 = 100\ \mu$m [68]. Measurement temperature = 23 °C.

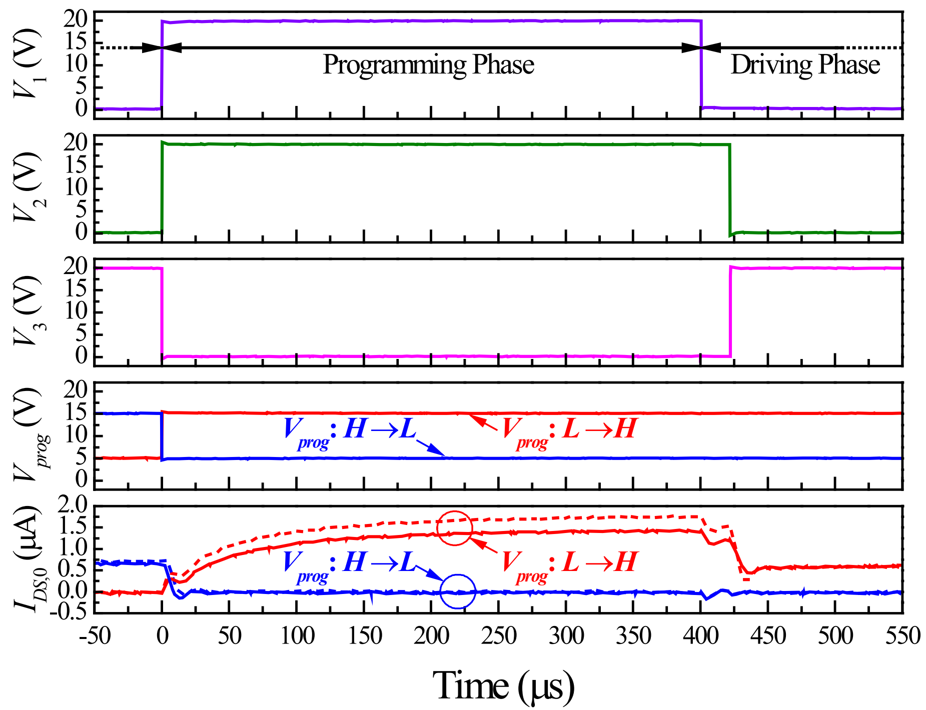


Figure 4.24: Measurement results of control signals and $I_{DS,0}$ *vs.* time of the proposed pixel circuit [68]. For $I_{DS,0}$, dash curves are the data before the 240-hour aging test, while solid curves are the data after the aging test. Measurement temperature = 23 °C.

4.7 Comparison to Conventional Pixel Circuits

4.7.1 ΔV_T-Compensation

The ΔV_T-compensation capability of the proposed pixel circuit is compared to those of conventional voltage-programmed pixel circuits which use V_T-generation techniques. In the first example, when the I_{OLED}^{driv} of a conventional 2-TFT pixel circuit drops by 35%, the one of the pixel circuit proposed in [76] increases by 8%, which is close to the maximum relative error (9%) of the I_{OLED}^{driv} of the proposed pixel circuit. In the second example, when $\Delta V_T = 2$ V, the I_{OLED}^{driv} of the pixel circuit proposed in [77] drops by about 5%, which is smaller than the maximum relative error (9%) of I_{OLED}^{driv} of the proposed pixel circuit. In the third example, when the I_{OLED}^{driv} of a conventional 2-TFT pixel circuit drops by 35%, the one of the pixel circuit proposed in [78] drops by 12.5%, which is larger than the maximum relative error (9%) of I_{OLED}^{driv} of the proposed pixel circuit. In the fourth example, when the I_{OLED}^{driv} of a conventional 2-TFT pixel circuit drops by 30%, the one of the pixel circuit proposed in [79] drops by 9%, which is the same to the maximum relative error (9%) of I_{OLED}^{driv} of the proposed pixel circuit.

The ΔV_T-compensation capability of the proposed pixel circuit is also compared to those of current-programmed pixel circuits. In the first example [80], when the ΔV_T of drive TFT is 2 V, the relative error of I_{OLED}^{driv} varies from 1.5% to 40% when I_{OLED}^{driv} is reduced from its maximum level to minimum level. In the proposed pixel circuit, the relative error of I_{OLED}^{driv}, which can be extracted from Figure 4.22(b), also increases when I_{OLED}^{driv} is reduced, and is larger than that of the current-programmed pixel circuit in [80]. The difference of ΔV_T-compensation capability is attributed to the fact that current-programmed pixel circuit can compensate not only ΔV_T but also other variations (*e.g.*, mobility, temperature, *etc*). In the second example [81], the relative error of I_{OLED}^{driv} after a 240-hour aging test is about 5.5%, while the maximum relative error of the proposed pixel circuit is 9%. Therefore, the ΔV_T-compensation capability of the current-programmed pixel circuit in [81] is better than that of the pixel circuit proposed in this thesis.

In short, the ΔV_T-compensation capability of the pixel circuit proposed in this thesis is similar to those of conventional voltage-programmed pixel circuits using V_T-generation techniques, but not as good as those of current-programmed pixel circuits. The aforementioned comparisons are summarized in Table 4.3. Symbol "+" is used to indicate a better ΔV_T-compensation capability.

4.7.2 Programming Speed

The durations of programming phase of the proposed and conventional pixel circuits are summarized in Table 4.3. Since the compared pixel circuits were not implemented by using the same sizing, their settling-down speeds in programming phase are not directly comparable. To make reasonable comparisons, a common base is needed. Therefore, assuming conventional pixel circuits (except for their OLEDs) are so scaled that the sizes of their drive TFTs become equal to the one of the proposed pixel circuit (*i.e.*, 100 μm / 25 μm), the settling-down speeds of conventional pixel circuits in programming phase are estimated in the footnotes below Table 4.3. The comparisons between the settling-down speed of the proposed pixel circuit and the ones converted from conventional pixel circuits indicate that the programming speed of the proposed pixel circuit is faster than or at least similar to the ones of conventional pixel circuits.

4.7.3 Simplicity and Power Consumption

The proposed pixel circuit also has advantages in terms of simplicity and power consumption, as summarized and compared in Table 4.3.

- In programming phase, the proposed pixel circuit does not need to use any sub-phase, whereas some conventional pixel circuits have to use multiple sub-phases for pre-charging, V_T-generating, and data inputting, requiring longer total programming time and more complicated external drivers.

- In the proposed pixel circuit, V_{DD} and V_{SS} are constant, V_{data} is constant in programming phase, and switch pulse voltages (*i.e.*, V_1, V_2, and V_3) are simple, so the proposed pixel circuit puts a minimal extra complexity on the design of external driver. In contrast, in some conventional pixel circuits, complicated pulse patterns and/or multiple voltage levels are used, complicating external driver design. Besides, in some conventional pixel circuits, V_{DD} or V_{SS} is a pulse voltage, so some transistors must be used in external driver between an external power supply and the bus line of V_{DD} or V_{SS}, resulting in a higher static power consumption.

- In programming phase, some conventional pixel circuits [76, 78] have to charge and discharge OLED capacitance, which is typically large (5 pF for a typical OLED size $(200 \times 100)\ \mu m^2$ [72]). In the proposed pixel circuit, the total capacitance on the gate of drive TFT in programming phase is only 2.23 pF, so dynamic power consumption is lower, and settling-down speed is faster.

Table 4.3: Comparison of Proposed Pixel Circuit (“Ckt 0”) to Conventional Voltage-Programmed Pixel Circuits (“Ckt 1” [76], “Ckt 2” [77], “Ckt 3” [78], and “Ckt 4” [79]) and Current-Programmed Pixel Circuits (“Ckt 5” [80] and “Ckt 6” [81]).

Pixel Circuit		Drive TFT	Compensate		Programming Phase		V_{DD} and V_{SS}		Data Signal		Switch Pulses		OLED		TFT and Capacitors			Bus Lines
Name	Type	W/L (μm/μm)	ΔV_T	ΔV_{OLED}	Time (μs)	Sub-Phases	Pattern	Levels (V)	Pattern	Levels	Pattern	Levels (V)	TFTs in I_{OLED} Path	Location	Area (μm^2)	TFTs	Cap.s	
Ckt 0	Proposed: Voltage Programmed; Charge Compensation	100/25	Good	Partial	250	1	Constant	V_{DD}=20 $V_{SS}=0$	Constant	V_{data}	Simple	0 (1) ~ 20	1	Source	13125	2	2 MIS	6
Ckt 1	Conventional: Voltage Programmed; V_T-Generation	400/23	Good	Partial	1000 (2)	4	Complex V_{SS} Pulse	V_{DD} = N/A V_{SS} = 28, 17, 0	Pulse	N/A	Complex	N/A	1	Drain (3)	19117	3	2 MIM	5
Ckt 2		400/23	Good+	Partial	70 (4)	2	Constant	N/A	Constant	V_{data}	Simple	0~30 -5~25	2	Source	26823	5	1 MIM	6
Ckt 3		400/23	Fine	Partial	250 (2)	3	Complex V_{DD} Pulse	V_{DD} = -10, 4~6, 20 $V_{SS}=0$	Pulse	V_{data} to 2V	Simple	-5V~25	1	Source	14000	2	1 MIM	4
Ckt 4		200/3.5	Good	N/A	30 (5)	3	Constant	$V_{DD}=20$ $V_{SS}=0$	Constant	V_{data}	Simple	-10V~25	2	Source	4315	6	1 MIM	5 (6)
Ckt 5	Conventional: Current Programmed	50/4	Good++	Partial	60 (7) 330 (8)	1	Constant	$V_{DD}=30$ $V_{SS}=0$	Constant	I_{data}	Simple	0~30	2	Source	32680	4	2 MIM	5
Ckt 6		750/23	Good+	N/A	120 (9)	1	Simple V_{DD} Pulse	V_{DD} = 4~20 $V_{SS}=0$	Constant	I_{data}	Simple	0~20	1	Source	126010	3	1 MIM	4

(1) $V^L_{1,2,3}=0$ V was used in aging tests because $V_{S,0}$ was connected to virtual ground. If OLED is included, V^L_2 should be set at a level close to V^{driv}_{OLED} (refer to section 4.5.3), and $V^L_{1,3}$ can be selected as equal to V^L_2 to simplify system design.

(2) In this circuit, OLED capacitance has a significant contribution to settling-down time. As a rough estimation, assuming OLED capacitance dominates the time constant of settling-down. Besides, assuming OLED size is fixed, OLED capacitance is fixed. If the whole pixel circuit (except for OLED) is so scaled that the W/L of drive TFT becomes 100μm/25μm, the drive strengths of TFTs reduce by about 4 times, so settling-down time increases by about 4 times. If taking into account the reduction of TFT capacitances, the actual settling-down time should increase by a ratio between 1 and 4.

(3) Using OLED at the drain of drive TFT may add extra complexity to the process in which OLED is integrated onto TFT back plane.

(4) This programming time was used, instead of measured, in measurements. In this circuit, V_T–generation sub-phase is ended before the gate voltage of drive TFT fully settles down. The time needed for a full settling-down is not reported.

(5) For this circuit, if the whole pixel circuit (except for OLED) is so scaled that the W/L of drive TFT becomes 100μm/25μm, storage capacitance increases by 3.57 times, while the drive strengths of TFTs reduce by 14.29 times, so the settling-down time of the scaled pixel circuit in programming phase should increase by 51.02 times, i.e., becomes 1530μs.

(6) This pixel circuit requires a direct connection from a TFT to OLED cathode. This requirement may add extra complexity to the process in which OLED is integrated onto TFT back plane.

(7) Authors did not take into account the parasitic capacitance of I_{data} bus line. Besides, this programming time was measured in simulation instead of measurement, at $I_{data}=1\mu$A. The a-Si:H TFT model in Synopsys Hspice, which was used by the authors, does not take into account the finite response speed of TFT channel. Therefore, the simulated settling-down time may be under-estimated. Besides, if the whole pixel circuit (except for OLED) is so scaled that the W/L of drive TFT becomes 100μm/25μm, storage capacitance increases by 12.5 times, while the drive strengths of TFTs reduce by 3.13 times, so settling-down time increases by 39.06 times, i.e., becomes 2344μs.

(8) This programming time was used, instead of measured, in measurements.

(9) Measured at $I_{data}=5.2\mu$A. Note that time constant is proportional to $(1/I_{data})^{1/2}$, so the worse-case settling-down time occurs when a minimum I_{data} is used. Assuming the minimum I_{data} is (5.2/100) μA, the worse-case settling-down time is 1200μs. If the whole pixel circuit (except for OLED) is so scaled that the W/L of drive TFT becomes 100μm/25μm, neglecting I_{data} bus line capacitance, settling-down time has no major change, because internal capacitance reduces by the same times as TFT resistance increases.

- The proposed pixel circuit uses only one TFT in OLED current path, while some conventional circuits [77, 79, 80] use multiple TFTs in the path. Given the same gate voltage of drive TFT, the more TFTs used in OLED current path, the higher V_{DD} is needed to achieve the same I_{OLED}^{drive}. Therefore, conventional pixel circuits using multiple TFTs in series in OLED current path have higher static power consumption.

4.8 Summary

In this chapter, a voltage-programmed pixel circuit using a novel ΔV_T-compensation mechanism is proposed. The proposed pixel circuit was developed to have fast programming speed and simple driving scheme, as well as ΔV_T-compensation capability. The novel ΔV_T-compensation mechanism and other design considerations are presented and discussed. The effectiveness of the proposed pixel circuit in ΔV_T-compensation and its programming speed are demonstrated by simulation and measurement results.

The proposed pixel circuit is also compared to conventional current-programmed and voltage-programmed pixel circuits. It is faster than or at least comparable to conventional pixel circuits because of its simplicity in circuit structure and operation. Besides, it uses a simple driving scheme and a constant power supply voltage, reducing the complexity of external driver. Also, it has lower power consumption. Although the ΔV_T-compensation capability of the proposed pixel circuit is not as good as those of current-programmed pixel circuits, it is similar to those of conventional voltage-programmed circuits. Therefore, the proposed pixel circuit is suitable for the applications which require fast programming speed, low power consumption, simple driving scheme as well as a certain level of ΔV_T-compensation capability.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

The development of AMOLED displays requires: (1) accurate compact device models of a-Si:H TFT for device characterization and circuit simulation; (2) a method to simulate the aging of a-Si:H TFT by using circuit simulator so that the impact of the aging of a-Si:H TFT on the stability of circuit performance can be investigated by using circuit simulation; and (3) novel pixel circuits to compensate the impact of the aging of a-Si:H TFT on the stability of pixel circuit performance. These challenges are addressed in this thesis.

The first contribution presented in this thesis is for the compact device model and parameter extraction of a-Si:H TFT. Several improvements and innovations for better accuracy and convergence were made to the compact device model of a-Si:H TFT. New parameter extraction methods with improved accuracy and consistency were also developed. The improved static and dynamic models and new parameter extraction methods of a-Si:H TFT are verified by measurement results.

The second contribution presented in this thesis is a method for circuit-level aging simulation of a-Si:H TFT. This simulation method uses differential equations to describe the ΔV_T of a-Si:H TFT so that ΔV_T can be simulated by using circuit simulator. The effect of the limited response speed of a-Si:H TFT on ΔV_T is taken into account. The developed ΔV_T model was implemented and inserted into a device model file of a-Si:H TFT. The proposed simulation method and ΔV_T model are verified by measurement results.

The third contribution presented in this thesis is a novel voltage-programmed pixel circuit developed for AMOLED displays. It uses a novel mechanism to compensate the

ΔV_T of a-Si:H TFT over stress time. The ΔV_T of drive TFT caused by voltage stress is compensated by an incremental gate-to-source voltage generated by utilizing the change of the charge transferred from drive TFT to a TFT-based MIS capacitor. A second MIS capacitor is used to inject positive charge to the gate of drive TFT to improve OLED drive current. The effectiveness of the proposed pixel circuit in ΔV_T-compensation is demonstrated by simulation and measurement results. The proposed pixel circuit is compared to several conventional pixel circuits. It has advantages in terms of fast programming speed, low power consumption, simple driving scheme, *etc.*

5.2 Future Work

For the compact device modeling of a-Si:H TFT, it is important to further investigate the static and dynamic model of contact region. This is especially important for short-channel TFTs, in which the behavior of contact region has a more significant impact on TFT performance. Besides, for short-channel TFTs, self-heating effect and channel length modulation should be further investigated. In addition, a more accurate dynamic model should be developed. Moreover, mechanical stress should be taken into account in TFT compact model, so that its impact on circuit performance can be investigated by using circuit simulation. Last but not the least, the accuracy of TFT model should be further verified by measurement results obtained from TFT-based circuits.

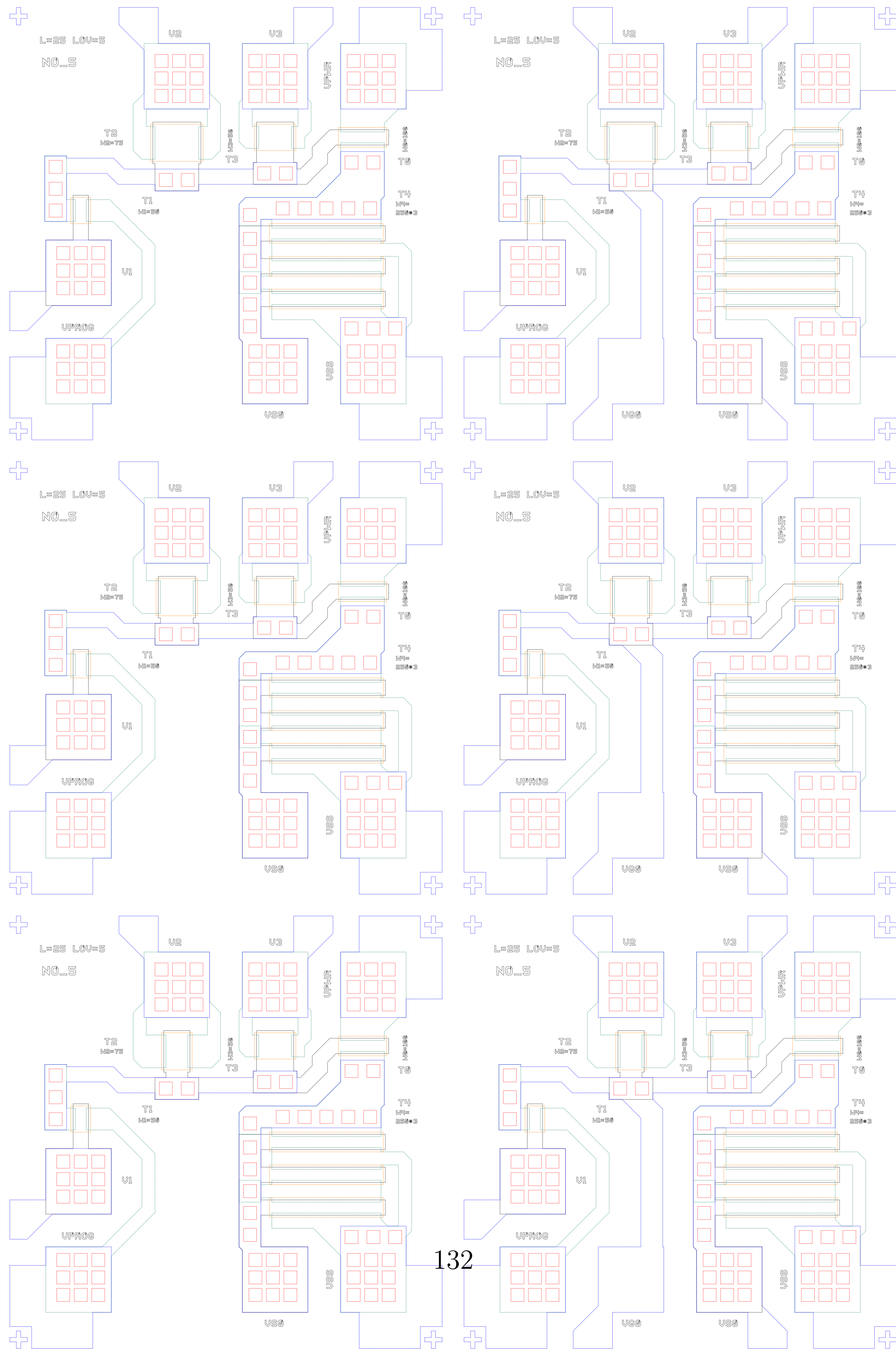
For circuit-level ΔV_T simulation, the presented method and model should be further verified by more aging tests with more different stress conditions on TFT-based circuits as well as discrete TFT samples. The method and model should also be further improved in terms of convergence and computational cost, especially for long-term ΔV_T simulation. Besides, the impacts of more stress variables (*e.g.*, temperature and mechanical stress) on ΔV_T should be included in circuit-level ΔV_T simulation.

To compensate ΔV_T, new pixel circuits using the proposed ΔV_T-compensation mechanism can be developed to further improve the accuracy of ΔV_T-compensation, accelerate programming speed, improve aperture ratio, and add the capability of ΔV_{OLED}-compensation. Besides, more investigations on the performance and stability of the proposed pixel circuit can be carried out in following aspects: (1) when using short-channel TFTs; (2) when using TFTs with materials other than a-Si:H; (3) when implemented on flexible substrate; and (4) when operated under different environmental temperatures.

APPENDICES

Appendix A

Layouts of Proposed Pixel Circuit


L=25 LOV=5
NO_5
V2
V3
VPWR
T2
W2=75
W3=50
T3
W0=100
T0
T1
W1=50
T4
W4=
250*3
V1
VPROG
VSS
VS0

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