Extended Bandwidth Doherty Power Amplifier for Carrier Aggregated Signals

by

Mehdi Naseri Ali Abadi

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

In the conventional classes of power amplifiers the efficiency drops at power back-off, whereas in order to maximize the spectral efficiency and data rate, wireless communication standards employ signals with high peak to average power ratio. This results in low average efficiency for power amplifiers, which in turn results in heavy cooling requirements and damage to the environment. To improve the low back-off efficiency Doherty technique has been widely investigated. But, the conventional Doherty power amplifiers are fairly narrowband, while modern transmitters are needed to support multiple standards and operate at multiple frequency bands.

This thesis proposes two novel output combiners for Doherty power amplifiers with extended bandwidth. It will be shown analytically how the problem of wideband Doherty can be converted into an impedance synthesization problem. Then two networks to synthesize the desired impedance are proposed. To achieve the proper load modulation over a wide bandwidth, the first proposed combiner employs a quarter-wave short-circuited stub at the output of the peaking transistor and the second proposed combiner uses a parallel LC tank at the same node.

In addition to inherent wideband characteristics, the proposed Doherty output combiners have three other important benefits. First, they present small low-frequency impedance for both the main and peaking transistors, which results in improved linearity and linearizability when the amplifier is concurrently driven with multi-band modulated signals. Second, the new combiners result in smaller group delay variation across the band compared to the conventional Doherty amplifier, which results in improved linearizability when the amplifier is driven with extra wideband modulated signals. Finally, the output capacitance of the peaking transistor can be easily absorbed into the combiners without compromising the performance of the amplifier.

The thesis starts with an overview of the Doherty power amplifier principles and provides a bandwidth analysis for the conventional Doherty power amplifier. Then it continues with the new approach to extend the bandwidth of Doherty amplifiers with respect to requirements of multi-band transmission. Based on the proposed combiners, two Gallium Nitride 20 W Doherty power amplifiers have been designed and fabricated. The measurement results have been provided to validate the developed theory. The first amplifer covers 1.72 GHz to 2.27 GHz and the second one covers 700 MHz to 950 MHz and both maintain higher than 48% of drain efficiency at 6 dB back-off across the band. The two amplifiers are successfully linearized when driven with carrier aggregated modulated signals.

Acknowledgements

I would like to thank my parents and my two brothers for their endless support. It is their unconditional love that motivates me to follow superior goals.

I would also want to thank my Master's supervisor, Dr. Slim Boumaiza, for his help and support throughout my studies as a Master student.

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Last, but not least, I would like to thank Dr. Peter Levine and Dr. Karim Karim for reading my thesis and giving their valuable comments.

Dedication

This is dedicated to my parents.

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Nomenclature

AC	Alternating Current
ACLR	Adjacent Channel Leakage Ratio
CW	Continuous Wave
DC	Direct Current
DE	Drain Efficiency
DPA	Doherty Power Amplifier
GaN	Gallium Nitride
HGA	High Gain Amplifier
HMET	High Electron Mobility Transistor
ITR	Impedance Transformation Ratio
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LNA	Low Noise Amplifier
LTE	Long Term Evolution
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
PDF	Probability Density Function
RFPA	Radio Frequency Power Amplifier

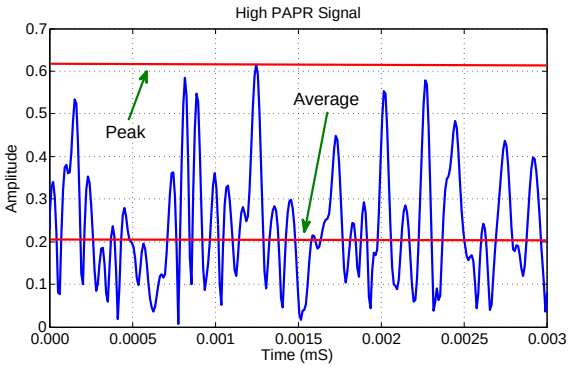
SRFT	Simplified Real Frequency Technique
WCDMA	Wideband Code Division Multiple Access

Chapter 1

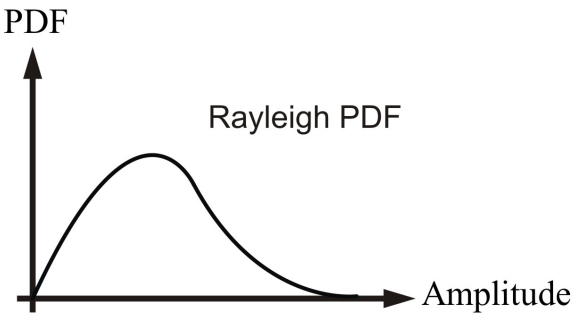
Introduction

1.1 Motivation

In order to maximize the spectral efficiency, wireless communication standards employ signals with a high peak to average power ratio (PAPR). An example of a high PAPR signal, four carrier Wideband Code Division Multiple Access (4C-WCDMA), is shown in Fig.1.1(a). The probability density function (PDF) of the amplitude of these signals follows the Rayleigh PDF, as shown in Fig.1.1(b). Efficient amplification of such high PAPR signals requires an amplifier which is linear and has high efficiency at power back-off as well as peak power.



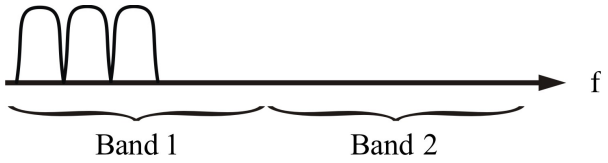
(a)



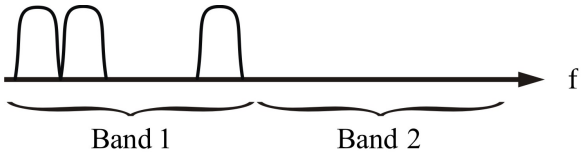
(b)

Figure 1.1: (a) The amplitude of 4C-WCDMA signal (b) Rayleigh PDF

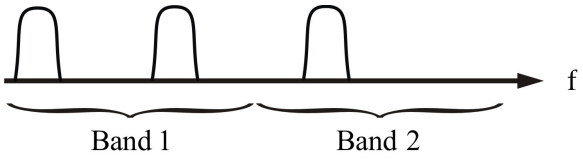
To further increase the bit-rate, the Long Term Evolution (LTE) Advanced uses carrier aggregation [1]. There are three different scenarios for carrier aggregation, which are shown in Fig.1.2. The first scenario in which all the component carriers are contiguous and are within the same operating frequency band is called intra-band contiguous and is illustrated in Fig.1.2(a). Depicted in Fig.1.2(b) is the case when carriers are within the same band but they are separated by a gap, or gaps, in between. This case is known as intra-band non-contiguous. Finally, when the carriers are in different bands it is called inter-band non-contiguous and is depicted in Fig.1.2(c). The amplification of such carrier aggregated signals requires an amplifier which is wideband and is capable of amplifying wideband and multi-band signals.



(a) Intra-band, contiguous



(b) Intra-band, non-contiguous



(c) Inter-band, non-contiguous

Figure 1.2: Different scenarios for carrier aggregation in LTE-Advanced

Therefore, future communication systems require radio frequency (RF) power amplifiers (PAs) which are linear, efficient and capable of supporting multiple standards and operating at multiple bands, even concurrently.

1.2 Problem Statement

In the conventional classes of power amplifiers (e.g. class-A, AB, B) the efficiency drops at power back-off. Therefore, amplification of high PAPR signals with such amplifiers results in low average efficiency, which in turn results in heavy cooling requirements. This not only increases the costs, but also causes damage to the environment.

To address the limited back-off efficiency of PAs, efficiency enhancement techniques such as Doherty [2] have been extensively investigated. Although the conventional Doherty power amplifiers (DPAs) are successful in improving the back-off efficiency, they are fairly narrow-band (less than 10%). Therefore, they are not suitable for wideband applications. Also, they usually fail to amplify carrier aggregated signals, especially when there is a large gap between the component carriers. Although, there have been several attempts to extend the bandwidth of DPA in recent years (a review of such works is provided in the next chapter), they have not addressed the case where the DPA is driven with carrier aggregated signals.

In this thesis, a novel approach to extend the bandwidth of DPA has been proposed. The proposed combiner is simple to implement and enables concurrent amplification of multi-band signals. A single PA which supports multiple communication bands results in cost and complexity reduction of base-station transmitters.

1.3 Thesis Organization

The organization of this thesis is as follows. Chapter two starts with an overview of conventional classes of RFPAs. Then it continues with a brief overview of the principles of operation of the conventional DPA followed by the bandwidth analysis. Finally a literature review of the previous works on wideband DPAs closes the chapter.

Chapter 3, which constitutes the core of the thesis, introduces the new approach to extend the bandwidth of the DPA. This approach converts the problem of wideband DPA into an impedance synthesization problem. In the rest of this chapter, two networks have been proposed to synthesize the desired impedance needed for a wideband DPA. Other characteristics of the new combiners are also discussed, including the group delay and low-frequency impedance. It has been explained why maintaining small low-frequency impedance is critical for successful linearization of the PA when it is concurrently driven with multi-band signals.

To verify the developed theory, two wide-band DPAs have been designed and fabricated based on the proposed combiners, the measurement results of which are presented in chapter 4. Finally, chapter 5 finishes with conclusions from the thesis.

Chapter 2

Overview of the Conventional Doherty Power Amplifier

2.1 Overview of RFPAs

A PA is an amplifier which amplifies power. In other words, its output power and power gain are important. The gain of a PA is defied as:

$$G = \frac{P_{out}}{P_{in}} \tag{2.1}$$

where P_{in} is the input RF power to the amplifier and P_{out} is the RF power delivered to the load in Watt. To deliver the power P_{out} to the load, the amplifier consumes Direct Current (DC) power from a DC source, i.e. P_{DC}. P_{DC} is higher than P_{out} and the difference would be dissipated as heat. If for the same amount of output power the amplifier consumes less DC power or in other words dissipates less power as heat the amplifier is more efficient. The efficiency (drain efficiency) of a PA is defined as:

$$Drain \;\; Efficiency = \eta = \frac{P_{out}}{P_{DC}} \tag{2.2}$$

The above figure of merit does not include the gain and input power to the PA. In fact, very efficient PAs can be designed with no gain. To include the gain, another figure of merit called the Power Added Efficiency (PAE) is defined is follows:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \eta(1 - \frac{1}{G}) \tag{2.3}$$

As can be seen, if the amplifier has a high gain ($G \to \infty$) the two values converge.

In a high gain amplifier (HGA) the input as well as the output are conjugate matched to maximize the gain. In a low noise amplifier (LNA)the input is noise matched to lower the noise figure and the output is conjugate matched to get a reasonable gain. In a power amplifier, however the input side is conjugate matched for the gain and the output side is power matched to get the maximum power out of the device. Assuming that the transistor can be modelled with an ideal current source, the power match at the output means terminating the drain with a resistance equal to so called R_{opt}, where R_{opt} is defined as:

$$R_{opt} = \frac{V_{DC}}{I_{max}/2} \tag{2.4}$$

where V_{DC} is the drain supply voltage (which approximately is equal to $V_{max}/2$) and I_{max} is the maximum allowed drain current. Terminating the output with R_{opt} ensures that the device is pushed into its limits in terms of voltage and current and hence maximum possible power can be delivered to the load without causing damage to the transistor.

2.1.1 Conventional Classes of Operation

The class of operation of a PA is defined based on the biasing point of the transistor and its load termination (both at the fundamental and at the harmonics). Fig.2.1 illustrates the transfer and output characteristics of a transistor, assuming that the transistor is modelled with an ideal voltage controlled current source. It is also assumed that the transistor has an abrupt turn on when the gate-source voltage (V_{GS}) reaches the threshold voltage (V_{th}) and has a sharp saturation when the current reaches its maximum.

In a class-A PA, the transistor is biased at $I_{max}/2$. The output current at peak input voltage has an amplitude equal to $I_{max}/2$ which is also equal to the its average. The drain bias voltage is half of the maximum allowed drain-source voltage, $V_{DS,max}/2$. In a class-A PA, the transistor consumes DC power even if the input voltage is equal to zero. As a mater of fact, because the output voltage and current are perfect sinusoids, their average is always equal to $V_{DS,max}/2$ and $I_{max}/2$, regardless of the input drive magnitude. Therefore, the efficiency at peak power can be calculated as:

$$P_{DC,A} = \frac{V_{max} * I_{max}}{4} \tag{2.5}$$

$$P_{out,A} = \frac{1}{2} * \frac{V_{max} * I_{max}}{4} \tag{2.6}$$

$$\eta_A = \frac{P_{out,A}}{P_{DC,A}} = \frac{1}{2} = 50\% \tag{2.7}$$

Therefore, a class-A PA has two major drawbacks: first it consumes power without the input drive and second, its peak efficiency is 50%, i.e. half of the consumed DC power will be dissipated as heat. The important benefit of a class-A PA is that it has the highest gain among all classes of operation.

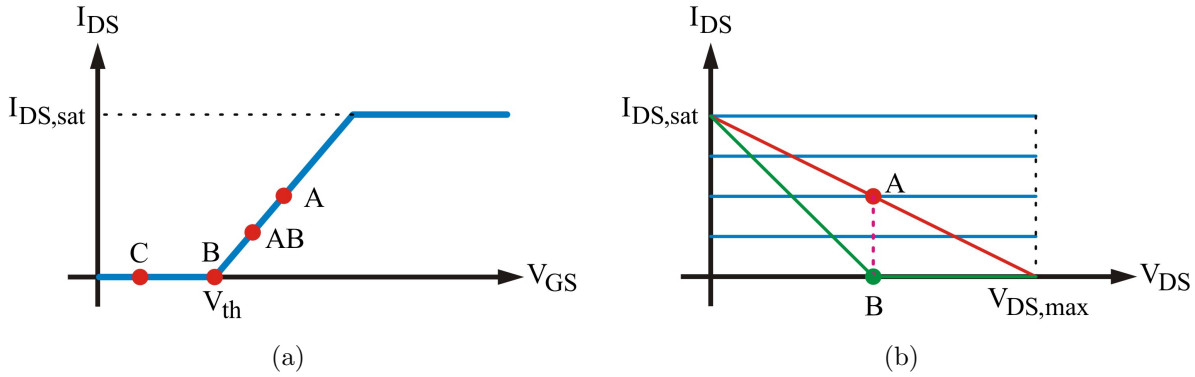


Figure 2.1: (a) Transfer and (b) Output characteristic of an ideal transistor

In order to increase the efficiency, the gate bias voltage can be moved towards the cut-off. In a class-B PA the gate bias is equal to the threshold voltage. Therefore, without the input signal, the transistor does not draw any DC current and therefore the consumed DC power is equal to zero. Also, the amplifier only conducts for half of the input cycle, so in a class-B PA the so called conduction angle is equal to π, as illustrated with purple curves in Fig.2.2.

The DC and fundamental components of a half sine current (as is the case in class B) are equal to I_{max}/π and $I_{max}/2$, respectively. Therefore, the efficiency at peak power can be calculated as:

$$P_{DC,B} = \frac{V_{max} * I_{max}}{2 * \pi} \tag{2.8}$$

$$P_{out,B} = \frac{1}{2} * \frac{V_{max} * I_{max}}{4} \tag{2.9}$$

$$\eta_B = \frac{P_{out,B}}{P_{DC,B}} = \frac{\pi}{4} = 78.5\% \tag{2.10}$$

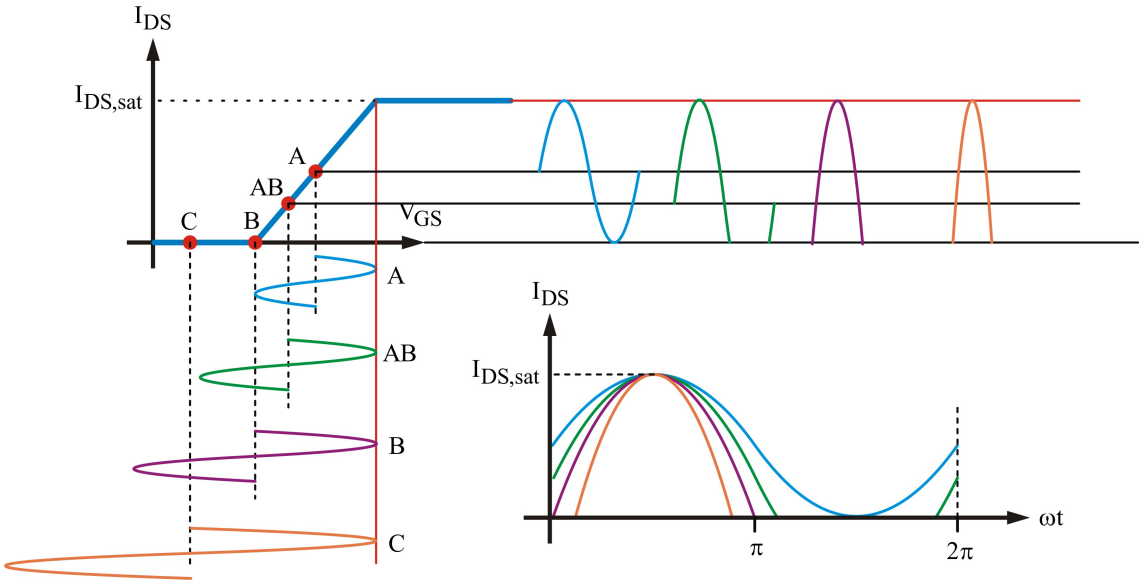


Figure 2.2: Current waveforms and conduction angles in different classes of operation

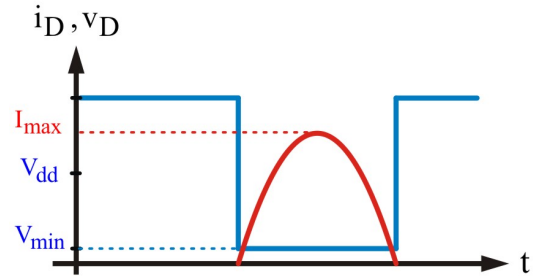
Therefore a class-B PA has two major benefits: first it consumes no DC power without the input drive and second, its peak efficiency is 78.5%, i.e. only 22.5% of the consumed DC power will be dissipated as heat. The disadvantage of a class-B PA is that the input drive should be doubled in order to push the transistor to its maximum limits. This means that the gain of a class-B PA is 6 dB lower than that of a class-A PA.

As the current waveform moves away from a perfect sinusoid, harmonic components start to appear at the output current. Therefore, in an ideal class-B mode, all the harmonics should be terminated with short-circuited impedance.

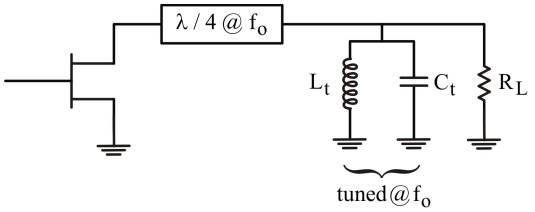
When the conduction angle is between π and 2π, the class of operation is called class AB. The efficiency at the peak power in this case is somewhere between 50% and 78.5%. Moving closer to class-B mode, the efficiency goes up while the gain goes down.

Finally, when the conduction angle is lower than π the PA is operating in class-C. The efficiency gets closer to 100% as the conduction angle gets closer to zero, although there would be no gain remaining there.

So far, it has been assumed that all the harmonics are terminated with a short circuited impedance. It can be shown that by proper use of harmonics higher efficiencies can be achieved, e.g. in class F. In a class-F PA the bias point is in the AB region (it is usually



(a) Class-F current and voltage waveforms



(b) An implementation of class-F PA

Figure 2.3: Class-F amplifier

very close to the class-B bias point). The voltage and current waveforms corresponding to this class of operation are square and half-sine waves, respectively, as shown in Fig.2.3(a), leading to ideally 100% drain efficiency at full rail-to-rail voltage swing. To achieve these waveforms, the required harmonic load terminations of the transistor should be as follows:

$$Z_L(f_o) = R_L \tag{2.11}$$
$$Z_L(2kf_o) = 0 \tag{2.12}$$
$$Z_L((2k+1)f_o) = \infty \tag{2.13}$$

Comparing a class-F PA with the class-B, one can conclude that,

$$V_m^F = \frac{4}{\pi} V_m^B \tag{2.14}$$

where V_m is the magnitude of fundamental drain voltage of the transistor, and F and B superscripts represent class-F and B quantities, respectively. Subsequently, the peak

output power of the two PAs can be written as

$$P_{out}^{B} = \frac{1}{2} V^{B} I^{B} \tag{2.15}$$

$$P_{out}^{F} = \frac{1}{2} V^{F} I^{F} \tag{2.16}$$

Assuming that the output power of the two cases are equal, one can deduce the relation between the required fundamental voltage and current components of the class-F PA at peak power in terms of those of the class-B PA, i.e.,

$$V^{F} = \frac{4}{\pi} V^{B} \tag{2.17}$$

$$I^{F} = \frac{\pi}{4} I^{B} \tag{2.18}$$

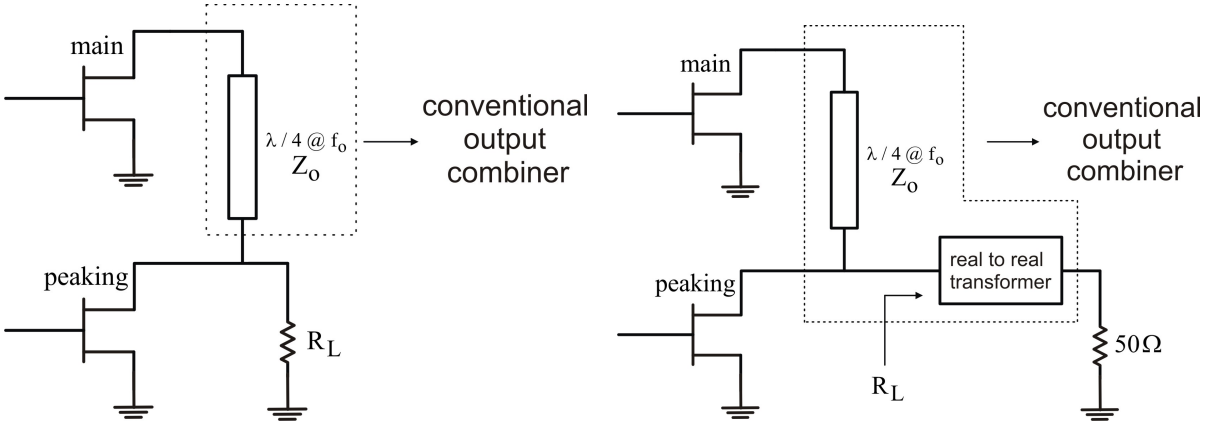
In other words, the maximum current provided by the class-F PA has to scale down by a factor of $\pi/4 = 0.785$ for the same output power. Therefore, the optimum load impedance of the class-F main transistor at full power can be calculated as

$$R_{opt}^{F} = \frac{V_{M}^{F}}{I_{M}^{F}} = \left(\frac{4}{\pi}\right)^{2} R_{opt}^{B} \tag{2.19}$$

Therefore, to get the ideal 100% efficiency, the transistor is needed to be terminated with the above impedance at the fundamental and with short circuit at even and open circuit at odd harmonics. Although in practice, the harmonic termination is usually realizable up to three harmonics. This gives a better efficiency than a class-B PA, but still far from the ideal 100% efficiency.

2.2 Conventional DPA (Principle of Operation)

Fig.2.4(a) depicts the schematic of a conventional DPA. Doherty power amplifier is suitable for efficiently amplifying high PAPR signals, since it maintains its peak efficiency over a certain range (e.g., 6 dB) of back-off, depicted in Fig.2.5. In order to do so, it uses an auxiliary (also called peaking) transistor to modulate the impedance seen by the main (also called carrier) transistor. The main and peaking transistors are operating in class B and C, respectively.



(a) The load impedance is equal to R_L

(b) A real-to-real impedance transformer transforms 50Ω to R_L

Figure 2.4: The schematic of conventional DPA combiner

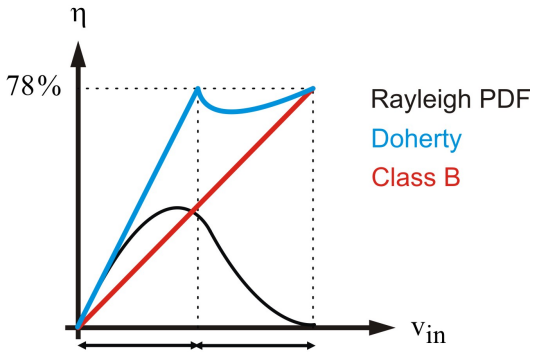


Figure 2.5: Comparison of the efficiency of class-B and Doherty PA

The characteristic impedance of the quarter-wave line that connects the drain of main and peaking transistors, Z_o, is equal to R_{opt} and the value of load impedance, R_L, is equal to $R_{opt}/2$, where R_{opt} is the optimum load impedance of the main transistor.

The drain current and voltage profiles of the main and peaking transistors are illustrated in Fig.2.6. These figures are drawn for the case when the second efficiency peak occurs at 6 dB back-off of the peak power, because the peaking transistor turns on when the input voltage is half of its maximum value.

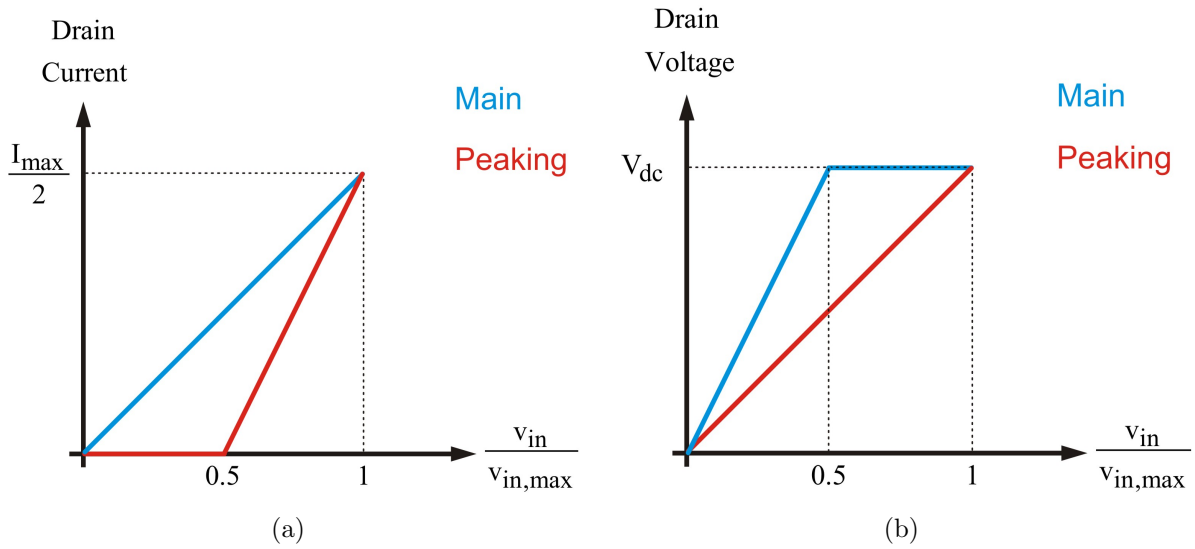


Figure 2.6: The drain (a) current and (b) voltage profiles of the main and peaking transistors in Doherty amplifier

Fig.2.6(b) shows that the voltage excursion of the main transistor is maximized in the upper half of the the input drive. Hence, it operates with its maximum efficiency in this region. In order to maintain linearity while keeping this maximum swing, the peaking current along with the quarter-wave inverter modulates the impedance seen by the drain of the main transistor as depicted in Fig.2.7.

In the first half of the input drive, only the main transistor contributes to the output power, while during the upper half the output power is a combination of the main and peaking output powers. This has been illustrated in Fig.2.8.

2.3 Bandwidth Analysis of Conventional DPA

For now,is has been assumed that $R_L = R_{opt}/2$ regardless of frequency (i.e., an ideal wideband real-to-real impedance transformer such as a tapered line with infinite length has been used; see Fig.2.4(a)). With this assumption, $R_m = real\{Z_m\}$ and $X_m = imag\{Z_m\}$ versus frequency can be plotted for the conventional DPA combiner, where Z_m is the impedance seen by the drain of the main transistor. It is also assumed that the transistors

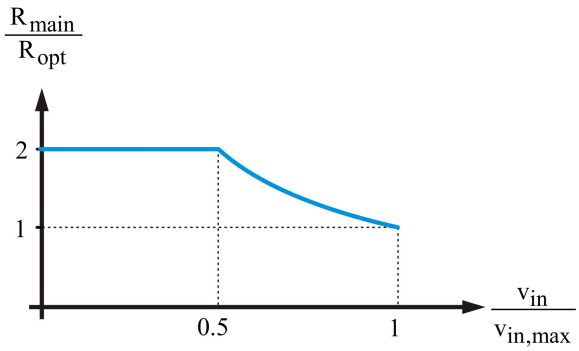


Figure 2.7: Modulation of the main impedance through the peaking current

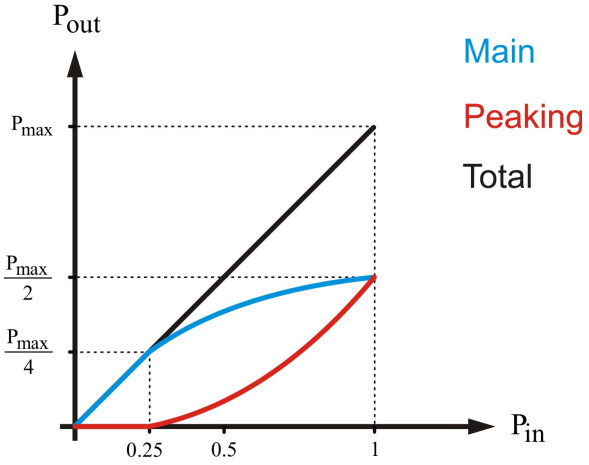


Figure 2.8: Contribution of the main and peaking transistors to the output power in Doherty amplifier

are ideal current sources, as depicted in Fig.2.9.

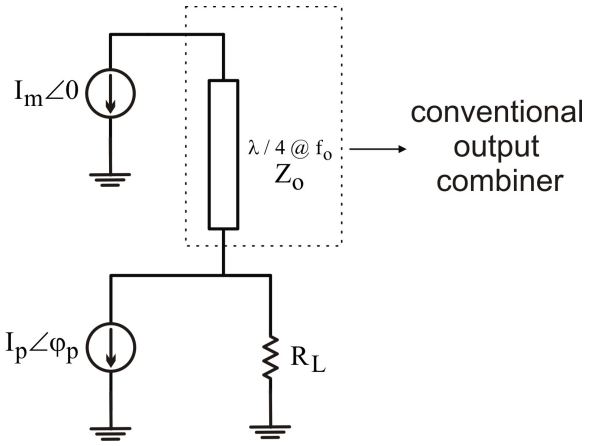
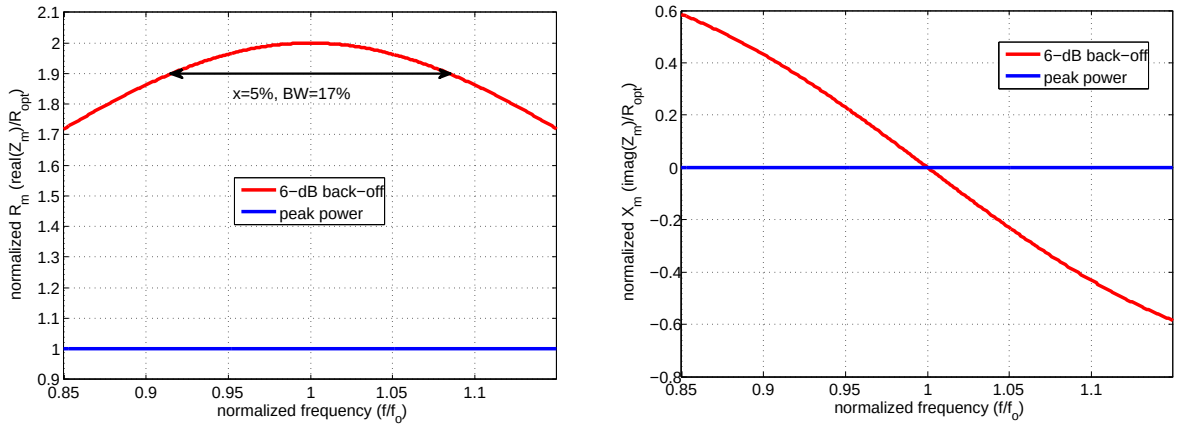


Figure 2.9: The conventional DPA output combiner with the transistors replaced with current sources

Fig.2.10 shows the normalized R_m and X_m at peak power and 6 dB back-off for the conventional DPA. It is important to note that since the load impedance is $R_{opt}/2$, these plots are valid for any DPA regardless of the power level. In this figure,it has been assumed that

- @ 6 dB back-off: $I_p = 0$
- @ peak power: $|I_p| = |I_m|$ & $\varphi_p = -\frac{\pi}{2} * \frac{f}{f_o}$, where f_o is the center frequency (this phase profile can be realized using a Wilkinson power divider with a quarter-wave line at the input of the peaking transistor).

Assuming 5% variation in R_m at back-off is acceptable within the bandwidth (this translates to a 5% reduction in efficiency), Fig.2.10(a) shows that the bandwidth of the conventional DPA is about 17%, irrespective of the value of R_{opt}. However, in practice, the larger output capacitances of the main and peaking transistors are more difficult to absorb in the combiner at high power levels and usually higher power translates to lower bandwidth. Fig.2.10(a) also illustrates that in a conventional DPA, as frequency deviates from the center frequency, the 6 dB back-off efficiency falls, but the peak power efficiency is constant versus frequency (if a Wilkinson divider has been used at the input).



(a) (b)

Figure 2.10: (a) R_m and (b) X_m of the conventional DPA output combiner at 6 dB back-off from peak power

The real-to-real transformer of Fig.2.4(b) transforms the 50Ω load to $R_{opt}/2$ and usually is a single-section quarter-wave transformer, a multi-section quarter-wave transformer, or a tapered line. At low power levels, where the impedance transformation ratio (ITR) is low (e.g., less than 4), the single-section quarter-wave transformer provides acceptable bandwidth and is preferable due to its physical length being smaller than the tapered line. Alternatively, at high power levels, where the ITR is high, the bandwidth of the single-section transformer limits the bandwidth of the amplifier and therefore using a double-section transformer or a tapered line is preferred.

The response of the real-to-real transformer versus frequency has an important impact on the performance of the conventional DPA. Here, the case where a single-section transformer has been used as the real-to-real impedance transformer is discussed as shown in Fig.2.11.

It is important to note that any plot in this section is dependent on R_{opt} and hence on the power level, because the 50Ω load is always constant and the performance of the real-to-real transformer is a function of its ITR. Here, the plots for the typical case of $R_{opt} = 30\Omega$ (which corresponds to a peak output power of 20 W with 28 V DC supply) are illustrated.

Fig.2.12 shows the normalized R_m and X_m at peak power and 6 dB back-off for the

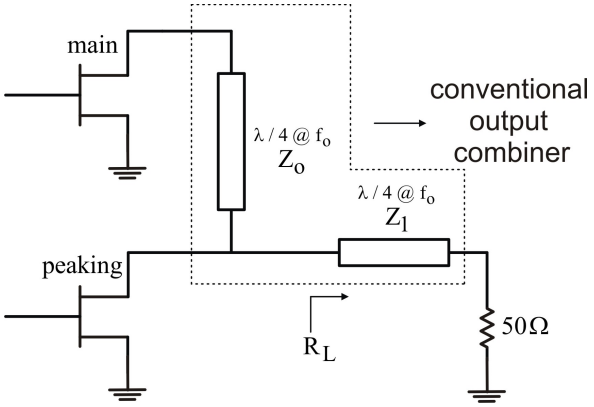


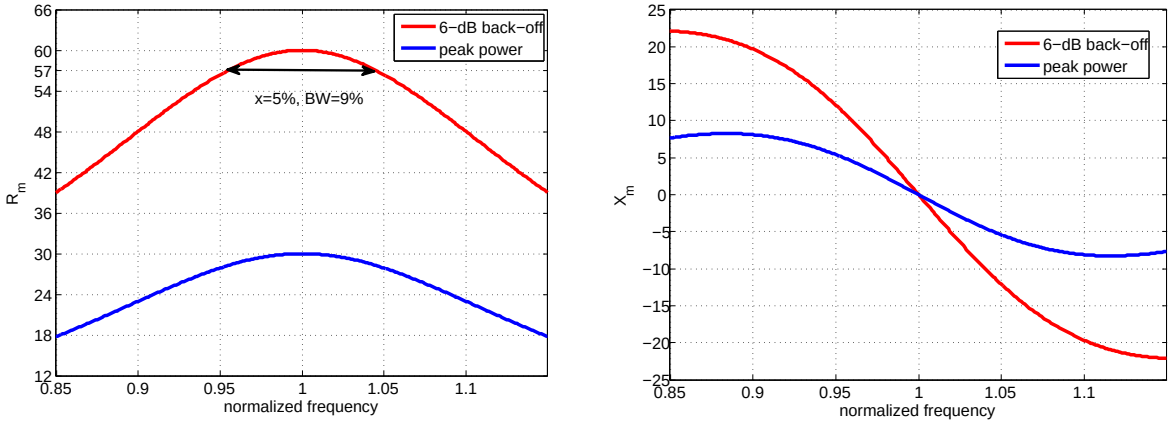
Figure 2.11: The conventional DPA output combiner with single-section quarter-wave transformer

conventional DPA with a single-section quarter-wave transformer for $R_{opt} = 30\Omega$. In this case $Z_o = 30\Omega$, $Z_1 = \sqrt{15 * 50} = 27.5\Omega$ and $ITR = \frac{50}{\frac{R_{opt}}{2}} = 3.33$. In this figure,it has been assumed that

- @ 6 dB back-off: $I_p = 0$
- @ peak power: $|I_p| = |I_m|$ & $\varphi_p = -\frac{\pi}{2} * \frac{f}{f_o}$

Assuming 5% variation in R_m at back-off is acceptable within the bandwidth, Fig.2.12(a) shows that the bandwidth of the conventional DPA with a single section transformer is about 9%, when $R_{opt} = 30\Omega$. This bandwidth can be increased to 17% using a tapered line as has been shown in the previous part (although the physical length of a tapered line is much larger than of a single-section transformer). Fig.2.12(a) also suggests that as the frequency deviates from the center frequency, the efficiency at both 6 dB back-off and peak power will decrease.

Finally, the schematic of a complete conventional DPA is illustrated in Fig.2.13. The biases of the main and peaking transistors are applied either through large inductors (open at AC) or through high-Z $\lambda/4$ lines, in order for the bias feeds not to affect the performance of the amplifier at RF. Also, like most RFPAs, a set of grounding capacitances have by-passed the supply node from low frequencies to operating frequency and at the harmonics.



(a) (b)

Figure 2.12: (a) R_m and (b) X_m of the conventional DPA output combiner at 6 dB back-off and peak power (a single section quarter-wave transformer is used to match 50Ω to $\frac{R_{opt}}{2}$)

2.4 Literature Review on wideband DPA

As mentioned in the previous chapter, to address the limited back-off efficiency of RFPAs, efficiency enhancement techniques such as Doherty [2] have been extensively investigated in the literature. Traditional DPA design methods presented in the literature have been band-limited (less than 10% fractional bandwidth) due to theoretical and practical issues such as offset lines, the quarter-wave transformer, and transistor parasitics.

Several attempts to extend the traditional DPA to amplify multi-standard and multi-band signals have been reported [3]-[20]. The approaches have mainly attempted to extend the bandwidth of the DPA to incorporate multiple communication bands [3]-[19] or develop a multi-band DPA architecture capable of operating at two discrete frequencies [20]. In this work, the focus is on extending the bandwidth of the DPA to allow concurrent amplification of multiple communication signals at multiple bands.

Most of the recent work attempting to extend the bandwidth of the DPA utilizes either one or both of the following approaches: relying on a mixed-signal setup to allow the separate adjustment of input amplitude and phase of the main and peaking transistor across the bandwidth, or focusing on the output combiner to extend the bandwidth of the DPA.

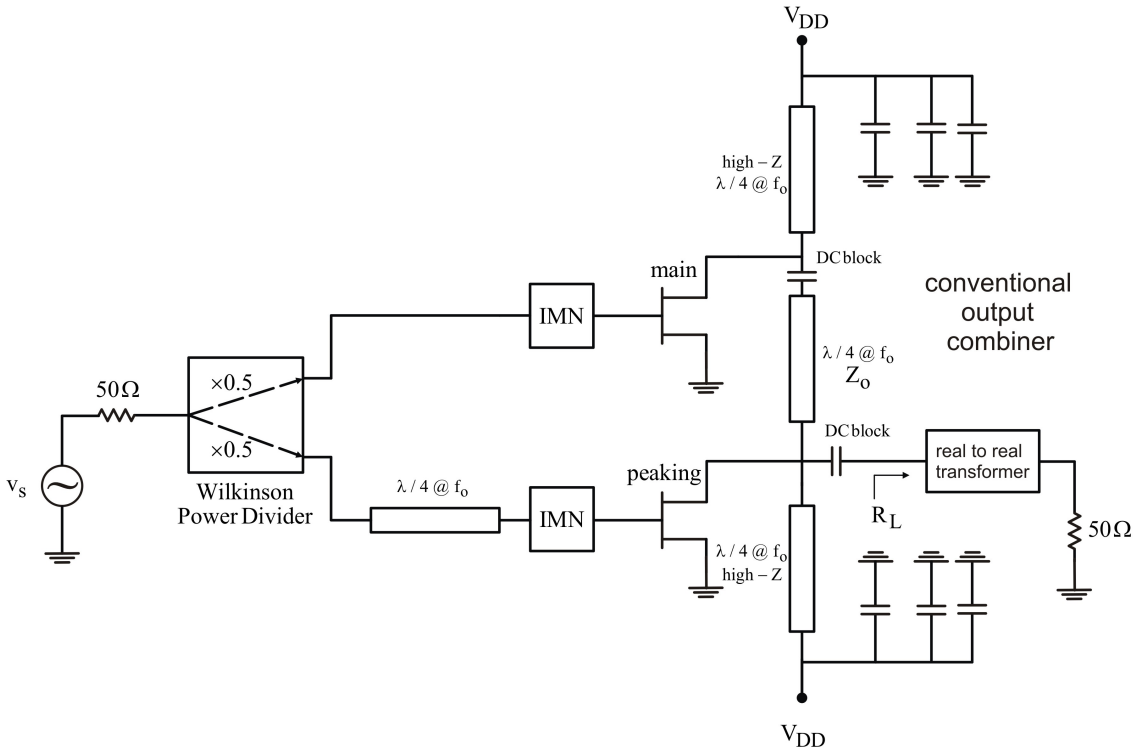


Figure 2.13: Complete schematic of a conventional DPA

The first approach, while capable of achieving excellent back-off efficiency and bandwidth [7]-[9], [19] (e.g., the DPA in [9] maintains more than 50% drain efficiency at 6 dB back-off for 40% fractional bandwidth), requires a more complicated mixed signal setup. Furthermore, concurrent amplification of multi-band signals using such a DPA is more complex and has not been presented in the literature.

In the second approach, the authors try to increase the bandwidth by modifying the output combiner. For example, authors in [7] and [15] have replaced the quarter-wave transformer with a lumped component model which alleviates the bandwidth limitation of the DPA through absorption of the transistor's parasitics. Also, new output combiners are presented in [9], [12], and [13] which mitigates the bandwidth limitation of the traditional two-way DPA for different power back-offs, however, this method requires two different supply voltages for the main and peaking transistors which results in a high breakdown voltage requirement for the peaking transistor.

The focus of two-way DPA has been on efficiency improvement for up to 6 dB back-off range. For efficient amplification of higher PAPR signals, authors in [14] proposed a new three-way DPA output combiner to extend the back-off range of the DPA to 9 dB while maintaining high bandwidth.
The authors in [20] proposed a concurrent dual-band DPA for two wide-spacing frequencies (i.e. 0.85 GHz and 2.33 GHz). For doing so, they replaced all the components of DPA with their dual-band versions (i.e. dual-band power divider, offset-line, and inverter).

Finally, Table 2.1 summarizes some of the works on wideband two-way DPA, which provides a benchmark for comparison to what has been done in this thesis.

Table 2.1: Summary of two-way DPA

	Technology	Frequency (GHz)	Gain (dB)	P_{out} (dBm)	$\eta_{(6\ dB)}$ min/max(%)
[4]	GaN**	2.2-3	7	40.5	35/48
[5]	GaN	3-3.6	10	43	38/43
[6]	GaN	1.96-2.46	11	41	40/46
[7]*	LDMOS***	1.7-2.3	13	43	35/54
[8]*	GaN	1.96-2.46	13	43	40/54
[9]*	GaN	1.6-2.4	9	42	50/60
[12]	GaN	0.7-1	15.3	49.9	48/57
[16]	GaN	1.5-2.14	11	43.8	34/48
[17]	GaN	1.7-2.25		49	53/65
[18]	GaN	1.6-2.25		53	40/60

* Digital input setup has been used.

** GaN stands for Gallium Nitride.

*** LDMOS stands for Laterally Diffused Metal Oxide Semiconductor.

Chapter 3

Bandwidth Extension of DPA

3.1 New Approach for Bandwidth Extension of DPA

Fig.3.1 depicts the load variation of the main and peaking transistors versus the normalized input voltage at the center frequency of a conventional DPA. This load modulation profile garantees the perfect linearity and Doherty efficiency. But, as discussed in the previous chapter, as the frequency deviates from the center frequency, because of the dispersive behaviour of the inverter, the impedances drop and therefore the conventional DPA is narrowband. Therefore, In a wideband DPA one needs to maintain the same load modulation profile of Fig.3.1 over a wide bandwidth.

Fig.3.1 depicts a general DPA in which the main and peaking transistors have been replaced with ideal current sources. In a wideband DPA, $R_L(\omega)$, $X_L(\omega)$, and $\varphi(\omega)$ are needed to be fined for the following criteria to be satisfied over a wide frequency range (however not larger than one octave due to the short circuited harmonic requirement of main amplifier which operates in class B),

- At 6 dB back-off ($I_p = 0$): $R_m = 2R_{opt}, X_m = 0$
- At peak power ($|I_p| = |I_m|$): $R_m = R_{opt}, X_m = 0$
- At peak power ($|I_p| = |I_m|$): $R_p = R_{opt}, X_p = 0$

where φ can be any (even non-linear) function of ω and S_M can be any lossless passive network.

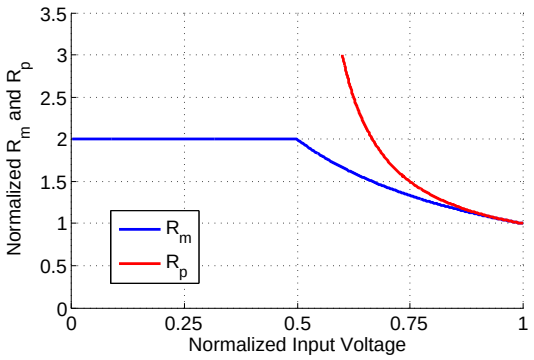


Figure 3.1: Load modulation versus normalized input voltage in a conventional DPA at center frequency

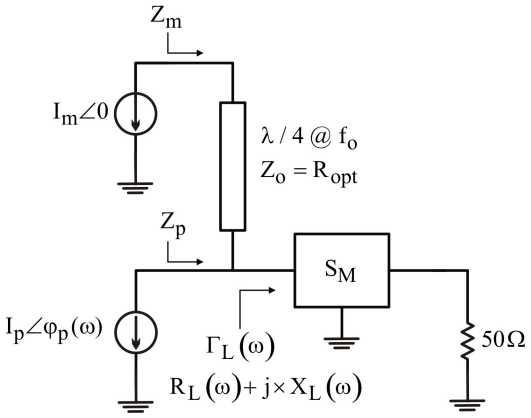


Figure 3.2: General Doherty configuration

At frequencies where $R_m < 2R_{opt}$ at back-off and $R_m < R_{opt}$ at peak power, the efficiency will be lower than that of the ideal case. Frequencies where $mag(Z_m) > 2R_{opt}$ ($R_m > 2R_{opt}$ if X_m is sufficiently small) at back-off or $mag(Z_m) > R_{opt}$ ($R_m > R_{opt}$ if X_m is small) at peak power are not acceptable because the amplifier will not be linearizable at those frequencies. Although in practice, due to the presence of the harmonics and soft transition to the knee region, R_m can be a few percent larger than the optimal value. Furthermore, X_m needs to be as small as possible (ideally zero) with respect to R_{opt} versus frequency and input power, although relatively small reactance values are tolerable.

Regarding Fig.3.1, at 6 dB back-off:

$$Z_m^{BO} = R_{opt} * \frac{R_L + jX_L + jR_{opt}tan(\theta)}{R_{opt} + j(R_L + jX_L)tan(\theta)} \tag{3.1}$$

$$R_m^{BO} = real(Z_m^{BO}) = 2R_{opt} \tag{3.2}$$

$$X_m^{BO} = imag(Z_m^{BO}) = 0 \tag{3.3}$$

and at peak power:

$$Z_m^{PP} = \left(\left(\frac{cos(\theta) + \frac{jR_{opt}sin(\theta)}{R_L + jX_L}}{\frac{jsin(\theta)}{R_{opt}} + \frac{cos(\theta)}{R_L + jX_L}} \right) (cos(\theta)\angle\varphi + 1) \right) - jR_{opt}sin(\theta)\angle\varphi \tag{3.4}$$

$$R_m^{PP} = real(Z_m^{PP}) = R_{opt} \tag{3.5}$$

$$X_m^{PP} = imag(Z_m^{PP}) = 0 \tag{3.6}$$

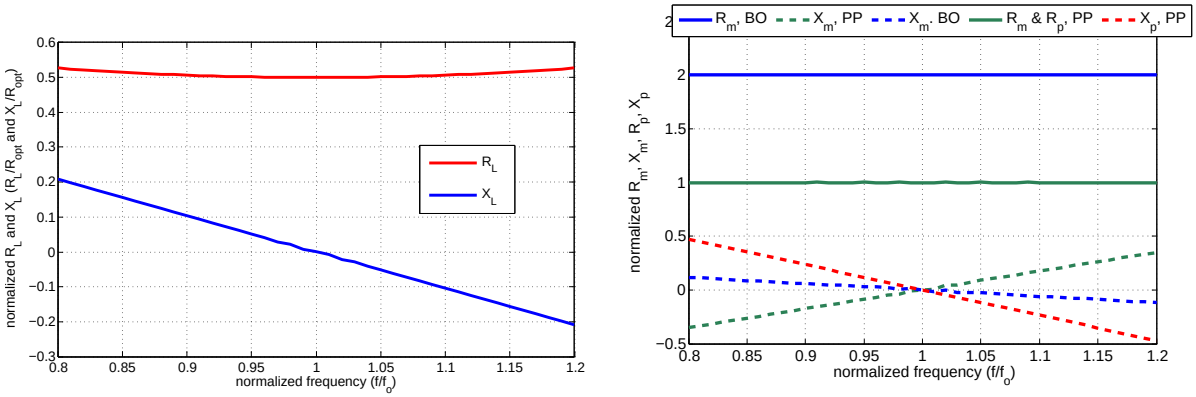
$$Z_p^{PP} = \frac{(1\angle - \varphi) + cos(\theta)}{\frac{jsin(\theta)}{R_{opt}} + \frac{cos(\theta)}{R_L + jX_L}} \tag{3.7}$$

$$R_p^{PP} = real(Z_p^{PP}) = R_{opt} \tag{3.8}$$

$$X_p^{PP} = imag(Z_p^{PP}) = 0 \tag{3.9}$$

Equations 3.2,3.3,3.5,3.6,3.8, and 3.9 constitute a set of six equations with three unknowns ($R_L, X_L, and\ \varphi$). Since in a DPA, small values of X_m and X_p are tolerable, only the criteria on the real parts (equations 3.2, 3.5, and 3.8) need to be considered. Solving for R_L, X_L, and φ in equations 3.2, 3.5, and 3.8 results in:

$$\varphi = -\frac{3}{4} + \frac{1}{4}\left(\frac{f}{f_o}\right) \tag{3.10}$$



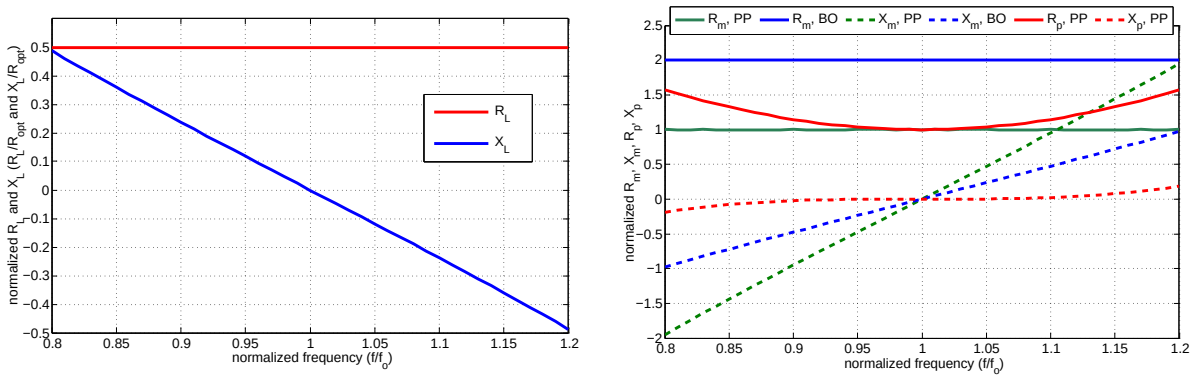
(a) (b)

Figure 3.3: (a) Solution of 3.2, 3.5, and 3.8, (b) Load variation versus frequency at peak power and back-off corresponding to the solution of 3.2, 3.5, and 3.8

also, R_L and X_L along with the corresponding R_m^{BO}, X_m^{BO}, R_m^{PP}, X_m^{PP}, R_p^{PP}, and X_p^{PP} are shown in Fig.3.3(a) and Fig.3.3(b), respectively.

It is important to note that although 3.10 is the solution of 3.2, 3.5, and 3.8, this phase profile is not easily realizable. therefore, 3.2 and 3.5 for the following three phase profiles, which are close to the 3.10 and at the same time are easy to realize, will be solved.

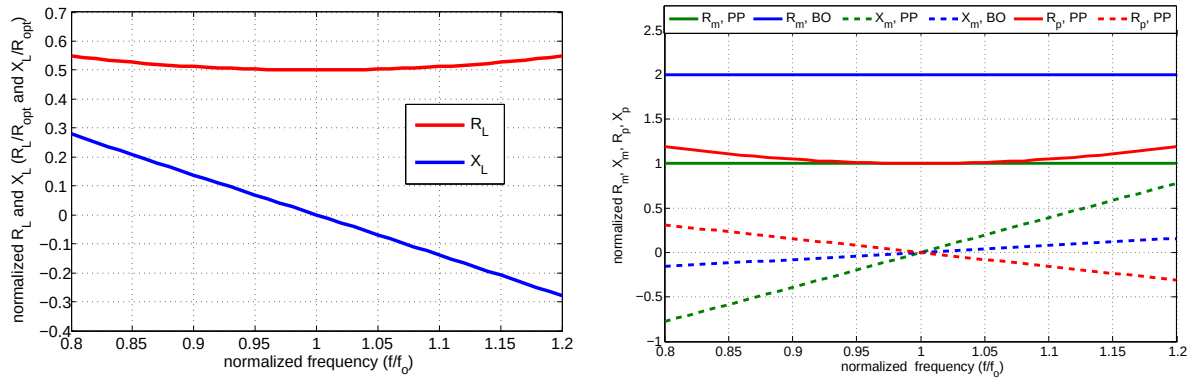
- $\varphi = -\frac{\pi}{2}\left(\frac{f}{f_o}\right)$,this phase profile can be realized using a Wilkinson divider with a quarter-wave line at the input of the peaking transistor. For this case, the R_L and X_L along with the corresponding R_m^{BO}, X_m^{BO}, R_m^{PP}, X_m^{PP}, R_p^{PP}, and X_p^{PP} are shown in Fig.3.4(a) and Fig.3.4(b), respectively.



(a) (b)

Figure 3.4: (a) Solution of 3.2, 3.5, when $\varphi = -\frac{\pi}{2}\left(\frac{f}{f_o}\right)$, (b) Load variation versus frequency at peak power and back-off corresponding to the solution of 3.2, 3.5, when $\varphi = -\frac{\pi}{2}\left(\frac{f}{f_o}\right)$

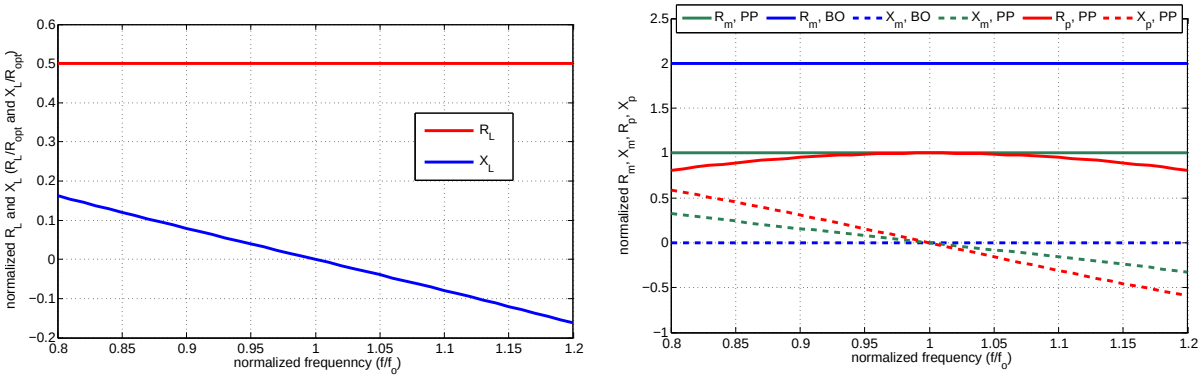
- $\varphi = -\frac{\pi}{2}$,this phase profile can be realized using a 90-degree hybrid. For this case, the R_L and X_L along with the corresponding R_m^{BO}, X_m^{BO}, R_m^{PP}, X_m^{PP}, R_p^{PP}, and X_p^{PP} are shown in Fig.3.5(a) and Fig.3.5(b), respectively.



(a) (b)

Figure 3.5: (a) Solution of 3.2, 3.5, when $\varphi = -\frac{\pi}{2}$, (b) Load variation versus frequency at peak power and back-off corresponding to the solution of 3.2, 3.5, when $\varphi = -\frac{\pi}{2}$

- $\varphi = -\pi + \frac{\pi}{2}\left(\frac{f}{f_o}\right)$, this phase profile can be realized using a 180-degree hybrid with a quarter-wave line at the input of the main transistor. For this case, the R_L and X_L along with the corresponding R_m^{BO}, X_m^{BO}, R_m^{PP}, X_m^{PP}, R_p^{PP}, and X_p^{PP} are shown in Fig.3.6(a) and Fig.3.6(b), respectively.



(a) (b)

Figure 3.6: (a) Solution of 3.2, 3.5, when $\varphi = -\pi + \frac{\pi}{2}\left(\frac{f}{f_o}\right)$, (b) Load variation versus frequency at peak power and back-off corresponding to the solution of 3.2, 3.5, when $\varphi = -\pi + \frac{\pi}{2}\left(\frac{f}{f_o}\right)$

Among the above cases, $\varphi = -\frac{\pi}{2}$ and $\varphi = -\pi + \frac{\pi}{2}\left(\frac{f}{f_o}\right)$ result in load variations versus frequency that are close to the case where $\varphi = -\frac{3}{4} + \frac{1}{4}\left(\frac{f}{f_o}\right)$, but since $\varphi = -\frac{\pi}{2}$ is simply realizable using a 90-degree hybrid it is preferable.

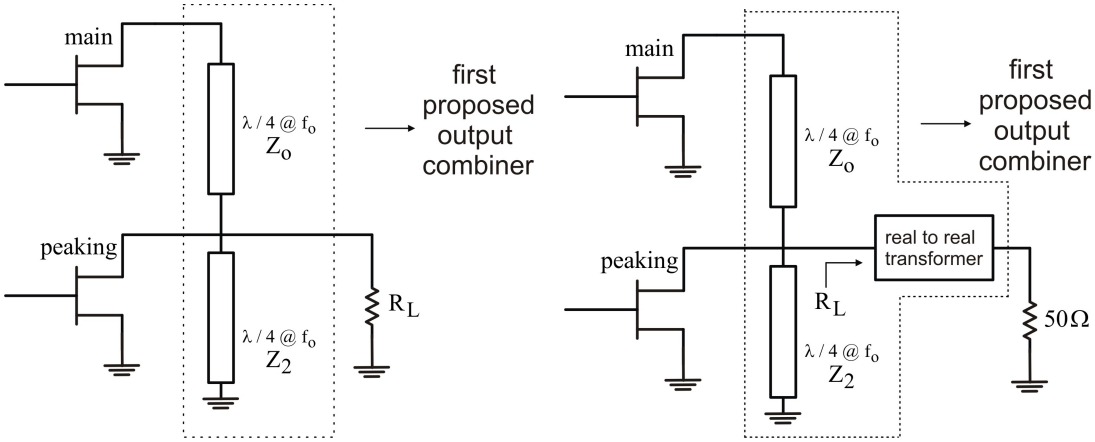
After finding the proper value for $Z_L = R_L + jX_L$, which is depicted in Fig.3.5(a), the impedance must be synthesized. When doing this, there are two issues to consider:

- Bias and baseband impedance
- Parasitic absorption

In the next two sections, two topologies that realize the proper Z_L and satisfy the above criteria have been proposed.

3.2 Broadband DPA using New TL-based Combiner Network

The purpose of this chapter is to propose a Doherty combiner that can realize the Z_L of Fig.3.5(a) over as wide band as possible. Fig.3.7(a) illustrates the schematic of the first proposed combiner, where the 50Ω load is usually transformed to R_L via a real-to-real impedance transformer, as illustrated in Fig.3.7(b).



(a) The load impedance is equal to R_L

(b) A real-to-real impedance transformer transforms 50Ω to R_L

Figure 3.7: The first proposed Doherty combiner

As shown in Fig.3.7(b), the first proposed combiner adds a quarter-wave short-circuited stub to the output of the peaking transistor. As will be discussed, the characteristic impedance of this stub, Z_2, has a critical impact on the performance of the proposed DPA.

In both the conventional and the proposed DPA combiners, the values of R_L and Z_o are equal to $R_{opt}/2$ and $2R_{opt}$ (when the second efficiency peak occurs at 6 dB back-off from the peak output power), respectively. Therefore, at the center frequency the performances of the proposed and conventional DPAs are identical; the difference being their performance across the bandwidth which is determined by Z_2.

The value of R_{opt} and hence R_L depends on the output power of the amplifier. Since the load value usually is equal to 50Ω, a matching network is needed to transform 50Ω to $R_L = R_{opt}/2$. For now, is is assumed that $R_L = R_{opt}/2$ irrespective of frequency (i.e., an

extremely wide-band real-to-real impedance transformer such as a tapered line with infinite length has been used). With this assumption, $R_m = real(Z_m)$ and $X_m = imag(Z_m)$ versus frequency for the proposed Doherty combiner can be plotted, where Z_m is the impedance seen by the drain of the main transistor. It is also assumed that the transistors are ideal current sources, as depicted in Fig.3.8.

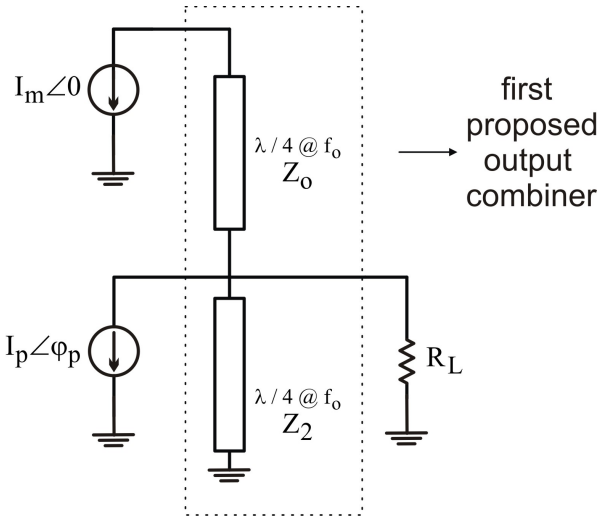


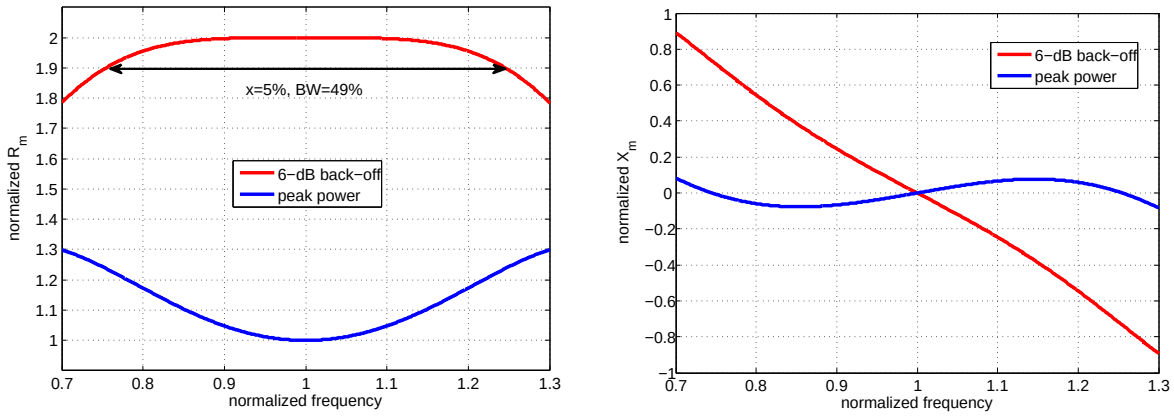
Figure 3.8: The first proposed Doherty combiner with the transistors replaced by current sources

Fig.3.9 and Fig.3.10 show the normalized R_m and X_m at peak power and 6 dB back-off for the proposed DPA for two different values of $Z_2 = \frac{2}{3}R_{opt}$ and $Z_2 = \frac{6}{5}R_{opt}$. It is important to note that since the load impedance is $R_{opt}/2$, these plots are valid for any DPA regardless of the power level.

As can be seen from Fig.3.9, if $Z_2 = \frac{2}{3}R_{opt}$, then for R_m at back-off ($I_p = 0$) at the center frequency:

$$if\ Z_2 = \frac{2}{3}R_{opt} \quad then, \quad \frac{\partial R_m}{\partial f} = \frac{\partial^2 R_m}{\partial f^2} = 0 \quad @\ back-off \tag{3.11}$$

However, in the conventional DPA, the second order derivative is non-zero. So, $Z_2 = \frac{2}{3}R_{opt}$ results in a flat R_m versus frequency at back-off.

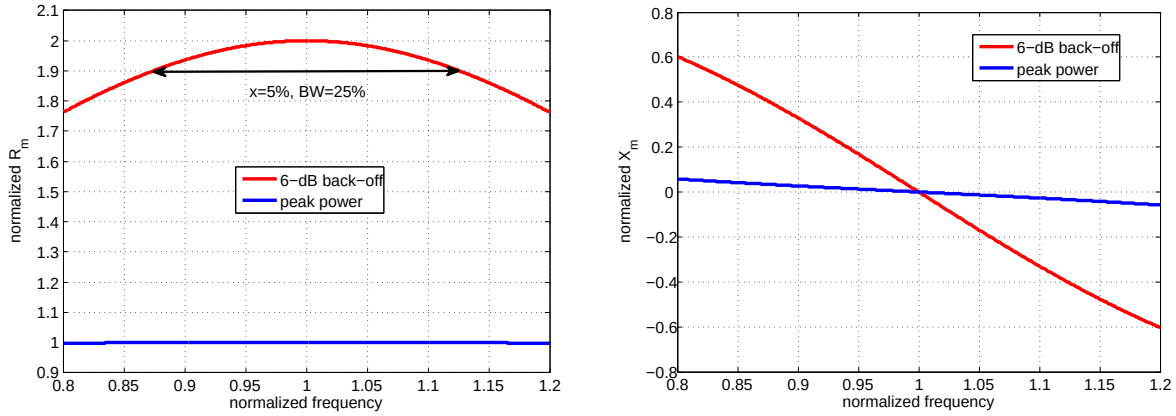


(a) R_m (b) X_m

Figure 3.9: The first proposed Doherty combiner with $Z_2 = \frac{2}{3}R_{opt}$

Assuming that 5% variation in R_m at back-off is acceptable within the bandwidth, Fig.3.9(a) shows that the bandwidth of the proposed Doherty is about 49%, irrespective of the value of R_{opt}. But, as mentioned earlier, since the value of normalized R_m at peak power is larger than 1, the value of Z_2 is not useful due to linearity issues. Although R_m can be a few percent (e.g., 3%) larger than R_{opt} at peak power as the transition to knee region is not abrupt, the result is more than 20% larger which is not acceptable. Therefore, it is needed to find a value for Z_2 which makes R_m flat versus frequency at peak power. Setting $Z_2 = \frac{6}{5}R_{opt}$, then for R_m at peak power ($I_p = I_m\angle -90$) at the center frequency:

$$if\ Z_2 = \frac{6}{5}R_{opt} \quad then, \quad \frac{\partial R_m}{\partial f} = \frac{\partial^2 R_m}{\partial f^2} = 0 \quad @\ peak\ power \tag{3.12}$$



(a) R_m (b) X_m

Figure 3.10: The first proposed Doherty combiner with $Z_2 = \frac{6}{5}R_{opt}$

Again, assuming a 5% variation in R_m at back-off is acceptable within the bandwidth, Fig.3.10(a) shows that the bandwidth of the proposed Doherty is about 25%, irrespective of the value of R_{opt}. In this case, R_m at peak power is flat versus frequency, so the bandwidth of the amplifier is improved without compromising the linearity.

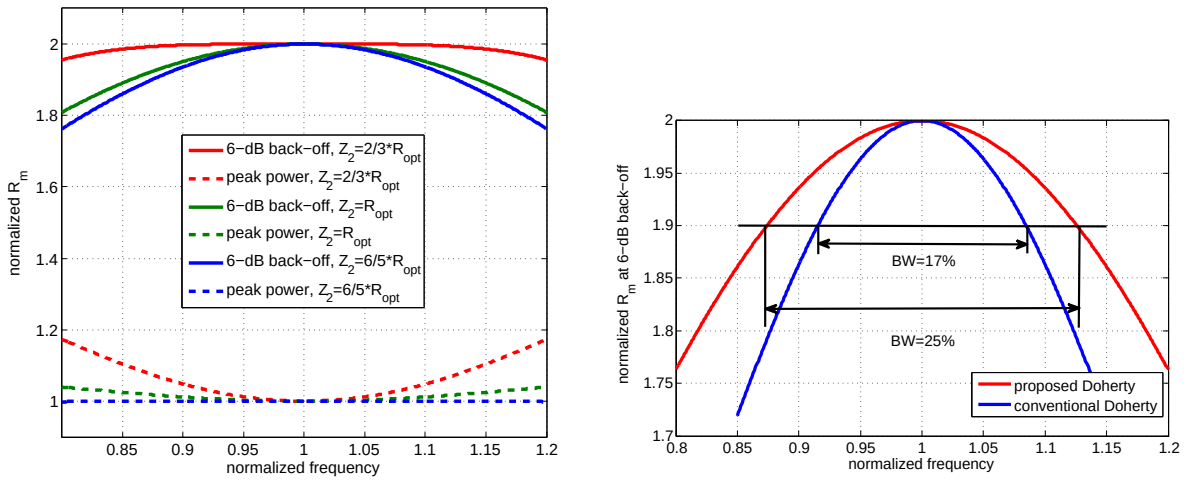
For purposes of comparison, Fig.3.11(a) shows R_m at 6 dB back-off and peak power for $Z_2 = 2/3R_opt$, R_opt ,and $6/5R_opt$. Fig.3.11(b) illustrates R_m at 6 dB back-off for both a conventional DPA and the proposed DPA with $Z_2 = \frac{6}{5}R_{opt}$.

As will be discussed in the section on baseband impedance, it is important to make Z_2 as small as possible. To achieve this, Fig.3.11(a) suggests that one can start with a slightly smaller value for R_{opt} and optimize Z_2 for bandwidth, as we are ultimately interested in small variations in R_m rather than zero derivatives across the band, since the percentage variation of R_m across the band is equal to the percentage variation of the efficiency.

3.2.1 Group Delay

Group delay is relevant to examine in the content of wideband signal amplification. Its variation in the conventional and proposed DPA will be reviewed.

- Group delay: $\tau = -\frac{d\phi}{d\omega}$



(a) (b)

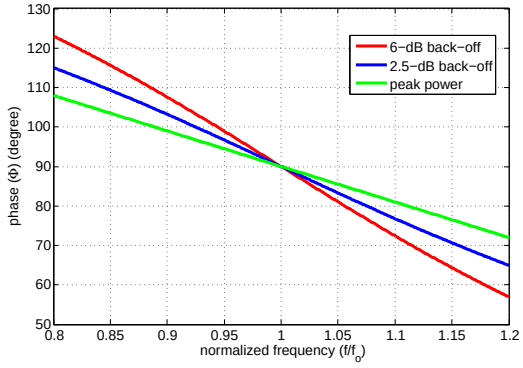
Figure 3.11: (a) R_m versus frequency for different values of Z_2 in the first proposed Doherty, (b) R_m at 6 dB back-off in the proposed and conventional DPA

- Group delay variation (dissipation): $D_2 = \frac{d^2\phi}{d\omega^2}$

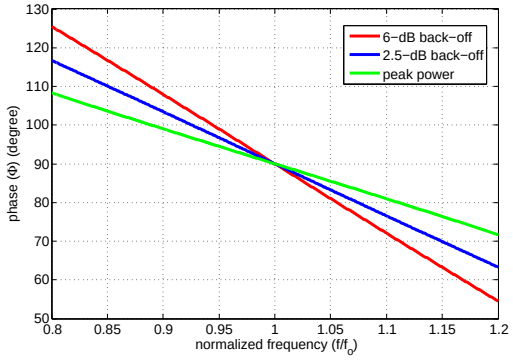
Fig.3.12 shows the phase of the output voltage, the normalized group delay ($-f_o * \frac{d\Phi}{df}$), and normalized group delay dissipation ($f_o^2 * \frac{d^2\Phi}{df^2}$) of the conventional and proposed DPA versus frequency at three different power levels:

- $v_{in} = 0.5$ (i.e., 6 dB back-off)
- $v_{in} = 0.75$ (i.e., 2.5 dB back-off)
- $v_{in} = 1$ (i.e., peak power)

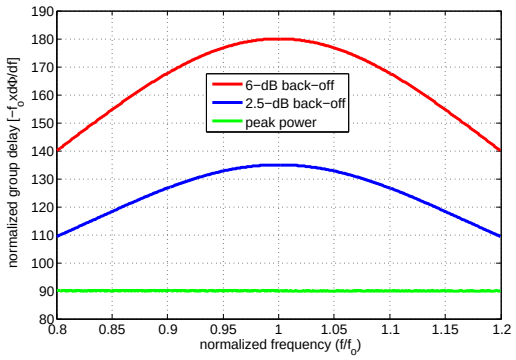
Fig.3.12 reveals two important points. First, the phase depends on the power level as the frequency deviate from the center frequency in both cases. This AM/PM is inherent to DPA operation and exists even if all of the components in the amplifier are ideally linear. Second, and more importantly, the group delay dissipation of the proposed DPA is smaller than that of the conventional DPA (more than 5 times). This feature, along with the low baseband impedance level of the proposed DPA (discussed in the next section), makes it suitable for amplification of wideband signals.



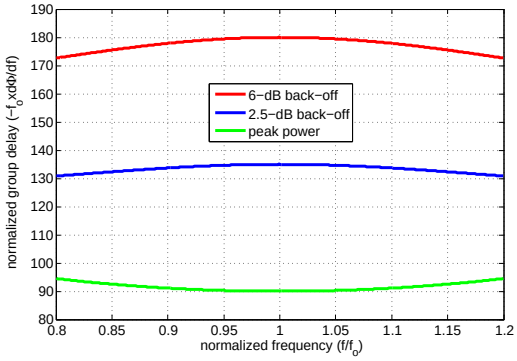
(a) Phase of the conventional DPA



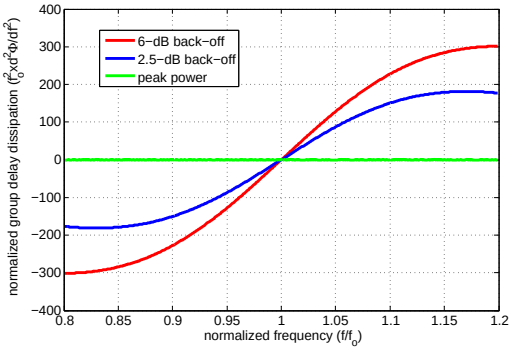
(b) Phase of the proposed DPA



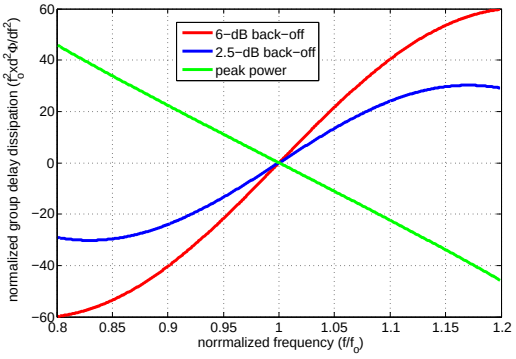
(c) Normalized group delay of the conventional DPA



(d) Normalized group delay of the proposed DPA



(e) Normalized group delay dissipation of the conventional DPA



(f) Normalized group delay dissipation of the proposed DPA

Figure 3.12: Phase, group delay, and group delay dissipation of the conventional and proposed DPA versus frequency at three different power levels

3.2.2 Baseband Impedance

In a conventional DPA, the bias of the main and peaking transistors are applied either through a large inductor (open at AC) or through a high-Z $\lambda/4$ lines as depicted in Fig.3.13. Most RFPAs include a set of grounding capacitances bypassing the supply node from low frequencies to operating frequency and at the harmonics.

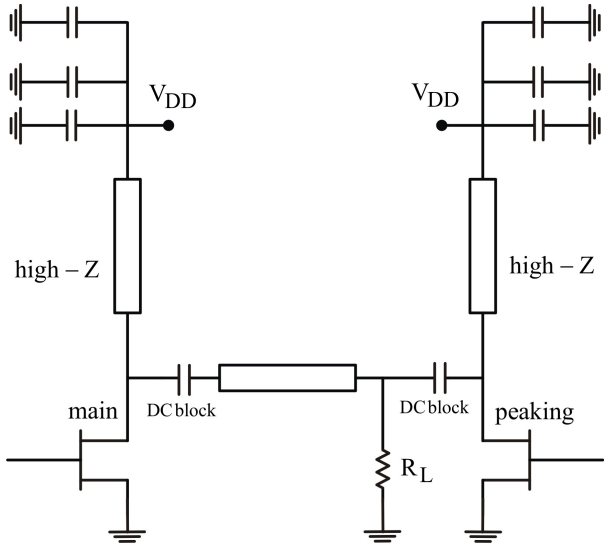


Figure 3.13: Applying bias voltage in a conventional DPA

The bias feeds are high-Z so that they will not affect the AC operation of the amplifier. Due to the presence of the DC block capacitors and large inductance of the high-Z lines, usually one (or even more) resonance occurs at the baseband impedance. This has a negative impact when the amplifier is concurrently amplifying multi-band signals as it results in significant bias supply modulation and degrades the linearity of the amplifier[21].

In the new combiner, the bias of the main and peaking transistors can be applied through the parallel low-Z stub (Z_2) as depicted in Fig.3.14. This provides low low-frequency impedance to the drain of the main and peaking transistors, which helps avoid bias supply modulation and improves the linearity and linearizability of the amplifier when it is driven with concurrent multi-band modulated signals. Fig.3.15(a) illustrates the $mag\{Z_m\}$ from DC to f=BW for the case where $Z_2 = \frac{6}{5}R_{opt}$. Fig.3.15(b) compares the typical baseband impedance of the conventional and proposed Doherty.

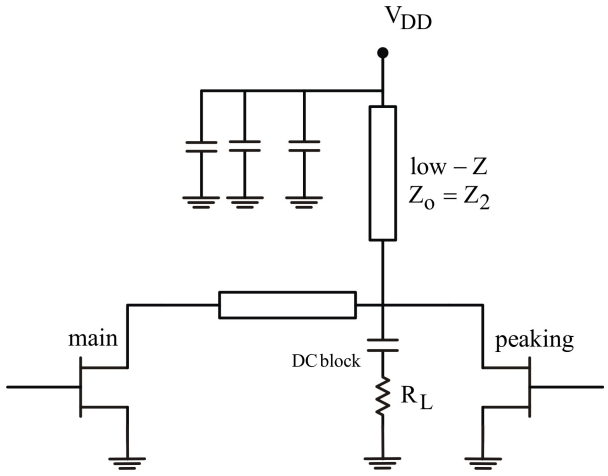
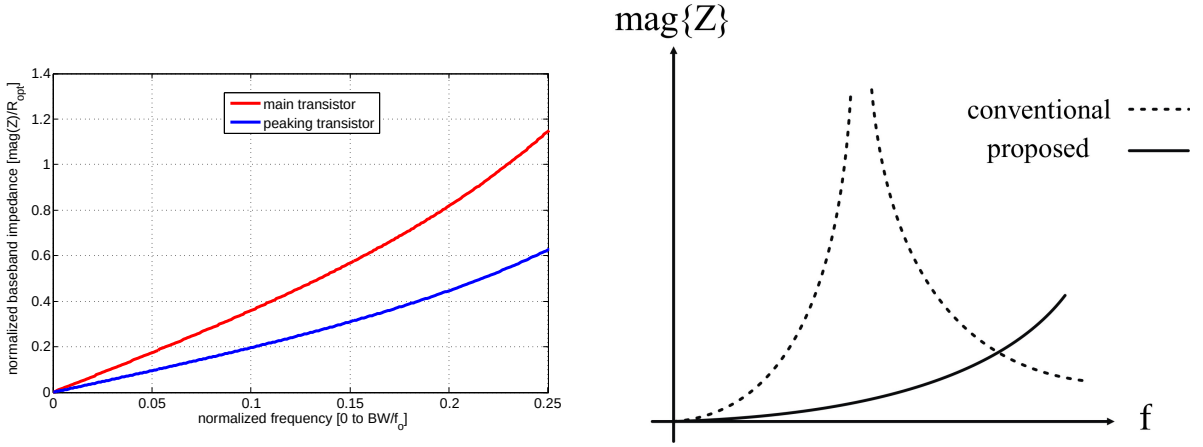


Figure 3.14: Applying bias voltage through the parallel $\lambda/4$ stub



(a) (b)

Figure 3.15: (a) The normalized baseband impedance seen by the drain of main and peaking transistor ($Z_2 = \frac{6}{5}R_{opt}$), (b) Typical baseband impedance for the conventional and the proposed DPA

As can be seen, $mag\{Z_m\}$ is small for baseband frequencies up to the bandwidth of the amplifier. Also, the impedance seen by the peaking device is smaller than the main

device since it is connected to ground through a single low-Z $\lambda/4$ line. In the real case, after the absorption of the main and peaking transistors' output capacitances, one usually will end up with lines whose lengths are smaller than 90 degrees and this, in turn, will result in even lower baseband impedance. In the next few sections, it will be shown how using different real-to-real transformers can further decrease the baseband impedance.

3.2.3 Parasitic Absorption

Another important benefit of the proposed combiner is that the parasitic capacitance of the peaking transistor can be easily absorbed in the parallel low-Z stub without compromising the bandwidth.

3.2.4 Real-to-Real Impedance Transformer

As mentioned earlier, the real-to-real transformer of Fig.3.7(b) transforms the 50Ω load to $R_{opt}/2$ and usually is a single-section quarter-wave transformer, a multi-section quarter-wave transformer, or a tapered line. The response of the real-to-real transformer versus frequency has an important impact on the performance of the proposed DPA, because it is part of the S_M network in Fig.3.1 and can be designed to shape the Z_L profile versus frequency, as will be discussed in detail below.

The first case to consider is when a single-section transformer is used as the real-to-real impedance transformer as shown in Fig.3.16.

It is important to note that any plot in this section is dependent on R_{opt} and hence on the power level, because the 50Ω load remains constant and the performance of the real-to-real transformer is a function of its ITR. Here, some plots for the typical case of $R_{opt} = 30\Omega$ (which corresponds to peak output power of 20 W with 28 V DC supply) are illustrated.

Fig. 18 shows R_m and X_m of the proposed combiner at back-off and peak power versus frequency where $R_{opt} = 30\Omega$. In this case $Z_o = 30\Omega$, $Z_1 = \sqrt{15 * 50}\Omega$, and $Z_2 = 7.6\Omega$. In this figure, it is assumed that:

- @ 6 dB back-off: $I_p = 0$
- @ peak power: $|I_p| = |I_m|$ & $\varphi_p = -\frac{\pi}{2}$

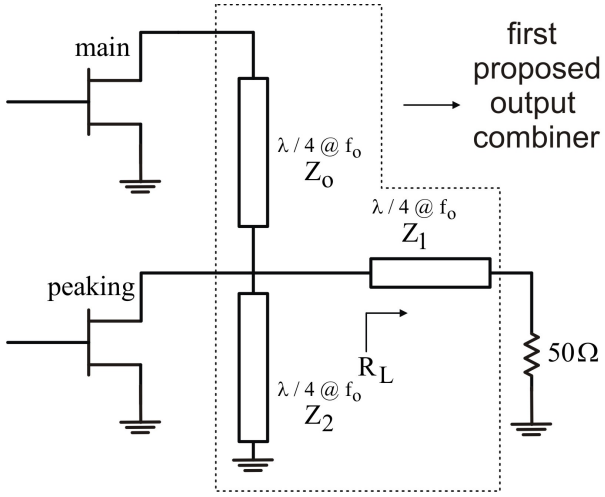
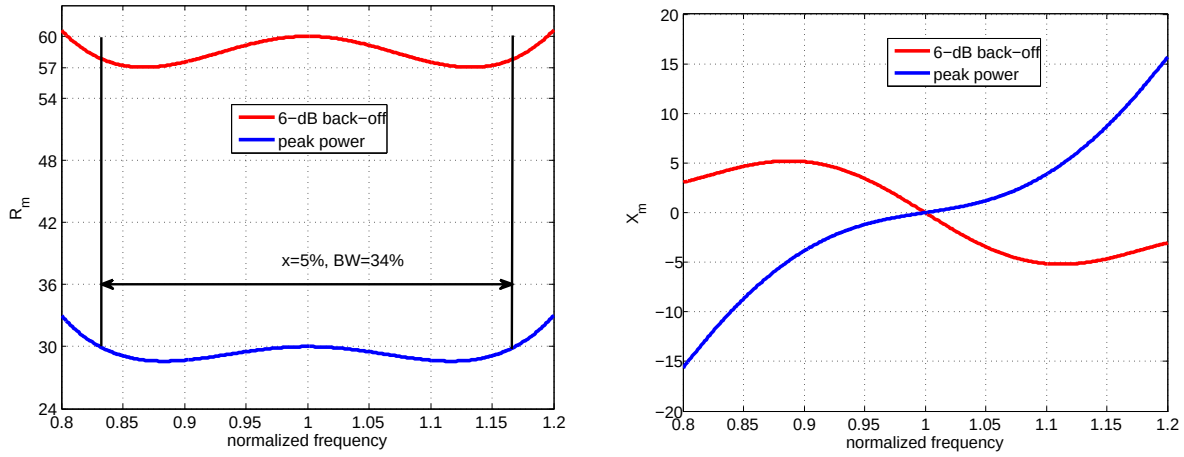


Figure 3.16: The first proposed DPA output combiner with single-section quarter-wave transformer



(a) (b)

Figure 3.17: (a) R_m and (b) X_m of the proposed DPA output combiner at 6 dB back-off of peak power (a single section quarter-wave transformer is used to match 50Ω to $\frac{R_{opt}}{2}$)

In this case, R_m is equal to $2R_{opt}$ at the center frequency. As the frequency deviate from

the center, R_m falls until it reaches a local minimum and then increases. The value of Z_2 has been chosen such that $Real\{Z_m\}$ varies by 5% across the bandwidth. It is important to note that the ideal Doherty operation occurs only at the center frequency where the load varies from 60Ω at back-off to 30Ω at peak power. At frequencies where $Real\{Z_m\} < 60\Omega$ at back-off and $Real\{Z_m\} < 30\Omega$ at peak power the efficiency will be lower than that of the center frequency. Frequencies where $mag\{Z_m\} > 60\Omega$ ($real(Z_m) > 60\Omega$ if X_m is small) at back-off or $mag\{Z_m\} > 30\Omega$ ($real(Z_m) > 30\Omega$ if X_m is small) at peak power are not acceptable because the amplifier will not be linearizable at these frequencies (although in reality, because the transition to the knee region is not abrupt, such values as 31Ω or 32Ω are still acceptable). Fig.3.17 shows that for the case where $R_{opt} = 30\Omega$, the bandwidth is about 34% where 5% variation is maintained across the band, which is significantly larger than the bandwidth of the conventional DPA. In fact, the value of Z_2 as a degree of freedom, can be calculated or optimized to make a compromise between the bandwidth of DPA and the variation of $Real\{Z_m\}$ across the band. By applying the following criteria at back-off, one can calculate the value of Z_2 for x% variation in R_m.

$$\frac{\partial(real(Z_m(f))}{\partial(f)} = 0 \quad @ \quad f = f_c \tag{3.13}$$

$$\frac{2R_{opt} - Real(Z_m(f_c))}{2R_{opt}} = x \tag{3.14}$$

Here, f_c is the frequency of the local minimum.

Fig.3.18 shows the $Re(Z_m)$ of the proposed combiner at back-off and peak power versus frequency where $R_{opt} = 30\Omega$. In this case $Z_o = 30\Omega$, $Z_1 = \sqrt{15 * 50}\Omega$, $Z_2 = 7.6\Omega$ ($x = 5\%$), and $Z_2 = 8.4\Omega$ ($x = 10\%$). As previously discussed, the bandwidth can be increased at the cost of increasing the performance variation across the band.

Fig.3.18 shows that the value of Z_2 as a degree of freedom can be optimized to either increase the bandwidth at the cost of larger performance variation across the band, or minimize the performance variation across the band for a smaller bandwidth.

For easier comparison, Fig.3.19(a) illustrates the $Re(Z_m)$ at back-off and peak power versus frequency for the conventional and proposed combiners ($x = 5\%$) for $R_{opt} = 30\Omega$. This figure shows that adding the parallel stub from the drain of the peaking transistor to ground results in significant improvement in the bandwidth. The load modulation and efficiency for the two cases is also illustrated in Fig.3.19(b), Fig.3.19(c), Fig.3.19(d), and Fig.3.19(e).

The value of Z_2 used in this case was 7.6Ω which is much lower than the case where a tapered line was used as the real-to-real transformer (in that case, $Z_2 = 6/5 * R_{opt} = 36\Omega$).

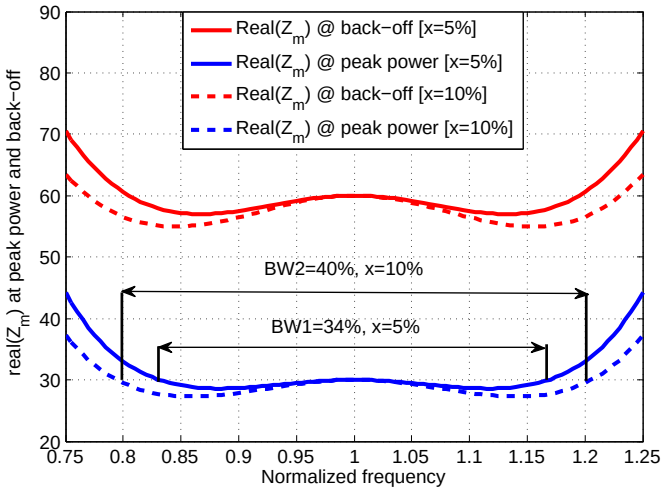


Figure 3.18: R_m of the proposed DPA output combiner at back-off and peak power versus frequency for two different values of Z_2

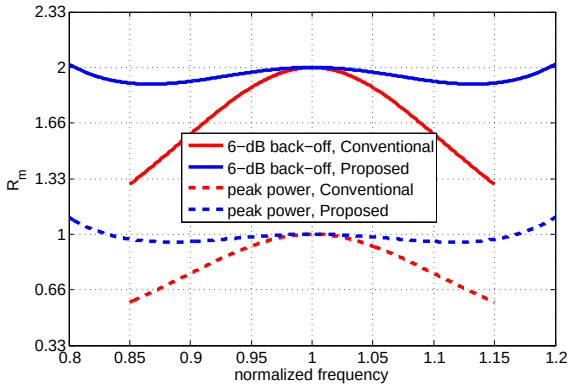
This in turn results in lower baseband impedance for the same power level, as illustrated in Fig.3.20.

As mentioned at the beginning of this section, since the 50Ω load is constant, the ITR increases as the power level increases and the optimum value of Z_2 is not a straightforward function of R_{opt}. Fig.3.21 depicts the optimum value of Z_2 as function of R_{opt} for the case where $x = 5\%$.

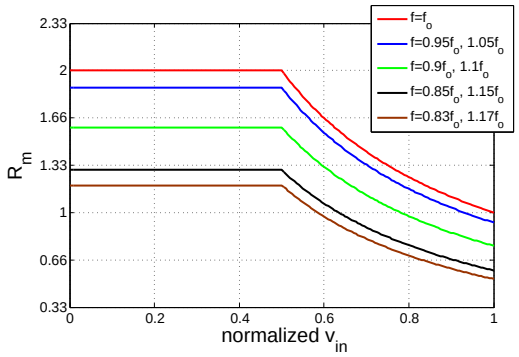
At high power levels (low R_{opt}), with a single section transformer, the value of Z_2 will be too low and is not feasible to implement. In this case, a tapered line can be used as the real-to-real transformer and Z_2 will be larger.

The blue curve in Fig.3.21 represents the case where an N-section quarter-wave transformer with a large N has been used. The red curve is for the case of $N = 1$. The optimum value of Z_2 for the case of $N = 2, 3, \ldots$ will be somewhere in between the two curves (as N increases, so does Z_2).

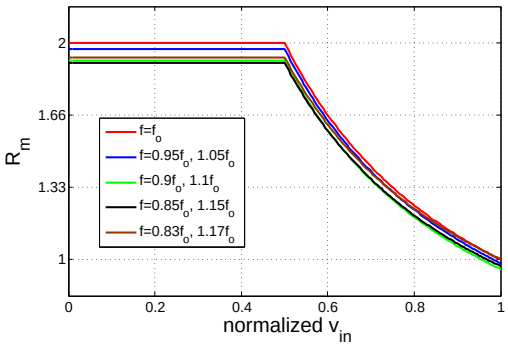
In the case of $N = 2$, the characteristic impedance of one of the quarter-wane lines in the real-to-real transformer (e.g. Z_3) is also a degree of freedom and can be optimized for the bandwidth. In this case a good strategy is to set Z_2 equal to the minimum realizable value and optimize Z_3 for bandwidth, since for the sake of baseband impedance the lowest (feasible) value of Z_2 is preferable.



(a)



(b)



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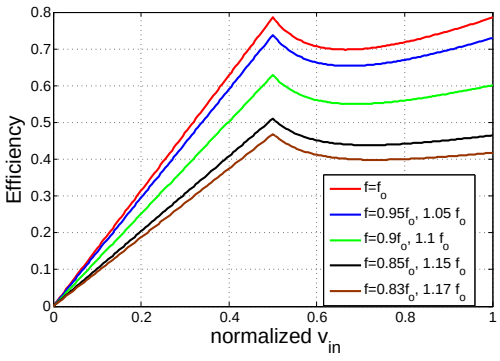
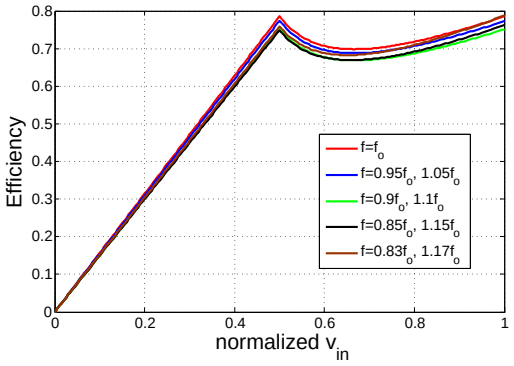


(d)



(e)

Figure 3.19: (a) R_m of the conventional and proposed combiners at back-off and peak power for $R_{opt} = 30\Omega$, (b) Load modulation in the conventional DPA, (c) load modulation in the proposed DPA, (d) Efficiency of the conventional DPA, (e) Efficiency of the proposed DPA

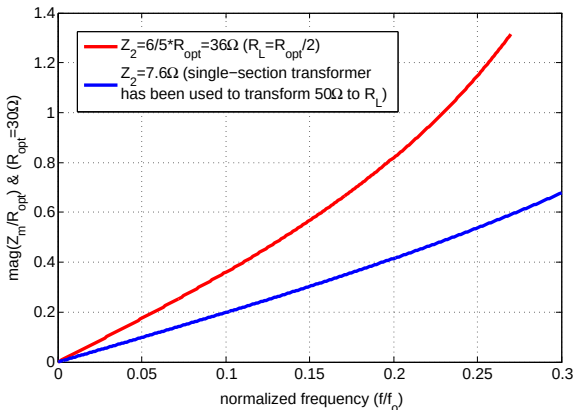


Figure 3.20: Normalized baseband impedance seen by the drain of main transistor when $Z_2 = \frac{6}{5} * R_{opt} = 36\Omega$ (tapered line) and when $Z_2 = 7.6\Omega$ (single-section)

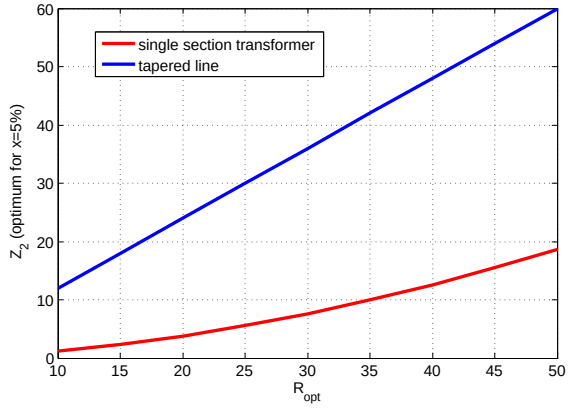


Figure 3.21: Optimum value of Z_2 of the proposed combiner for $x = 5\%$

Also, at medium to high power levels where the value of Z_2 is too low with a single section transformer, the use of a double-section or triple-section transformer is preferable to a tapered line (if that results in a reasonable value for Z_2) because of the large physical size of tapered lines.

Finally, the schematic of the complete first proposed DPA is illustrated in Fig.3.22.

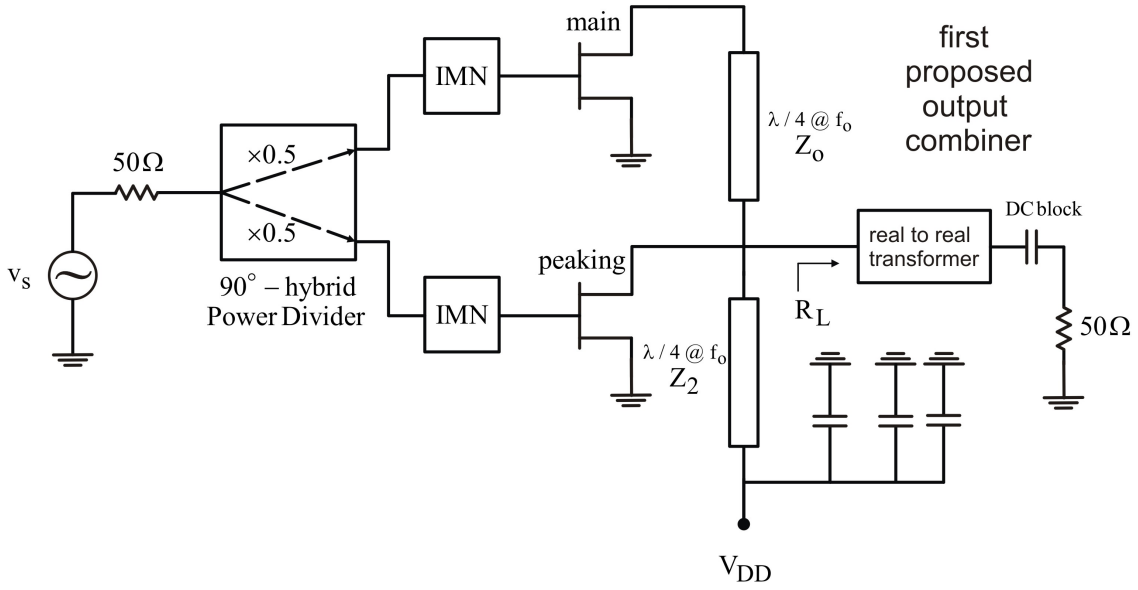


Figure 3.22: Complete schematic of the first proposed Doherty amplifier

3.3 Broadband DPA using New Combiner Network with Discrete Resonator

A short-circuited quarter-wave stub is a resonator, whose behaviour around the center frequency can be approximated by a parallel LC tank, as depicted in Fig.3.23.

So, in the second proposed combiner the short-circuited quarter-wave stub can be replaced with its equivalent LC tank, illustrated in Fig.3.24. As a result the bandwidth will be improved compared to the conventional DPA. It also results in lower group delay dissipation. The output capacitance of the peaking device can be easily absorbed in C_t.

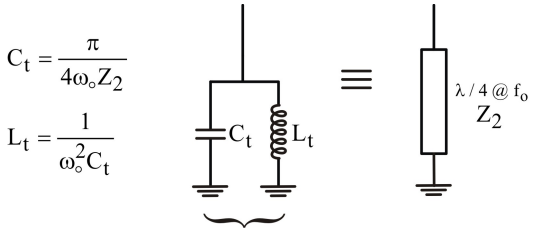


Figure 3.23: Short-circuited quarter-wave stub as a resonator

Finally, the inductor L_t can be used as the biasing feed of the main and peaking transistors as depicted in Fig.3.25 and this again results in low low-frequency impedance.

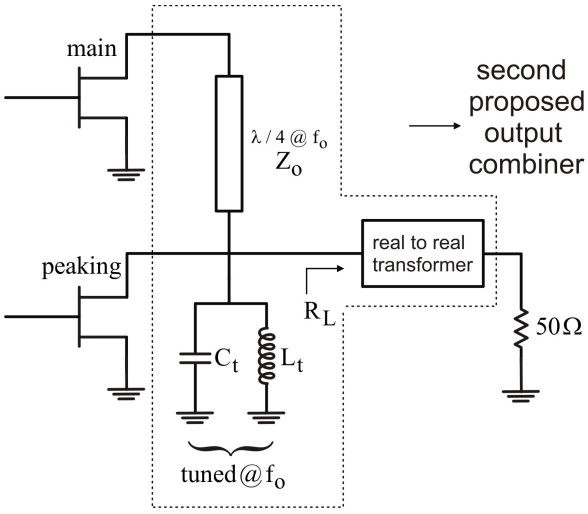


Figure 3.24: Second proposed output combiner

The parallel LC tank and a short-circuited quarter-wave stub are equivalent around the center frequency, but their behaviour is different at the harmonics. Assuming that the capacitor C_t is large enough, the LC tank is effectively short circuited at all of the harmonics while the quarter-wave stub is short at even and is open at odd harmonic. So, the impedance seen by the main transistor at second harmonic is a short circuit and at third harmonic is an open circuit due to the presence of a quarter-wave line between the main transistor and the LC tank. This makes the main amplifier operate in class F mode[22]. So, the design equations which are conventionally developed for a class B-C Doherty have

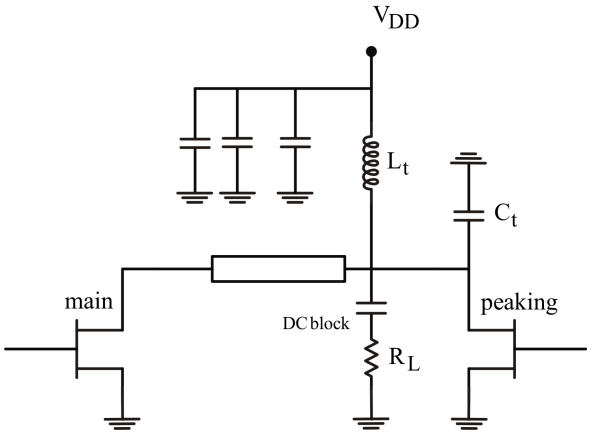


Figure 3.25: Applying bias voltage through the tank inductor L_t

to be modified for a class F-C Doherty.

$$Z_L\left(f_o\right) = R_L \tag{3.15}$$

$$Z_L\left(2kf_o\right) = 0 \tag{3.16}$$

$$Z_L\left(\left(2k+1\right)f_o\right) = \infty \tag{3.17}$$

Comparing a DPA with its main stage operating in ideal class-F with the conventional DPA whose main stage is in class-B, one can conclude that,

$$V_m^F = \frac{4}{\pi} V_m^B \tag{3.18}$$

where V_m is the magnitude of the fundamental drain voltage of the main transistor, and F and B superscripts represent class-F and B quantities, respectively. Subsequently, the peak output power of the main stage of the two DPA structures can be written as

$$P_{out,M}^B = \frac{1}{2} V_M^B I_M^B \tag{3.19}$$

$$P_{out,M}^F = \frac{1}{2} V_M^F I_M^F \tag{3.20}$$

Assuming that the output power of the two cases are equal, one can deduce the relation between the required fundamental voltage and current components of the class-F DPA at

peak power in terms of those of the class-B DPA:

$$V_M^F = \frac{4}{\pi} V_M^B = \frac{4}{\pi}(V_{dd} - V_k) \tag{3.21}$$

$$I_M^F = \frac{\pi}{4} I_M^B \tag{3.22}$$

where V_{dd} and V_k denote the drain supply voltage and the transistor knee voltage, respectively. In other words, the maximum current provided by the main class-F PA has to scale down by a factor of $\frac{\pi}{4} = 0.875$ for the same output power. Therefore, the optimum load impedance of the class-F main transistor at full power can be calculated as

$$R_{opt}^F = \frac{V_M^F}{I_M^F} = \left(\frac{4}{\pi}\right)^2 R_{opt}^B \tag{3.23}$$

Our ultimate goal is to determine the class-F DPA circuit parameters, Z_O and R_L. The output voltage swing of the peaking transistor, V_P, or equivalently the voltage across the load, V_L, is related to the current of the main device through the traditional quarter-wave line impedance inverter:

$$V_L = V_P^F = Z_o I_m^F \tag{3.24}$$

where V_P^F is the magnitude of the fundamental drain voltage of the peaking transistor for the DPA whose main stage operates in class-F mode. It is assumed that the peaking transistor is an ideal class-C PA, with no harmonic tuning, unlike the main PA. In other words, at maximum power $V_P^F = V_P^B = V_{dd} - V_k$. Consequently, Z_o can be calculated by evaluating (10) at the peak power as in,

$$Z_o = \frac{V_{dd} - V_k}{I_M^F} \tag{3.25}$$

or

$$Z_o = \frac{4}{\pi} R_{opt}^B = \frac{\pi}{4} R_{opt}^F \tag{3.26}$$

For proper Doherty operation, we should look at the modulation of the impedance of the main transistor by the peaking current. This can be easily done by evaluating the main impedance at two power points: 6 dB power back-off where the first efficiency peak occurs and at peak power. At 6 dB back-off, where the peaking transistor is still off:

$$Z_{m,BO}^F = \frac{Z_o^2}{R_L} = 2R_{opt}^F \tag{3.27}$$

In fact, 3.27 ensures that the main transistor has a maximum voltage swing and efficiency when the input drive is half of its peak value, equivalent to 6 dB input back-off. Substituting 3.23 in 3.27, one can determine the new load resistance, R_L in terms of the optimum load impedance of the class-B main PA as follows:

$$R_L = \frac{R_{opt}^B}{2} \tag{3.28}$$

which is the exact same value as in a conventional class-B DPA. This means that the output transformer for matching the standard 50Ω does not need to be changed compared to the conventional case. At peak power, the impedance of the main device must reduce to R_{opt}^F by proper action of the peaking device:

$$Z_{m,F}^F = Z_o \left(\frac{Z_o}{R_L} - \frac{I_P^F}{I_M^F} \right) = R_{opt}^F \tag{3.29}$$

Therefore, the ratio of the current from the peaking device to that of the main device at peak power, is determined to be

$$I_P^F = \frac{4}{\pi} I_M^F \tag{3.30}$$

or

$$I_P^F = \frac{4}{\pi} I_M^F = I_M^B = I_P^B \tag{3.31}$$

As a matter of fact, both the voltage and current swings of the peaking device remain unchanged, and so does the peaking optimum load impedance. Hence, one can calculate the impedance seen by the main and peaking transistors when the main device is a harmonically-tuned class-F amplifier as a function of the voltage drive as follows:

$$Z_m(v_{in}) = \begin{cases} 2\left(\frac{4}{\pi}\right)^2 R_{opt}^B, & 0 < v_{in} < 0.5 \\ \left(\frac{4}{\pi}\right)^2 R_{opt}^B / v_{in}, & 0.5 < v_{in} < 1 \end{cases} \tag{3.32}$$

$$Z_p(v_{in}) = \begin{cases} \infty, & 0 < v_{in} < 0.5 \\ \frac{1}{2} R_{opt}^B \frac{v_{in}}{v_{in} - 0.5}, & 0.5 < v_{in} < 1 \end{cases} \tag{3.33}$$

Fig.3.26 displays the main and peaking impedance profiles versus normalized voltage drive. As can be observed, unlike the class-B DPA, the impedance of the main and peaking transistors are no longer equal at the peak point.

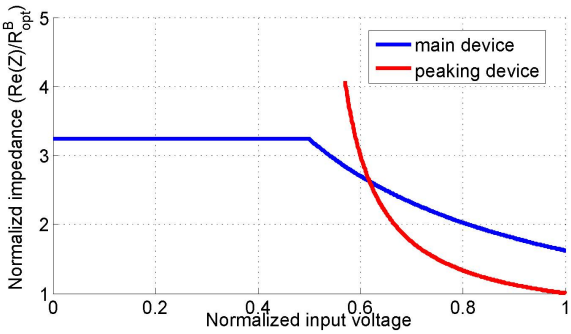


Figure 3.26: Load modulation versus normalized input voltage

The next step is to calculate the required power division ratio between the main and peaking transistors. Assuming a constant g_m for the transistors for simplicity:

$$\frac{V^B_{in,m}}{V^F_{in,m}} = \frac{I^B_m}{I^F_m} = \frac{\pi}{4} \tag{3.34}$$

Consequently,

$$V^F_{in,m} = \frac{\pi}{4} V^B_{in.m} \tag{3.35}$$

$$V^F_{in,p} = V^B_{in,p} \tag{3.36}$$

Therefore, the input power ratio of the main and peaking amplifiers can be expressed as

$$P^F_{in,m} = \frac{\pi^2}{16+\pi^2} P_{in} \tag{3.37}$$

$$P^F_{in,p} = \frac{16}{16+\pi^2} P_{in} = \left(\frac{4}{\pi}\right)^2 P^F_{in,m} \tag{3.38}$$

In other words, unlike the conventional class-B DPA, the power has to be unevenly split between the two transistors, with a ratio of 62% to 38% in favour of the peaking device, assuming similar gains for the two cells. Therefore, a new input power divider must be designed for the desired division ratio. The drawback would be a decreased gain of about 1.2 dB.

Finally, a complete schematic of the second proposed DPA is illustrated in Fig.3.27.

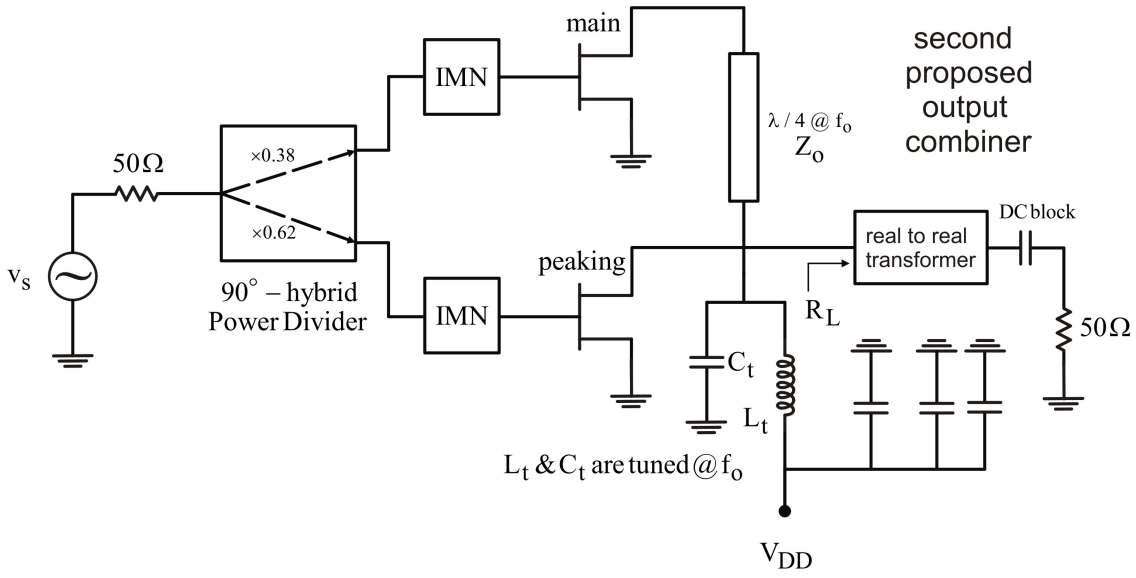


Figure 3.27: Complete schematic of the second proposed DPA

Chapter 4

Measurement Results

4.1 Fabricated Amplifier Based on the First Proposed Combiner

In order to validate the first proposed output combiner, a $20W$ wideband DPA was designed and fabricated using $10\,W$ and $25\,W$ GaN HEMT Cree packaged devices for the main and peaking transistors, respectively, as shown in Fig. 4.1. At the design power level , the characteristic impedance of the resonator is chosen equal to 7Ω to make the back-off impedance flat versus frequency. The same line has also been used as the biasing feed for the main and peaking transistors.

To assess the performance of the fabricated DPA, efficiency and gain versus output power at different frequencies was measured with continuous wave (CW) signals. Fig. 4.2 and 4.3 show the measured gain and efficiency of the DPA at different frequencies in the band. As Fig. 4.3 illustrates, the DPA maintains good efficiency across the entire band which supports the theoretically predicted behavior of the proposed Doherty configuration. Fig. 4.4 illustrates the efficiency of the PA at peak output power and $6\,dB$ and $10\,dB$ back-off versus frequency. it can be seen that the proposed DPA maintains more than 49% efficiency at $6\,dB$ back-off from $1.72\,GHz$ to $2.27\,GHz$, corresponding to 28% fractional bandwidth.

The linearity and linearizability of the proposed DPA was validated using single-band and dual-band modulated signals. The amplifier was linearizable under WCDMA and LTE single- and dual-band modulated signal excitations. Fig. 4.5 shows the measured spectrum of the DPA, before and after linearization, when the amplifier was excited with a $20\,MHz$

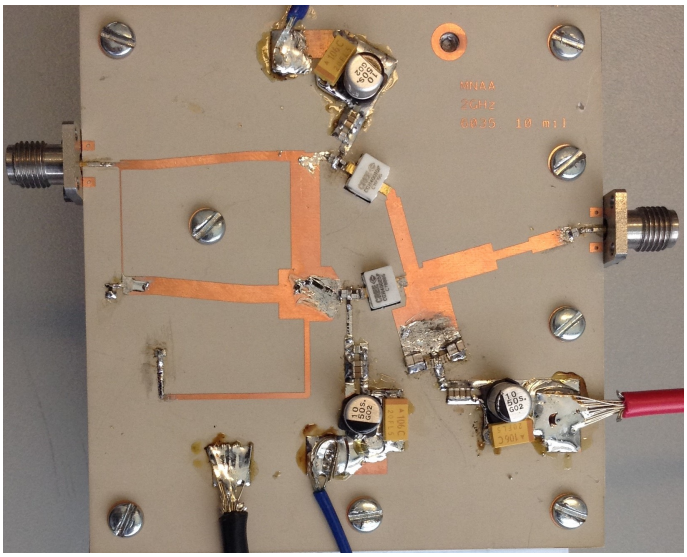


Figure 4.1: Fabricated amplifier based on the proposed combiner

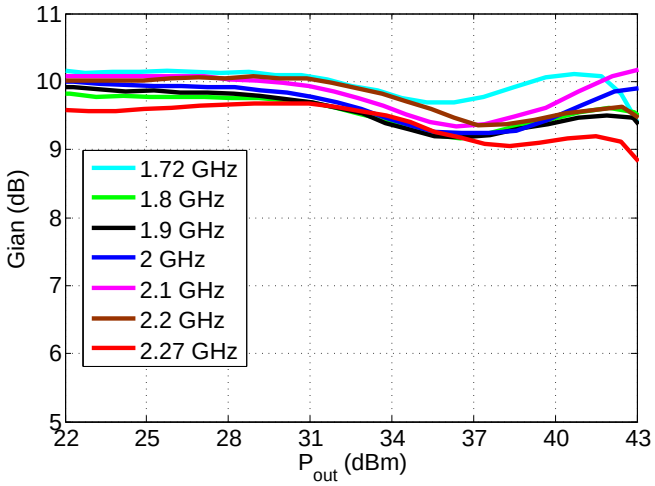


Figure 4.2: Measured CW gain versus output power for the proposed DPA.

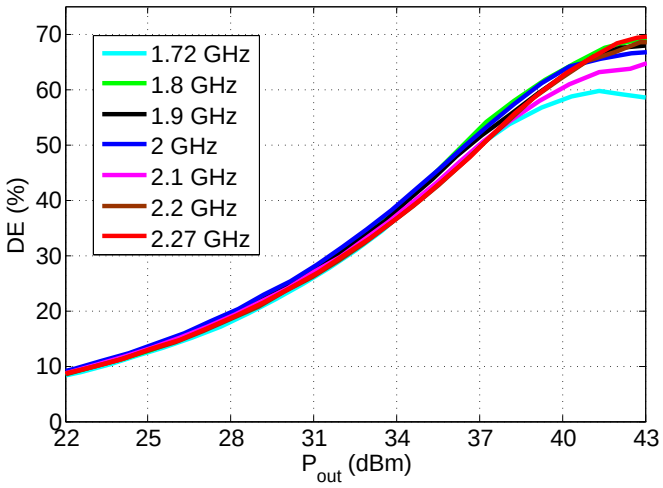


Figure 4.3: Measured CW efficiency versus output power for the proposed DPA.

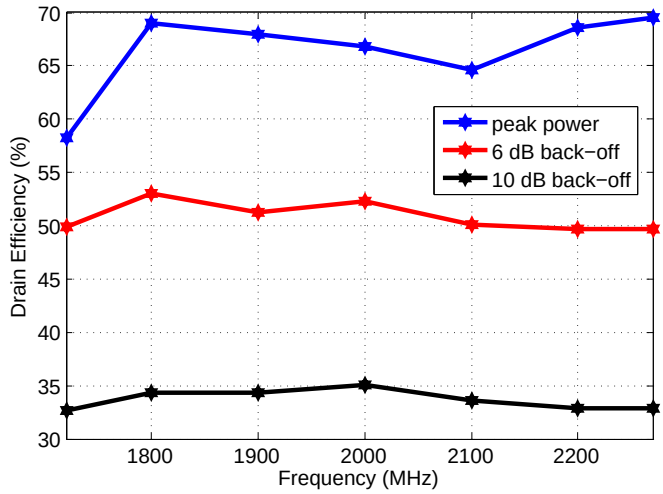


Figure 4.4: Measured efficiency at peak output power and 6-dB and 10-dB back-off for the proposed DPA versus frequency.

WCDMA signal at $1.8\,GHz$, $2\,GHz$, and $2.2\,GHz$. The amplifier achieved $52\,dB$ adjacent channel leakage ratio at an average output power of $36.9\,dBm$ and exhibited an average drain efficiency of 53% at $1.8\,GHz$, 55% at $2\,GHz$, and 48% at $2.2\,GHz$, with a PAPR of $7.14\,dB$.

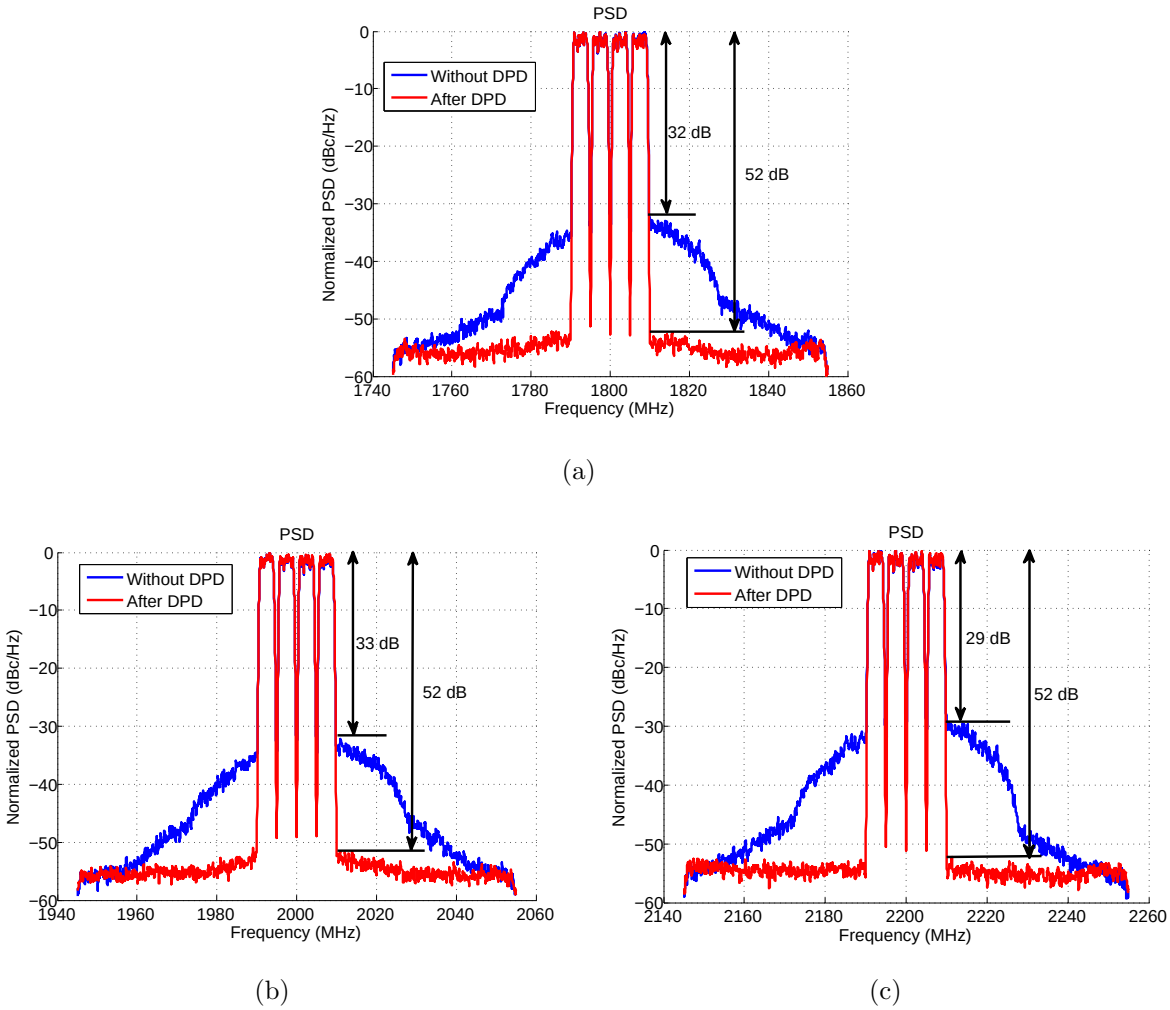


Figure 4.5: Measured spectrum of the output of the first proposed DPA before and after linearization when driven with four-carrier WCDMA signal at (a) $1.8\,GHz$, (b) $2\,GHz$, and (c) $2.2\,GHz$.

Fig. 4.6 shows the measured spectrum of the DPA, before and after linearization, when

the amplifier was excited with a 80 MHz signal at 2 GHz. The amplifier achieved 48 dB adjacent channel leakage ratio at an average output power of 32.7 dBm and exhibited an average drain efficiency of 35% , with a PAPR of 10.25 dB.

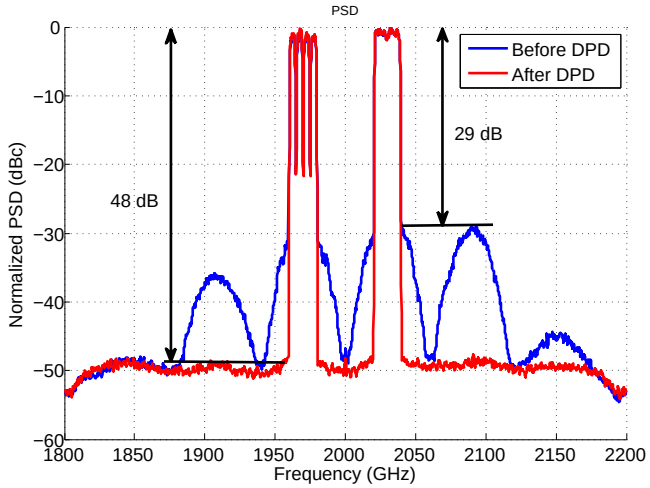
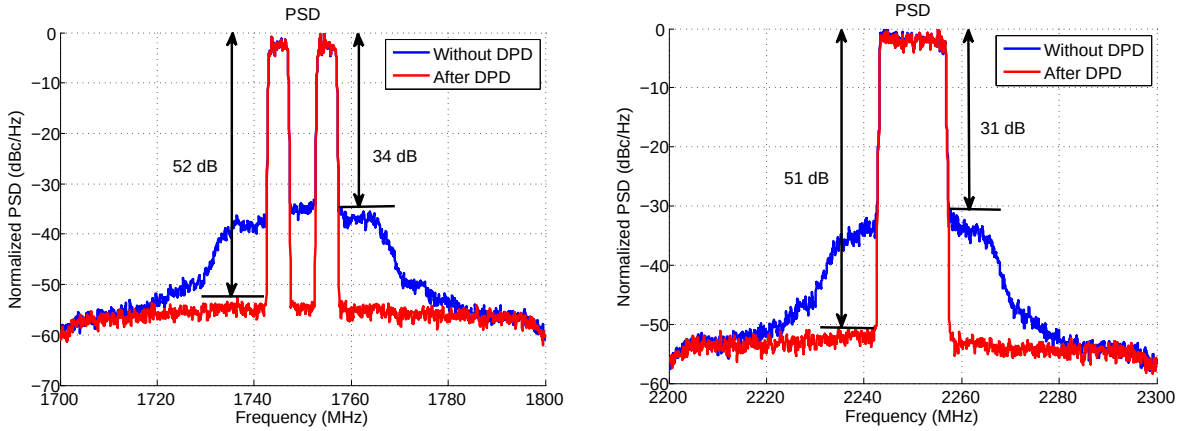


Figure 4.6: Measured spectrum of the output of the first proposed DPA before and after linearization when driven with 80 MHz modulated signal.

Fig. 4.7 shows the measured spectrum of the DPA, before and after linearization, when the amplifier was concurrently excited with 15 MHz WCDMA (101) and 15 MHz LTE signals at 1750 MHz and 2250 MHz respectively. The linearization was conducted using a dual-band base-band equivalent Volterra based digital pre-distortion. The amplifier achieved 52 dB and 51 dB adjacent channel leakage ratio for the two bands at an average output power of 33.6 dBm and exhibited an average drain efficiency of 36% , with a combined PAPR of 9.4 dB.



(a) Band I – 15 MHz WCDMA at 1750 MHz

(b) Band II – 15 MHz LTE at 2250 MHz

Figure 4.7: Measured spectrum of the output of the first proposed DPA before and after linearization when driven with dual-band modulated signal.

4.2 Fabricated Amplifier Based on the Second Proposed Combiner

In order to validate the second proposed output combiner, a 20 W wideband DPA was designed and fabricated using 10 W and 25 W GaN HEMT Cree packaged devices for the main and peaking transistors, respectively, as shown in Fig. 4.8. The design parameter values are presented in Table 4.1. At the design power level and frequency, the resonance tank inductance and capacitance have been chosen equal to 1.9 nH and 19 pF to make the back-off impedance flat versus frequency. The resonance inductor, L_t, was realized using a short transmission line which was also used as the biasing feed for the main and peaking transistors.

To assess the performance of the fabricated DPA, efficiency and gain versus output power at different frequencies was measured with continuous wave (CW) signals. Fig. 4.9 and 4.10 show the measured gain and efficiency of the DPA at different frequencies in the band. As Fig. 4.10 illustrates, the DPA maintains good efficiency across the entire band which supports the theoretically predicted behavior of the proposed Doherty configuration. Fig. 4.11 illustrates the efficiency of the PA at peak output power and 6 dB and 10 dB

Table 4.1: Summary of the design parameters of the second proposed DPA

Design Parameter	**Expression**	**Value**
R_{opt}^{F}	$\left(\frac{4}{\pi}\right)^2 R_{opt}^{B}$	$48.6\,\Omega$
Z_o	$\frac{4}{\pi}R_{opt}^{B} = \frac{\pi}{4}R_{opt}^{F}$	$38\,\Omega$
R_L	$\frac{R_{opt}^{B}}{2}$	$15\,\Omega$
$P_{in,m}^{F}$	$\frac{\pi^2}{16+\pi^2}P_{in}$	$0.38P_{in}$
$P_{in,p}^{F}$	$\frac{16}{16+\pi^2}P_{in} = \left(\frac{4}{\pi}\right)^2 P_{in,m}^{F}$	$0.62P_{in}$

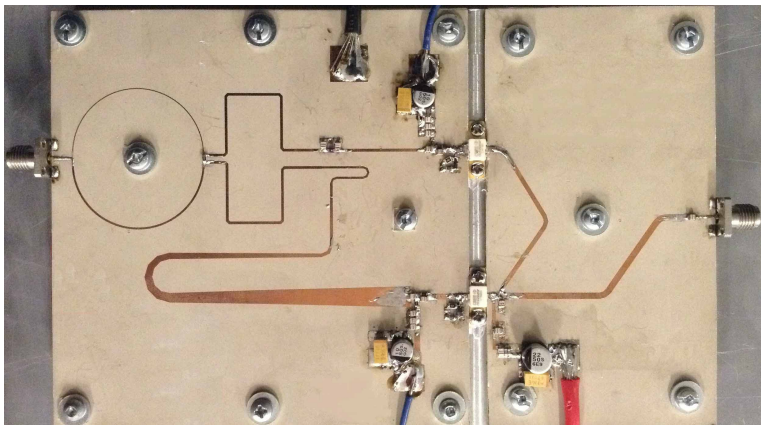


Figure 4.8: Fabricated amplifier based on the proposed combiner

back-off versus frequency. it can be seen that the proposed DPA maintains more than 48% efficiency at 6 dB back-off from 700 MHz to 950 MHz, corresponding to 30% fractional bandwidth.

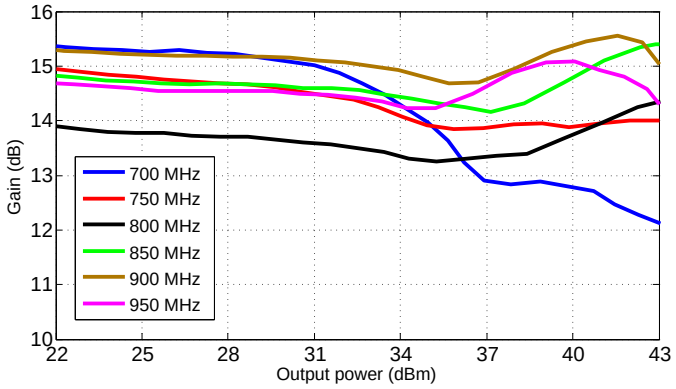


Figure 4.9: Measured CW gain versus output power for the proposed DPA.

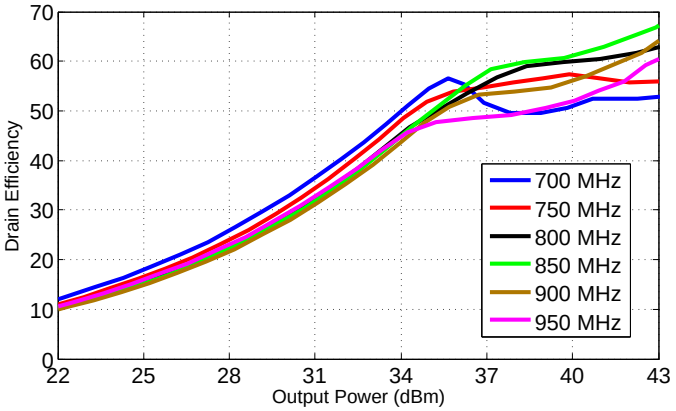


Figure 4.10: Measured CW efficiency versus output power for the proposed DPA.

The linearity and linearizability of the proposed DPA was validated using single-band and dual-band modulated signals. The amplifier was linearizable under WCDMA and LTE single- and dual-band modulated signal excitations. Fig. 4.12 shows the measured spectrum of the DPA, before and after linearization, when the amplifier was excited with a 40 MHz signal at 825 MHz. The amplifier achieved 48 dB adjacent channel leakage ratio

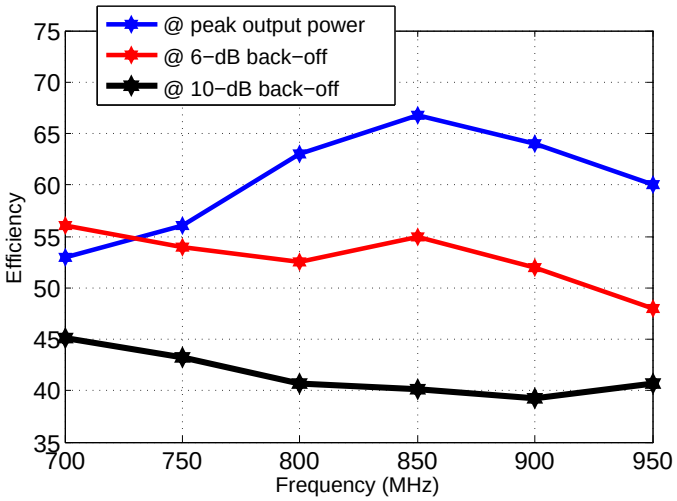


Figure 4.11: Measured efficiency at peak output power and 6-dB and 10-dB back-off for the proposed DPA versus frequency.

at an average output power of 34.5 dBm and exhibited an average power added efficiency of 46% , with a combined PAPR of 8.45 dB.

Fig. 4.13 shows the measured spectrum of the DPA, before and after linearization, when the amplifier was concurrently excited with 15 MHz WCDMA (101) and 15 MHz LTE signals at 750 MHz and 900 MHz respectively. The linearization was conducted using a dual-band base-band equivalent Volterra based digital pre-distortion. Twenty-five coefficients were used in each band. The amplifier achieved 50 dB and 48 dB adjacent channel leakage ratio for the two bands at an average output power of 33.5 dBm and exhibited an average power added efficiency of 42% , with a combined PAPR of 9.4 dB.

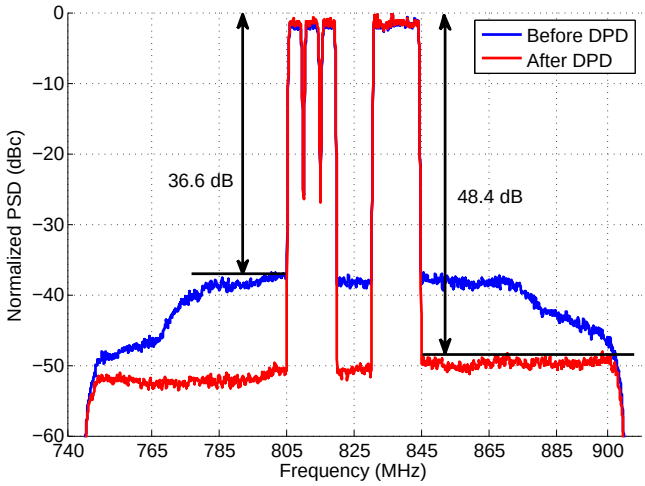
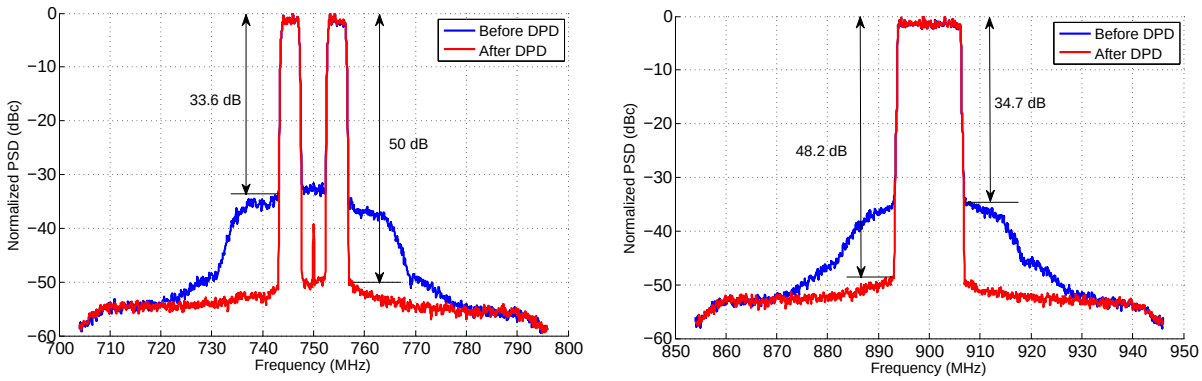


Figure 4.12: Measured spectrum of the output of the second proposed DPA before and after linearization when driven with 40 MHz modulated signal.



(a) Band I – 15 MHz WCDMA at 750 MHz

(b) Band II – 15 MHz LTE at 900 MHz

Figure 4.13: Measured spectrum of the output of the second proposed DPA before and after linearization when driven with dual-band modulated signal.

Chapter 5

Conclusions and Future Works

5.1 Conclusions

This thesis tried to address some of the challenges that future power amplifiers are facing, specifically the high PAPR of signals and carrier aggregation. The thesis started with a brief overview of conventional classes of operation of RFPAs and introduced different figures of merit. Then, chapter two explained the key idea behind the Doherty operation. After that, it moved to the bandwidth analysis of the conventional DPA. Finally, chapter two ended with literature review on wideband DPAs.

In chapter three, the new perspective from which we looked at the wideband DPA problem has been explained. Deriving the governing equations, it was shown how this problem can be converted into an impedance synthesization problem. Then, two networks to realize the desired impedances were proposed. In doing so, we were also careful about the baseband impedance and it was explained why it is important to maintain low baseband impedance, especially when dealing with carrier aggregated signals.

The new combiners will have the following beneficial impacts on the performance of the DPA:

- improved bandwidth
- improved baseband impedance
- improved group delay dissipation
- ease of parasitic absorption

Theoretically, the efficiency of the second proposed DPA is larger than that of the first ($\frac{4}{\pi}$ times), but its gain is smaller ($\frac{\pi}{4}$ times $= -1.2\ dB$).

Two GaN DPAs were fabricated based on the proposed combiners. The measurement results have been provided to validate the developed theory. The first amplifier covers 1.72 GHz to 2.27 GHz and the second one covers 700 MHz to 950 MHz and both maintain higher than 48% of drain efficiency at 6 dB back-off across the band. The two amplifiers are successfully linearized when driven with extra wideband and multiband carrier aggregated modulated signals.

The Table 5.1 compares the two fabricated PAs of this work with some of the references:

Table 5.1: Performance comparison

	Technology	Frequency (GHz)	Gain (dB)	P_{out} (dBm)	$\eta_{(6\ dB)}$ min/max(%)
[4]	GaN	2.2-3 (31%)	7	40.5	35/48
[5]	GaN	3-3.6 (18%)	10	43	38/43
[6]	GaN	1.96-2.46 (23%)	11	41	40/46
[12]	GaN	0.7-1 (35%)	15.3	49.9	48/57
[16]	GaN	1.5-2.14 (34%)	11	43.8	34/48
[17]	GaN	1.7-2.25 (28%)		49	53/65
[18]	GaN	1.6-2.25 (34%)		53	40/60
PA 1*	**GaN**	**1.72-2.27 (28%)**	**9.5**	**43**	**49/53**
PA 2*	**GaN**	**0.7-0.95 (30%)**	**14**	**43**	**48/59**

* Capable of concurrently amplifying carrier aggregated signals.

5.2 Future Work

As future work, one can try the Laterally Diffused MOS (LDMOS) based DPAs with the proposed combiners to validate the effectiveness of the new approach with LDMOS transistors as well. Especially for the applications that are targeting higher power at lower frequency bands.

Another possibility is to try to find new networks to realize the desired impedance (e.g. using the simplified real frequency technique (SRFT)) and compare the properties of different networks in terms of bandwidth, efficiency and linearity. This might help to find DPAs in which the main and auxiliary transistors are operating at different classes than the conventional class B-C (e.g. in the second proposed combiner the main transistor is operating at class-F which resulted in higher back-off efficiency when the auxiliary transistor is off). In this view, finding a DPA whose main (and auxiliary) are operating at class-J would be valuable.

References

[1] J. Wannstrom. (2013) Carrier Aggregation explained [Online]. Available FTP: http://www.3gpp.org/technologies/keywords-acronyms/101-carrier-aggregation-explained

[2] W. H. Doherty, A new high efficiency power amplifier for modulated waves, Proceedings of the Institute of Radio Engineers, vol. 24, pp. 11631182, Sep. 1936.

[3] K. Bathich, A. Z. Markos, and G. Boeck, Frequency response analysis and bandwidth extension of the Doherty amplifier, IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 4, pp. 934944, Apr. 2011.

[4] G. Sun and R. H. Jansen, Broadband Doherty power amplifier via real frequency technique, IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 1, pp. 99111, Jan. 2012.

[5] J. M. Rubio, J. Fang, V. Camarchia, R. Quaglia, M. Pirola, and G. Ghione, 33.6-GHz wideband GaN Doherty power amplifier exploiting output compensation stages, IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 8, p. 25432548, Aug. 2012.

[6] M. Akbarpour, M. Helaoui, and F. M. Ghannouchi, A transformerless load-modulated (TLLM) architecture for efficient wideband power amplifiers, IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 9, p. 28632874, Sep. 2012.

[7] J. H. Qureshi, N. Li, W. C. E. Neo, F. Rijs, I. Blednov, and L. C. N. de Vreede, A wideband 20W LMOS Doherty power amplifier, in IEEE MTT-S International Microwave Symposium Digest, Anaheim, CA, May 2010, pp. 1504 1507.

[8] R. Darraji, F. M. Ghannouchi, and M. Helaoui, Mitigation of bandwidth limitation in wireless Doherty amplifiers with substantial bandwidth enhancement using digital

techniques, IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 9, p. 28752884, Sep. 2012.

[9] D. Gustafsson, C. M. Andersson, and C. Fager, A modified Doherty power amplifier with extended bandwidth and reconfigurable efficiency, IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 1, pp. 533 542, Jan. 2013.

[10] C. Ma, W. Pan, S. Shao, C. Qing, and Y. Tang, A wideband Doherty power amplifier with 100 MHz instantaneous bandwidth for LTE-advanced applications, IEEE Microwave and Wireless Components Letters, vol. 23, no. 11, pp. 614 616, Nov. 2013.

[11] J. Xia, X. Zhu, L. Zhang, J. Zhai, and Y. Sun, High-efficiency GaN Doherty power amplifier for 100-MHz LTE-advanced application based on modified load modulation network, IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 8, pp. 2911 2921, Aug. 2013.

[12] D. Y.-T. Wu and S. Boumaiza, A modified Doherty configuration for broadband amplification using symmetrical devices, IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 10, pp. 32013213, Oct. 2012.

[13] D. Wu and S. Boumaiza, A mixed-technology asymmetrically biased extended and reconfigurable Doherty amplifier with improved power utilization factor, IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 5, pp. 19461956, May 2013.

[14] H. Golestaneh, F. A. Malekzadeh, and S. Boumaiza, An extended bandwidth three-way Doherty power amplifier, IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 9, pp. 3318 3328, Sep. 2013.

[15] D. Kang, D. Kim, Y. Cho, B. Park, J. Kim, and B. Kim, Design of bandwidth-enhanced Doherty power amplifiers for handset applications, IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 12, pp. 34743482, Dec. 2011.

[16] K. Bathich, A. Markos, and G. Boeck, A wideband GaN Doherty amplifier with 35

[17] K. Bathich and G. Boeck, Wideband hamonically-tuned GaN Doherty power amplifier, in IEEE MTT-S International Microwave Symposium Digest, Montreal, QC, Canada, Jun. 2012, pp. 13.

[18] K. Bathich, M. T. Arnous, and G. Boeck, Design of 200 W wideband Doherty amplifier with 34

[19] D. Gustafsson, J. C. Cahuana, R. Hellberg, and C. Fager, A 13-GHz digitally controlled dual-RF input power-amplifier design based on a Doherty-Outphasing continuum analysis, IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 10, pp. 3743 3752, Oct. 2013.

[20] W. Chen, S. Zhang, Y. Liu, Y. Liu, and F. M. Ghannouchi, Concurrent dual-band uneven Doherty power amplifier with frequency-dependent input power division, IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 61, no. 2, pp. 552561, Feb. 2013.

[21] S. C. Cripps, "Advanced Techniques in RF Power Amplier Design," Norwood, MA, Artech House, 2002.

[22] T. H. Lee,"The Design of CMOS Radio-Frequency Integrated Circuits," Cambridge University Press, 2004.