Fabrication of Novel Suspended Inductors

by

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ABSTRACT

With the rapid growth in the wireless industry there has been increasing demand to make devices with better performance. This means lower power, lower voltage, smaller, and in general more efficient. This has lead to the interest in and necessity for good quality passive components. Good quality passive components make better filters, baluns, voltage controlled oscillators, and matching networks.

There has been a lot of work over the last ten years focused on improving the quality of inductors. Typical inductors fabricated on silicon have Q factors of approximately 10. This is because silicon is conductive and therefore acts like a lossy ground plane and develops interfering currents. Improvements that have been attempted include thicker metal layers, thicker dielectric layers, patterned ground shields, as well as using multiple metal layers. These methods, however, still do not improve inductors to the quality of those built on insulating substrates such as glass. The main successful attempt on silicon has been where the inductor coil is released so that it is in the air supported by posts. In some work the inductor coil is raised 50 to 100μm above the underpass by methods like etching or photoresist molding.

The suspended inductor approach was applied to an insulating substrate to fabricate and characterize unique suspended inductors and transformers. Inductors were released to have 1μm of air underneath the coil by the use of a release etch. Transformers were made in a similar way except two released layers where used. The top coil, done in plated gold, was released as well as an interconnection layer. Such a small air gap and the transformers with two released metal layers are a couple of the unique features of this thesis work.

The devices were characterized up to 20GHz before and after release. An improvement in the peak Q factor (up to 70), as well as in the self-resonance frequency (up to 4GHz higher) was noticed after release. This is expected due to the reduction in parasitics. The results were then compared with simulations and a couple closed form expressions, both of which were able to give a reasonable accuracy. There was also success in getting good high frequency transformers.

Even though some good high-Q inductors were fabricated as part of this thesis, there is still further work that can be done. This includes packaging, integration with capacitors, and further optimization.

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1.0 Introduction

As reported almost everywhere these days, there has been a rapidly increasing interest in wireless technology and devices over the past decade [1]. Not only does the cell phone market still have room to expand and evolve but wireless technology has been dreamed into many applications [2]. In fact, in [2] we see that cell phone shipments are up this year so far by over 1,000,000 from last year. From having an internet or Bluetooth connection on a fridge, to using wireless technology in cars for accident avoidance and inter-vehicle communication, and even freeing the internet of wires with the WLAN standards, the potential for the wireless marketplace is wide open [3]. With newly researched wireless areas such as ultra wide band systems, even the home entertainment market is pictured as eventually shedding wires [4]. Some comparison data on wireless systems including a 900MHz cell phone system is given in table 1.1 below [5].

At the same time, these devices have been under pressure to shrink, be more efficient and to perform better [6]. This is partially in order to satisfy customer demand/expectation of continual improvement, as well as to deal with the extremely crowded EM spectrum. In the immediate area of 2.45GHz, for example, there are already at least four devices (Bluetooth, cordless phones, WLAN, and microwave ovens) operating at this frequency band. This means there is a good deal of concern and possibility for interference. For this reason, accurate radios with intelligent frequency selection or other schemes are required to reduce interference and make efficient use of bandwidth [7]. This requires good quality passive components such as inductors and capacitors in order to build the radio front ends. In fact in [8] it is plainly stated that better performance devices are required to meet the demands of wireless communications which include, as mentioned, power efficiency, higher frequency performance, low dissipation, low voltage, and low noise. It is well known that passive components make better filters, baluns, transformers, voltage controlled oscillators, matching network components, etc than distributed elements [9][10]. All of these circuits can be built

Features	IrDA (Infrared)	Bluetooth	802.11b	Cellular	MaxStream
Range	10 m (directional)	10 – 100 meters	50 meters	Cellular network	up to 20 miles (32 km)
Receiver Sensitivity	(optical)	-70 dBm	2Mbps: -90 dBm (typical) 11 Mbps: -84 dBm (typical)	-123 dBm	-114 dBm
Supported Interfaces	Custom	USB, PCI	USB, PCI	Serial, USB	Serial, USB
Transmit Speed	Up to 4 Mbps	Up to 1 Mbps	1 to 11 Mbps	Up to 38.4 kbps	Up to 38.4 kbps
Frequency Band	980 nm light	2.4 GHz	2.4 GHz	869–894 MHz	902–928 MHz & 2.4 GHz
Disadvantages	Line-of-Site only, No multi-point	Short Range, Complex software	Short Range, Power Consumption, Complex Software	Dial-in access to remote device, national coverage	Limited simultaneous network support
Advantages	Low price, high speed	Multiple vendors, plug&play	Multiple vendors, High speed	Line-of-Site only, No multi-point	Long range, Low Price, Low Power, Advanced Networking & Security

Table 1.1 Comparison of some Wireless Systems

including inductors as an essential part. This has lead to an increased interest in the improvement of passive components and especially inductors on silicon processes such as CMOS or Bipolar technologies. There is naturally hope for integration as a silicon circuit is required anyhow for a radio. A typical radio front end is shown in Figure 1.1 below.

An example of the need for high quality inductors from Gennum Corporation can be given. Upon designing a 2.5GHz Bluetooth bandpass filter, it was found that with two out of four inductors having a quality factor of 35, the insertion loss was a poor -4dB. A redesign with all inductors having a quality factor between 80 and 100 improved the insertion loss of the filter to ~ -2dB. This is also true for baluns and matching networks.

Increasing the quality factor of an inductor can lead to a similar improvement in insertion loss in these circuits. Better insertion loss, in turn, allows you to work with weaker

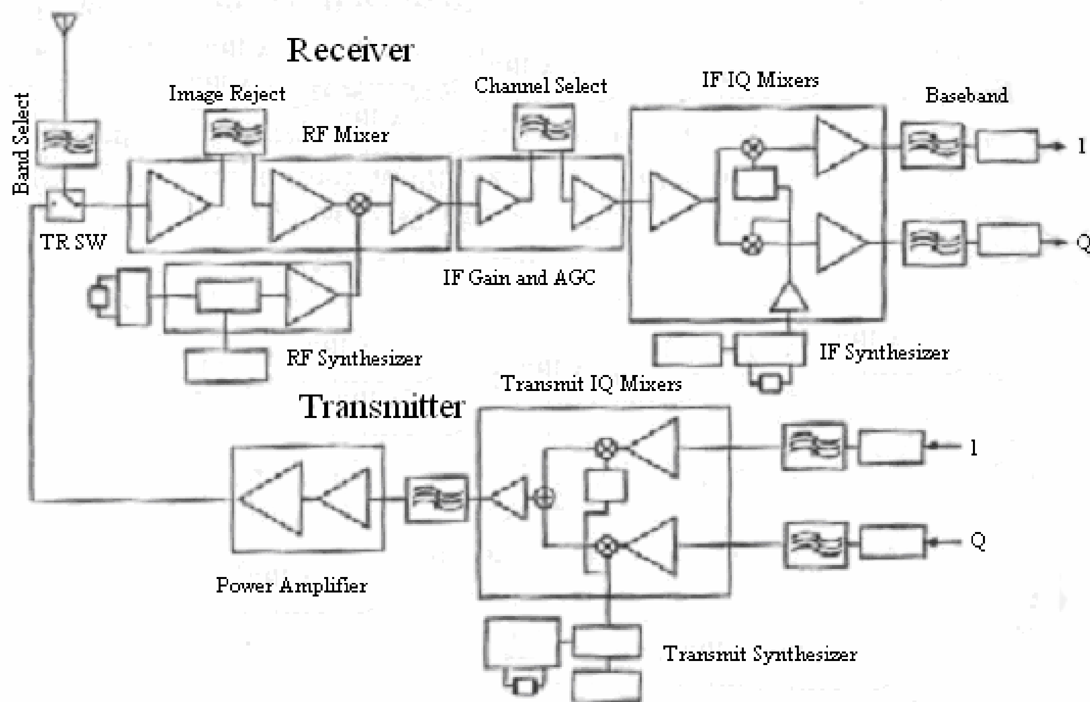


Figure 1.1: A Typical Radio Front end [9]

power levels. This is because with less loss, less power is needed to compensate for the loss in passive circuits such as baluns and filters. In the case of a voltage controlled oscillator (VCO), an increase in the quality factor translates to better phase noise performance.

The approach of integrating good quality inductors onto silicon is only one of the two main approaches that are being taken. The other approach is one where MCM-D, LTCC or another ceramic or glass based technology, which can inherently make good passives, is used to create a supporting RF chip for the required silicon baseband chip. This work takes this second approach, where a ceramic substrate, separate from the silicon substrate, is used in an attempt to create some of the best inductors possible. The next sections outline what was done in this work in detail.

1.1 Previous Work

It is important beforehand to summarize the work that has lead up to this investigation of optimizing inductors and the difficulties with silicon that have lead to work on other substrates. As mentioned, there has been at least ten years of work that has been put into improving the quality of inductors, especially for wireless applications. Silicon substrates have traditionally been chosen in order to facilitate integration with CMOS processes. Using a silicon substrate allows for one-chip integration with the CMOS processes. The problem on a silicon substrate is that the resistivity of the silicon is such that the magnetic field of the inductor can penetrate a significant amount into the silicon, and thus create eddy currents. These currents create their own small magnetic field which opposes the magnetic field of the inductor and thus interfere [11]. A good description, from [9], is that the substrate acts like a poor ground plane.

In an inductor, current loops are used to induce a magnetic field. This magnetic field stores energy much the same way as the electric field in a capacitor can store energy. These loops can be implemented in two main ways. One is the more traditional way of making inductors, which is by winding metal around a core: air, magnetic, or other. For large inductance values, a magnetic core is usually required. The other way of implementing an inductor is in a two dimensional fashion in planar technology. In this case, the 'loops' are implemented as a 2D or possibly quasi-3D coil in one or multiple metal layers. In this case, μH inductors can also be made. This can be done by adding a ferrite, or magnetic, layer in the area where the inductor's magnetic field will be. For the small inductance values required for wireless applications, typically in the nH range, ferrite material and magnetic cores are not required and in fact tend to only degrade the inductor performance.

A measure of the quality of an inductor or capacitor is called the Q factor. The larger the Q factor, the better the inductor. Although there are a variety of ways that the Q factor has been defined, and some of these will be discussed again in detail in later

sections, it is essentially a measure of the ratio of stored energy versus dissipated energy [12]. On silicon, typical Q values have been below 10, which is far below acceptable, so many things have been tried in an effort to improve this [13][14]. From a circuit point of view, the Q factor manifests itself as the amount of insertion loss in a filter or balun, the amount of phase noise in a VCO, the quality factor of these components, etc [15]. S parameters and insertion loss will be covered when measurement and extraction is discussed in the results section.

There has been a lot of work [16][10][17][18] on insulating passive substrates using MCM-D (multichip module-deposited) LTCC (low temperature cold-fired ceramics) or other similar architectures to create integrated passives chips. The bulk of this work has come out of IMEC (Interuniversity MicroElectronics Center) in Belgium. A lot of their work has been focused on using glass substrates. Some of that work involved embedding a silicon chip in the glass substrate [16][10]. Q factors up to 80-100, among the best achieved for inductors in a planar technology, have been achieved in this technology. The glass substrate is well insulating, they were using thick metals, a copper interconnect and they had the benefits of a low-loss dielectric. These considerations were key in achieving these impressive Q factors. This work at IMEC also includes work on using a BCB (benzocyclobutene) dielectric with copper. This work also included modeling work (described in later sections) for these inductors even beyond self-resonance. [17][18][19] A lot of this work, since it includes integrated capacitors, has been combined and verified with microstrip circuits such as filters, VCOs (voltage controlled oscillators), and baluns [16][10][17] This work has similarities to the work which has been undertaken in this thesis work. The work undertaken in this thesis also uses an insulating substrate (alumina). Table 1.2 shown below gives the properties of substrates discussed in this thesis [20][21]. One will notice that silicon has the highest dissipation factor and dielectric constant, which is one reason it is not a good microwave substrate. Note that silicon also has a higher conductivity than the other substrates.

Substrate	Dielectric Constant	Dissipation Factor
Alumina	9.8	0.0001
Glass (Quartz)	3.8	0.00002
Silicon	11.8	0.008
Sapphire	9.39	0.0001
Aluminum Nitride	8.9	0.0005

Table 1.2 Substrate Properties

Inductors have been made on silicon with thick metal to reduce metal losses, via lower resistivity, and thick dielectric to create distance between the inductor and the substrate. This also reduces parasitic capacitances between the coil and the underpass and substrate [22]. This can quantitatively be estimated by calculating the overlap capacitance between the inductor coil and underpass. An actual equation is given in the modeling section. Both of these actions were found to create better quality inductors than in a standard process [22]. In fact simply using ~6µm of a low dielectric material, such as BCB or polyimide, with a low resistivity metal such as copper has improved the Q factor up to 25 in one case and 17 in another [23][24][14]. Although almost all work being undertaken currently uses copper, there was also investigation undertaken to see the effect of different metals. As expected, and as shown by the following graph, the more conducting the metal, the better the inductor performs. Each metal also has slightly different magnetic properties and hence different penetration depths of magnetic fields. This is something known as the skin effect and will be described in later sections.

Inductors have been attempted in various SOI (silicon on insulator) processes [25]. In an SOI process where the bulk is removed, there has been work on suspending inductors on the insulator and using it as a membrane for passives [26]. There has also been work on inductors on membranes not in an SOI process [27]. A silicon nitride or silicon dioxide layer can be used as an insulating membrane to support inductors [26]. Silicon on sapphire has also been used to integrate inductors. Since sapphire has similar insulating properties to glass, it is expected that this would be a promising area of research, however it is very expensive. This technique has, unfortunately, not met with a

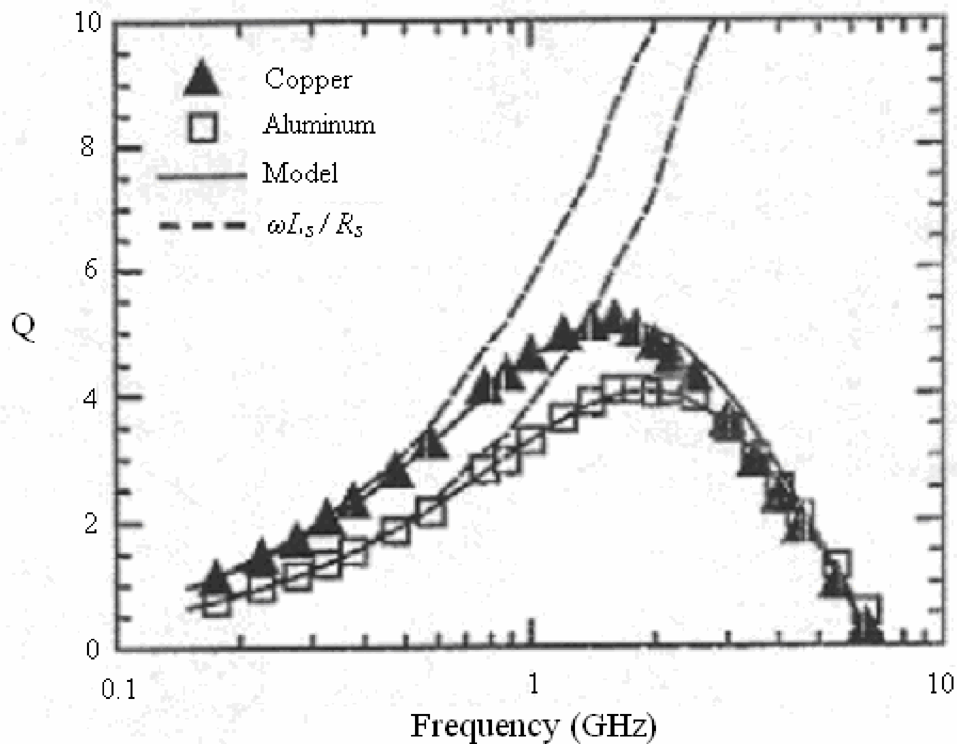


Figure 1.2: Effect of Metal on Q Factor [32]

lot of success so far [28]. In some cases, a MEMS technique or deep etch has been used to leave the devices on an oxide or nitride membrane [29][30]. By completely removing the substrate, clearly the substrate parasitics are also removed, which should improve performance. Another improvement that has been tried is the use of a high resistivity substrate. This will not remove the substrate parasitics, but was done in order to try to minimize the substrate parasitics [14]. The author of this thesis has also been involved in some proprietary Gennum Corporation work that obtained results approaching those achieved on ceramic using very high resistivity float zone silicon.

It has also been common to attempt building the inductor coil using multiple layers of metal [31]. This has been found to have the effect of improving the Q factor but decreasing the self-resonance frequency [12]. This is because the metal layers create more parasitics between each other – capacitances, mutual inductances, etc. Also, there is a very likely probability that lower metal layers will be used in building these

multilayer coils, bringing the inductor closer to the substrate. The increase in parasitics causes the lowering of the self-resonance frequency. Despite the increase in parasitics, using multiple metal layers also lowers resistance, explaining why the Q factor increases even with the increase in parasitics. Using multiple metal layers is similar to using a thicker metal. Fig. 1.3 shows some results that have been achieved [32].

The self-resonance frequency of an inductor is another important factor that defines an inductor. It is caused as a result of the inductance resonating with a parasitic capacitance. What happens is that at a certain frequency, the imaginary parts of the inductance and the capacitance will cancel each other out. This means that at this frequency the device has only a real impedance and is 'resonating'. In most cases the first resonance is usually between the inductor and the parasitic capacitance between the coil and the underpass. This parameter is important because for most applications, the inductor is only useful up to frequencies approaching the self-resonance frequency. After self-resonance, the inductor behaves like a capacitor until the next resonance. An improvement on using multiple metal layers is to spread the inductor coil out over the

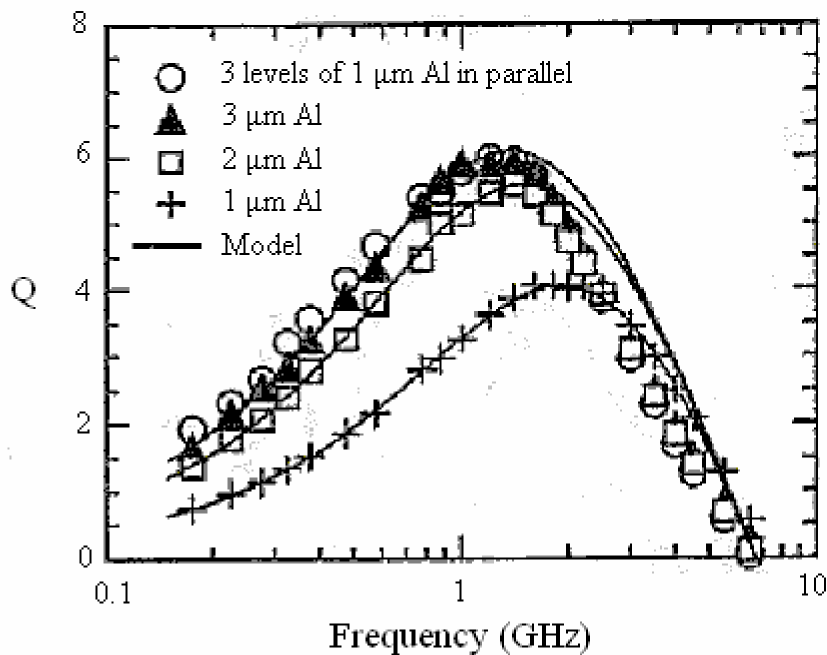


Figure 1.3: Effect of Multiple Metal Layers on Q Factor[32]

layers rather than copy the inductor on each layer [33]. This can easily be done in any multilayer CMOS process and the idea is to basically put a couple windings on each layer [33]. It was found that this improves the self-resonance frequency of the inductors, however, the Q factors reported from this work in 2002 are still less then ten [33]. However, the Q factors reported from this work are similar to those reported for a simple multilayer metal inductor, but with a higher self-resonance frequency, and so is still an improvement.

In order to minimize the eddy currents and effect of non-insulating substrates, another potential solution that has been investigated is the use of a ground shield [34][35]. The innovative idea is to let the eddy currents occur and die out in the shield rather than the substrate. In fact, a patterned ground shield has been found to be more effective, although Q values are typically still below 20. The improved effectiveness is because the pattern can be generated specifically to counter the eddy currents and direct them to take only very short paths before dissipating [34]. Similarly, in [36], a Copper damascene process is used, both with and without a ground shield, and then post processing is performed to get inductors with a Q value of 26-30. Figure 1.4 shows a patterned ground shield used in [9]. The work in [35] specifically investigates different ground shield materials in a six metal level process. Their conclusion was that polysilicon was one of the best choices [35]. This is thought to be because polysilicon with silicide provided better eddy current shielding then metal.[35] A ground shield need not be considered for any work on an insulating substrate.

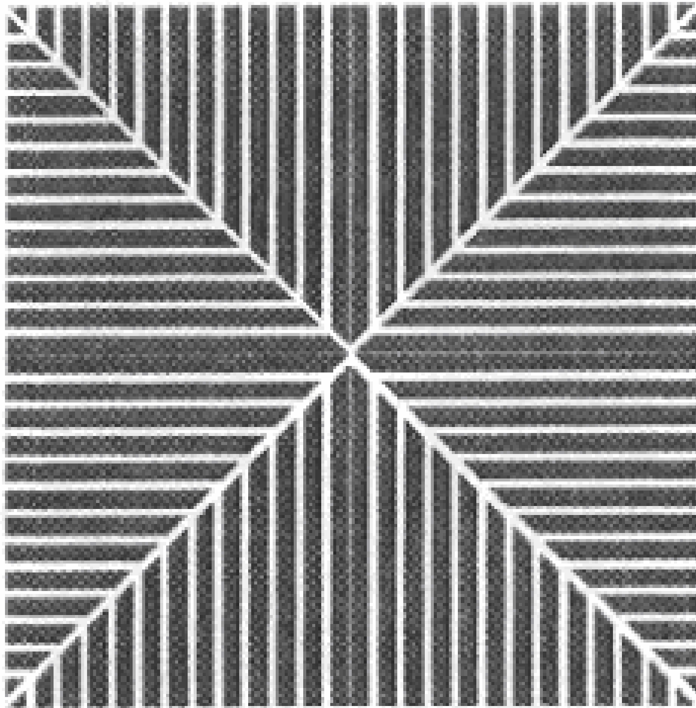


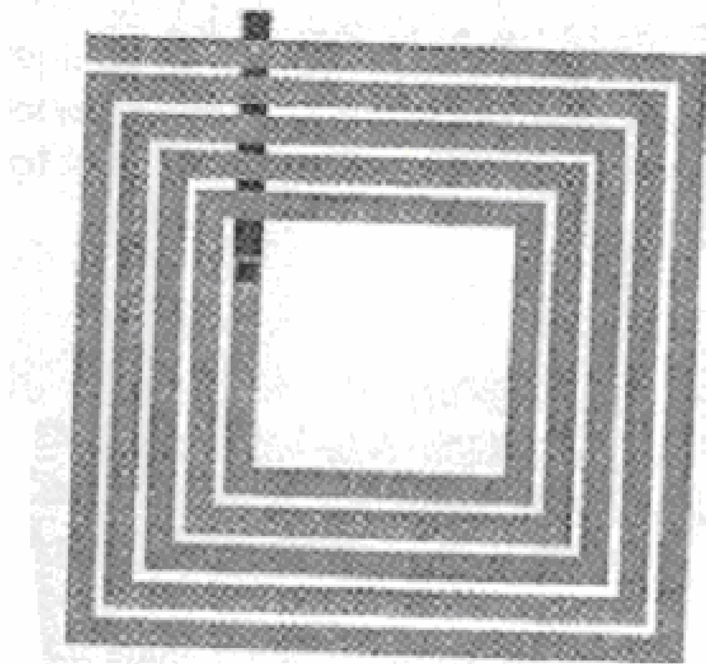
Figure 1.4: A Patterned Ground Shield [9]

1.2 MEMS Approach to Inductors

In some cases, a MEMS approach to inductors has been used. One method that has been used to remove the substrate parasitics is to essentially remove the substrate [26]. For example, in [37], an etch is used to remove the silicon under the inductor. This is one of many MEMS type of techniques used to enhance inductor performance. This differs from the previously mentioned substrate removing techniques, since it does not involve a membrane. One of the most unique MEMS implementations is where gold-coated polysilicon coils are pushed up to 250 μm above the substrate by an actuator [38]. In [39] another interesting MEMS technique is applied to inductors. In this case, mini inductor 'chiplets' are released into deionized water [39]. Capillary forces, surface tension control, and a low temperature solder are then used to allow these chiplets to self assemble onto a substrate [39]. Good Q factors in the range of 35-60 have been claimed [39].

A MEMS approach that has been used by a few different groups is that of bending the inductor ninety degrees so that it ends up being perpendicular to the substrate [40][41][42]. Because the magnetic field is in the middle of the coil, this means that there will be significantly less magnetic field that penetrates the lossy silicon substrate. In [42] the coil is not rotated to vertical but simply allowed to curl away from the substrate. The work in [42] uses meltable hinges at the base of the inductor. It appears that the downside to this approach is that the Q factors are still below 10 in some cases [41]. Perhaps this is because there is still a silicon substrate and also because there may be parasitics added due to the hinges or whatever MEMS structures are required to rotate the inductor. The other issue with this approach is that these vertical inductors are both frail and very hard to package, making them not very manufacturable.

Instead of planar, coil inductors, some groups have produced on chip solenoid inductors using MEMS or photolithography techniques [43][7][44][45][46]. In both [43] and [7] a photoresist mold is used. A solenoid is basically a helical coil and by creating a solenoid, better inductors are expected because the magnetic field is in a plane parallel to the substrate, similar to the rotated inductors, and similar to the wound inductors that are typically known and described previously. In fact, a magnetic core could probably be introduced to this process as these are 3D inductors. These have an advantage, as will be discussed in the modeling section, in that they can easily be designed and modeled since they follow a linear relation between inductance and number of turns. An interesting approach to the solenoid inductor is demonstrated in [47] where stress engineering is used to curl thin metal strips up into a solenoid helix. The two halves of the coil curl together and lock. This is then used as a seed for plating to obtain thick metal coils [47]. Q factors in the range of 50 to 70 have been obtained by this method [47]. It appears, however, that it can be quite hard to ensure that the two parts of the coil will curl the perfect amount and lock together [47]. So this particular process still has lots of work before becoming manufacturable. Figure 1.5 shows a solenoid inductor and a planar inductor for comparison.



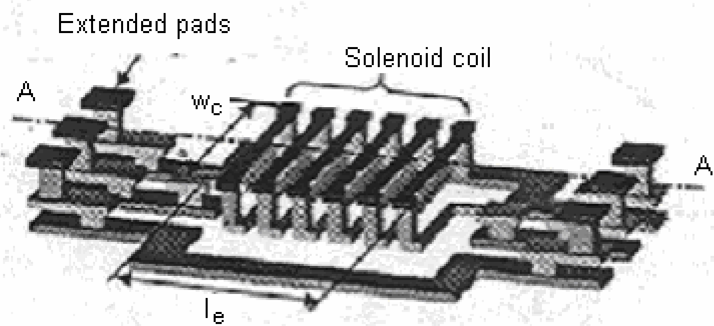


Figure 1.5: A Planar Spiral Inductor (Top) and a Solenoid Inductor (Bottom) [7][9]

Another mainstream MEMS approach to inductors is to suspend them by creating an air gap between the coil and the underpass. Suspending the inductors greatly improves insulation by isolating the inductor from the substrate material. There are also several potentially manufacturable approaches for achieving such a suspension. It has

been done by a variety of approaches including photoresist molding, etching, and flip chip techniques. Out of the MEMS approaches that have been attempted, this and the solenoid approach have the greatest chance of becoming a manufacturable process. This suspension approach is the one approach taken in this work, where a 1µm air gap was created between the coil and the underpass. We have shown the need for good quality passive components, and so this work has chosen one of the optimum substrates, alumina. Since the air gap is relatively small, thus resulting in only some substrate isolation, a good substrate is essential. We have also seen that MEMS has a lot to offer to create good quality inductors and that a simple and manufacturable way to create good inductors would be desirable. This work aims to be a step in that direction and will be described in the following sections and compared in detail with the other suspended inductor work.

1.3 Thesis Organization

In the subsequent chapters this thesis work will be further outlined. In chapter 2 the fabrication and design of the suspended inductors will be described. This will be followed by the results of the characterization, an analysis of the results, a description of previous suspended inductor work, and a comparison of the results to simulation and to the previous work in chapter 3. In chapter 4, the modeling of inductors will be described and summarized. A discussion on the future work that could come from this thesis and some conclusions will be made in chapter 5. Finally, the references used are listed in chapter 6 which is the reference section.

2.0 Design and Simulation

As was argued in the previous section, there is a need for good quality passive components for many wireless applications and so the work that is outlined in this report was generated with those needs and the question “how can the best possible inductors be made” in mind.

All the devices that are part of this work were fabricated at Gennum Corporation in Burlington. The process was therefore necessarily selected as a compromise between Gennum capability, as a gracious corporate sponsor, and the best choice to optimize the inductors and transformers. The goal was also to produce unique structures rather than duplicate previous work, which is still very important as well but for leading into the future rather than replication. Being generated out of more industrial interest, the aim was also for a simpler process that could become relatively easily manufacturable.

2.1 Experimental Fabrication

The substrate of choice, due to good performance at high frequencies, was aluminum oxide, also known as alumina. The main sequence of processing steps are illustrated in Figure 2.1. The first step was sputter deposition of ~1.6-1.8µm of pure aluminum at 200°C and 10mTorr, this will be referred to as M1. Aluminum was chosen here simply for the reason that gold or copper were not options due to contamination concerns, and so aluminum was the best option available as far as conductivity. For most of the inductors, this metal layer was actually not used. Only for two inductors and all the transformers was this metal layer used. In the case of the transformers, this layer formed one of the two coils. In the case of the two inductors, this aluminum layer was used as the inductor coil even though it is directly on the substrate and not suspended. The aluminum was then patterned using standard photolithography techniques. Following this patterning step, approximately 1.2µm of a spin-on-glass(SOG) / phosphosilicate glass(PSG) was deposited as an interlayer dielectric. The phosphosilicate

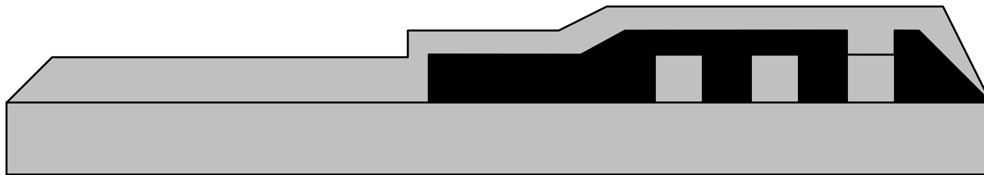
Starting Alumina wafer

1.5µm of Aluminum is sputtered at 200°C, 10mTorr. Deposition takes slightly more than 1 minute.

Aluminum is patterned with photolithography using photoresist.

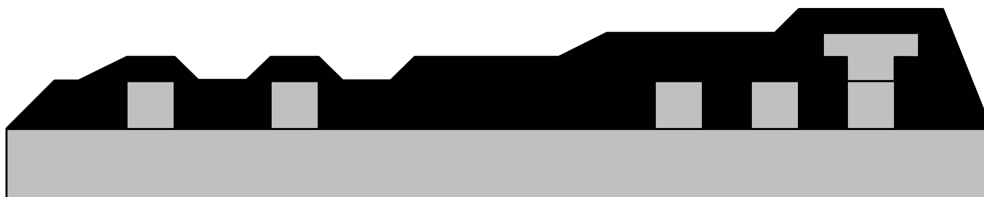
1.2µm SOG/PSG dielectric formed on the wafer. A PSG layer is done in an oven. Then SOG is spun onto the wafer and baked at 250°C. The SOG is etched back. A second PSG layer is done in the oven.

Via etch patterns the SOG/PSG

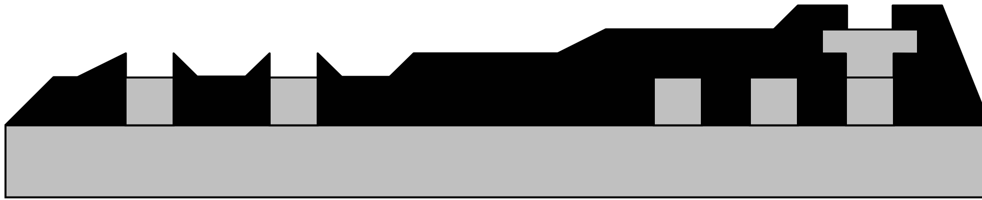


1.5µm of Aluminum is sputtered onto the wafer as before.

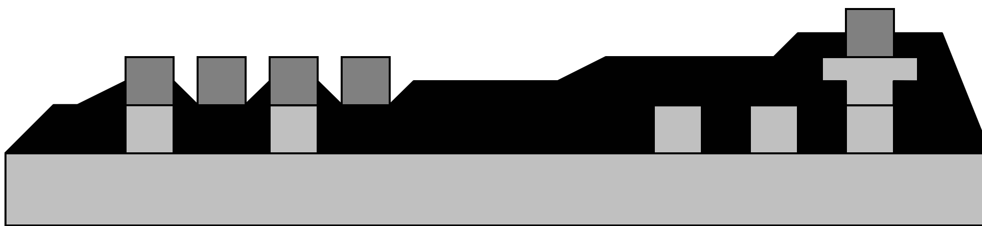
Aluminum is patterned with photolithography.



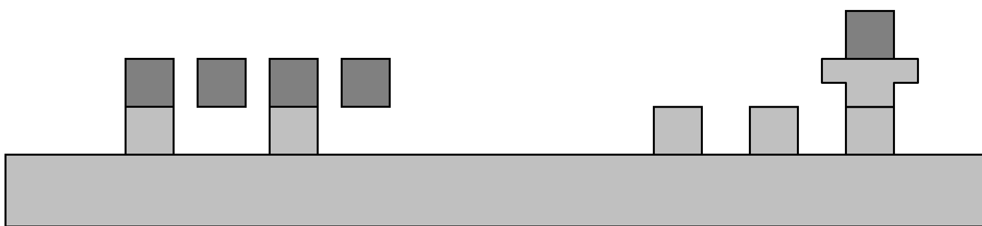
1.2µm of SOG/PSG is again deposited on the wafer as before.



Via etch patterns the second SOG/PSG layer.



6μm of Gold is electroplated. A seed layer is deposited. Photoresit is deposited and patterned. The gold is plated at 50ºC using 4mA/cm^2. The seed layer is etched.



The release etch is performed in BOE for ~2 hours.

Figure 2.1 Process Flow

glass was grown in an oven, followed by an SOG spin and etch-back, and finished with a second PSG growth. This allows a good planarity for the next step. It was felt that even a 1µm air gap between the coil and substrate/underpass would make a significant difference and would also be a cheaper process. The main effect of introducing an air gap is expected to be an increase in self-resonance frequency and peak Q factor. Although, the larger the air gap, the higher the self-resonance frequency and peak Q factor, this thesis work is interested in the frequency range up to 5GHz. This is why an air gap of 1 µm is expected to be significant enough. By using equation 4.38 to calculate the parasitic capacitance (overlap capacitance between the coil and the underpass) and then using equation 3.19, the self-resonance frequency can be estimated for a given air gap. It was also felt that the structures could be more easily released and perhaps more stable because of this as well. The choice of SOG/PSG was made for ease of processing and the planarity provided. Since it is intended to be a sacrificial layer, there were no strict requirements aside from compatibility with the release etch desired.

After the deposition of this dielectric, it was patterned with a via etch to allow the subsequent metal layer to contact the first metal layer, as indicated in Figure 2.1. This via through the dielectric, was opened on approximately half of each die in order to allow the next metal layer to contact the substrate and form the underpass for the inductors on half of the die. (I.e. on half the die it is M2 and not M1 that lies directly on the substrate) Following the via etch, a second, identical layer of aluminum was sputter deposited (M2). This layer was used for the underpass in all but the two previously mentioned inductors. It was used to form an overpass connection to the center of the coil in those two inductors that were created in different layers than the others. This layer was also used as a connection layer on the transformers to connect the two coils together or to bring out an end of one of the coils to a test pad. This second layer of aluminum was then patterned with the same process as the first aluminum layer.

Following this, the 1.2µm of SOG/PSG was also repeated as the second interlayer dielectric. As before, this was patterned by a via etch before proceeding. In the next step, a thin combination metal seed layer was blanket sputtered on the wafer. Photoresist was

then patterned on top of the seed layer to act as a mold for electroplating. Approximately 6μm of gold was electroplated in this manner to form M3 and then annealed. The plating conditions were 50ºC and 4mA/cm^2. Following the plating, the seed layer was then patterned (etched where there is no gold to prevent the entire chip from being shorted). This gold layer was used for the inductor coil on all but two of the inductors (the same two unique inductors mentioned in previous steps) and was also used for the second coil of the transformers. Gold was chosen for its good conductivity, which will make for a good Q factor. In fact, it would have been nice to have had the possibility of doing all three metal layers in gold. The thickness of 6μm was chosen so that the thickness will be greater than two times the skin depth at 2.5GHz. At high frequencies, the current tends to crowd to the edges of the conductor and travel in a ring. This is because the presence of an EM field causes the current to rapidly decay in a good conductor. [48] The skin depth represents the thickness that that ring of current extends into the conductor from the edge. It can be calculated by the following expression [48]:

$$\delta = \frac{c}{\sqrt{2\pi\sigma\omega\mu}}$$

Equation 2.1

Here δ is the skin depth, c is the speed of light, ω is 2*π*frequency, σ is the conductivity of the metal and μ is the magnetic permeability of the metal.

In the case of gold at 2.5GHz, the skin depth is approximately 1.6 μm, so extra caution has been taken, especially since the resistivity of the gold is hard to measure and so had to be approximated [49]. This is because the sheet resistance is extremely low; approximately 3mohms/square. Process variation in the gold thickness is also expected.

At this stage, the processing was paused in order to allow for pre-release testing to be done. Results and testing details are in the following chapter. After this testing was completed, a two hour release in a BOE etch was carried out to remove the interlayer dielectrics from the wafer.

The devices were now complete. Due to a variety of unfortunate circumstances, including the power outage in August 2003, and a few errors during fabrication, only one wafer was able to arrive to this final step and provide released data. A cross sectional view of the structures/process is shown in figure 2.2. Also shown, below this figure, in figures 2.3a and b are some scanning electron microscope (SEM) images of the devices.

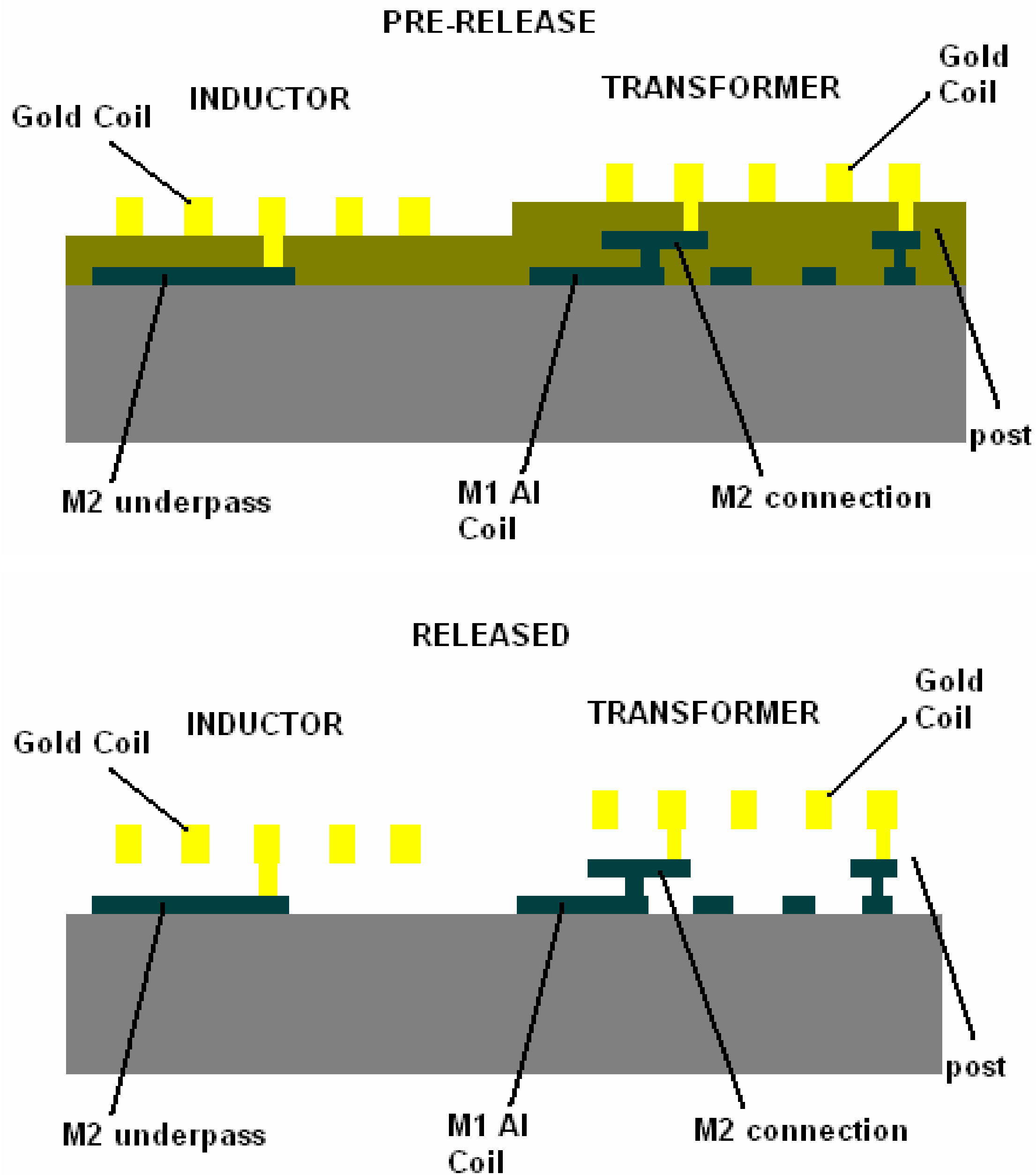
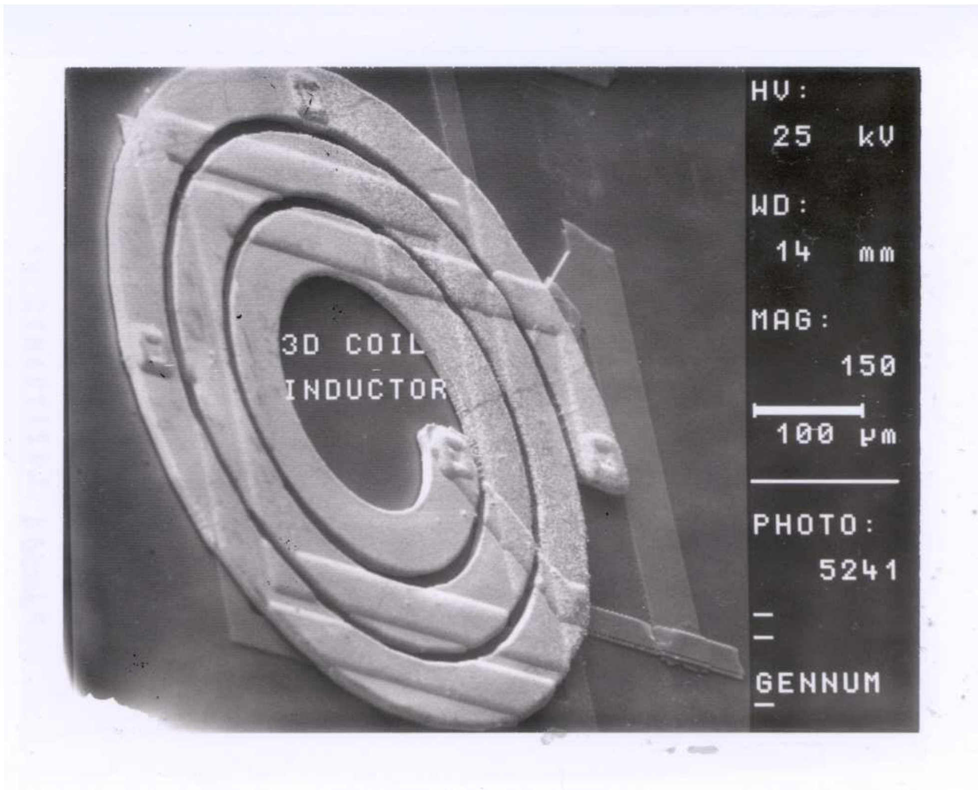


Figure 2.2: Cross Sectional View of the Devices



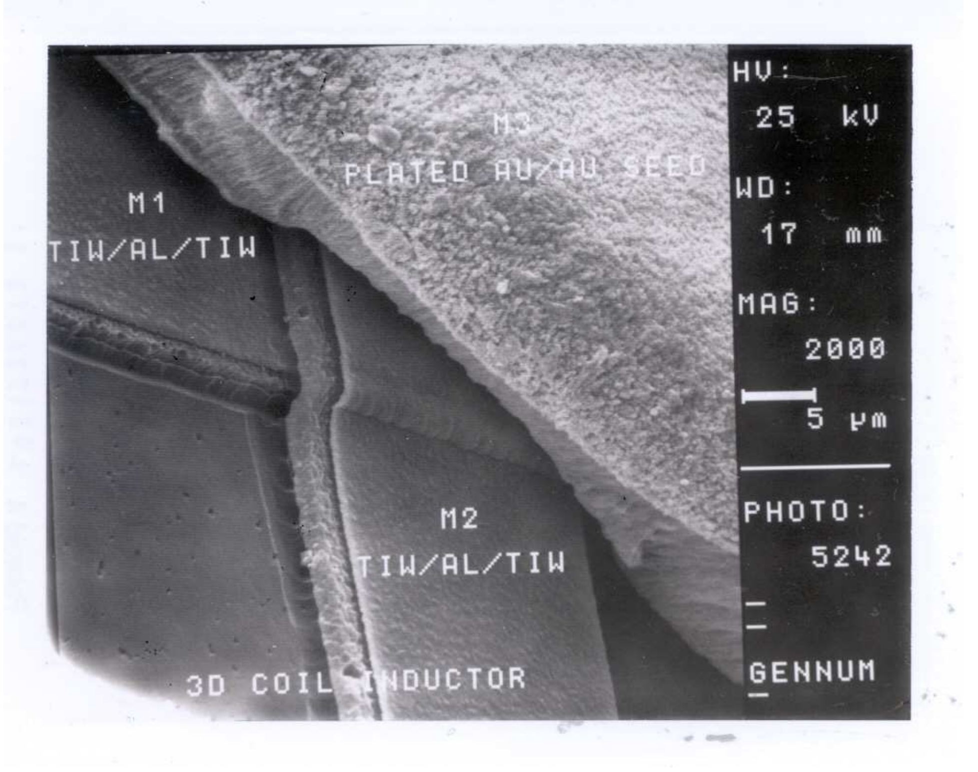


Figure 2.3a and b: SEM Images of the Devices

2.2 Inductor Design

Having set the process, the next step was to design the structures. Many things were considered when coming up with a plan for the design. The range of inductance to include, the variables to include, de-embedding technique, test structures for the release etch and for stress gradient measurements. Alignment structures for the layers as well as the inter-die street size also had to be designed. Another aspect that was taken into account was creation of a DRC(design rule check) file for Dracula. Dracula is a UNIX program that, among other things, is able to check a design file against a set of design rules for the various layers.

A range of 1nH to 27nH was chosen for inductance since this covers both a useful range of inductance for RF circuits for wireless communications, as well as a range that should be good for use as RF chokes for management of DC currents at the same time as the AC currents. The de-embedding technique chosen was to simply use an open and a short structure. The open structure was created by removing the inductor and just leaving the leads, and the short created by removing the inductor and shorting the leads to the test ground. This was chosen as a well recognized technique in the industry that has been successfully used for years at Gennum. For the structure to test the release and measure the stress gradient, advice was gathered from a colleague, Mircea Capanu, who is a MEMS expert at Gennum Corporation. Based on this advice, a series of cantilevers were created in each of the two released layers. These were clamped-free cantilevers so that one end would be free to bend under stress upon release. Beside each cantilever, the identical cantilever as a clamped-clamped structure was placed for use as a reference. On both of these structures there were tabs designed every 50µm so that the deflection could be more easily measured. This will hopefully lead to being able to measure the stress gradient across the clamped-free cantilever. The cantilevers were designed with 30µm and 50µm widths and 200µm, 500µm, 700µm, and 900µm lengths. Tables 2.1 and 2.2 below outline the devices that were designed for this project. Note that the number of posts does not include the connection to the underpass, but only the number of support posts.

Inductance	Number of Turns	Spacing	Width	Number of Posts	Coil Metal	Underpass Metal	Shape
10nH	3.25	26	26	7	Gold	aluminum	square
10nH	3.25	26	26	2	Gold	aluminum	square
4nH	2	26	40	4	Gold	aluminum	square
4nH	2	26	40	2	Gold	aluminum	square
3nH	2	24	35	4	Gold	aluminum	square
3nH	2	24	35	2	Gold	aluminum	square
4nH	3	22	50	1	Gold	aluminum	round
1.4nH	2	22	70	1	Gold	aluminum	round
1.6nH	2	22	70	5	Gold	aluminum	square
1.6nH	2	22	70	2	Gold	aluminum	square
27nH	7.25	22	20	16	Gold	aluminum	square
27nH	7.25	22	20	7	Gold	aluminum	square
4nH	2	26	40	0	1st aluminum	aluminum(over)	square
3nH	2	24	35	0	1st aluminum	aluminum(over)	square

Table 2.1: Inductors included in the design.

	top coil	bottom coil	Inverting
Transformer 1	round 1.4nh	3nh	No
Transformer 2	10nh	3nh	No
Transformer 3	10nh (few posts)	4nh	No
Transformer 4	3nh	3nh	No
Transformer 5	3nh	3nh	No
Transformer 6	3nh	3nh	Yes

Table 2.2: Transformers included in the design (measured)

The final chip design is shown in figure 2.4 below. Note that there are a few transformers that were not measured. This is due to probing limitations, with the network analyzer only having two ports, as well as time constraints. A round of measurements on one wafer, at five sites requires ten hours of testing.

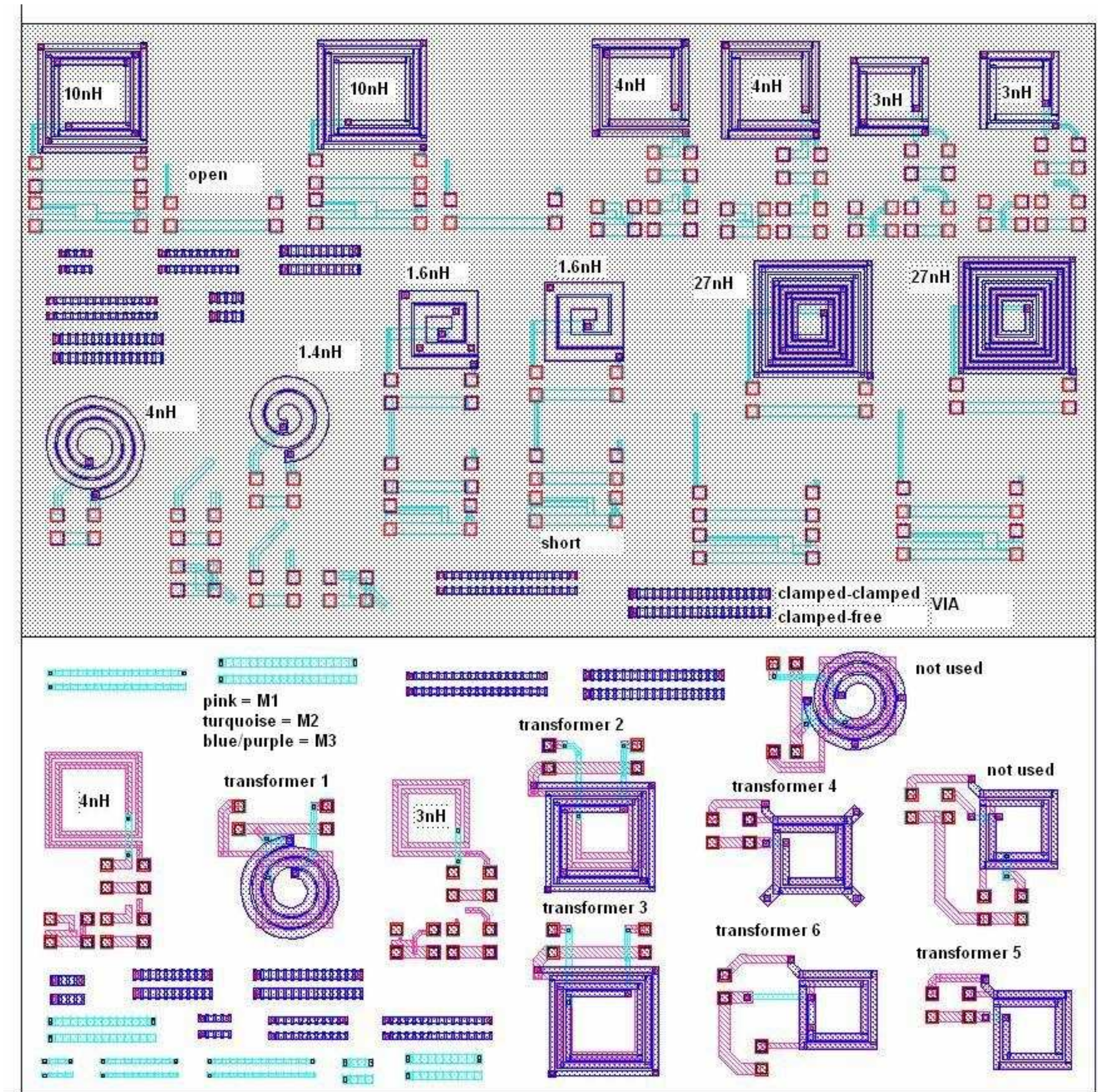


Figure 2.4:Image of Design used in this Work. Inductors, transformers and cantilevers are indicated.

The inductors were designed in a free EM simulation program called ASITIC. This program was developed at the University of California, Berkeley. [8] It solves Maxwell's equations for inductors, capacitors, and transformers using Green's functions with the input of a technology file with the layer details. One can then build coils right in the program. This program has the ability to generate CAD drawings and to give one the inductance of the coil very quickly. It can also generate a Q value estimate and π model, however, this aspect of ASITIC was not used as a more accurate 3D EM simulation tool was available. The inductors were designed, imported into Cadence, and put together to

form a chip. Cadence is a well known semiconductor CAD tool for design. The drawings were put on the appropriate layers, the posts to hold up the coil when suspended were added, the transformers were designed, and the cantilever structures were designed. Everything was then connected to AC pads for measurements and the de-embedding structures created. The design was then reviewed and a design rule check performed. Masks were created at Gennum Corporation and the fabrication began.

In order to predict the performance of the devices, all the devices except for the cantilevers were simulated in Ansoft HFSS, a 3D EM simulator. This simulator divides the design into tetrahedra and then solves for the electric and magnetic field on the surface of the tetrahedra in order to extrapolate for the fields on the inside of the tetrahedra. Depending on the type of port that is used, this determines how the simulation will start. A lumped gap port, for example, simply declares a voltage difference (or essentially a ground reference for the simulation) and goes from there; a wave port will solve a 2D microstrip problem at the port and then let this solution propagate into the 3D matrix.

For the purposes of these simulations, a few approaches were used to try to maximize accuracy. The first step was simply importation of the design from a cadence gdsII file directly into 3D geometries in HFSS. This was possible due to the use of a technology file which was created. Then the simulation was set up with material assignment and port and boundary assignment. Because we want a Q estimate, for all metal parts the 'solve inside' option was selected. This will ensure that the skin effect is taken into account. Lumped gap ports were used between the two signal pads and the ground pad so that the exact same AC pad and setup that would be measured was simulated. Other options that were selected were solving with low order basis functions as well as trying to allow/setup a larger than usual number of mesh elements on the surfaces. Simulations required approximately 30 minutes of setup and one hour of simulation time. Simulation results are compared with measured results in the following chapter on results.

3.0 Experimental Results of the Inductors and Transformers

3.1 Measurement Set Up

All the devices were measured in the research and development lab at Gennum Corporation. A Hewlett Packard 8720 network analyzer in conjunction with their IC-CAP software was used to measure and record the data. This analyzer is capable of measuring up to 20GHz. 24GHz shielded SMA coaxial cable was used to connect the analyzer to the GGB Industries ground-signal (GS) microwave probes. Before any measurements were performed, a thirty minute instrument warm-up period was allowed followed by instrument calibration using a CS-8 calibration substrate, also from GGB industries. This substrate provides a short-open-load-through (SOLT) type calibration. As it was allowed by the analyzer, an isolation measurement was also performed as part of the calibration. In order to remove the effect of the measurement pads and leads, de-embedding structures consisting of an open and short (device removed, as described in the previous section) were also measured. During measurement sessions, a calibration was performed approximately every four hours. The IC-CAP software handled the data collection and all the GPIB (general purpose instrument bus) communication with the analyzer. So the S parameter data was available to view and run routines on immediately after the measurement.

3.2 Parameter Extraction

The desired parameters were then extracted from the data, which is received in the form of scattering parameters (S Parameters). All the measurements reported here are two port so we have four S parameters. S_{11} and S_{22} represent the reflected signal from port 1 and 2 respectively. S_{12} and S_{21} represent the transmitted signal in the forward and reverse direction respectively between port 1 and port 2. For a symmetric, passive, two port network, S_{12} and S_{21} should theoretically be equal. Obviously in a real measurement there is some variation due to manufacturing and material tolerances as well as

measurement error. When measuring the reflected parameters, S_{11} and S_{22}, the other port is terminated by 50 ohms to ground. In order to get the de-embedded results, S_{11} and S_{22} from the open structure are subtracted from S_{11} and S_{22} of the device. This removes the parasitic capacitances associated with the measurement pads. S_{12} and S_{21} of the short measurement are subtracted from S_{12} and S_{21} of the device measurement. This removes the parasitic inductance of the leads going to the device. By making these simple subtractions, the performance of the device, without leads and pads, can be accurately assessed. This de-embedding technique is relatively well known, and has been successfully used at Gennum.

To extract parameters such as inductance, Q factor, etc, we need to convert to admittance parameters (Y parameters). This conversion is done by the following set of equations [50]:

$$Y_{11} = \frac{Y_o\left[(1-S_{11})(1+S_{22})+S_{12}S_{21}\right]}{\left[(1+S_{11})(1+S_{22})-S_{12}S_{21}\right]}$$

Equation 3.1

$$Y_{12} = \frac{-2Y_oS_{12}}{\left[(1+S_{11})(1+S_{22})-S_{12}S_{21}\right]}$$

Equation 3.2

$$Y_{21} = \frac{-2Y_oS_{21}}{\left[(1+S_{11})(1+S_{22})-S_{12}S_{21}\right]}$$

Equation 3.3

$$Y_{22} = \frac{Y_o\left[(1+S_{11})(1-S_{22})+S_{12}S_{21}\right]}{\left[(1+S_{11})(1+S_{22})-S_{12}S_{21}\right]}$$

Equation 3.4

Y_o in these equations is $1/Z_o$ or 1/(characteristic impedance). In the case of this work, a 50 ohm characteristic impedance was used, as everything was measured in a 50 ohm system. From these Y parameters we can use the equivalent model shown in figure 3.1 below to extract a π model [51].

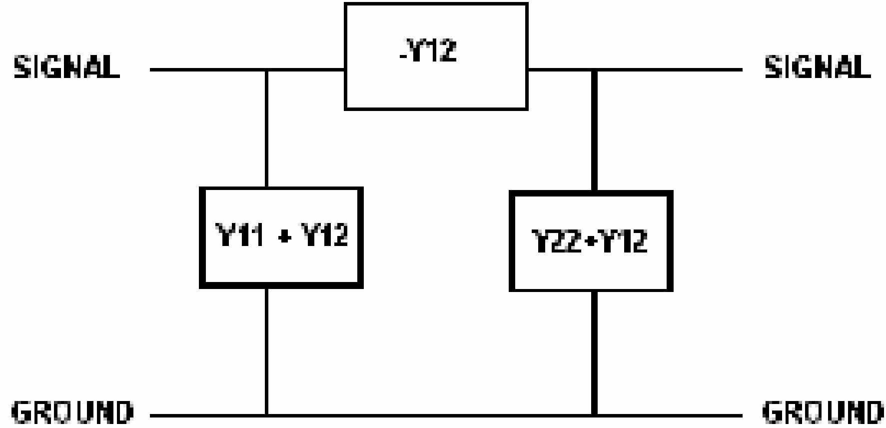


Figure 3.1: Pi Equivalent Circuit for a 2 port network

Now Y_{12} is the impedance across the device, as we can see from the figure. We can simply use the following to then find the series inductance and resistance [50][51].

$$L = \frac{\mathrm{Im}\left[\frac{-1}{Y_{12}}\right]}{\omega}$$

Equation 3.5

$$R = \mathrm{Re}\left[\frac{-1}{Y_{12}}\right]$$

Equation 3.6

This is from $-1/Y_{12}$ = series impedance = $Z = R + j\omega L$.

Note that since we can only extract the real and imaginary part of the impedance between the two ports and from each port to ground, we really can not accurately extract both an inductance and a capacitance between the same two points by this method. One way to be able to extract both an inductance and a capacitance is with the aid of software. In IC-CAP, for example, one can input an equivalent circuit and get the software to fill in the values based on the measurement data. This was not done for this work, however. There are also ways of trying to do this analytically as well. One way is to set up a system of three equations (i.e. three frequency points) and three unknowns, R, L and C by expanding the equation shown above to:

$$-Y_{12} = Z = \frac{1}{(R + j\omega L)^{-j\omega C}}$$

Equation 3.7

A more rigorous approach is given in the work in [52]. Here the real and imaginary parts of Y_{12} are isolated. Doing this, they obtained [52]:

$$-Y_{12} = \frac{R}{\left(R^2 + (\omega L)^2\right)} + j\left[\omega C - \frac{\omega L}{\left(R^2 + (\omega L)^2\right)}\right] = g - jb$$

Equation 3.8

Now if one recognizes that b = b(ω,L(ω),R(ω),C(ω)), then for two points that are close to each other we get [52]

$$\Delta b = \left(\frac{\delta b}{\delta \omega}\right)\Delta\omega + \left(\frac{\delta b}{\delta L}\right)\Delta L + \left(\frac{\delta b}{\delta R}\right)\Delta R + \left(\frac{\delta b}{\delta C}\right)\Delta C$$

Equation 3.9

$$L = \frac{\Delta\omega\left[1-\left(\frac{R}{\omega L}\right)^2\right]\left[1+\frac{d\ln L}{d\ln\omega}-2\left(\frac{R}{\omega L}\right)^2\left(\frac{d\ln R}{d\ln\omega}\right)\right]}{\omega^2\left[1+\left(\frac{R}{\omega L}\right)^2\right]^2\left(-\Delta b-\Delta(\omega C)\right)}$$

Equation 3.10

Where the L shown above is the full solution as given in [52]

Following from [52] we now make the following assumptions: Δω C << Δb (true below self-resonance), a slowly varying L (ie: d ln L/d ln ω is small), and R << ωL. This leads to the following two equations [52].

$$R = 0.5g\left(1-\sqrt{1-2(2g\omega L)}\right)$$

Equation 3.11

$$L = -\frac{\left[1-\left(\frac{R}{\omega L}\right)^2\right]\Delta\omega}{\omega^2\left[1+\left(\frac{R}{\omega L}\right)^2\right]^2\Delta b}$$

Equation 3.12

By starting with R/ ωL = 0, the above two equations can be iteratively solved for L and R [52]. Following that C can be found from the following equation given in [52]

$$C = \left(\frac{1}{\omega}\right)\left(\left(\frac{\omega L}{\left(R^2+(\omega L)^2\right)}\right)-b\right)$$

Equation 3.13

For this thesis work, the first, simple method was used. What will come out in that case is a frequency dependant inductance value, rather than a combination of an

inductor in parallel with a capacitor where both have static values. Using this approach, of a frequency dependent inductance, the self-resonance frequency can then be identified by the point where the inductance value maximizes and then quickly becomes negative. The inductance becoming negative is simply a mathematical result of the above formulae used for extraction. It simply indicates that the device has gone from being inductive to being capacitive and is a mathematical artifact due to dealing with imaginary numbers. In reality, the skin effect causes the inductance to decrease with frequency, but via this extraction method our inductance is tied in with the capacitance.

The shunt parasitics are simpler to extract, though can suffer the same problems. They are given below:

$$R_{p1} = \mathrm{Re}\left(\frac{1}{(Y_{11}+Y_{12})}\right)$$

Equation 3.14

$$C_{p1} = \frac{\mathrm{Im}(Y_{11}+Y_{12})}{\omega}$$

Equation 3.15

$$R_{p2} = \mathrm{Re}\left(\frac{1}{(Y_{22}+Y_{21})}\right)$$

Equation 3.16

$$C_{p2} = \frac{\mathrm{Im}(Y_{22}+Y_{21})}{\omega}$$

Equation 3.17

Once again, we have simply used the pi model definition and split it into real and imaginary parts.

3.3 Q Factor

Finally we will have a look at the extraction of the quality factor (Q factor). The Q factor is a measure of the efficiency of the inductor and is an indication of how much energy is lost or dissipated in the inductor. One method of calculating the Q factor is given by the following equation [53]:

$$Q = \frac{\mathrm{Im}\left(\frac{1}{Y_{11}}\right)}{\mathrm{Re}\left(\frac{1}{Y_{11}}\right)}$$

Equation 3.18

Where Im stands for the imaginary part of the parameter ($1/Y_{11}$) and Re stands for the real part of the parameter ($1/Y_{11}$). As seen from the equation, this method can be calculated directly from the Y parameters. The reason to choose Y_{11} is that it is actually the most common way reported in literature. Using Y_{11} means that one is treating the inductor as a 1 port device, where port 2 is terminated by 50 ohms to ground.

The other method of calculating the Q factor that has been used in this work is called the 3dB method. In this method what is done is that at each frequency, for the purpose of calculation, it is considered that there is a capacitor in parallel with the inductor. The capacitance value that is chosen is the value that will make this parallel combination resonate at the calculation frequency. The 3dB bandwidth of this resonance is then measured. The following equation can be used to determine the capacitance value to create resonance at a given frequency:

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

Equation 3.19

Here f_o is the resonance frequency and L and C are the inductance value and capacitance value respectively. For the purposes of measured data, a better definition is to insert an ideal capacitor in shunt with the inductor with an admittance equal to the imaginary part of Y_{11} [8]. So the admittance becomes

$$Y' = j\omega C + Y_{11}$$

Equation 3.20

$$C = \frac{-\mathrm{Im}\left[Y_{11}(\omega_o)\right]}{\omega_o}$$

Equation 3.21

This will resonate the device at the frequency of interest and we can simply measure the 3dB bandwidth of the resonance to get the Q [8]:

$$Q = \frac{\omega_o}{\Delta\omega_{3dB}}$$

Equation 3.22

Here ω_o is the value of ω at the frequency the Q factor is being calculated at, and $\Delta\omega_{3dB}$ is the 3dB bandwidth of the resonance. The interest in the 3dB method to calculate the Q factor is that it is more accurate near the self-resonance frequency of the device. The main failing of the 3dB method is that, if a coarse step is used in measurement frequency, then interpolating the bandwidths to calculate the Q factor can lead to poor accuracy. So, for example, this method would not work on data that is very coarse and had a frequency step of 0.5GHz.

Another method of Q calculation, is calculating the derivative of the phase, as shown in [8]:

$$\left({}^{\delta\varphi}\!/_{\delta\omega}\right)_{\omega_o} = \frac{2Q}{\omega_o} = \frac{ang\left(Y'\left(\omega_o + \delta\omega\right)\right) + ang\left(Y'\left(\omega_o - \delta\omega\right)\right)}{2\delta\omega}$$

Equation 3.23

There are also two or three other methods of calculating the Q factor but they are rarely reported or used so will not be listed here.

Using routines that were developed at Gennum Corporation and available directly in IC-CAP, these extractions were performed and all of this data was calculated for each device.

3.4 Measurement Results

Devices were measured before and after release. Five sites were measured on the one properly processed wafer after release. There is actually pre-release data from five sites on three wafers. The following series of tables shows the averages of the results of these measurements.

INDUCTANCE VALUES

	Site 1		Site 2		Site 3		Site 4	
	Pre-release	Post-release	Pre-release	Post-release	Pre-release	Post-release	Pre-release	Post-release
10nH 4post	9.42602	9.21998	9.42965	9.21093	9.43738	9.22031	9.45704	9.2471
10nH 2post	9.44992	9.16817	9.44327	9.10627	9.45085	9.18892	9.44853	9.19931
4nH 4post	3.81638	3.79423	3.81219	3.78115	3.81245	3.79819	3.83108	3.83997
4nH 2post	3.81996	3.77364	3.82457	3.75517	3.79653	3.75367	3.84575	3.82524
3nH 4post	2.895	2.89659	2.90602	2.88866	2.904	2.9053	2.89627	2.97015
3nH 2post	2.90659	2.88328	2.89903	2.88127	2.9137	2.90038	2.90434	2.95964
4nH_rnd	3.83598	3.80291	3.83402	3.84388	3.84296	3.82352	3.83452	3.8871
1nH_rnd	1.23913	1.2689	1.24906	1.27991	1.27048	1.28333	1.25338	1.34708
1.5nH 4post	1.61117	1.61142	1.6001	1.63208	1.61291	1.63553	1.61267	1.68633
1.5nH 2post	1.59786	1.6212	1.60053	1.6382	1.62246	1.63294	1.61808	1.68897
27nH 4post	30.5307	28.7245	30.4364	28.7108	30.5351	28.5212	30.4477	28.5104
27nH 2post	30.5209	28.3219	30.428	28.1167	30.5111	27.9107	30.4103	27.9983
4nH_al	4.06068	4.03858	4.05369	4.04801			4.05343	4.10368
3nH_al	3.11683	3.1277	3.11175	3.13321	3.12981	3.15301		3.18173

	Site 5		AVG		STD DEV	
	Pre-release	Post-release	Pre-release	Post-release	Pre-release	Post-release
10nH 4post	9.45058	9.2903	9.440134	9.237724	0.013338	0.032358
10nH 2post	9.39677	9.23292	9.437868	9.179118	0.023161	0.046971
4nH 4post	3.82497	3.83351	3.819414	3.80941	0.008319	0.025834
4nH 2post	3.81032	3.80291	3.819426	3.782126	0.018213	0.031222
3nH 4post	2.91658	2.95442	2.903574	2.923024	0.008692	0.036744
3nH 2post	2.90084	2.94226	2.9049	2.913366	0.005735	0.035637
4nH_rnd	3.84195	3.87661	3.837886	3.846804	0.004248	0.035318
1nH_rnd	1.25465	1.35152	1.25334	1.306148	0.011355	0.039782
1.5nH 4post	1.6276	1.68441	1.61289	1.649954	0.009785	0.033626
1.5nH 2post	1.61556	1.68602	1.610898	1.653466	0.011005	0.031685
27nH 4post	30.5172	28.4334	30.49342	28.58006	0.047524	0.130175
27nH 2post	30.4801	27.7803	30.47008	28.02558	0.04927	0.206284
4nH_al	4.07051	4.10398	4.059578	4.073563	0.008025	0.035162
3nH_al	3.11403	3.18757	3.118105	3.156644	0.008075	0.027321

Table 3.1: Measured Inductance Values for the Devices (1GHz values before self-resonance rise)

SELF-RESONANCE FREQUENCIES

	Site 1		Site 2		Site 3		Site 4	
	Pre-release	Post-release	Pre-release	Post-release	Pre-release	Post-release	Pre-release	Post-release
10nH 4post	5.7	10.5	5.7	10.9	5.6	10.8	5.6	10.8
10nH 2post	5.7	16	5.7	10.3	5.6	16.2	5.7	16
4nH 4post	8.2	10.3	8.4	13.9	8.2	13.7	8.2	13.8
4nH 2post	8.3	10.1	8.4	15.2	8.2	15.1	8.2	14.9
3nH 4post	11	15.4	11.1	18.5	10.9	18.3	10.9	18.3
3nH 2post	11	15.3	11	18.8	10.9	18.6	10.9	18.7
4nH_rnd	9.9	16.7	9.5	>20	9.8	19.6	9.9	16.1
1nH_rnd	>20	>20	>20	>20	>20	>20	>20	>20
1.5nH 4post	10.5	>20	10.6	>20	10.5	>20	10.5	>20
1.5nH 2post	10.5	>20	10.6	>20	10.5	>20	10.5	>20
27nH 4post	3.3	5.1	3.3	5.3	3.3	5.5	3.3	5.5
27nH 2post	3.3	5.7	3.3	5.7	3.3	5.9	3.3	6
4nH_al	7.9	12.7	7.9	12.6		10.1	7.8	12.7
3nH_al	10.5	16.1	10.4	16	10.3	16.2		16.1

	Site 5		AVG		STD DEV	
	Pre-release	Post-release	Pre-release	Post-release	Pre-release	Post-release
10nH 4post	5.7	9.3	5.66	10.46	0.05477226	0.6655825
10nH 2post	5.7	16.7	5.68	15.04	0.04472136	2.6651454
4nH 4post	8.1	14	8.22	13.14	0.10954451	1.5915401
4nH 2post	8.1	15.2	8.24	14.1	0.11401754	2.2394196
3nH 4post	11	18.8	10.98	17.86	0.083666	1.3903237
3nH 2post	11	18.9	10.96	18.06	0.05477226	1.5469324
4nH_rnd	10	>20	9.82	17.466667	0.19235384	1.8717194
1nH_rnd	>20	>20	N/A	N/A	N/A	N/A
1.5nH 4post	10.7	>20	10.56	N/A	0.08944272	N/A
1.5nH 2post	10.7	>20	10.56	N/A	0.08944272	N/A
27nH 4post	3.3	5.6	3.3	5.4	0	0.2
27nH 2post	3.3	6	3.3	5.86	0	0.1516575
4nH_al	7.9	12.8	7.875	12.18	0.05	1.1649034
3nH_al	10.4	16.1	10.4	16.1	0.08164966	0.0707107

Table 3.2: Table showing the pre and post-release self-resonance frequencies

Q FACTOR @ 2.5GHz (3dB method)

	Site 1		Site 2		Site 3		Site 4	
	Pre-release	Post-release	Pre-release	Post-release	Pre-release	Post-release	Pre-release	Post-release
10nH 4post	27.36495	27.42855	27.5836	28.1523	28.0116	29.8588	26.1566	29.72725
10nH 2post	27.37275	35.33755	29.4378	32.2093	28.1779	37.97215	26.5544	39.05605
4nH 4post	39.55385	41.3602	6.06041	41.1541	39.9772	43.3468	39.3349	35.5901
4nH 2post	39.539	41.7352	6.059815	43.05645	40.5232	46.1464	39.31775	36.8912
3nH 4post	41.04735	38.4589	40.0765	40.0252	40.68995	42.75605	40.87245	33.898
3nH 2post	40.56565	41.38965	40.99985	39.9722	40.42735	43.8228	41.449	34.97035
4nH_rnd	40.76665	41.10035	19.87781	45.20495	39.48215	43.8968	41.99175	36.60415
1nH_rnd	36.92225	32.17235	19.57731	37.3872	33.1539	34.4204	39.33725	27.0043
1.5nH 4post	34.0627	32.5868	36.42235	35.42035	33.0764	34.6975	48.1682	28.22085
1.5nH 2post	35.07775	34.63675	35.58145	36.36325	32.4317	35.2412	43.13475	28.40325
27nH 4post	9.03986	8.707555	8.852445	10.2928	9.82378	9.16955	9.17618	9.033405
27nH 2post	9.28233	9.900195	9.26772	10.97603	9.89127	10.92774	8.864425	9.5199
4nH_al	22.31895	20.55635	21.51935	21.58995	1.079628	0.692493	21.4572	18.64335
3nH_al	20.13635	19.13965	19.42025	20.3572	18.6425	20.1572	0.632488	17.8409

	Site 5		AVG		STD DEV	
	Pre-release	Post-release	Pre-release	Post-release	Pre-release	Post-release
10nH 4post	30.2904	25.75015	27.88143	28.18341	1.51249575	1.7089404
10nH 2post	18.92215	35.15065	26.093	35.94514	4.14747618	2.6806441
4nH 4post	47.48375	35.91615	34.482022	39.47347	16.2504139	3.5043559
4nH 2post	51.2468	37.64895	35.337313	41.09564	17.1075652	3.8510056
3nH 4post	41.01985	34.3525	40.74122	37.89813	0.39782309	3.7752751
3nH 2post	39.44275	35.1121	40.57692	39.05342	0.74970546	3.9132652
4nH_rnd	38.9779	36.41645	36.219252	40.64454	9.21004792	4.0553605
1nH_rnd	39.38505	27.2348	33.675153	31.64381	8.27989502	4.5260291
1.5nH 4post	26.32755	28.10985	35.61144	31.80707	7.95841432	3.4838472
1.5nH 2post	17.882	28.46015	32.82153	32.62092	9.25218512	3.8741199
27nH 4post	9.412275	9.24757	9.260908	9.290176	0.37503998	0.5972854
27nH 2post	9.513895	10.90671	9.363928	10.446115	0.37616391	0.6857155
4nH_al	22.2245	18.70385	17.7199257	16.037199	9.31053905	8.6691811
3nH_al	20.8239	17.73445	15.9310976	19.04588	8.59064908	1.2384679

Table 3.3: 3dB Q Factor values @ 2.5GHz for the devices

Q Factor @ 2.5GHz (Traditional Method)

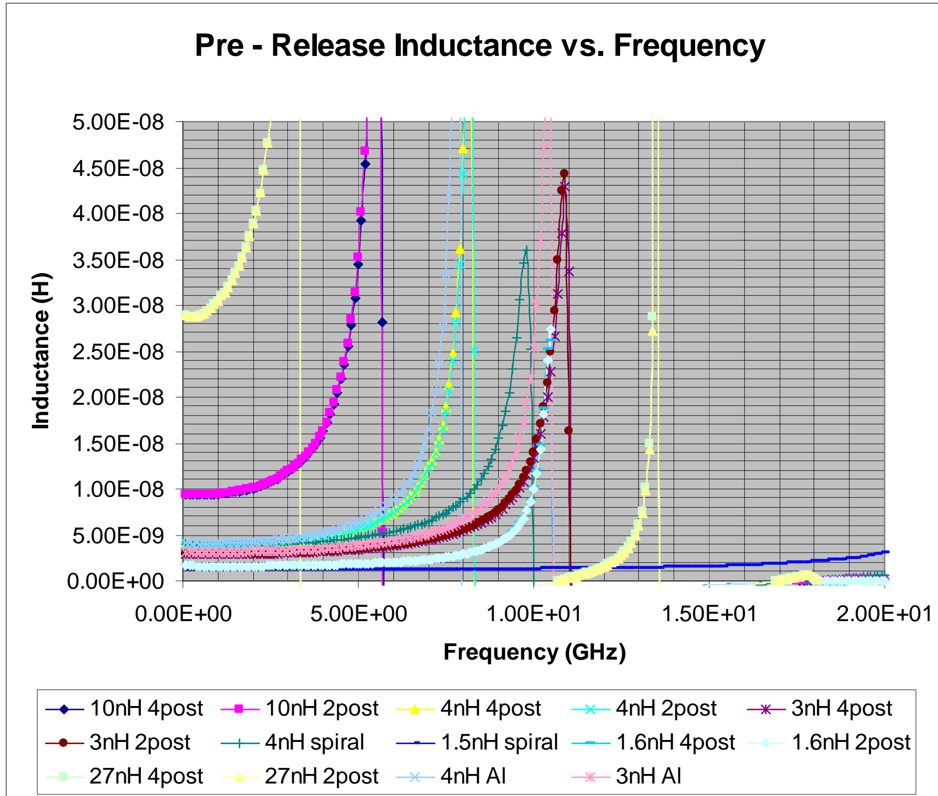
	Site 1		Site 2		Site 3		Site 4	
	Pre-release	Post-release	Pre-release	Post-release	Pre-release	Post-release	Pre-release	Post-release
10nH 4post	14.89845	17.656	14.25655	17.25905	14.1169	19.3686	14.1526	19.10675
10nH 2post	14.84795	24.4785	15.11725	19.61485	14.2144	27.04795	14.31445	27.399
4nH 4post	29.67775	30.8951	29.67585	32.4804	28.0656	36.2801	29.24875	29.33335
4nH 2post	29.65905	31.4533	29.1459	34.86065	28.5014	39.9737	29.2396	31.06935
3nH 4post	33.2398	30.5557	30.6912	33.32405	31.54825	37.56515	33.2757	29.38755
3nH 2post	32.7761	33.09375	31.49255	33.4348	31.3009	38.96425	33.9015	30.55135
4nH_rnd	31.82465	33.3076	30.4984	41.9747	31.1142	39.64355	32.07325	30.9799
1nH_rnd	33.30005	29.9266	30.8919	41.08055	31.0335	36.54965	32.4776	27.24525
1.5nH 4post	22.102	21.58415	22.56715	25.7456	22.1022	24.6884	23.78365	20.72345
1.5nH 2post	22.5704	22.6537	22.2219	26.35065	21.7897	25.02915	22.12855	20.86445
27nH 4post	-1.21326	1.176517	-1.25694	1.88577	-1.65705	1.85894	-1.55853	1.57191
27nH 2post	-1.19801	2.208385	-1.27680	2.64416	-1.61306	3.019485	-1.50634	2.51675
4nH_al	15.93425	16.2892	15.5219	17.38055	113.7223	207.3382	15.93775	15.565
3nH_al	16.0761	16.50915	15.8534	17.4802	15.4059	17.3189	16.0062	16.0526

	Site 5		AVG		STD DEV	
	Pre-release	Post-release	Pre-release	Post-release	Pre-release	Post-release
10nH 4post	13.2821333	17.440767	14.1413267	18.166233	0.57564075	0.9924564
10nH 2post	10.56386	26.274433	13.811582	24.962947	1.85348754	3.1952472
4nH 4post	27.0554667	28.887167	28.7446833	31.575223	1.15177853	2.9861941
4nH 2post	28.5648333	30.905233	29.0221567	33.652447	0.48697004	3.8882456
3nH 4post	31.8532667	29.230167	32.1216433	32.012523	1.12128221	3.5109149
3nH 2post	31.146	30.2387	32.12341	33.25657	1.18505755	3.5022008
4nH_rnd	29.6731667	31.122733	31.0367333	35.405697	0.98110873	5.0853876
1nH_rnd	32.9733667	27.602167	32.1352833	32.480843	1.11087515	6.0878409
1.5nH 4post	19.0554	20.836333	21.92208	22.715587	1.74386258	2.3373769
1.5nH 2post	22.4136667	21.0109	22.2248433	23.18177	0.29736108	2.4400881
27nH 4post	-1.83789767	1.4496367	-1.50473873	1.5885547	0.26619944	0.2961399
27nH 2post	-1.81416633	2.52287	-1.48167887	2.58233	0.25042928	0.2926596
4nH_al	15.6445667	15.2785	35.3521643	54.3703	43.810645	85.515533
3nH_al	16.2652333	15.753633	15.9213667	16.622897	0.32392466	0.7604579

Table 3.4: Tradition Q values for the devices at 2.5GHz.

The results show that, as was expected, the main effect of releasing the inductor coils is to increase their useful range by increasing the self-resonance frequency. This is because with air instead of dielectric, the capacitance between the coil and underpass, a parasitic capacitance in parallel with the device, is now reduced. Looking at the equation given earlier in this section we can see that the resonance frequency for a parallel LC combination depends on $1/\sqrt{LC}$. Therefore if the parasitic capacitance, C is lowered, the self-resonance frequency will increase. As we see, the self-resonance frequency increases by over 4GHz for certain devices and this increases the maximum Q value. For the frequency that was chosen to be of interest (due to the many applications such as Bluetooth, WLAN, cell phones, cordless phones, etc), 2.5GHz, the Q factor did not change noticeably, unfortunately. These devices are better for the 5GHz applications after release however. As expected, the posts did not seem to have an effect on the inductor prior to release. The Q values were very close to those achieved in similar inductors made at Gennum on alumina without posts, and unreleased. The inductances of all the devices were measured to be the expected values so it was found that the support posts did not affect the inductance values either.

Upon release, as expected, the data reflects the fact that there are more parasitics in the inductors with more posts. This is shown in the lower self-resonance frequencies and Q factors in the ‘four post’ devices as compared to the ‘two post’ devices. It is therefore better to design these suspended inductors with as few supports as necessary to minimize this degradation caused by the posts. There was a slight decrease in the inductance of all the inductors after the release step. This can most likely be attributed to differences in the magnetic field of the inductor in the air vs. the dielectric. The following figures give a summary of the inductor results.



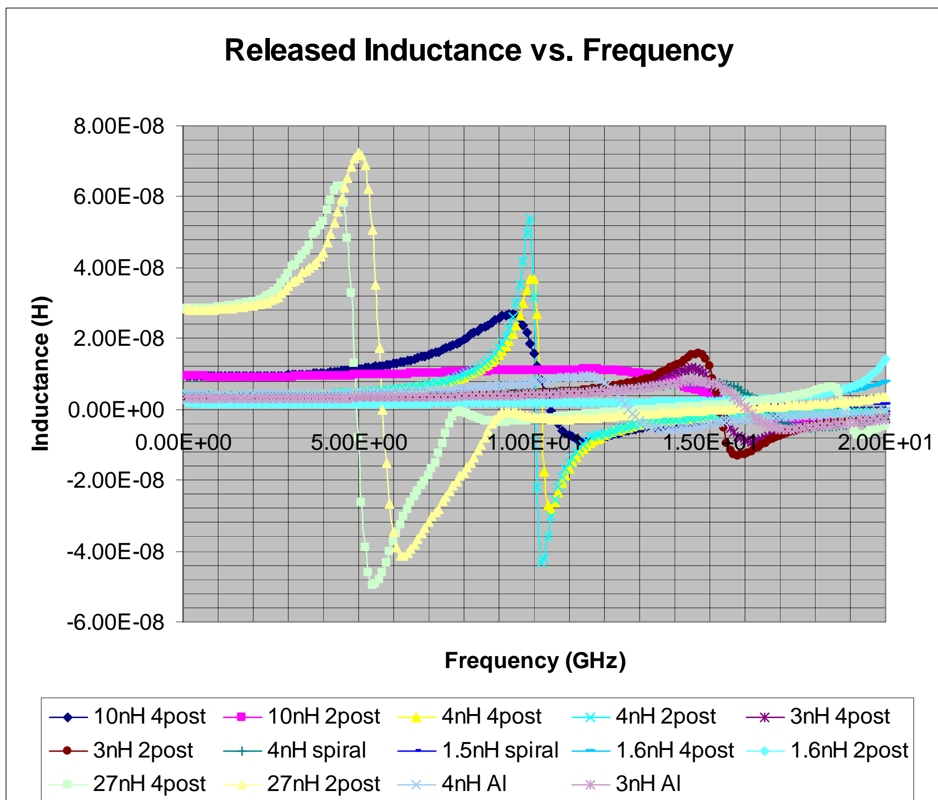
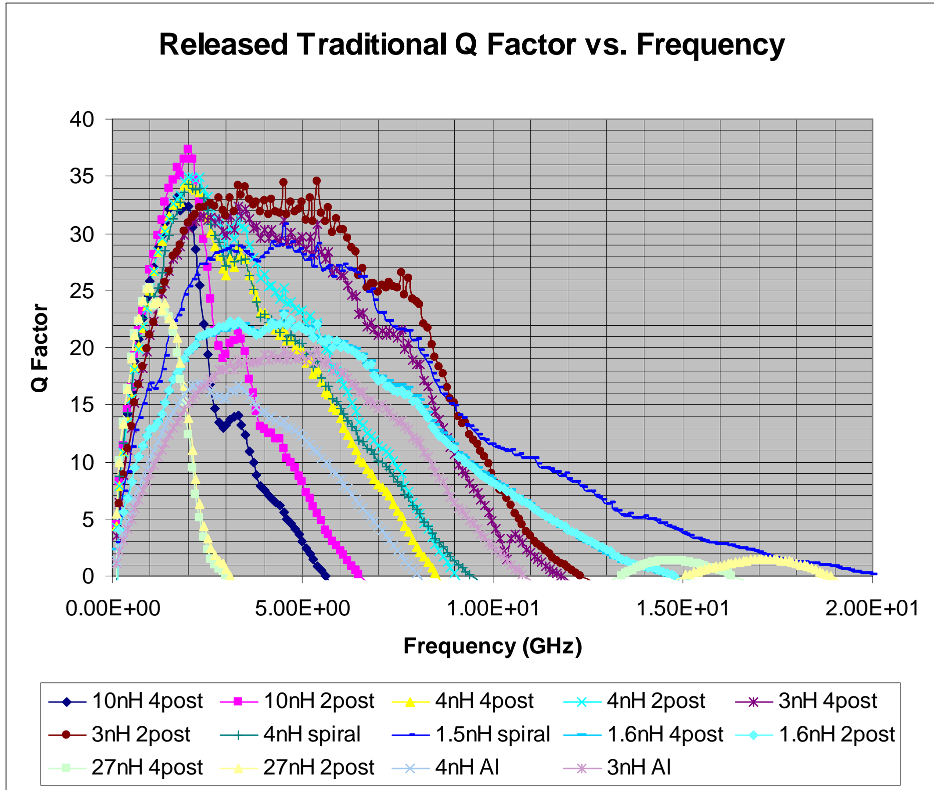


Figure 3.2: Inductance vs Frequency pre and post release



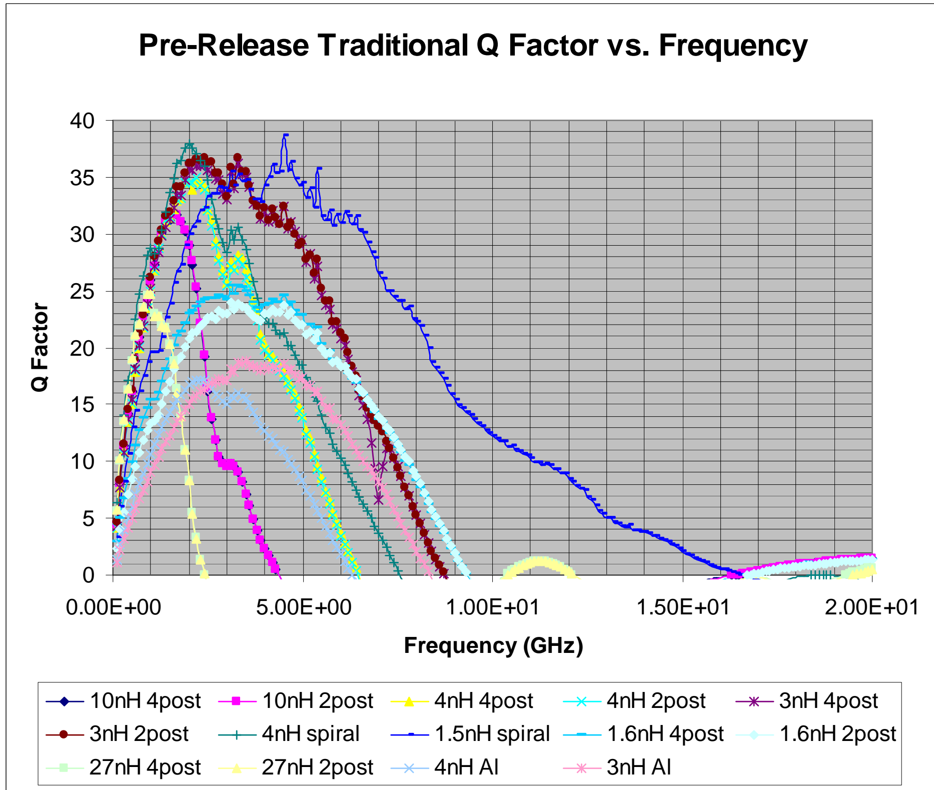


Figure 3.3: Traditional Q Factors before and after release

The results obtained, both before and after release for the inductors indicate that these inductors are suitable for the 1-5GHz applications targeted, even if the Q factor at 2.5GHz remained similar to the unreleased value. (Bluetooth, cellular systems, WLAN etc) The Q factor is high for most of the inductors in this frequency range and the self-resonance frequencies large enough that the devices can be used in this range. In fact, the performance of these inductors exceeds many of those available as discrete components in 0402 or similar packages that much of the industry uses [54]. A lot of these devices have more parasitics and lower self-resonance frequencies than the devices in this work [55]. In fact, some solutions for these applications are becoming completely integrated onto silicon and thus using inductors of much poorer quality. As will be shown in the next section, some silicon devices still have Q factors less than 15 [56]

3.5 Comparison with Previous Suspended Inductor Work

The release etch used in this work makes the release a lot easier than in many of the MEMS inductors that have been described in literature. Many of the other devices rely on using a multistage photoresist mold or else require special hinges and/or precise stress tuning in order to create released or vertical inductors [42][7]. What happens in the case of a photoresist mold is that a mask is used to impose a pattern in the resist, which is usually thick or a special resist like SU-8. Metal can then be plated in this pattern, using the resist like a mold. One thing that makes a sacrificial layer (as used in this work) easier is that in a manufacturing process, contamination concerns limit the equipment, temperatures, and processes that can be performed once photoresist is on the wafer. Another aspect is that with thick resist, line widths and spaces that can be used are limited. Typically the resolution will be on the order of the resist thickness [57]. This however, is a general problem in patterning very thick layers, which is a reason that only a 1μm dielectric was used in this work. Creation of vertical inductors relies on stress engineering of the materials and also produces devices that would be harder to encapsulate or package.

Much of the suspended inductor work that has been carried out to date has been on silicon substrates in hopes of CMOS integration. [51][55][56][58][6][59][60][61] This is because a suspended inductor has a good chance of being fabricated with a process that will be compatible with CMOS, i.e. low temperature and non-disruptive to existing features in the process. The work has taken on a variety of different approaches to date in order to achieve suspended inductors. The general trend in this research appears to be copper inductors on silicon substrates with an etch release or else a photoresist mold.

First, the suspended inductor research that is closest to the work in this thesis will be looked at in detail. The KAIST group in Korea [51][61] uses a two stage photoresist mold to create their suspended inductor, which then has a 50μm air gap between the coil and the underpass. This is fifty times larger than the gap used in this research. This will mean a coil to underpass capacitance that is 1/50 times that in this work. However, one must keep in mind that the other parasitics are determined by the substrate, metal, and geometry. Thick, 10μm, copper metallization is used for structural stability [51]. As well, 20μm diameter support posts are built to hold up the coil. [51] This group has also done work on encapsulation. Testing with a thick BCB dielectric degraded only slightly the performance of these inductors with a maximum degradation of approximately 5 in the Q factor.[61] Although the encapsulant that was recommended was PMDS due to the cost, transparency and low dielectric constant, results with this encapsulant were either not attempted or not reported [61]. Unfortunately, with the extremely small air gap in this thesis work, 1μm, adding a dielectric material back in between the coil and underpass would be expected to return the results to the pre-released state. This is because the inductors in this work start with a relatively low k material, approximately 3.9, in between the coil and underpass. In fact the encouraging results obtained with encapsulant in the KAIST work seems to indicate that the main difference in inductor performance is the reduction in substrate effects and parasitic capacitance (50μm low dielectric constant spacing added between the circuitry and the inductor coil) and not necessarily the released nature. (I.e. air is the best, but a low k material is the requirement) This is the same conclusion obtained in the work done in [41]. In fact, one could suggest

that building these inductors with a low k material like BCB may even produce better inductors as there would be no posts required so more parasitics could be eliminated, although some would be added as well by the dielectric material. In this research, there was not the opportunity to try such a thick dielectric layer.

The work in [59] is similar to this work as well. In this paper, a sacrificial polyimide layer is used to suspend 9μm thick copper coils 60μm above the substrate. Only inductances of over 10nH were reported, however [59]. Inductances this large are typically not useful for GHz range circuits. It was found in this work, common to most suspended inductors, that supports were needed.[59] In [62], a photoresist mold was used to suspend 5μm thick copper coils 60μm above a glass substrate. Posts were used to support the coils and various suspension heights were tried to determine the effect on peak Q factor [62]. As expected, the peak Q factor increased with increasing distance from the substrate relatively linearly.[62]

Finally, the best reported suspended inductors are part of the work in [63], published in 2003. In this work, an SU-8 photoresist mold was used to create inductors suspended 100μm above the substrate from 50μm plated copper [63]. The substrate used in this work was ceramic filled fiberglass with a low dielectric constant. [63] This approach eliminates almost all of the parasitics by using both a good substrate and good separation. The only disadvantages are that SU-8 can be hard to work with and the peak Q factor may potentially occur at a frequency that is too high for many applications (for example cell phone and Bluetooth applications considered in this work). This is a problem because it means that the Q factor may still be quite low and building up at these lower frequencies (1-5 GHz). As we will see by the results, and can be seen in many of the references, typically the Q factor rises up to a maximum and then starts to decline. This is because there are two competing effects, one is the fact that without any other considerations, Q would be proportional to $\omega_o L/Rs$ and so would rise with increasing frequency [27]. A maximum is reached, however, because there are parasitics involved and especially because of the skin effect, that was previously described.

In [56][58][6][64] various techniques are used to suspend an inductor in the middle of a silicon wafer. In one case an etch is used, [56], and in the other case [58][6] the insulating layer of an SOI type process is used to advantage as an etch stop to suspend the inductor. The work in [64] suspends the inductor by etching the silicon dioxide on the wafer using a variety of different hole patterns in the etch mask to create an air cavity. This does not seem like a simple process for a small performance gain. All of these methods of suspending the inductor only produce maximum Q factors of 15. [56][58][6][64] This is because these approaches still leave the inductor close to silicon and hence the main parasitic removed is the capacitance between the coil and the underpass. As will be discussed in the next section, the inductors in this thesis work achieve better than this even before release. In the case of the work in [56], posts are still required to support the coil making the inductors even less ideal. This is a reason that to create good quality inductors, silicon was not chosen for this work. Silicon is cheaper and may offer CMOS integration but alumina is a much better RF substrate. Silicon is a very poor insulator, with a resistance that needs to be taken into account, and is lossy at high frequencies adding many unwanted parasitics.

The work in [60] describes inductors that are suspended over a copper lined cavity. The inductor itself is made of polysilicon wrapped in approximately 1μm of copper [60]. In this case, care has to be taken when designing the depth of the cavity and the pattern in the copper that is created, since this copper acts like a ground shield and can carry eddy currents that will degrade performance [60]. Q factors in the range of 25-35 have been reported by this work, which is good, however this is not a cheap or easy way to fabricate inductors [60]. It is not cheap since this method does not allow inductors and active circuitry to occupy the same area so that inductors designed in this process use a lot of valuable real estate on a chip. Area on a CMOS wafer can be very costly. Also, wrapping the polysilicon in copper will not be an easy process and will not easily allow for thick metal to reduce the skin effect.

Suspended inductors have also been created by using flip chip assembly. [65][66] The work in [65] uses 6μm of plated gold on Titanium and Nickel. In [65] bump posts or

supports are required for the coil and Q values of up to 30 are claimed. The work in [66] uses a special tethering process in the flip chip transfer of the inductor. In this work Q factors are not reported, however the suspension height above the new substrate is reported to be 60μm in this case [66]. This approach is very different to the work done in this thesis and has the disadvantage that dimensions are limited by the size and pitch requirements of the flip chip process.

The present thesis work has benefited from the above research on suspended inductors. However, since the goal of this work is not CMOS integration, as described we have developed a unique and simple process. The process used in this work would not be of benefit to a CMOS process as the air gap used is too small to be effective on a silicon substrate as well some of the metal depositions may require too much thermal budget. The goal of this work however, was to create good quality inductors and transformers for applications in the 1-5GHz range such as Bluetooth, cellular phones, and WLAN as part of an RF passive specialized substrate. The idea being to work towards something like a two chip solution for these applications: silicon baseband/processing chip + RF passives chip. The process used in this work is manufacturable with the exception of packaging, at least at the present time. This process does not easily lend itself to encapsulation, however it is definitely not impossible. In fact the devices measured and described in this work were created on Gennum Corporation's manufacturing line with standard or very close to standard processes that are available.

The different processes just described that have created suspended inductors [51][55][56][58][6][59][60][67][63][61], all have varying success in creating high Q inductors and a variety of targets. Many designers of inductors on silicon substrates would seem to believe that Q factors greater than 10 are great, however many RF designers and some groups doing suspended inductor work find this level of Q factor unacceptable. In reality, one can not design a good passive component filter from elements with such low Q factor since there would be too much insertion loss. To see how the results of this present thesis research compare to the results of the other suspended inductor work, see Table 3.5 given below.

References to work	Inductance Range (nH)	Peak Q Factor Reported	Suspending Method	Substrate	Remarks
Thesis Work	1-30	50-70	Etch	Alumina	1μm gap
[51]	1-10	70	Double exposed PR mold	Silicon	50μm gap
[56]	n/a (~20)	<10	Etch	Silicon	Suspended in middle
[58][6]	n/a (~7)	<15	Etch	SOI	Above insulating layer
[59]	10-40	50-60	Etch	Glass	Sac. Layer
[60]	1-10	25-35	Etch	Silicon	Suspended over Cu lined trench
[63]	0.3-3	80- >100	PR mold	Ceramic filled fiberglass	resonant frequencies >50GHz
[61]	2-10	30	Double exposed PR mold	Silicon	Encapsulated with BCB
[64]	n/a (23)	<10	Etch	Silicon	
[65]	n/a (1.8)	30	Flip chip	Silicon	
[66]	18	Est. of 40	Flip chip	Silicon	For bias T
[62]	n/a (4)	35-40	PR mold	Glass	

Table 3.5: Comparison of suspended inductor results from various research

Comparing the results of the work in this thesis to the other suspended inductors, the present work rates within the top two or three as far as Q factor obtained. It is also the most comprehensive, whereas much of the material published for the other suspended inductors only show a single inductance value, many of which fall into the RF choke range at the frequencies of interest in this work. We can also see that this is the only work on alumina, and was able to achieve the very competitive Q factors with only a 1 μm air gap under the coil.

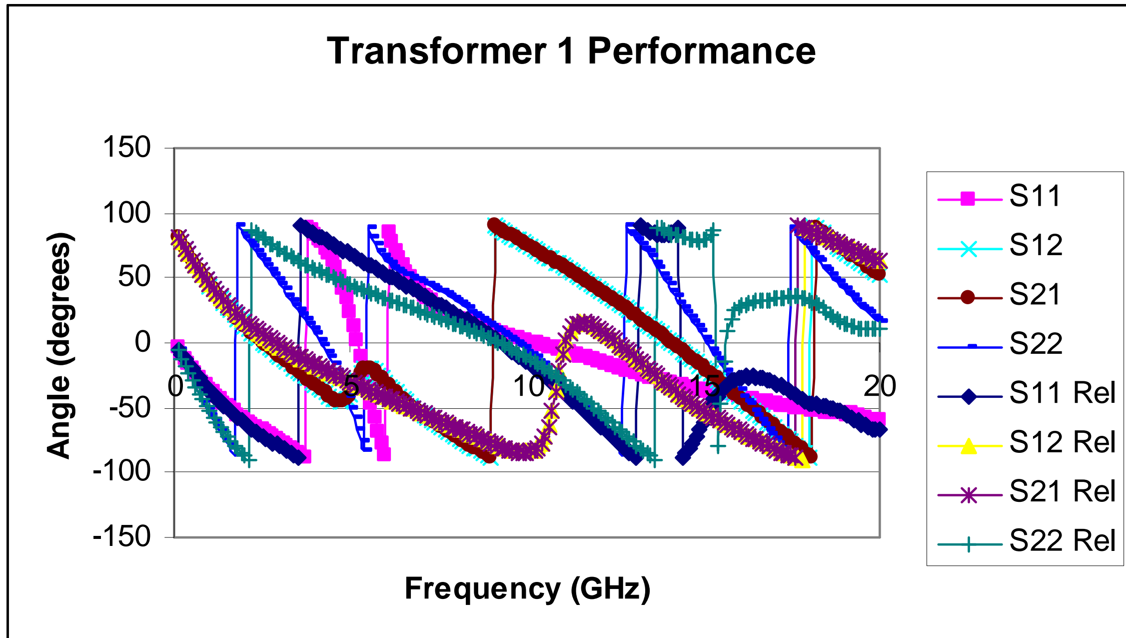
3.6 Transformers

In the following discussion, the results from some of the transformers will be analyzed. These, as previously described, were created with a double released stack of metal. These were the first attempt at any type of transformer in our technology at Gennum Corporation so there were no specific design targets. The target of the transformer work was to simply determine the type and quality of transformer that could be made with this process as a demonstration. Therefore, the transformers were built from the inductors whose results were just shown with no specific frequency or ratio as preference, although 180° and 0° transformers were built.

It was felt worth attempting transformers since various types of transformers can be made from inductors and it was possible in the process used in this work. This is because the magnetic field can be transferred from one inductor to another without any electrical contact making desired transformer properties possible such as voltage isolation, an impedance transition, a power level change, a balun etc. In fact, many transformers are created by two wound inductors in proximity to each other and such is the symbol for a transformer. Transformers can be used in many RF circuits, including those of interest for this work in the 1-5GHz range, as well for matching, or to create a balun. A balun is a component that takes an input RF signal and then divides the signal across two outputs with either a 180°, 90°, or 0° phase difference between the two outputs and half the power at each output. Obviously since one signal is being split into two, the power level will be

half at two of the ports. Since one can make either 180° or 0° transformers, one can see why these would lend themselves to this application.

The figures below show the performance of the 6 transformers before and after release.



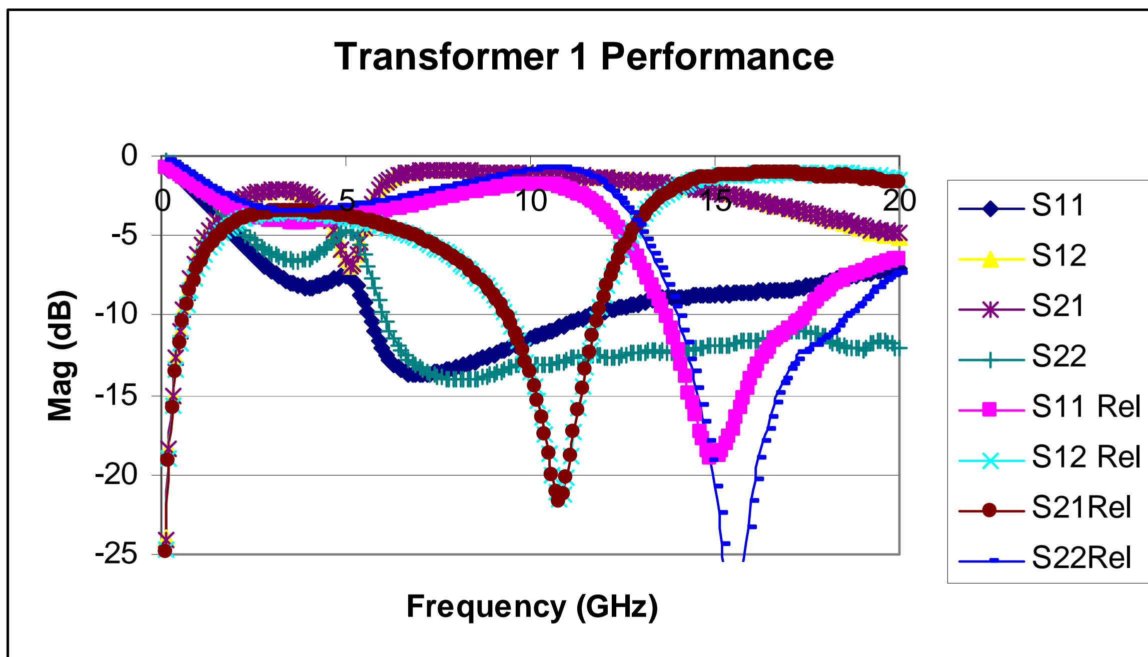
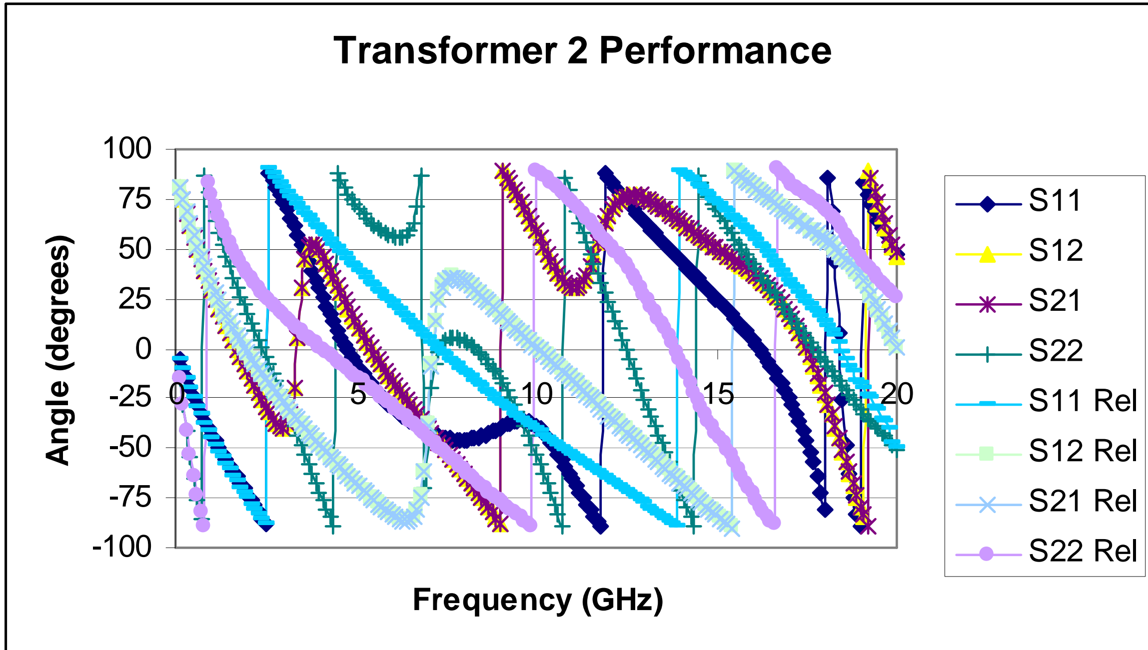


Figure 3.4: Transformer 1 Data



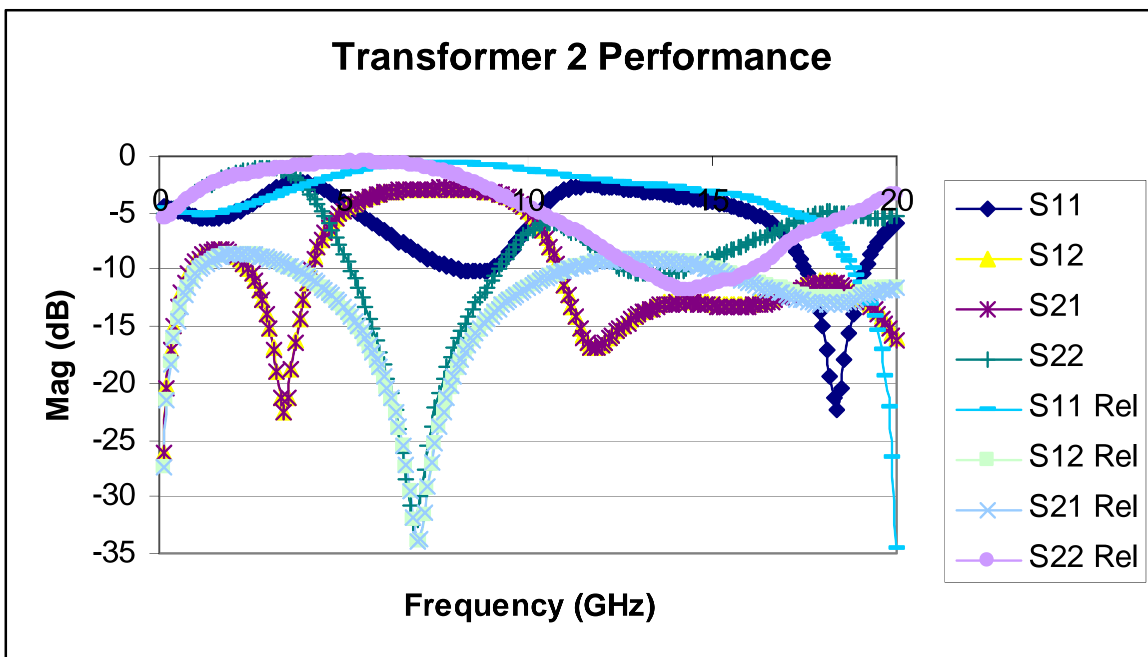
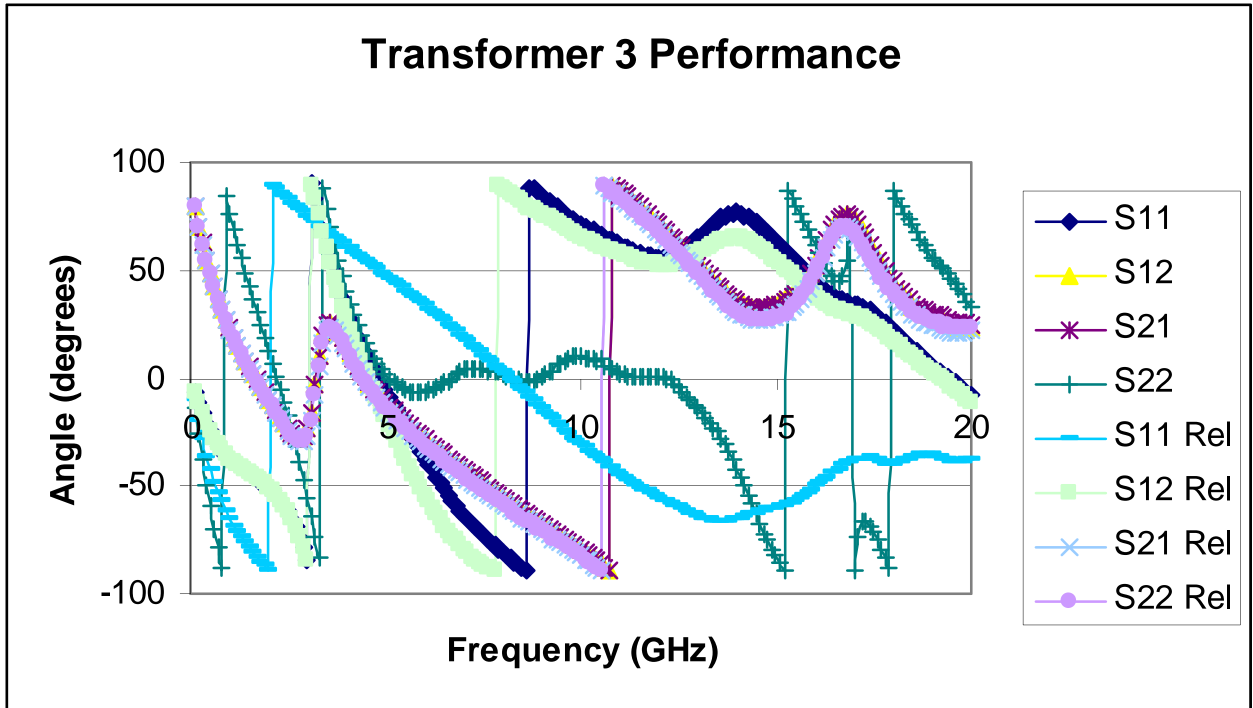


Figure 3.5:Transformer 2 Data



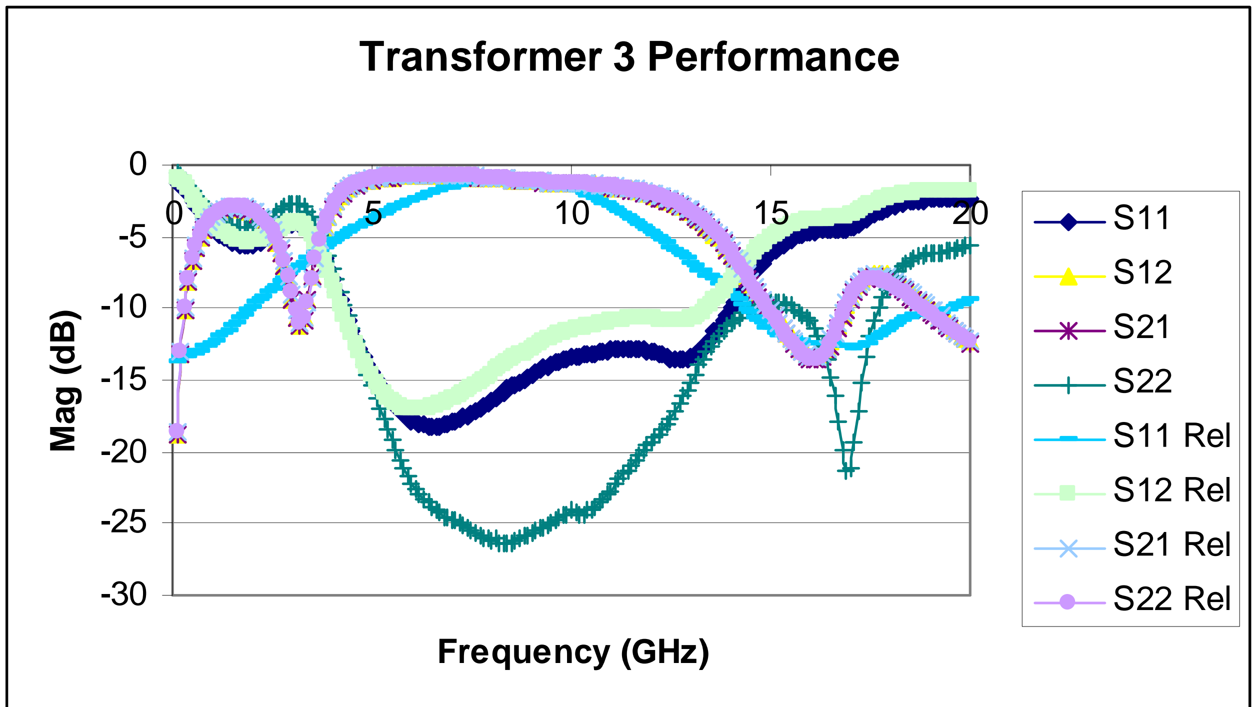
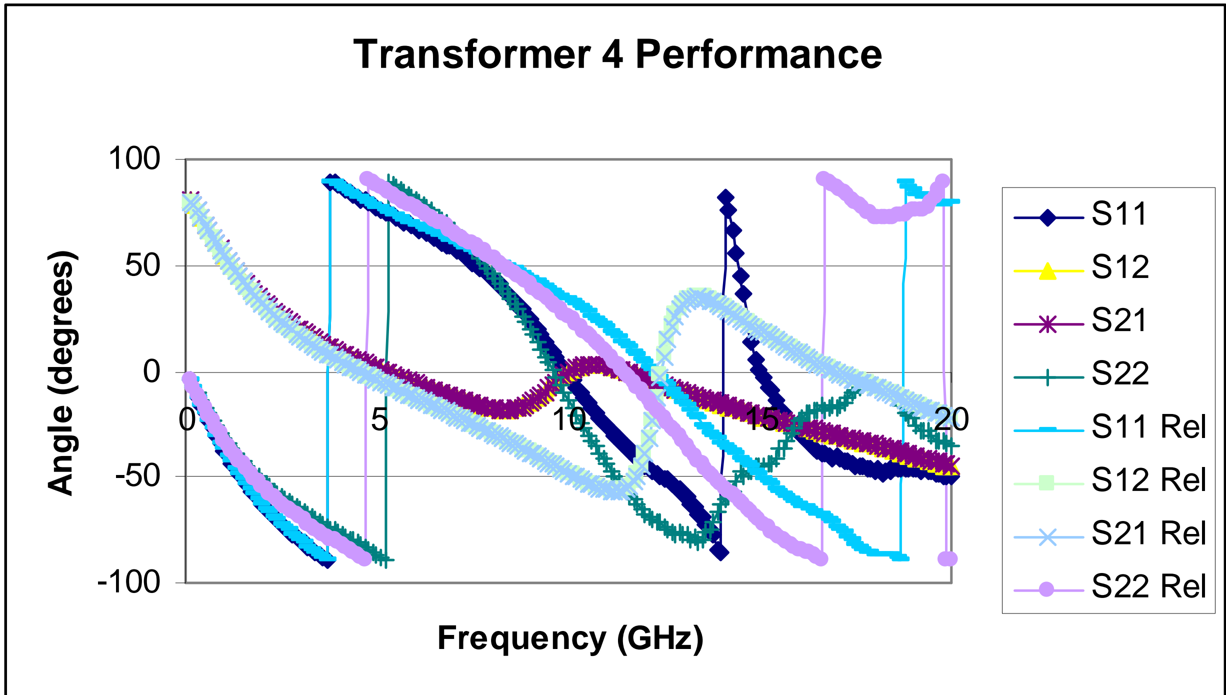


Figure 3.6: Transformer 3 Data



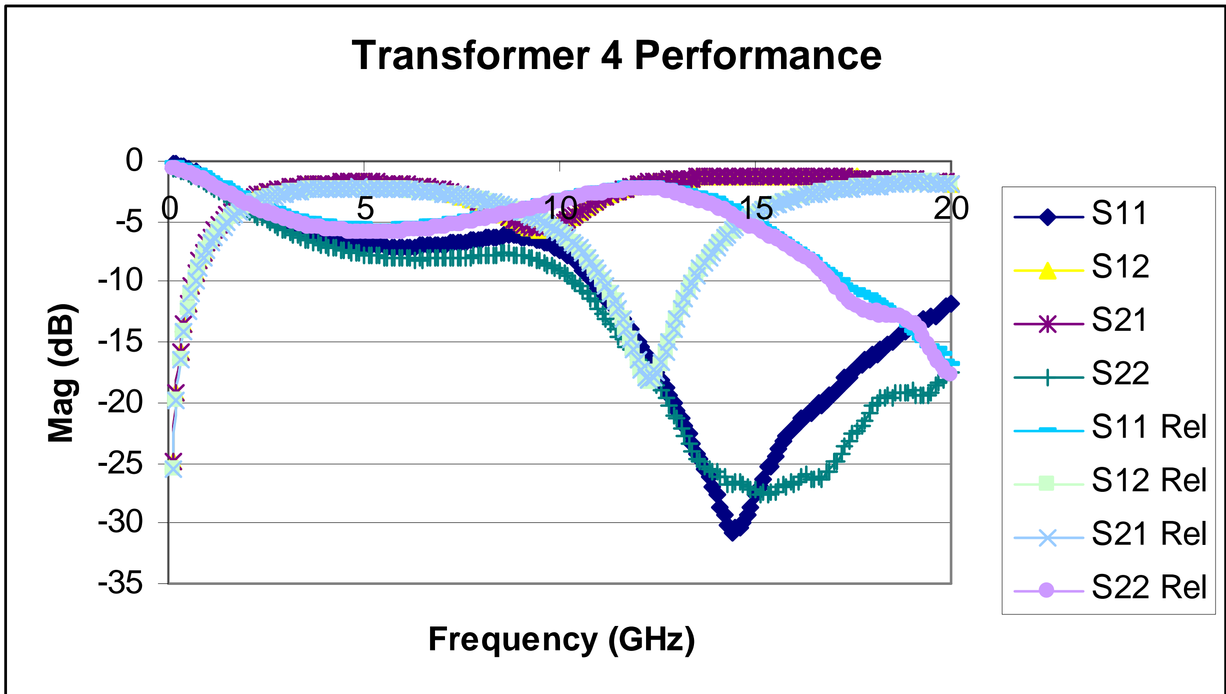
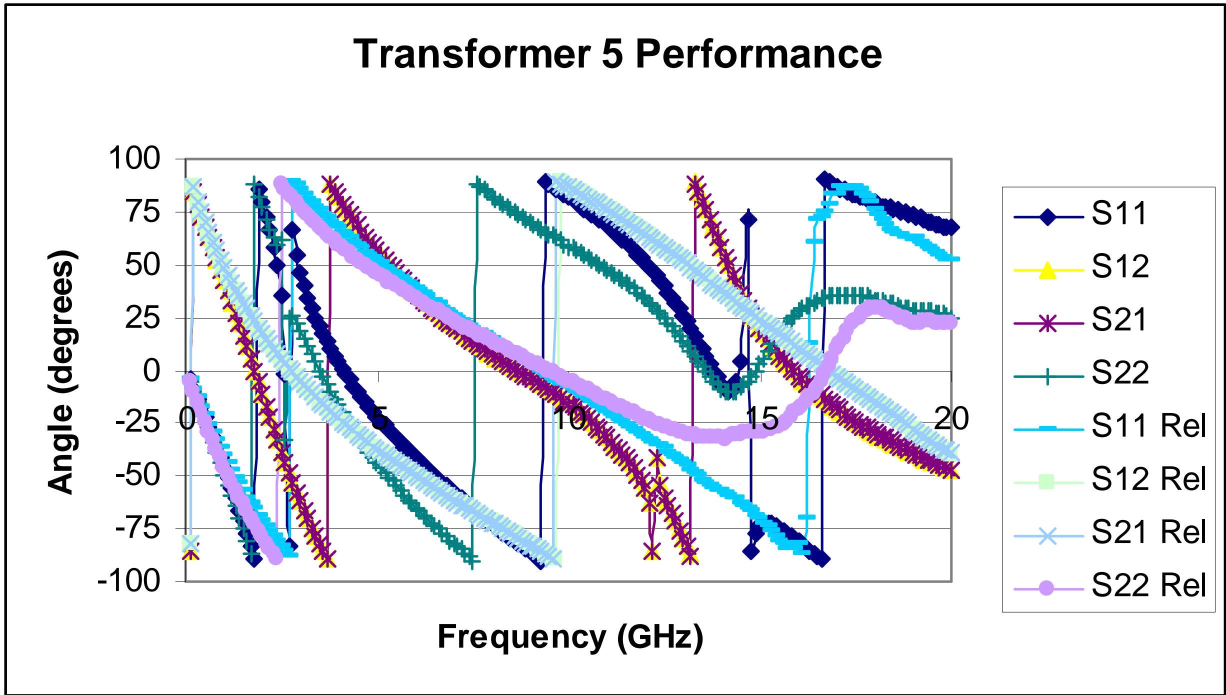


Figure 3.7: Transformer 4 Performance



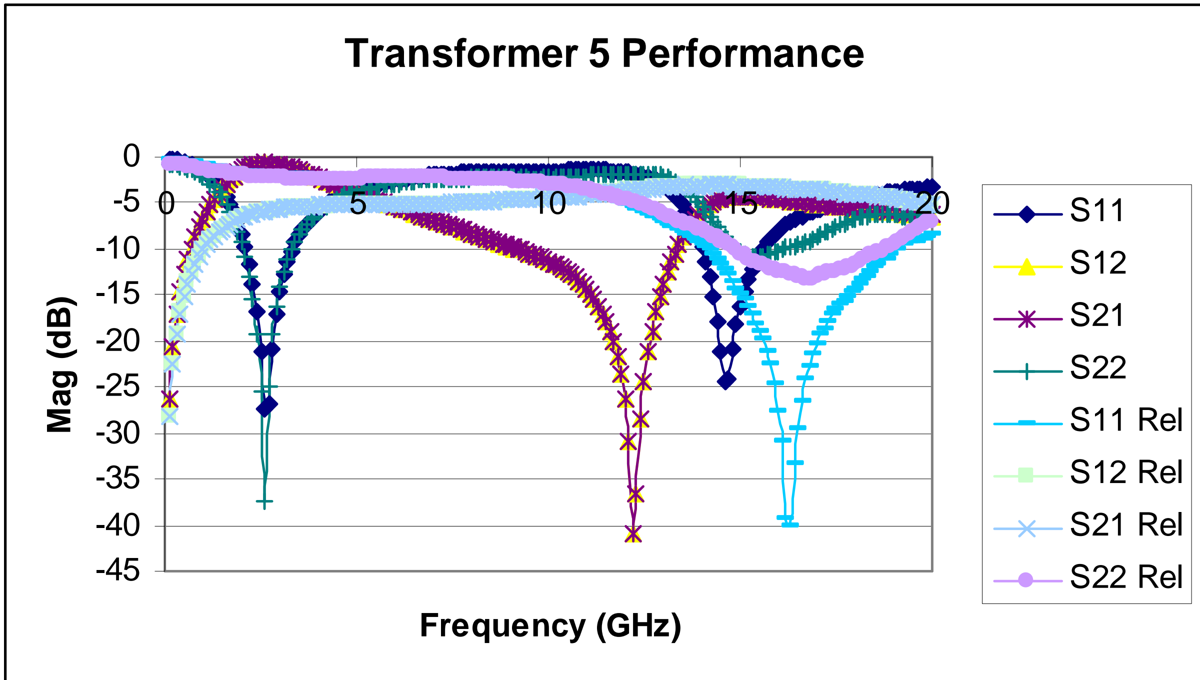
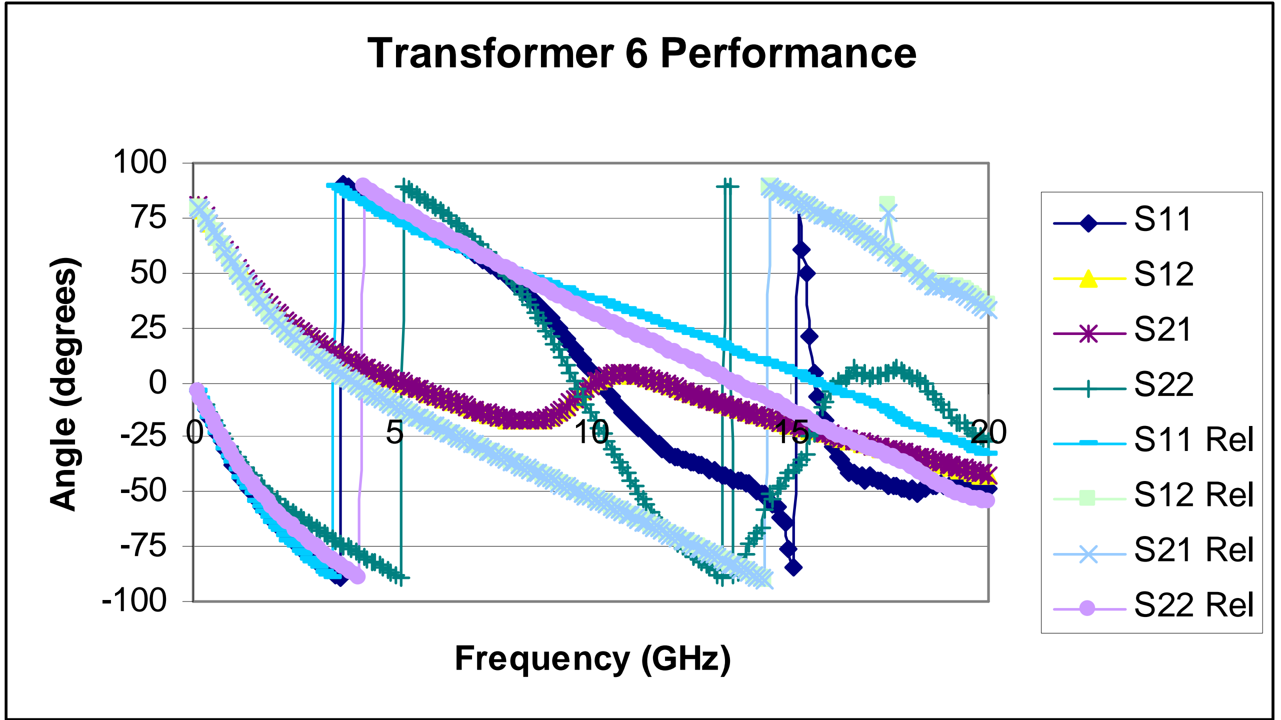


Figure 3.8: Transformer 5 Performance



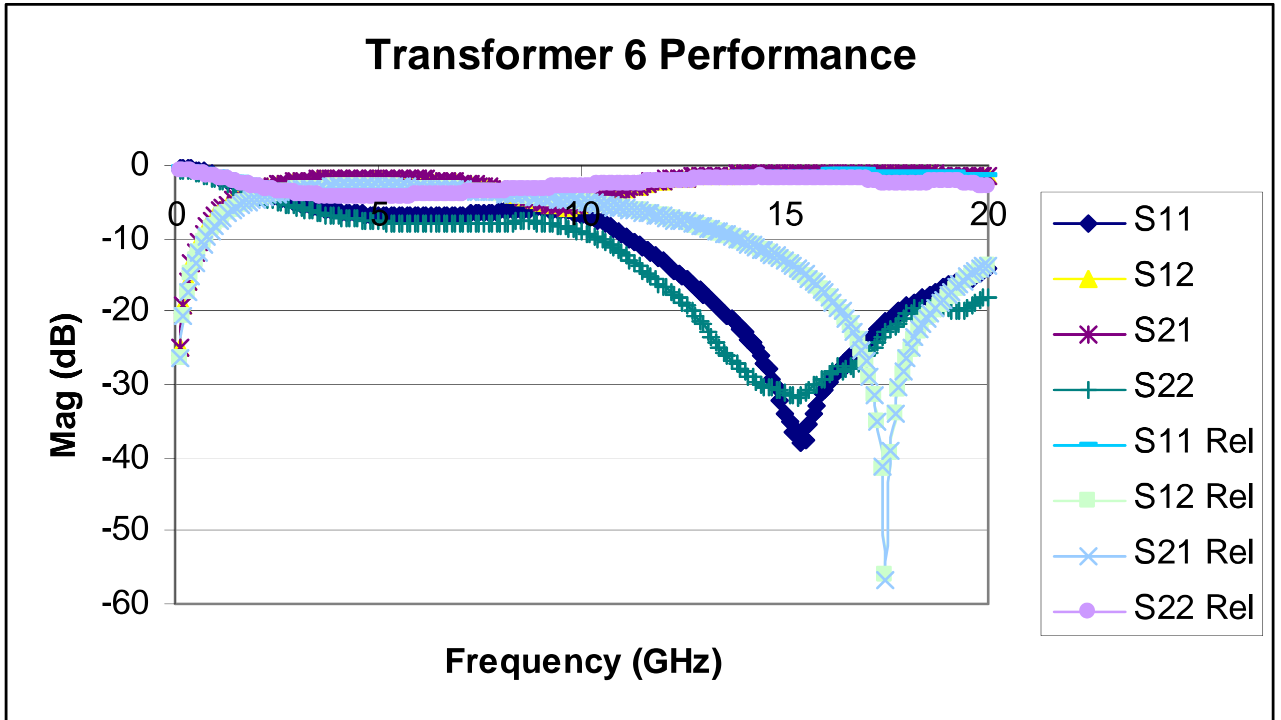


Figure 3.9: Transformer 6 Performance

As we can see from the transformer results, most transformers have quite a strong frequency dependence. All the measurements were done with two signal ports, one on each of the two inductors comprising the transformer, with the other points being connected to a common ground. There was no de-embedding performed on the transformer measurements. The results are encouraging since all of the transformers have a frequency range in which there is little insertion loss in transferring the signal from one coil to the other and a reflected signal as small as 10dB, except for transformer 3 after release. In fact, one of the most important transformer properties is the minimum insertion loss. Transformer 3 seems to behave quite poorly upon release in the measured frequency range. The other transformers performed well at varying frequencies between 5 and 16GHz. The performance can be further optimized by future work, however.

The reason for the good transfer of signal between the two inductor coils is believed to be the small gap, approximately 2μm, between the two coils. This means that the coil in which there will be an induced signal will feel the influence of almost the same strength magnetic field as that generated by the inductor with the initiating signal. Naturally, in order to encourage efficient transfer of the magnetic field from one inductor to the other, the inductor centers were lined up, where the magnetic field lines are strongest. Perhaps one optimization to try is to find a way to eliminate the intrusive metal connections between the two coils. Luckily, the released structures were not shorted. This was a potential problem if the stress in the metal layers was such that their deflection caused them to touch, given the 1μm gap between metal layers. The only problem was with transformer 2. This transformer did not produce good results since on two sites there was very little transmission at all across the two coils (looked like an open) and the other three sites were inconsistent. The other transformers gave repeatable results across the wafer.

In the previous section the design and simulation of these devices was discussed. The logical course now is to see how the predictions from the EM simulation tools match the results from the measurements that have just been shown. This is very important to know because to be able to predict the performance of such a device before fabrication

can make these structures quicker and cheaper to manufacture. It may help avoid one or two design iterations. Inductance excluded, many of the parameters of interest, in particular the Q factor, are non-trivial to calculate without software support. This is one of the other major benefits of good design tools. Given a tool that can estimate the Q factor to a reasonable accuracy, allows one to quickly get an idea of the optimal inductor for the frequency and size requirements.

3.7 Comparison of the Measured Results with the Simulation Results

Table 3.6 below shows a summary of simulation results from Ansoft HFSS vs. measured results for the released inductors.

Inductor	L(1GHz) HFSS	L(1GHz) Meas.	Q Trad. (2.5GHz) HFSS	Q Trad. (2.5GHz) Meas.	FSR HFSS	FSR Measured
10nH 4post	9.788	9.237724	32	18.16623333	8.25	10.46
10nH 2post	9.7	9.179118	26	24.96294667	7.5	15.04
4nH 4post	4.192	3.80941	36	31.57522333	9.75	13.14
4nH 2post	4.07	3.782126	25	33.65244667	11.5	14.1
3nH 4post	3.14	2.923024	32	32.01252333	16	17.86
3nH 2post	2.78	2.913366	22	33.25657	12	18.06
4nH_rnd	4.118	3.846804	39	35.40569667	19.25	17.46667
1nH_rnd	1.648	1.306148	37	32.48084333	>20	>20
1.5nH 4post	2.173	1.649954	32	22.71558667	16	>20
1.5nH 2post	2.14	1.653466	33	23.18177	16	>20
27nH 4post	22.798	28.58006	Q passed through 0	1.588554733	4.25	5.4
27nH 2post	28.52	28.02558	Q passed through 0	2.58233	4	5.86

Table 3.6: Summary of Measured vs. Simulated Results

As can be seen from table 3.6, the simulation results are not as accurate as one might hope, but they gave a reasonable idea of how the inductors would perform upon being released. Learning the various approaches for good simulations and measurements is always ongoing. The discrepancy between simulation and measurement can be attributed to a variety of sources. One source of discrepancy is that the released structures have a curvature to them that is not captured in these simulations, the materials

parameters were only known to a certain accuracy to enter into the simulations, and of course there is always error involved in measurements as well. Despite this, these are reasonable simulation results which are close to the measured results and show all the same trends. A graph of the S parameters of an inductor and a transformer simulation is shown below.

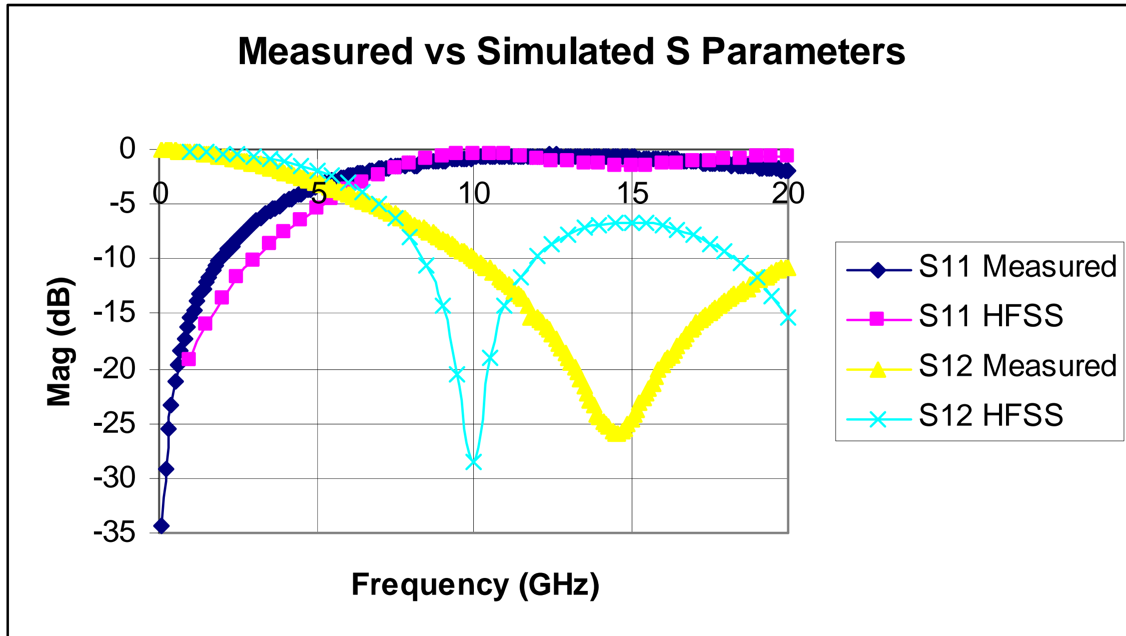


Figure 3.10: S parameters, measured and simulated, for a 3nH-2post inductor

Looking at the S parameters we can see that the main discrepancy is in the transmission parameter, S_{12}, rather then the reflection parameter S_{11}. It is this discrepancy that causes the self-resonance frequency to be off and hence the Q factor as well. The self-resonance frequency can also be determined by the minimum in S_{12} or S_{21}. This might suggest that going to 1 port measurements, where the inductor is measured across its two ports with one grounded, might aid by both reducing measurement and simulation parasitics. This result also suggests that perhaps the discrepancy between measured and simulated data is partially due to the de-embedding.

Figure 3.11 below shows the simulated (HFSS) vs. measured results for a sample transformer, in this case transformer 4.

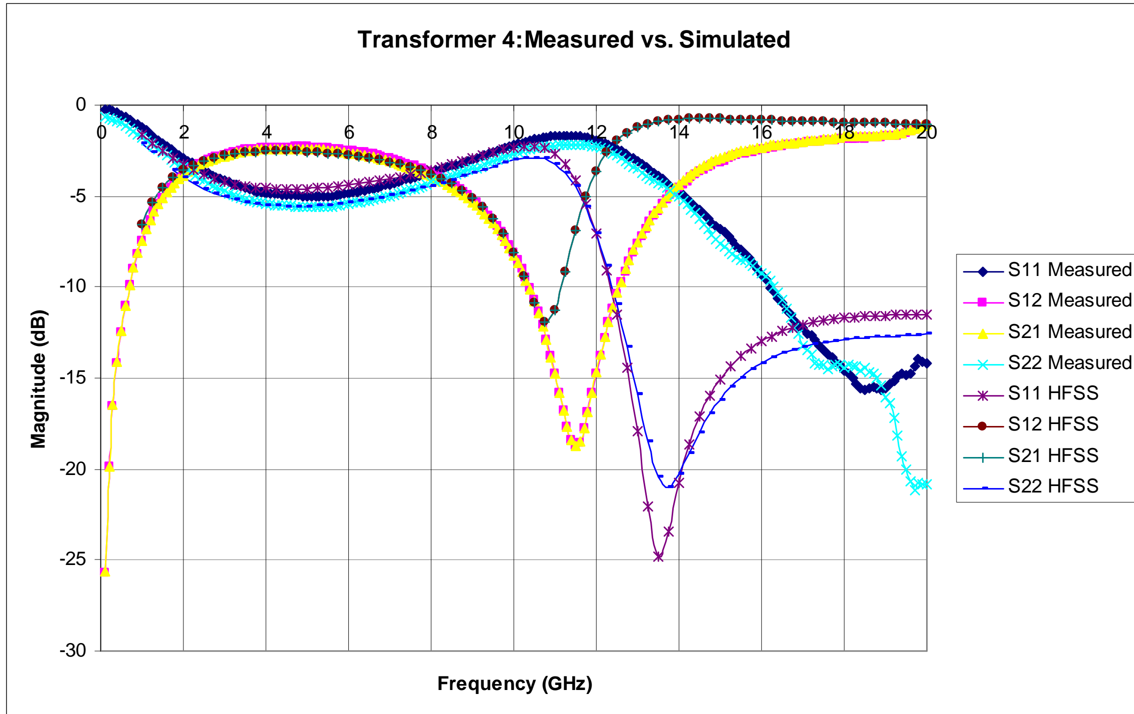


Figure 3.11: Measured vs. Simulated results for Transformer 4

We can see from figure 3.11 above that the simulated and measured results follow each other well until 11GHz. After 11GHz the simulated results seem to predict the rise in S_{12}/S_{21} and the roll off of S_{11}/S_{22} earlier in frequency. One possible reason for this is that the HFSS mesh may have required further refinement. The above simulation took over forty-eight hours, however, so this refinement was never attempted. Another potential source of error is that HFSS does not take into account the stress and bending of the released metal. Perhaps the boost in frequency seen in the measurement partially comes from the metal layers bending in a stress reducing manner. In any case, there is definitely work to be done on the HFSS model of the transformers.

In the next chapter, as EM simulation cannot always be used to design inductors, equivalent circuit modeling will be discussed. Equivalent circuits can also be used to design and model inductors in a less accurate but faster manner.

4.0 Modeling

Modeling is an important tool to have when designing inductors, or any circuit component. It can help to predict inductances and performance of various designs without going through with the expensive process of creating the inductors in a lab. As a result, a huge amount of time and effort has been spent in developing and improving modeling techniques. Although everyone has generally settled on a single equivalent circuit, many closed form equations have been proposed to describe inductors. As well, numerous tools have been developed to help in the modeling of an inductor.

In general the software tools used to model inductors start right at the basics and will solve Maxwell's equations by one method or another over the geometry and material parameters that are input. Fully 3D EM solvers like Ansoft HFSS, used in this work, or CST Microwave Studio tend to use some type of finite element technique combined with boundary conditions to solve Maxwell's equations. These programs solve for the 3D fields and therefore automatically take the skin effect into account and can give an accurate idea of inductor performance over frequency. 2.5D or 'quasi-3D' solvers like Agilent ADS, Ansoft Designer, etc. typically use a method of moments technique. Because of this, metal is usually considered to have no thickness and dielectric layers are assumed to be infinite in extent. This makes these tools a little less accurate on the Q factor and frequency performance.

While these tools are useful for confirming designs, building empirical models, and looking at a wide frequency range, their downside comes in that using them is quite time consuming. From experience, a typical inductor structure can take upwards of a half hour to simulate and a few minutes to set up as well. This is because a planar inductor typically has features on the order of micrometers in widths and thicknesses, so to obtain accuracy these features need to be resolved by the proper mesh. This creates a large mesh and a large problem for the program to solve. The accuracy of these tools also depends on the type of port and boundary conditions used. For example, if one is forced to do one's simulation in a grounded metal box, as some simulators force, it is important

to ensure enough space that this simulation environment does not interfere with the results. ASITIC falls into this second category. The inductance and capacitance matrix are calculated for the structures and then using Maxwell's equations along with Green's functions the problem is solved. ASITIC has a couple of advantages in that one can very quickly obtain a low frequency inductance value and one can export the inductor into a CAD format. To do an EM solve, however, ASITIC suffers the same time consumption as the other tools, but more so, as it only solves one frequency point at a time. This can take up to 20 minutes. In the present work EM tools were used in an attempt to try to predict the released behavior of the devices as they were novel.

In order to have a good model to both aid in design as well as to aid in extracting information from measurements and/or simulations it is important to have a good physically based equivalent circuit model. This can lead to good insight as to what parasitics are important for the inductor being designed or measured. It can also provide a good model that can then be entered into a circuit simulator for a fast approximation of the behavior over frequency. Since S parameters do not give the inductance or Q factor directly, it also gives a target circuit for extraction from these parameters. For inductors, the most commonly reported equivalent circuit is some version of a pi model [9][8][32][51][7][52][14][68].

4.1 The pi Model

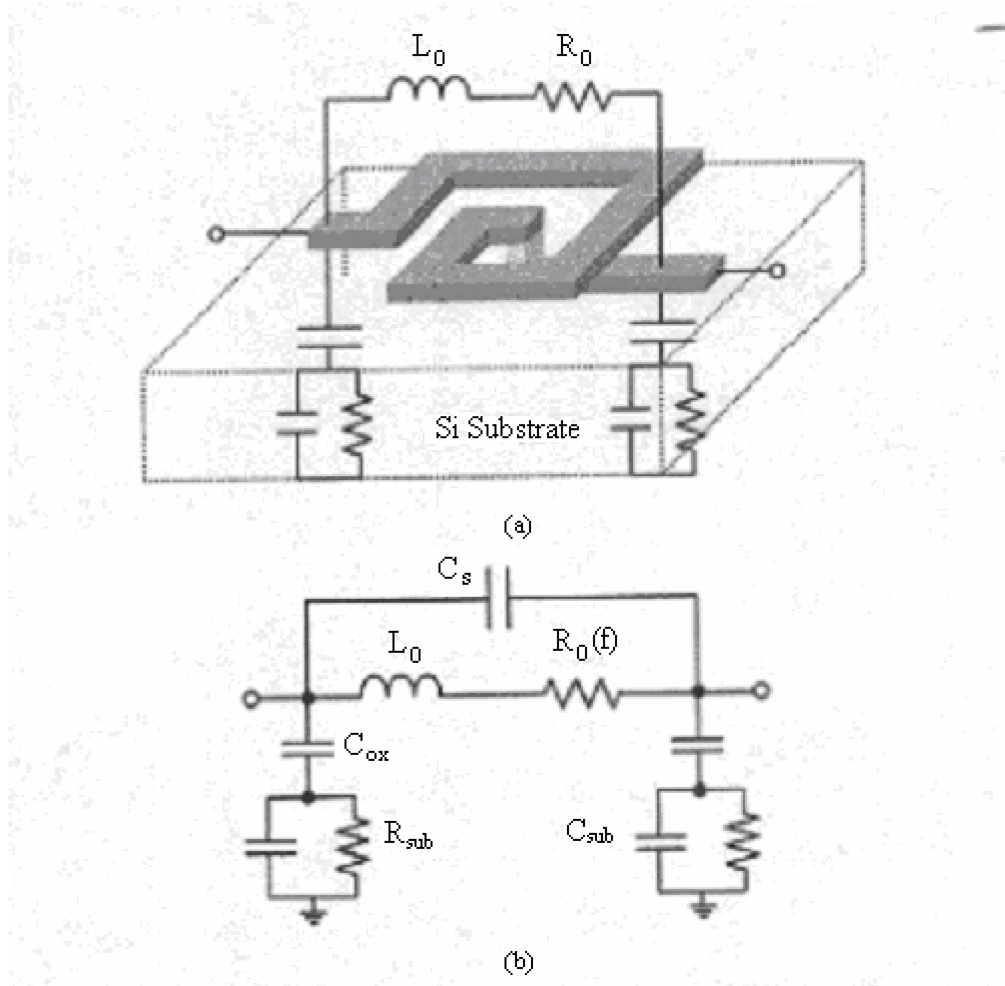


Figure 4.1: Lumped element equivalent circuit on Silicon from [69]

Figure 4.1 shows the most commonly used circuit on silicon. Here L_o represents the inductance of the coil. C_s represents the inductance between the underpass and overpass. As well, although not generally significant, it can include the capacitance between the windings. In order to take this properly into account, however, a multiple pi model should be used to distribute these capacitances. R_o represents the resistance of the coil. C_{ox} represents a parasitic capacitance down to the substrate. R_{sub} and C_{sub} are specifically added for a silicon substrate to represent the resistivity and capacitance of the substrate. For the present work, these can be excluded from the model used. The main drawback to using a model like this is that the resistance is not static across frequency.

The model as shown would require calculation at each frequency point and is also only good to the self-resonance frequency.

Both of these problems with the model have been investigated. A method that has been used to extend the model past self-resonance is to use a multiple pi model. In [69] a double pi model is used and claimed to be good past self-resonance. They also made an attempt to include the frequency dependence of the resistance by using ladder networks [69]. The purpose of the investigation in [70] was exactly this as well. The point was to come up with a broad band, frequency independent model based on ideal components. In [70] a two pi model was decided on due to limited scalability of a single pi model. The frequency dependencies were removed by the approach of using transformer loops to model the loss in the inductor [70]. This also eliminates the need for the parallel capacitor in the model [70]. A routine was programmed that took measured S parameter data and fit it to the model extracting values based on a least squares fit [70]. Similarly, the work in [71] discusses the pi model and then, starting with each major source of loss in the inductor, proposes a five element network model that is independent of frequency. The reason to have a model that is good past self-resonance is that in certain applications, such as mixers, the behavior beyond self-resonance is required to be a known [18]. Another method of extending the pi model is to either make it higher order or else to create a variation of it. Fig. 4.2 shows a model for beyond self-resonance

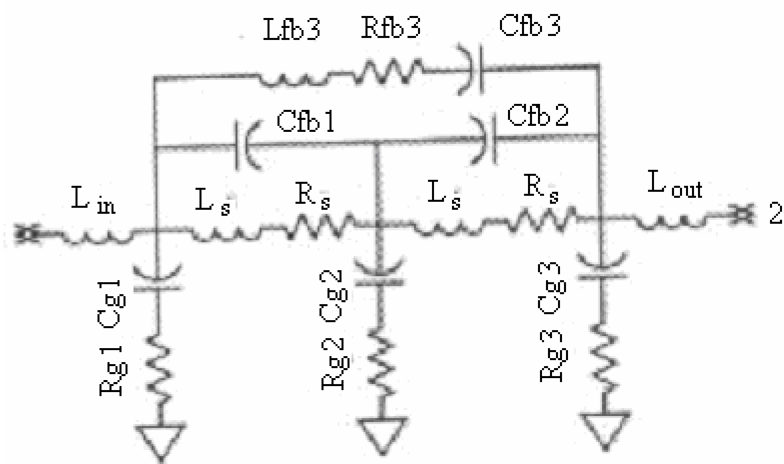


Figure 4.2: A model for beyond self-resonance. [18]

The work in [69] also gives a model that extends beyond self-resonance in great detail. For the work done in this thesis, it was felt that while it is important to know how to extend the model, these extensions were not critical to the modeling or utility of these particular devices.

4.2 Model Parameters-Greenhouse Method

Now having reviewed the type of model that can be easily applied to an inductor, it is important to see the methods used for fitting values to these models. We have already seen two methods in fact, and that is the extraction from S parameters that come from measurement or simulation. There has also been a lot of effort put into finding closed form expressions and analytical methods of finding the inductance.

The first really important work done modeling planar inductors, in the sense of inductance calculation, was that undertaken in the mid 1970s by Greenhouse and Grover [72]. [72] by Greenhouse, written in 1974, introduced a new and simple way to get the low frequency, DC, inductance of a planar coil. Basically he introduced a way to find the self and mutual inductance of the pieces of the coil, using the geometric parameters of the coil, and then showed how they were properly summed [72]. One assumption made in this work is that the metal has a permeability of 1 [72].

The work in [32], published in 2000, is also useful in going through this approach. The first step is to calculate the self inductance of each segment. This is given by the following formula [72]:

$$L = 2d\left[\ln\left(\frac{2d}{GMD}\right) - 1.25 + \frac{AMD}{d} + \frac{\mu T}{4}\right]$$

Equation 4.1

In this equation, L is the self inductance in nH, and w, d, and t are the width, length, and thickness respectively of the segment (given in cm). [32] This equation has a frequency fitting factor T which can be used to take the skin effect into account as well as the permeability, μ [72]. AMD is the arithmetic mean distance and for a straight line segment AMD = l/3 [72]. Substituting AMD = 1/3, the following approximation for GMD (geometric mean distance) = .2232 (w + t) given by Greenhouse for rectangular spirals, T = 1, and μ = 1 (to ignore the skin effect and permeability) will lead to a simpler form of the equation, also reported elsewhere [32][72].

$$L = 2d\left[\ln\left(\frac{2d}{(w+t)}\right) + 0.5 + \frac{(w+t)}{3d}\right]$$

Equation 4.2

The mutual inductance between two segments is given by M = 2Ql where d and w are again the length and width and Q is calculated as follows [32][72]:

$$Q = \ln\left[\frac{d}{GMD} + \sqrt{1+\left(\frac{d}{GMD}\right)^2}\right] - \sqrt{1+\left(\frac{d}{GMD}\right)^2} + \frac{GMD}{d}$$

Equation 4.3

$$GMD = geometric\ mean\ distance = \ln(p) - \frac{w^2}{12p^2} + \frac{w^4}{60p^4} + \frac{w^6}{168p^6} \ldots$$

Equation 4.4

Here p is the pitch between the two wires, again with everything entered in cm. There is only mutual inductance between segments that are parallel; hence the pitch can be defined as the center line to center line distance between the two segments [32]. Mutual inductance is added for segments with the current in the same direction and subtracted if the current is in the opposite direction [32]. A spiral shown below in Fig. 4.3, which Greenhouse uses as an example, will also be done here to show how to combine self and mutual inductances [72].

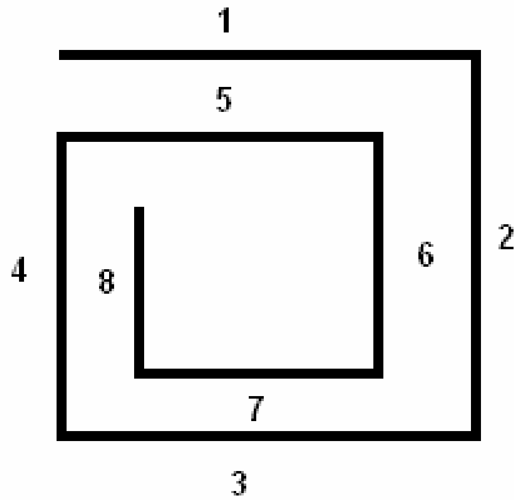


Figure 4.3: Example coil as given in Greenhouse [72]

In this example, the inductance would be given as follows [72]

$$L = L_1 + L_2 + L_3 + L_4 + L_5 + L_6 + L_7 + L_8 + 2(M_{1,5} + M_{2,6} + M_{3,7} + M_{4,8}) - 2(M_{1,7} + M_{1,3} + M_{5,7} + M_{5,3} + M_{2,8} + M_{2,4} + M_{6,8} + M_{6,4})$$

Equation 4.5

In [72] Greenhouse describes how to do the mutual inductance calculation for the case of two different length segments. Since this is the case for all spiral inductors we will go through this here.

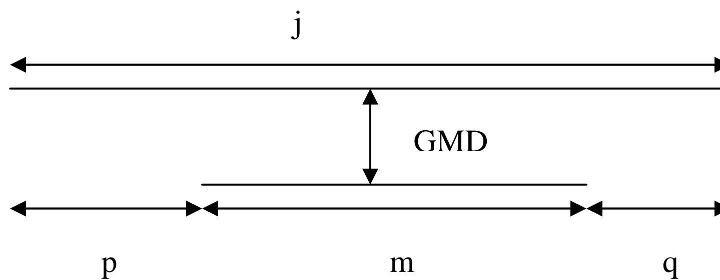


Figure 4.4: two lines of different length

In this case the mutual inductance can be found as follows [72].

$$2 M_{j,m} = M_{m+p} + M_{m+q} - (M_p + M_q)$$

Equation 4.6

Here, $M_{m+p} = 2\,(m+p)Q_{m+p}$ and can be calculated by the formulas given above [72]. We can calculate a couple of special cases, when p=q and when p=0: [72]

$$M_{j,m} = M_{m+p} - M_p \quad \text{(for p=q)}$$

Equation 4.7

$$2M_{j,m} = M_j + M_m - M_q \quad \text{(for p=0)}$$

Equation 4.8

In [73] a variation on this Greenhouse method is used with average lengths rather than a full calculation for every segment. In [72], the self and mutual inductance formulae are given as well as a final inductance estimate.

4.3 Closed Form Expressions

There have been many closed form equations developed for inductance as well, some empirical and some more theoretical. One caution with closed form expressions is that they can be dependent on the process or shape of the inductor coil, and do not tend to be as accurate as EM or more in-depth calculation methods. As will be discussed later in this section, two of these equations were found useful for the present work and were programmed into an inductance calculator created by the author of this thesis, as part of the investigation into modeling.

One expression for square spirals comes from [72] and is given below.

$$L(\mu H) = 0.467S^2\left[\log\left(\frac{2S^2}{(t+w)}\right) - \log(2.414S)\right] + .02032Sn^2\left[.914 + \frac{.2235(t+w)}{S}\right]$$

Equation 4.9

Dimensions are given in inches, w is the conductor width, t is the conductor thickness, and S is the maximum side length [72]. Another popular equation that has been used is Bryan's equation which is:

$$L = 0.0241an^{5/3}\log\left(\frac{8a}{c}\right)$$

Equation 4.10

Here dimensions are given in cm, where n is the number of turns, a is the (outside + inside diameter)/4, and c is (outside – inside diameter)/2 [59]. The inductance will then be given in µH. An empirical derivation based on Bryan's formula is formulated in [74]. This is intended to improve the accuracy, however uses a variety of fitting parameters which are expected to be determined by simulation or measurement. The modified version becomes:

$$L = a(s,t,H)N^{r(s,t,H)}\ln\left[b(s,t,H)\frac{(D+d)}{(D-d)}\right]\ln\left[c(s,t,H)\frac{(D+d)}{(D-d)}\right]$$

Equation 4.11

where D and d are the outer and inner diameters respectively, N is the number of turns, and a, r, and b are fitting parameters dependent on the inductor geometry. Coil spacing is given by s, metal thickness by t and substrate thickness by H. Typically a =0.0061µH/cm, b = 4 and r = 5/3 [74].

In [14] another semi-empirical formula is given for inductance, shown below:

$$L = 1.5\mu_o N^2 D\exp\left[\frac{-3.7(N-1)(W+S)}{D}\right]\left(\frac{D}{W}\right)^{0.1}$$

Equation 4.12

In this equation D is the inductor diameter, N is the number of turns, S is the coil to coil spacing, W is the coil width, and μ_o is the permeability of free space.

In the work from [75], the inductor is modeled by an inductance in series with a resistor. These elements are then placed in parallel with a capacitor. To calculate values for this model they propose:

$$R_{dc} = \frac{\rho \pi N \left(r_i + r_e \right)}{hw}$$

Equation 4.13

$$R_{ac} = R_{dc} \left(1 + \frac{\left(w + h \right) \sqrt{\frac{f \pi \mu_o \mu_r}{2\rho}}}{4} \right)$$

Equation 4.14

$$L = \frac{(14E-7) N^2 \left(r_i + r_e \right)^2}{2.14 r_e - r_i}$$

Equation 4.15

In these equations w is the coil width, N is the number of turns, h is the coil thickness, r_i is the internal radius, r_e is the external radius, ρ is the resistivity of the metal, and f is the frequency. They chose to calculate L from a version of Wheelers formula [75]. Wheelers formula, like Bryan's is well known. The capacitance for this model is fit from measurements [75].

4.4 Microstrip Model

A formula has been developed in [27] which treats the inductor like a microstrip.

$$L(nH) = 0.01AN^2\pi\left[\ln\left(\frac{8A}{C}\right)+\left(\frac{1}{24}\right)\left(\frac{C}{A}\right)^2\ln\left(\frac{8A}{C}+3.583\right)-\frac{1}{2}\right]$$

Equation 4.16

$$A = \frac{(DO+DI)}{4} \text{ in mils}$$

Equation 4.17

$$C = \frac{(DO-DI)}{2} \text{ in mils}$$

Equation 4.18

Here, N is the number of turns, DO is the outer coil diameter, DI is the inner coil diameter, and the expressions for A and C are given [27]. This equation is restricted to circular spiral inductors.

4.5 Additional Models

In [14] a semi-empirical equation is given for inductance. Their proposed equation is given by:

$$L = 1.5\mu_o N^2 D\left(\frac{D}{W}\right)^{0.1}\exp\left[\frac{-3.7(N-1)(W+S)}{D}\right]$$

Equation 4.19

In this equation μ_o is the permeability of free space, N is the number of turns, D is the inductor length, W is the conductor width, and S is the conductor spacing [14]. In [53] the domain decomposition method (DDM) is applied to inductors. This method decomposed an inductor spiral into a rectangular microstrip [53]. This simpler microstrip problem is then solved for the inductor parameters [53].

4.6 Fuzzy Logic Approach

Tang and Chow [76] describe a semi-empirical fuzzy logic method for calculating the inductance. The method is only good at low frequency in free space, ignores any capacitances involved, ignores any metal thickness, and assumes a square spiral on a grounded substrate [76]. The inductor is divided into 4 trapezoids. Adjacent ones have no mutual inductance (perpendicular currents) and opposing ones have mutual inductance just as seen from Greenhouse's work.

In [76] there is an estimate where the ground plane is neglected as the substrate is assumed to be thick, called a far asymptote [76]. Evaluating a trapezoidal plate of the shape and size of ¼ of the spiral, the capacitance of this plate is given by [76]

$$C(1/4solid) = C_{f1}\varepsilon_o\sqrt{8\pi A_{1/4}}$$

b_1 = (inner coil diameter – spacing)/2

b_2 = (outer coil diameter – spacing)/2

$$A_{1/4} = b_2^2 - b_1^2$$

Equation 4.20

C_{f1} is a shape factor that can be curve fit from a large number of inductors [76]. In [76], the following equation is given, where d_o and d_i are the outer and inner coil diameters respectively

$$C_{f1} = 0.90571 + 0.49425 \exp\left[\frac{-(d_o - d_i)}{0.12253(d_o + d_i)}\right]$$

Equation 4.21

Each ¼ of the inductor is then divided into N x M equal square segments of area W_s^2 [76]. $M = (b_1 + b_2)/W_s$ and $W_s = W + S$. Here, W is the coil width and S is the coil spacing [76]. This method attempts to use the fact that $LC = \mu_o \epsilon_o$ in order to go from capacitance to inductance [76]. The total C for the ¼ inductor, assumed to be far from a ground plane is then given by [76]

$$Cfar = \frac{1}{\frac{1}{C(1/4solid)} + \frac{(p1 - p2)}{NM} - \left(\frac{1}{4}\right)\pi\varepsilon_o r_o}$$

Equation 4.22

$$r_o = \frac{4\left(b_1^2 + b_1 b_2 + b_2^2\right)}{3(b_2 + b_1)}$$

Equation 4.23

$$p_1 = \frac{1}{\varepsilon_o C_f \sqrt{8\pi W W_s}}$$

Equation 4.24

$$p_2 = \frac{1}{\varepsilon_o C_f \sqrt{8\pi W_s^2}}$$

Equation 4.25

$$C_f = 0.865$$

Equation 4.26

Now we look at the other case, where we have a very thin substrate [76]. Here the capacitance calculation is as follows:

$$C_{near} = \frac{\varepsilon_o W A_{1/4}}{h W_s}$$

Equation 4.27

Combining the two cases for the entire inductor gives their inductor formula as follows [76]:

$$L = \frac{4\mu_o \varepsilon_o N^2 \left(b_1 + b_2\right)^2}{\left(C_{far}^n + C_{near}^n\right)^n}$$

Equation 4.28

$$n = 1.31461 - 0.6592 \exp\left[\frac{-.6139h}{W_s} + \frac{.2918h}{W}\right]$$

Equation 4.29

As mentioned previously, and shown by the variety of EM software tools available, the inductance of the coil can also be calculated by a direct application of Maxwell's equations. [9] and [8] give an excellent summary of this method. This method will only be very briefly summarized here as in itself it could generate thesis reports. What happens in this method is that Green's functions are applied to the structure in order to make Maxwell's equations discrete over currents and potentials. This is then solved by various methods of matrix handling and problem meshing. In [19] a partial EM method is described which starts from current density and approximates a circular spiral by a series of concentric rings. The self and mutual inductance are calculated by this method.

All of these methods for calculating the inductance of a coil are quite complicated compared to the simple model that can be used in the case of a solenoid, where inductance is linearly dependent on the number of turns. This is given for solenoids with one side attached to a substrate by [7][41] :

$$L = \frac{N^2 \mu w h}{l}$$

Equation 4.30

Here L is the inductance, N is the number of turns, μ is the magnetic permeability of the core, w is the core width, h is the core thickness, and l is the core length.

4.7 Equations used in this Thesis

There are two equations, proposed in [77], which have been found by this work to be very good for planar spiral inductors. One is a modification of Wheeler's formula, given by

$$L = K_1 \mu_o \left(\frac{n^2 d_{avg}}{(1 + K_2 \rho)} \right)$$

Equation 4.31

$$\rho = \frac{d_o - d_i}{d_o + d_i}$$

Equation 4.32

$$d_{avg} = \frac{d_o + d_i}{2}$$

Equation 4.33

Here d_o is the outer coil diameter, d_i is the inner coil diameter, n is the number of turns, μ_o is the permeability of free space, and K_1 and K_2 are geometry dependent parameters [77]. The parameters are given in the paper for square, hexagonal, and octagonal inductors. For this work, only the values for the square spirals ($K_1 = 2.34$, $K_2 = 2.75$) were required. The other equation used in [77] is a current sheet approximation to

the inductor. The inductor is treated like a series of current sheets with self and mutual inductances. Then it appears something similar to the Greenhouse approach is used to build the inductance of the coil from the geometric mean distance and the arithmetic mean distance. This equation is given as follows:

$$L = \left(\frac{\mu_o n^2 d_{avg} c_1}{2}\right)\left[\ln\left(\frac{c_2}{\rho}\right) + c_3\rho + c_4\rho^2\right]$$

Equation 4.34

Here the definitions are the same as the previous equation, only instead of two K parameters there are four c parameters used to fit the data. Once again, in [77] the appropriate values are given for different geometries. In the case of a square spiral c_1 = 1.27, c_2 = 2.07, c_3 = 0.18, and c_4 = 0.13. The accuracy of this method worsens as the coil spacing/width becomes large [77].

Both of the expressions given in [77] were implemented in an inductance calculator created by the author of this work. It was found that these expressions do accurately predict the DC inductance of the average coil. One thing that was implemented in the program that is part of this work is that instead of using the inner diameter, the average inner diameter was used. This was found to slightly improve the accuracy of these equations. The reason to use the average inner diameter is simply that this is a more accurate representation for the case where the inside of the inductor is not square but rectangular. This makes these equations more accurate for the case of fractional numbers of turns: 3.25 turns for example. These equations were compared to

Inductor	L(1GHz) Measured	L(DC) Modified Wheeler	L(DC) Current Sheet	L ASITIC
10nH 2post	9.179118	10.14062994	10.05622547	10.269
4nH 2post	3.782126	3.90901546	3.906532106	3.96
3nH 2post	2.913366	2.917714364	2.901832029	2.95
1.5nH 2post	1.653466	1.715063053	1.703645345	1.836
27nH 2post	28.02558	27.1464889	27.20677553	27.39

Table 4.1: Comparison of the two used DC equations

ASITIC as well as measured results with good results. This gives good hope for ease of design of both the inductors in this and other work. Both [77] and [78] give a suggested template equation with multiple fitting parameters to fit measured or simulated data to.

Table 4.1 above shows a comparison of these two equations for the inductors used in this work. The results are compared against measured as well as ASITIC values. From the equations, and the simulation results previously shown, we can see that these two equations predict the inductance with a similar accuracy. This makes these equations potentially quite useful. The only thing to note is that both the measured and ASITIC calculations take into account the underpass, the modified Wheeler and current sheet formulae do not. It should also be noted that these equations are for square spiral inductors and are not expected to be valid for circular spirals.

In order to understand the range of usefulness of these equations, they were compared to a wide variety of ASITIC simulations of inductors ranging in size from 100µm to 1100µm per side, with widths and spacing from 10 to 50µm and up to 27.5 turns. For very small inductors, below 0.5nH, both equations performed poorly with over 20% error in some cases. Both equations handled even 27 turns with reasonable accuracy. For these large spirals, inductance up to 300nH, the modified Wheeler equation had significantly more error; 8% vs. 1% for the current sheet. The test confirmed that for the range of inductance values that are typically required in RF applications, these equations have less then 10%, and less then 5% in the majority of cases.

4.8 Resistance and Capacitance

We have seen a variety of methods of analytically calculating the inductance of a coil, but this is only one element in our lumped element model that we have seen. Since all of the analytical formulas seen calculate a DC inductance value, it is therefore important to calculate the other model elements to help build a more accurate and broader band model.

To calculate the resistance of the inductor, represented by a resistor in series with the inductor, we can use the following approximation from [8]:

$\delta = \sqrt{\frac{\rho}{\pi \mu f}}$ =skin depth, also seen in the previous section

Equation 4.35

$$t_{eff} = \delta\left(1 + e^{-t/\delta}\right)$$

Equation 4.36

$$R = \frac{l\rho}{wt_{eff}}$$

Equation 4.37

In these expressions, f is the frequency in Hz, t is the thickness of the metal, ρ is the resistivity of the metal, l is the total length of the inductor coil, R is the series resistance of the inductor, μ is the permeability of the metal, and w is the width of the inductor coil [8][68].

To calculate the parallel capacitance, which is the capacitance between the coil and the underpass, we can use a very simple approximation. We can simply treat this capacitor as a capacitor with an area equivalent to the overlap area between the coil and the underpass [8]. This neglects the capacitance between the inductor coils, however, in most cases this is safe to do [8]. The parallel capacitance then becomes:

$$C_s = \frac{nw^2 \varepsilon_{ox}}{t_{ox}}$$

Equation 4.38

Here, n is the number of turns, w is the coil width, ϵ_{ox} is the dielectric constant of the material in between the coil and the underpass, and t_{ox} is the thickness of the dielectric or the air gap [8]. When using this expression, especially for inductors with

fractions of turns, it is important to watch out for cases where n might not be the number of turns but may be one greater or one smaller.

The next capacitance to calculate is that between the coil and the substrate. Two simplifications have been suggested here as well [8]. One is that the inductor area, rather than the coil area be used for the area in the inductance calculation [8]. If possible, using the real coil area should be more accurate. The other approximation is to assume that the capacitance is distributed such that each of the two inductor ends/ports sees half of the total capacitance [8]. Implementing this gives:

$$C_{ox} = \frac{lw\varepsilon_{ox}}{2t_{ox}}$$

Equation 4.39

Here l is the inductor length, w is the inductor width, ϵ_{ox} is the dielectric constant of the material in between the coil and the underpass, and t_{ox} is the thickness of the dielectric or the air gap as seen previously [8].

One interesting proposal from the work in [60] is to estimate the self-resonance frequency by calculating the resonance frequency of the inductance with the parallel capacitance. This will give:

$$F_{res} = \frac{1}{2\pi\sqrt{LC_p}}$$

Equation 4.40

For inductors on insulating substrates, such as those in this work, these calculations provide values for the entire lumped element model. We have seen that many of the equations of these elements are physically based, like the simple capacitance approximations used.

These models are very commonly used for inductors and provide a fast and easy way for designers to design, communicate, and connect inductors. One of the main benefits of these lumped element models is that they are very fast to simulate in a circuit simulator and can be easily connected to other components to build a circuit. These models, as we have seen, are applicable to this work and in fact to almost any planar inductor.

5.0 Conclusions and Future Work

A considerable amount of work has been carried out in recent years to improve the quality of passive components available. This is because passive components make the best filters, baluns, matching networks, etc [9]. These components are in increasing demand as the demand for wireless devices increases. Bluetooth, cell phones, WLAN are all expanding markets that are continually being driven towards improvement and miniaturization. There has therefore been a lot of work carried out on optimizing inductors in CMOS and in general thin film technologies including MMICs. Much of the work on inductors, however, is not on suspended inductors, but inductors in CMOS processes or else other types of MEMS inductors like solenoid inductors or inductors released into a vertical position by hinges and stress engineering.

The work presented in this thesis, which included released inductors and transformers made from aluminum and thick gold, was successful in producing good quality inductors with Q factor up into the 50-70 range. A simple process was chosen using a sacrificial dielectric layer (SOG/PSG) and a blanket release etch. Only a 1µm air gap was created between the coil and the underpass. A large range of inductance was tested from 1nH to 27nH. The main result upon releasing the inductors was that the self-resonance frequency increased, sometimes by up to 4GHz, increasing the useful range of these devices. The peak Q factor also increased as well.

Having compared this work to the other suspended inductors that are and have been researched, it can be seen that this work has many unique aspects including the small air gap, two released metal layers, the choice of an alumina substrate, and the inductance range used. Many different types of suspended inductors have been tried including etched, photoresist molded, and flip chip assembled. A lot of work is being done on silicon to improve the inductors which are possible in CMOS processes, but these are still poor in performance. In fact the present thesis work ranks among the top three as far as inductor performance achieved. The main feature of the other two papers reporting similar or better Q factors is that they use a much larger air gap (50-100µm),

thereby drastically reducing parasitic capacitances. In general this work shows a simple, manufacturable process that can achieve close to the best Q factor reported.

In this thesis work, we have also seen a well adopted pi model for the inductor. In addition many closed form expressions were shown and two were found to be accurate for planar spirals, the modified wheeler equation and the current sheet approximation. Both of these were also verified against both measured and ASITIC results. The model given could be applied to any suspended spiral inductor work.

Although this work is significant in the area of improving the quality of passive components available for 1-5GHz applications, there are many things that can be continued on into the future. The main next step would be to investigate the packaging or encapsulation of these devices. Since these inductors only have a 1μm air gap, an encapsulating material will most likely just return the inductors to their pre-release performance. It is still worth investigating, however, as some type of cavity formation should be the best way to package these devices. This will not be as complicated as for most MEMS devices since these devices do not require a vacuum, only preservation of the air gap.

Another idea of future work that can be done is to try to use copper in place or gold and perhaps aluminum. Copper is even lower resistance and is expected to increase the Q factor of these inductors even further. An estimate might be an increase of ~10 in peak Q. Most of the current research is using copper, and this is the reason. At the moment these inductors and transformers were the only devices fabricated in this process. It would be of great interest to continue developing the process so that capacitors can be integrated as well. This would allow RF circuits such as filters, baluns, matching networks, etc to be built with the integrated suspended inductors. This would also be an easy way to test these devices in an actual circuit for an application such as WLAN or Bluetooth. This will be a challenging addition to the process as careful consideration will need to be taken to ensure good quality films for the capacitors as well as some type of effective etch stop/barrier layer(s) so that the capacitors do not get released. This can

also potentially be accomplished with a release mask, depending on the design. A release mask is used in a MEMS process to selectively release only certain areas of the wafer. This may not be a wise option since the etch used for these structures was close to isotropic, in order to etch under and release the inductors. This means there may need to be wasted real estate near the inductors, however it is a simpler solution compared to etch stop layers.

If it is found to be very advantageous to have transformers as developed in this work, future work could also consist of an optimization of these transformers. This work has shown that good released transformers can be made successfully. One such optimization is to optimize the connections out from the center of the two coils. The inductors themselves can be optimized still further. One such optimization is to use ground-signal-ground pads. At the time of design, no such probes were available at Gennum, so the ground-signal pads were used. Also, perhaps smaller inductance values could be tried and/or testing out to higher frequencies.

There are many ways that this work can be continued and expanded. This work is really just the first step in this area that can lead to among the best, if not the very best, inductors that can be made in thin film technology with a simple process. To the best of our knowledge this is the first suspended inductor and transformer work on Alumina.

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