MoS_2 Thin Film Transistors using PECVD Dielectrics and Optical Contrast Modeling for Thickness Measurement

by

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Authors Declaration

I thereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Nicholas George Vardy

Abstract

The discovery of graphene has led to considerable interest in the use of two-dimensional materials for use in transistors. Unlike graphene TMDCs such as MoS_2 possess a band gap allowing them to obtain sufficient on/off ratios for digital logic applications. For MoS_2 transistors, thermal SiO_2 or high-k dielectrics such as Al_2O_3 and HfO_2 are often used as gate dielectrics due to their high quality interfaces. However, MoS_2 also shows considerable promise for large area TFT applications where a-Si:H (μ_e~$1cm^2V^{-1}s^{-1}$) is conventionally used. For TFT applications conventional PECVD dielectrics such as SiN_x and SiO_x are necessary for low temperature large area deposition.

MoS_2 TFTs were fabricated in the bottom common gate configuration on PECVD dielectrics and using mechanically exfoliated flakes ~75nm thick showing mobilities of 13 $cm^2V^{-1}s^{-1}$ - ,sub threshold swings of 1.05 V/dec and ON/OFF current ratio of ~10^5. While this demonstrates the promise of TFTs made from these materials, considerable improvements are expected from MoS_2 approaching one monolayer thickness. However, the process of scanning the substrate for MoS_2 flakes using an optical microscope and measuring by AFM is time consuming and was unable to yield thin layers that were large enough to pattern using photolithography.

In order to improve the process of optical identification and thickness measurement the RGB color models applied to the study of graphene on thermal SiO_2 were adapted to the study of MoS_2 on PECVD dielectrics. Using these models color charts for MoS_2 on PECVD dielectric were generated and dielectrics were optimized for the visibility of monolayer MoS_2. A rapid non-destructive method for measuring the thickness of MoS_2 using images taken from a microscope camera is also presented. These calculations will help improve the fabrication process of mechanically exfoliated MoS_2 devices in the future.

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Chapter 1 Introduction

This thesis demonstrates the use of plasma enhanced chemical vapor deposition (PECVD) dielectrics silicon nitride (SiN_x) and silicon oxide (SiO_x) in the fabrication of thin film transistors (TFTs) from mechanically exfoliated multilayer molybdenum disulphide (MoS_2). SiO_x and SiNx are commonly used in the fabrication of TFTs and are well suited to large area low temperature deposition. To date PECVD dielectrics have not been employed for TFT fabrication with MoS_2. The transistors fabricated in this study show promise for using MoS_2 in large area electronics as a high mobility alternative to amorphous silicon.

Optical contrast is commonly used to identify the thickness of Graphene or MoS_2 on conventional dielectrics such as silicon dioxide (SiO_2). While this was initially restricted to monochromatic light, CIE color models have been previously employed on graphene to predict the RGB color enabling the generation of color charts. In this work these models are extended to MoS_2 and adapted for use with the PECVD dielectrics used in transistor fabrication. This allows color charts for MoS_2 on PECVD dielectrics to be generated and dielectric film thicknesses to be further optimized to improve MoS_2 visibility. This will aid in the fabrication of MoS_2 transistors on PECVD dielectrics in the future by allowing thinner flakes to be identified.

1.1 Graphene

Two-dimensional (2D) materials have attracted considerable attention since the discovery that atomically thin films of graphene could be isolated by mechanical exfoliation of highly ordered pyrolitic graphite [1].Graphene consists a single plane of carbon atoms bonded in a two dimensional honeycomb lattice, in graphite these planes are stacked vertically and held together by van der walls forces [2]. Graphene was first isolated by mechanical exfoliation, a process by which layers of graphite are repeatedly peeled using adhesive tape, breaking the interlayer interaction until only a single layer remains[2]. Prior to this discovery, it was believed that

thermal fluctuations would cause dislocations making such free standing atomically thin films unstable [1].

The electronic structure of graphene is quite unique being a zero band gap semiconductor with a linear dispersion relation $E = \bar{h}v_f k$ giving it a cone shaped band structure as well as zero density of states at the Fermi level as shown in Figure 1 [3]. Electrons near the Fermi level behave as quasi particles called massless Dirac fermions having a relativistic velocity of $10^8 \frac{cm}{s}$ [2].

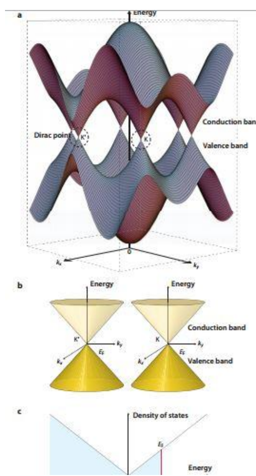

Figure 1 Band Structure and Density of States of Graphene [3]

When used in transistors graphene shows an ambipolar field effect, allowing the concentration of electrons or holes to be continuously tuned to as high as $10^{13} cm^{-3}$ with room temperature mobilities as high as $15000 \frac{cm^2}{Vs}$ [2]. Theoretically, the thin channel region of graphene allows for the suppression of short channel effects that plague state-of-the-art silicon transistors [4]. However, in practice the absence of a band gap in graphene makes the transistor impossible to fully turn off leading to on/off ratios of only 2-20 [4]. Additionally, these transistors do not fully saturate at high drain source voltages but instead switch conduction type leading to a second linear regime [4]. Typical graphene transistor transfer and output characteristics are shown in Figure 2.

Considerable effort has been put into engineering a band gap into graphene by using nanostructuring or chemical fictionalization but this leads to a loss of mobility in exchange for only a very small band gap [5] . For this reason, graphene transistors are poorly suited to digital logic applications where on/off ratios of 10^4-10^7 are required, but are instead better suited to high frequency applications where the cutoff frequency f_T is the main figure of merit [4].

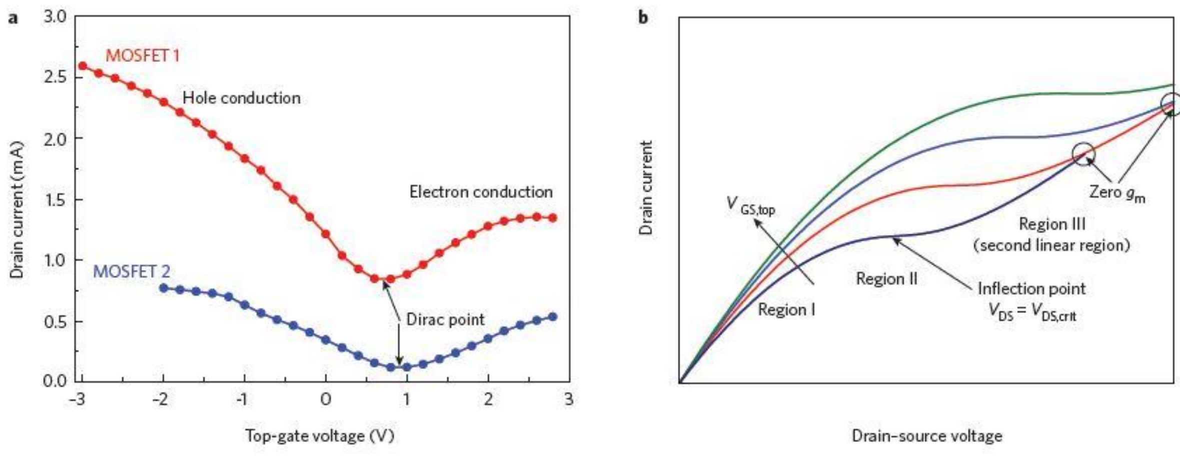

Figure 2 Typical Transfer and Output Curves of Graphene Transistors [4]

1.2 Molybdenum Disulphide

The discovery that atomically thin layers of graphene could be isolated from bulk graphite has lead renewed interest in other layered materials, most notably transition metal dichalcogenides (TMDCs). TMDCs have the chemical formula MX_2 where M is a transition metal from group IV V or VI and X is a chalcogen (S Se or Te) [5] .For transistor applications MoS_2 is particularly promising because unlike graphene it is semiconducting and has a band gap [6]. Additionally, crystals of MoS_2 are naturally occurring in the form of the mineral molybdenite [6]. The 2H-MoS_2 polytype which is most commonly occurring has a layered structure with two hexagonal planes of sulfur atoms separated by a hexagonal plane of molybdenum atoms having triagonal prismatic coordination as shown in Figure 3 [5]. Each MoS_2 monolayer (ML) has a thickness of approximately 0.65nm [6].

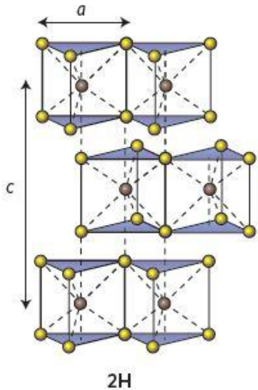

Figure 3 MoS_2 Crystal Structure (Mo is purple and S is yellow) [5]

MoS_2 has a number of layer dependent properties going from an indirect band gap of 1.2eV in the bulk to a direct band gap of 1.9eV for a ML as shown in Figure 4 [5]. The direct band gap of ML MoS_2 makes this material particularly promising for optoelectronic devices [5]. Conduction band states at the K point are mainly due to localized d orbitals on the Mo atoms which being sandwiched between planes of sulfur atoms are only weakly dependent on interlayer coupling [5]. However, states near the Γ occur due to combinations of antibonding p_z orbitals on the sulfur atoms and d orbitals on the molybdenum atoms and are strongly stabilized by interlayer coupling [5]. As a result the energy of the conduction band near the Γ point is raised for the monolayer making the direct transition at the K point the lowest energy [5].

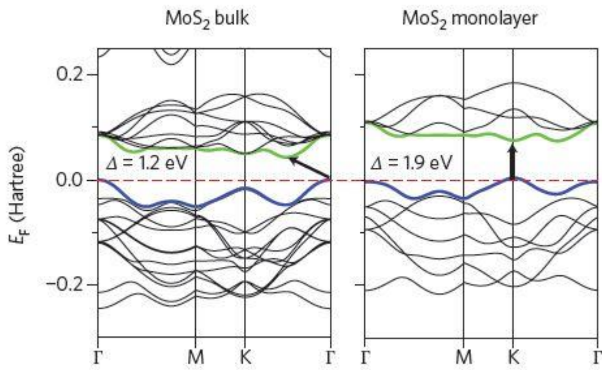

Figure 4 Bandstructure of MoS_2 Bulk and Monolayer [5]

MoS_2 also shows a change in vibration properties with the number of layers. The main raman active phonon modes are the out of plane A_{1g} and in plane $E_{2g}^1$and modes which are located near

406cm^{-1} and 382cm^{-1}[5] . These modes experience a layer dependent shift in peak position as shown in figure 5. This shift in the raman peak is often used to verify the number of layers present in thin MoS_2 although the peak shift saturates at the bulk value after only a few layers.

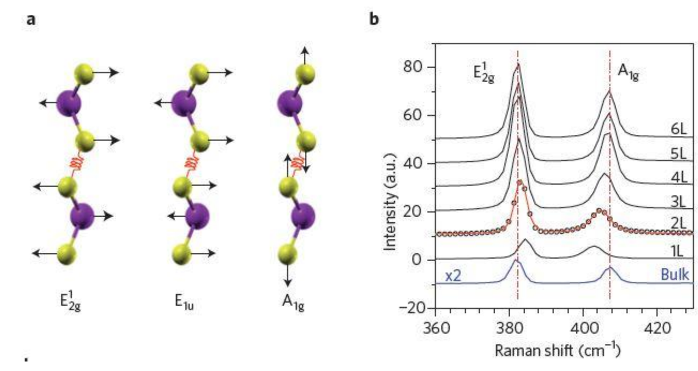

Figure 5 Vibration Modes and Raman Spectra of 2H-MoS_2[5]

1.2.1 MoS_2 Transistors

The bonds in MoS_2 are partially ionic which creates large polarization fields from lattice vibrations scattering electrons and limiting the mobility to a theoretical value of 410cm^{2}V^{-1}s^{-1} at room temperature [5]. However, realizing this theoretical mobility in transistors has proven difficult. Early MoS_2 transistors fabricated on thermal silicon dioxide (SiO_2) as the dielectric showed low mobilities in the range of 0.5-3cm^{2}V^{-1}s^{-1} [6] and large sub threshold swings >1V/dec [7] . While the layered structure of MoS_2 is free of dangling bonds at the surface the dielectric in general is not. Temperature dependent transport measurements have revealed hopping or thermally activated transport rather than band transport [8]. This is believed to be caused by traps present in the dielectric which through random potential fluctuations create band tail and localized states in MoS_2 as illustrated in Figure 6 [9].

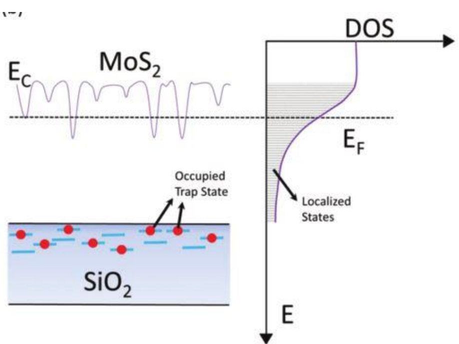

Figure 6 Dielectric Traps and Resulting Localized States in MoS_2 [9]

In addition to lattice vibrations the second major scattering mechanism is coulomb scattering which results from the interaction of the electron with the electric field of charged particle impurities within MoS_s or on its surface [5]. The main sources of coulomb impurities are likely chemical residues, adsorbed gasses or dangling bonds on the surface of the dielectric [10] The use of high-k dielectrics such as aluminum oxide (AlO_2) and hafnium oxide (HfO_2) deposited by atomic layer deposition (ALD) have been used to screen coulomb forces enabling field effect of ~$100cm^2V^{-1}s^{-1}$ in bottom gated structures and ~$200cm^2V^{-1}s^{-1}$ in top gated structures [6] as well as small sub threshold swings of 70-80mV/dec [7].

Much of the early work on MoS_2 transistors featured large work function metals such as gold (5.4eV) which were believed to create n-type ohmic contacts [11]. Considering the electron affinity of MoS_2 is 4.0eV [11] such ohmic contact would not be expected based on the difference in work functions. More systematic studies have revealed that the MoS_2-metal interface is strongly impacted by Fermi level pinning near the conduction band of MoS_2 [11]. All metals studied were found to form a Schottky barrier with MoS_2 with the barrier height being significantly less for low work function metals such as scandium (3.5eV) and titanium (4.3eV) [11]. Ohmic contact is perceived due to tunneling through the schottky barrier but this significantly limits the current flowing through the transistor masking the true mobility of MoS_2, particularly for large work function metals [11]. The effect of Fermi level pinning explains why nearly all MoS_2 transistors demonstrate n-type characteristics [11].

To date very few MoS_2 transistors more than a few layers thick have been reported [11]–[18] in contrast to many monolayer or bi-layer devices [6], [8] . Most work has focused on monolayer

and bi-layer MoS_2 due to the interest in reducing short channel effects in state-of-the-art metal oxide semiconductor field effect transistors (MOSFETs)[6]. Multilayer MoS_2 is particularly advantageous for TFT applications due to its three times higher density of states and the existence of multiple channels for conduction enabling higher currents [12]. Initially mobility increases with MoS_2 thickness but shows a maximum at an intermediate number of layers and then begins to decrease [10], [11]. The optimum layer thickness varies by study but appears to be below 15nm. This trend can be explained by a high interlayer resistance in MoS_2 with increasing layer number as well as a decreased influence of coulomb scattering at the dielectric interface [10], [11].

1.2.2 MoS_2 Deposition

Mechanical exfoliation often employs an adhesive such as Scotch ® tape to cleave layers of MoS_2 from the bulk crystal. This has a number of disadvantages, namely very poor control of the lateral dimensions and thickness of the exfoliated flakes as well uncontrollable purity and poor yield [6]. Over time techniques have been developed for epitaxial or chemical vapor deposition (CVD) of graphene [19]. Such techniques are necessary for scalable manufacturing allowing for large area deposition and integration with standard micro/nano fabrication processes.

The growth of MoS_2 has been demonstrated using three main precursors: ammonium thiomolybdate [$(NH_4)MoS_4$] solution, pre-deposited molybdenum (Mo) films, or molybdenum trioxide (MoO_3) powder [6]. The most promising technique so far is the use of solid precursors of MoO_3 and sulfur which is improved by the use of perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt (PTAS), 3,4,9,10-perylene-tetracarboxylicacid-dianhydride (PTCDA), or reduced graphene oxide (r-GO) as seed promoters [6]. All of these techniques tend to produce polycrystalline films with grain sizes that are less than those produced by mechanical exfoliation exhibiting poorer mobilities due to grain boundary scattering [6]. These techniques also require high temperatures of 700-1000C which are incompatible with glass substrates. Significant progress will need to be made in the area of MoS_2 deposition techniques before large area fabrication of TFTs from this material can be fully realized.

1.3 Optical Identification

When 2D materials such as graphene or MoS_2 are mechanically exfoliated only a small number of monolayers exist among a large number of thicker sheets [2], [20]. A key element in the discovery of graphene was the observation that significant optical contrast exists between a dielectric substrate of carefully chosen thickness due to interference effects (Figure 7) [2], [20]. While scanning probe techniques like atomic force microscopy (AFM) can be used to measure the thickness of graphene flakes this has very low throughput and is thus not practical for scanning over large areas [2].

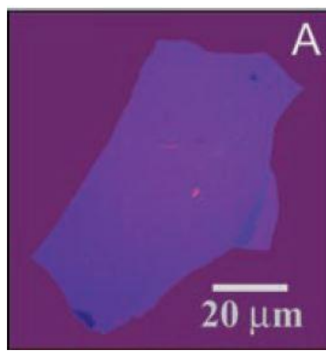

Figure 7 Optical Contrast of Graphene [1]

Early research on the optical contrast of graphene focused on illumination under monochromatic light through the use of a series of narrow band filters [20]–[23]. Contrast is then calculated from Eqn. 1 where $R_0(\lambda)$ is the reflectance of the substrate under the illumination wavelength λ and $R(\lambda)$ is the reflectance of the graphene on top of the dielectric layer [21]. The contrast can then be calculated from an image taken by the microscope camera after splitting the image into red, green, and blue channels and comparing the pixel intensity between the substrate and graphene.

$$\boldsymbol{C(\lambda) = \frac{R_0(\lambda) - R(\lambda)}{R_0(\lambda)}} \quad \textbf{(1)}$$

Under white light illumination graphene shows different color bands for different thickness ranges which make thickness easy to distinguish by eye or from colored images taken by the microscope camera [24]. An understanding of the perceived color contrast when viewed by the eye or calculated color contrast from a microscope image requires an understanding of the CIE color system [24]–[27]. Color charts for easily identifying graphene layers of ranging

thicknesses on different dielectrics have been calculated [25]. Graphene thicknesses can also be calculated directly from the intensity of microscope images but when white light is used this requires an understanding of the light source and the instrument dependent properties that determine how an image is created [28]. While device independent schemes such as the ratio of color differences have been implemented these are only applicable to limited thickness ranges [28]. Recently, research on the optical contrast of graphene has applied to other 2D semiconductors such as MoS_2 [29]–[33] . So far this research has focused on the monochromatic contrast on conventional dielectrics such as SiO_2 and no attempts have been made to utilize the CIE color system in these calculations.

Chapter 2 Background on Thin-Film Transistors

Prior to the discussion of thin-film transistors (TFTs) made from MoS_2 some general background on the operation of TFTs will be presented. A TFT is a three terminal electronic device which is a type of field-effect transistor (FET) which consists of a gate (G) which acts to modulate the flow of carriers from the source(S) to the drain (D). TFTs work using a similar principle to the metal oxide semiconductor field effect transistor (MOSFET) shown in Figure 8. For the n-type MOSFET shown here the source is typically grounded and positive voltages V_G and V_D are applied to the gate and drain respectively. The most basic principle of such a transistor is that the junction formed between the p-type substrate and n-type drain is reverse biased and will not allow current to flow. However, when a voltage is applied to the gate which exceeds the threshold voltage V_T the surface of the semiconductor will be inverted to n-type allowing a current I_D to flow from source to drain.

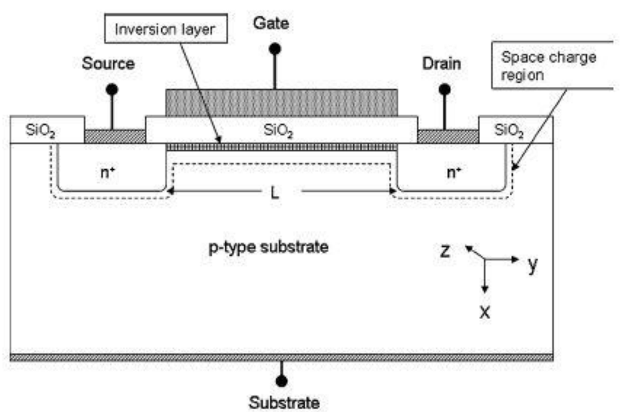

Figure 8 MOSFET Structure [34]

2.1 MIS Structures

The action of switching on a field-effect transistor is based on the metal-insulator-semiconductor (MIS) structure formed between the gate metal, gate insulator (SiO_2) and substrate. This structure acts like a capacitor attracting or repelling carriers to the surface of the semiconductor depending on the voltage applied to the gate. The band diagram for the ideal case when the Fermi level (E_F) of the metal and the semiconductor align is shown for a p-type substrate in

Figure 9a. Here there is no band bending in the semiconductor and the carrier concentrations are given by the doping level of the substrate, this is referred to as the flat band condition.

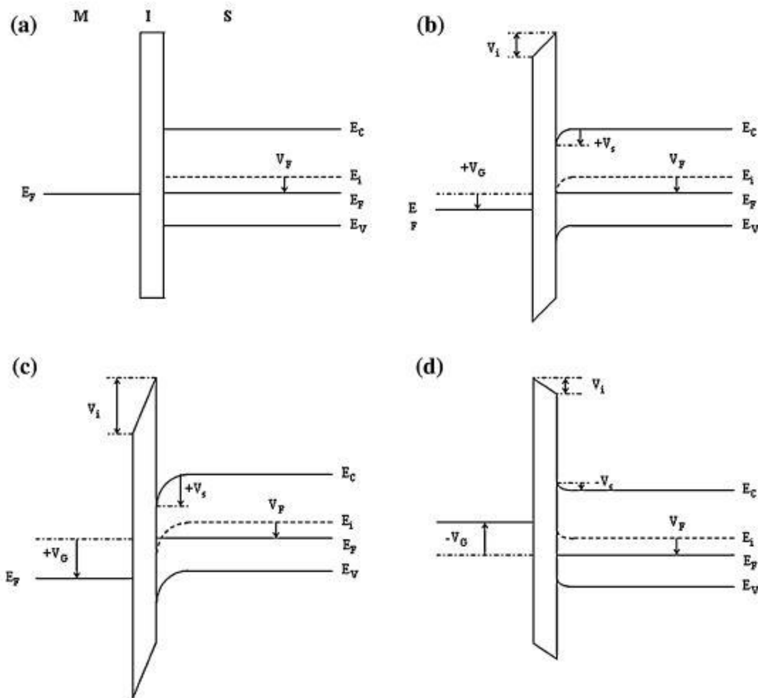

Figure 9 MIS Band Bending a) Flat Band b) Depletion c)Inversion d) Accumulation [34]

When a positive voltage is applied to the gate the Fermi level of the semiconductor will now be raised by an energy qV_g with respect to the gate. This will induce downward band bending in the semiconductor as the majority carrier holes are pushed away from the surface of the semiconductor leaving behind the minority carrier electrons and the negative ionized acceptors to create a space charge region [35]. This is referred to as depletion and is shown in Figure 9b.

As the gate voltage becomes more positive holes continue to be pushed away from the interface and eventually the surface of the semiconductor will inverted to n-type as shown in Figure 9c. Eventually, the surface of the semiconductor will be as n-type at the surface as the bulk is p-type. This is referred to as the threshold inversion point and any further increase the gate voltage will rapidly increase the electron concentration without changing the width of the depletion region. If a negative voltage is applied to the gate this will induce upward band bending in the

semiconductor as shown in Figure 9d, this is referred to as accumulation and leads to a rapid increase in the hole concentration without the formation of a depletion region.

2.1.1 Non-Ideal MIS Structures

Any real MIS structure may have a difference between the Fermi level of the metal and semiconductor as well as charges trapped in the dielectric or traps states within the band gap of the semiconductor[34]. A difference in work functions will cause band bending even in the absence of an applied gate bias or change the carrier concentration at the surface of the semiconductor. The amount of band bending at V_G=0 defines the flat band voltage V_{FB} which is the voltage which must be applied to the gate in order to create the flat-band condition shown in Figure 9a.

In general the bands in the metal and semiconductor will not be aligned prior to electrical contact and will have an offset defined by the work function or the electron affinity as shown in Fig 10a. The work function ϕ is the difference in energy between the vacuum level and E_F while the electron affinity χ is the difference between the vacuum level and the conduction band minimum. The electron affinity is often specified because the work function of the semiconductor will depend on the doping level.

When the metal and semiconductor in an MIS structure are electrically connected the Fermi levels must be the same everywhere and so this will induce band bending at the surface of the semiconductor as shown in Fig 10b. Without considering trapped or interface charges it can be shown that the flat band voltage will be the difference between the metal and semiconductor work functions (Eqn. 2) [34]. In this case inducing depletion or accumulation requires a positive or negative voltage respectively relative to the flat band voltage

$$V_{FB} = \phi_M - \phi_S = \phi_{MS} \quad (2)$$

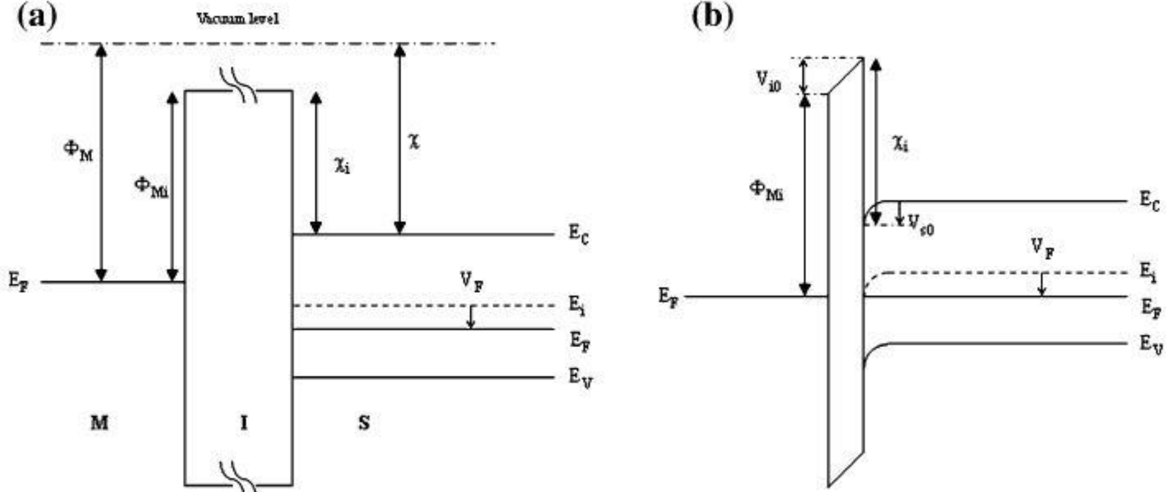

Figure 10 MIS Band Structure a) Prior to electrical contact b) thermal equilibrium [34]

Many dielectrics show a fixed charge which induces an opposite charge at the semiconductor surface [34]. This fixed charge can be caused by non-stoichiometric ratios in the dielectric leading to dangling bonds or due to ionic impurities [36]. Charges may be distributed throughout the dielectric but their influence decays as the distance from the semiconductor/dielectric interface increases [34]. Since the exact position of fixed charges is rarely known this charge is expressed by the surface charge density (Q'_{ss}) which is the net effect of the distributed charge if it were all located at the interface (Eqn. 3) [34]. The effect this charge has on the flat band voltage depends on the capacitance per unit area of the capacitance of the gate dielectric $C_g{}'$.

$$\boldsymbol{V_{FB} = \phi_{MS} - \frac{Q'_{ss}}{C_g{}'}} \quad \textbf{(3)}$$

Trap states may also exist within the band gap of the semiconductor and carry a charge depending on the position of E_F [34]. States which are above the intrinsic Fermi level are said to be acceptor states while those below the intrinsic Fermi level are said to be donor states [34]. If E_F moves above the intrinsic Fermi level E_{Fi} acceptor states are filled and carry a negative charge and if E_F moves below E_{fi} donor states are emptied and carry a positive charge. Overall, the existence of surface states has the effect of requiring larger gate voltages to induce band bending in the semiconductor [34]. The effect of donor states inducing downward bending in the semiconductor is shown in Figure 11.

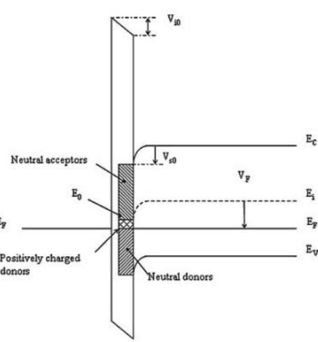

Figure 11 Band Bending due to Interface States [34]

2.2 Current Voltage Relations of a Transistor

The equations used to describe the current voltage (I-V) relationships in MOSFETS are often used to describe the behavior of TFTs and define important parameters such as the threshold voltage (V_T), field effect mobility μ, ON/OFF currents and sub threshold slope (SS).

For low V_D the transistor behaves like a resistor with the gate voltage linearly increasing the carrier concentration in the channel as it exceeds the threshold voltage [34]. Below the threshold voltage there will be no inversion charge and ideally no current through the transistor. The total current will depend on the field-effect mobility and the width (W) and length of the transistor (L). This is called the linear regime and the transistor behaves as a resistor whose resistance decreases linearly with increasing gate voltage (Eqn. 4) [34].

$$I_D = \frac{W}{L}\mu_n C_i (V_G - V_T) V_D \quad (4)$$

As the drain voltage increases the potential of the channel near the drain is also increased so that less charge is being induced by the gate at the drain relative to the source [TFT]. This will cause the resistance of the transistor to increase. At the saturation voltage V_D(sat) given by Eqn. 5 the inversion charge will be zero at the drain edge of the channel causing the channel to be pinched off at the drain [34]. Carriers will travel to the edge of the pinched off channel and will be swept by the depletion region into the drain causing the current to saturate [34].

$$V_D(sat) = V_G - V_T \quad (5)$$

By making use of the gradual-channel approximation I-V equations can be derived for the linear (Eqn. 6) and saturation regimes (Eqn. 7) [TFT]. In this derivation, it is assumed that the electric field across the channel is smaller than the electric field across the gate, so that short channel effects are not observed. Resistances of the source drain contacts, potential leakage current across the gate dielectric or any parasitic capacitances are not considered. Also, since it is assumed that all charge induced in the channel is free to conduct current, this does not consider the presence of interface states which are not mobile and will therefore manifest as a decrease in the mobility.

Experimental I-V transfer curves for a MOSFET are shown in Figure12 showing linear behavior for small V_D and increasing current with increasing gate voltage V_G. As V_D approaches $V_D(sat)$ the resistance of the channel begins to increase and the current levels off. The saturation point increases for increasing V_G as does the saturation current.

$$I_D = \frac{W\mu_n C_i}{2L}\left[2(V_G - V_T)V_D - V_D^2\right] \; for \; 0 \leq V_D \leq V_D(sat) \quad (6)$$

$$I_D(sat) = \frac{W\mu_n C_i}{2L}(V_G - V_T)^2 \; for \; V_D > V_D(sat) \quad (7)$$

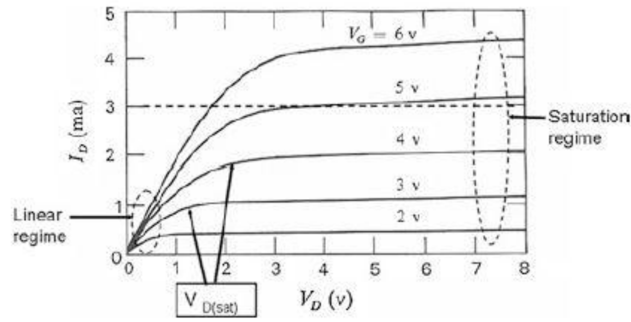

Figure 12 Typical MOSFET Transfer Curves [34]

2.2.1 Sub threshold Current

So far it has been assumed that below V_T the transistor will not conduct any current. In reality, there will be weak inversion of the channel between the flat band voltage and threshold voltage which are exponentially dependent on the gate voltage as shown in Figure 13 [34]. On a semi-log plot the drain current will be linear with respect to V_G and is characterized by the inverse of the

slope, the sub threshold swing (S) [34]. When used as a switch a small S is desirable as it means that the transistor can be taken from the OFF state to the ON state quickly over a narrow range of voltage [TFT]. The theoretical sub threshold swing (Eqn. 8) is determined by the gate capacitance C_i and the depletion region capacitance C_s(which increases with substrate doping) and gives a theoretical minimum of 59.5 mV/decade in silicon [34].

$$\boldsymbol{S \equiv \frac{dV_g}{d\log I_d} \approx \frac{k_B T}{e}\left(1+\frac{C_s}{C_i}\right)\ln 10} \quad \textbf{(8)}$$

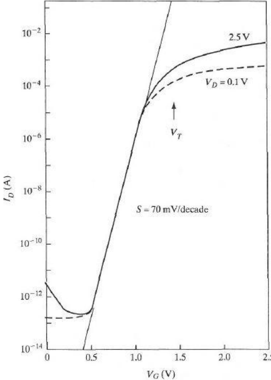

Figure 13 Typical MOSFET Output Curve [34]

When a large number of trap states exist within the semiconductor the depletion capacitance becomes dominated by the interface/trap density causing a reduction in the induced charge leading to mobile carriers (increase in sub threshold swing) [34]. Interface states create a capacitance C_{ss} which is dependent on the number of trap states N_{ss} (Eqn. 9) [34] . This capacitance is in parallel with the depletion capacitance (Eqn. 10) which allows N_{ss} to be determined from the sub threshold swing.

$$\boldsymbol{C_{SS} \sim eN_{ss}} \quad \textbf{(9)}$$

$$\boldsymbol{S \approx \frac{k_B T}{e}\left(1+\frac{C_s+C_{ss}}{C_i}\right)\ln 10} \quad \textbf{(10)}$$

2.2.2 Extracting Transistor Parameters

Transistor Parameters such as the V_T and field effect mobility μ are often extracted by fitting data from the linear or saturation regimes. In the linear regime when $V_D << V_D(sat)$ I_D is given by

Eqn. 4 and can be fit to a straight line with respect to V_G, the mobility can then be obtained in the linear region from the slope of this line (Eqn.11). Similarly, in the saturation regime, the drain current depends on the square of V_D(sat) so the x-intercept of a plot of $\sqrt{I_D}$ vs Vg gives the threshold voltage and the mobility can similarly be obtained from the slope (Eqn.12).

$$\boldsymbol{\mu_n = \frac{L}{WC_iV_D}\frac{\partial I_D}{\partial V_G}\ for\ V_D \ll V_D(sat)}\ \textbf{(11)}$$

$$\boldsymbol{\mu_n = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_D(sat)}}{\partial V_G}\right)^2\ for\ V_D > V_D(sat)}\ \textbf{(12)}$$

Chapter 3 MoS_2 Thin-Film Transistors

3.1 PECVD Dielectrics

In TFTs, the quality of the gate dielectric is critical to the overall performance of the transistor. It is generally desirable to have low leakage current with high capacitance as well as a low density of fixed charges and interface states, low pin-hole density and good bias-stress stability [34]. While stoichiometric Si_3N_4 and SiO_2 are often employed in integrated circuits and have good dielectric properties their deposition requires high temperatures [34]. TFTs are often fabricated on glass which requires a low temperature (<450°C) below the softening point [34]. The deposition of dielectrics is often performed using plasma enhanced chemical vapor deposition (PECVD) which allows low temperature deposition with good uniformity over large areas [34]. The resulting films are amorphous and non-stoichiometric being represented by the expressions SiN_x and SiO_x to reflect their variable properties depending on deposition conditions [34].

Amorphous silicon nitride (a-SiN_x:H) is the preferred gate dielectric for use in hydrogenated amorphous silicon (a-Si:H) TFTs and is typically deposited using a low temperature PECVD process using siliane (SiH_4) and ammonia (NH_3) along with hydrogen(H_2) as a diluent gas. For a-Si:H TFTs, SiN_x often contains a large positive fixed charge, which in this circumstance is favorable because it positively impacts the defect distribution of a-Si:H [34] .

In TFTs using alternative channel layers such as polycrystalline silicon (poly-Si), nanocrystaline silicon (nc-Si:H) and gallium-indium-zinc-oxide(GIZO), PECVD deposited SiO_x gate dielectrics are generally preferred [34]. SiO_x is preferred for these applications because it tends to have a much lower density of trapped charge which reduces unnecessary negative shifts in the threshold voltage [34]. Similar to SiN_x, SiO_x is often deposited by PECVD using SiH_4 in addition to nitrous (N_2O) in the presence of a carrier gas such as H_2. A major disadvantage of SiO_x is that it tends to be very porous having poor bulk properties [34].

In order to identify a suitable dielectric for MoS_2 TFTs three dielectrics were deposited and tested using FTIR as well as capacitance voltage (CV) and current voltage (IV) measurements of metal insulator semiconductor (MIS) capacitors. The three dielectrics tested were 250nm SiN_x , 100nm SiO_x and a bi-layer consisting of 200nm SiN_x and 50nm SiO_x. The SiO_x film was made thinner in order to have a comparable capacitance while the bi-layer was made to take advantage of both the good interface properties of SiO_x and the good bulk properties of SiN_x.

3.1.1 FTIR

Fourier transform infrared spectroscopy (FTIR) is a characterization technique where the absorption of a thin film in the infrared can be measured. Phonon vibration modes which produce a net change in dipole moment are activated by photons of the same frequency leading to absorption [37]. This gives information about what species and bonds are present within a given material. Frequencies are often given by the wavenumber $\bar{\upsilon}$ [cm^{-1}] which is proportional to the inverse of the wavelength. The positions and relative heights of FTIR peaks give information regarding the bond densities and composition of the film [37].

FTIR spectra of PECVD SiN_x, SiO_x and bi-layer SiN_x/SiO_x are shown in Figure 14. The SiO_x dielectric shows Si-O rocking (~450 cm^{-1}), bending (~815cm^{-1}) and symmetric stretching (~1070 cm^{-1}) modes in addition to small peaks for Si-H stretching (~2150cm^{-1}) and Si-OH stretching (~3620 cm^{-1}) modes indicative of hydrogen content in the films [38]. Similarly, for SiN_x dielectric shows Si-N bending (~470 cm^{-1}) and stretching (~870 cm^{-1}) modes exist in addition to N-H stretching (~3350 cm^{-1}) and bending (~1180 cm^{-1}) and Si-H stretching (~2150 cm^{-1}) modes [38]. As expected the bi-layer dielectric shows many of the peaks of the nitride film as well as a small Si-O stretching peak at (~1070 cm^{-1}) due to the presence of the thin oxide layer.

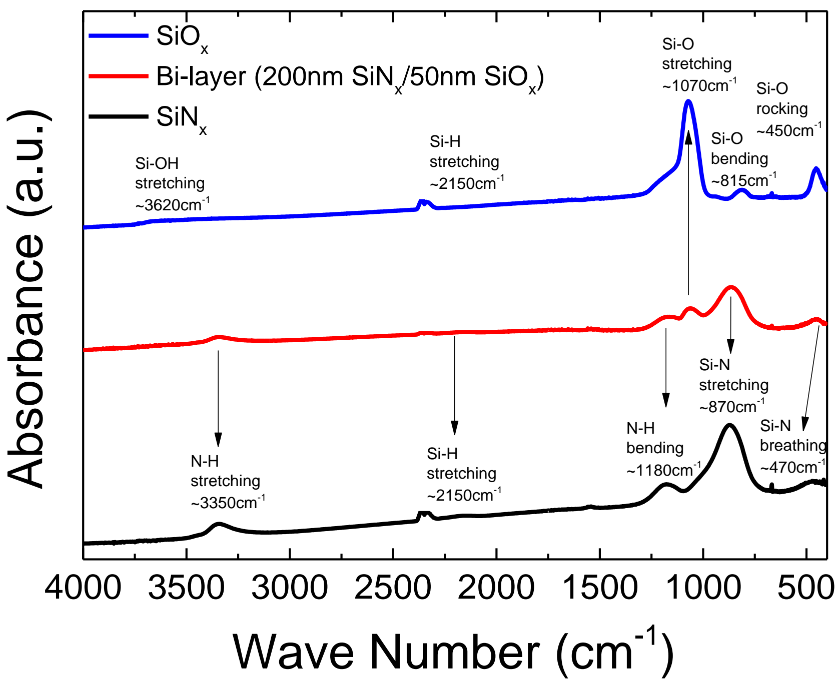

Figure 14 FTIR of PECVD Dielectrics

Analysis of the relative peak heights and positions can also give some characteristics of the film. For the nitride film the bond densities can be determined by Eqn. 13 and 14 which suggest that the stoichiometric ratio in SiN_x is x~1.6 which is rich in nitrogen relative to stoichiometric Si_3N_4 where $x = \frac{4}{3}$ [39]. The large N-H peaks also suggest that the SiN_x film is rich in hydrogen. Similar analysis of the peak heights in the SiOx film shows it is almost stoichiometric having x=1.8 (close to stoichiometric) and comparably low hydrogen content indicated by the small Si-OH peak. The stoichiometric composition is consistent with the refractive indices of these materials presented in Chapter 5.

$$\mathbf{3[N] = [Si - N] + [N - H] + 2[N - H]} \quad \mathbf{(13)}$$

$$\mathbf{4[Si] = [Si - N] + [Si - H] + 2[Si - Si]} \quad \mathbf{(14)}$$

3.1.2 MIS Capacitors

MIS capacitors were fabricated by depositing PECVD dielectrics on top of lightly doped (resistivity $1-5\Omega cm$) p-type <100> crystalline silicon (c-Si) wafers. The capacitors used here are formed from crystalline silicon in a top gate configuration but still provide useful information regarding the quality of the dielectrics which will be used for MoS_2 transistors. Measurement of the dielectric properties is also necessary for calculating transistor mobilities. Aluminum (Al) was deposited on top of the dielectric as the metal and patterned to define the active area of 1.10×10^2 cm^2. For the bi-layer SiN_x/SiO_x, oxide was deposited first (inverted) so that it is at the interface with the semiconductor. All measurements were taken after annealing at 180°C in air for 2 hours.

Capacitance-voltage (CV) measurements were made by superimposing a small high frequency AC voltage on top of a sweeping dc voltage. The capacitance gives the differential charge induced in the semiconductor. The capacitance is measured by the impedance of the capacitor (Z) using an LCR meter using a model where all resistance is assumed to be in series with the capacitor (Eqn. 15).

$$\boldsymbol{Z = R - j\frac{1}{\omega C} = \left|\frac{V}{I}\right| e^{j\theta}} \quad \textbf{(15)}$$

CV curves for the three dielectrics studied are shown in Figure 15 with normalized capacitance values. These curves show behavior expected for a p-type semiconductor at high frequency with accumulation at large negative voltages and depletion and a minimum capacitance in inversion at positive voltages [35]. In the accumulation regime the capacitance is given by the dielectric alone which allows the dielectric constant to be calculated from Eqn. 16 where ε_0 is the permittivity of free space, ε_r is the relative dielectric constant, A is the area defined by the contact metal and t is the dielectric thickness [35]. The calculated dielectric constants are 7.0 and 3.0 for SiN_x and SiO_x respectively, which are slightly less than the stoichiometric values of 7.5 and 3.9 for Si_3N_4 and SiO_2 [35].

The effective dielectric constant of the bi-layer is 6.1 for a total film thickness of 250nm. Considering that the capacitance of the bi-layer is given by the series combination of the two films this should yield a value of 5.9 for 200nm SiN_x and 50nm SiO_x. The total thickness of the

bi-layer was verified to be 250nm but the individual thicknesses were not suggesting the film actually contains more SiN_x and less SiO_x. The observed capacitance of the dual dielectric is consistent by having a SiO_x thickness of 28nm and SiN_x thickness of 222nm. This value is a similar result which is obtained from fitting the reflectance spectra in Chapter 5.

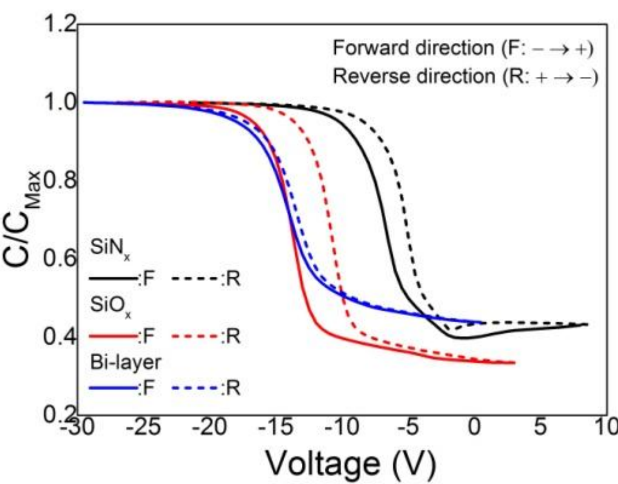

Figure 15 Normalized CV Curves for PECVD Dielectrics

$$\boldsymbol{C_G = \frac{\varepsilon_r \varepsilon_0 A}{t}} \quad \textbf{(16)}$$

The most noticeable features in the C-V curves of the different dielectrics are a shift in the flat band voltage as well as hysteresis depending on the scanning direction. The flat band voltage is determined by reading the voltage at the flat band capacitance given by Eqn. 17 where $\varepsilon_s$the dielectric constant of the semiconductor (11.7 for silicon) is and N_A is the doping level in the semiconductor [35]. Given the resistivity of the wafer the doping level is in the range of 10^{15}-10^{16} cm^{-1} and will be assumed to have a value of $5x10^{15}cm^{-3}$. From this the flat band voltage was determined upon forward and reverse scanning directions as shown in Table 1. The flat band capacitance is not very sensitive to the doping level in this range and so using the approximate doping level is a reasonable assumption.

$$\boldsymbol{C_{FB} = \frac{\varepsilon_r \varepsilon_0 A}{t + \left(\frac{\varepsilon_r}{\varepsilon_s}\right)\sqrt{\left(\frac{k_B T}{e}\right)\left(\frac{\varepsilon_s}{e N_A}\right)}}} \quad \textbf{(17)}$$

Table 1 Flat band Voltage and Hysteresis of MIS Capacitors

	SiN_x	SiO_x	Bi-layer
V_{FB}(Forward)	-8.50 V	-15.00 V	-16.00 V
V_{FB}(Reverse)	-6.50 V	-12.00 V	-15.50 V
ΔV_{FB}	2.00	3.00	0.50

For a MIS capacitor without trap states the flat band voltage is given by the work function difference ϕ_{MS}. For p-type silicon the work function is given by Eqn. 18 which puts the semiconductor work function (ϕ_S) at around 4.9eV [35]. Given that the work function of aluminum is 4.3eV [35] the negative flat band voltage must be caused by positive fixed charge in all dielectrics. Additionally, considering the relative capacitance values of the dielectrics tested the SiO_x has twice the trapped charge of SiN_x. The bi-layer dielectric has a fixed charge similar to SiO_x which is expected since SiO_x is present at the semiconductor interface.

$$\phi_s = \chi + \frac{E_g}{2} + \frac{k_B T}{e} \ln \frac{N_A}{n_i} \quad (18)$$

A particular advantage of the bi-layer dielectric is that it shows comparably low hysteresis ~0.5V compared with ~2V and ~3V for SiN_x and SiO_x respectively. As with the fixed charge this difference cannot be explained by the difference in the capacitance value. Hysteresis in the capacitance voltage curve could be caused by mobile charge in the dielectric or a change in the occupation of interface states. It remains unclear why the bi-layer film shows very low hysteresis despite having SiO_x at the semiconductor interface but this is a desirable property regardless.

Current voltage (I-V) measurements of the MIS capacitors were taken by applying a large voltage between the metal and the semiconductor leading to a DC leakage current. Since the thickness of the films varies the voltage was normalized by the thickness to express the electric field strength along with the current density in Figure 16. The SiO_x film has a much higher leakage current on the order of 10^{-4}A/cm^2 while the leakage of the SiN_x and bi-layer dielectric are similar and on the order of 10^{-7}A/cm^2. This suggests the SiN_x in the bi-layer dielectric is blocking the current flow.

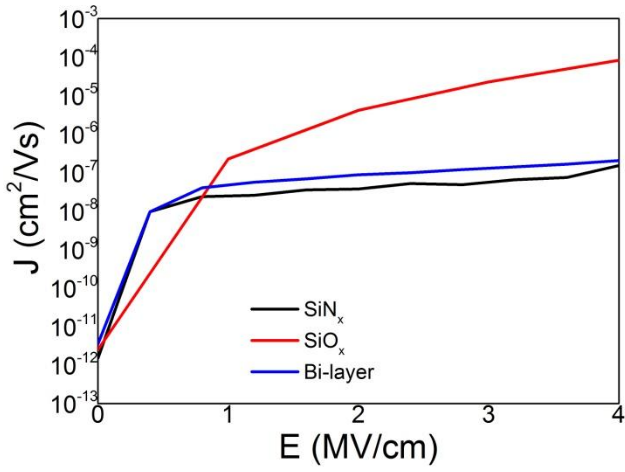

Figure 16 DC Leakage Current of MIS Capacitors

The high leakage current and large hysteresis of SiO_x makes it an unsuitable dielectric for this TFT fabrication. SiN_x has a much larger dielectric constant giving it a higher capacitance for a given film thickness and also has low leakage current. However, both SiN_x and SiO_x show very large hysteresis in the CV curve which is suppressed in the bi-layer dielectric when a thin film of SiO_x is present at the semiconductor interface. For this reason TFT fabrication will proceed using the bi-layer dielectric.

3.2 MoS_2 Thin-Film Transistors

MoS2 thin-film transistors were fabricated in a bottom common gate configuration without any top passivation. The bi-layer dielectric consisting of ~50nm SiO_x on top of ~200nm SiN_x was deposited onto highly doped p-type <100> c-Si wafers using a standard parallel plate 13.56 MHz PECVD system at a maximum deposition temperature of 260°C. MoS_2 flakes were then mechanically exfoliated using the Scotch ® tape method onto the common gate dielectric. At this stage the surface of the dielectric was screened for suitably sized flakes (large enough for photolithography) and then screened for thickness using atomic force microscopy (AFM). Aluminum source drain contacts were chosen due to their low work function (4.3eV) and deposited by DC magnetron sputtering. Patterning of the contacts was done by a standard liftoff process where negative photo resist AZ NLP was spin coated and patterned and developed prior to aluminum deposition and stripped following deposition. The bottom gate contact was created by dipping a small part of the wafer in hydrofluoric acid to remove the dielectric and allow contact to the conductive highly doped c-Si. The overall device structure is shown in Figure 17.

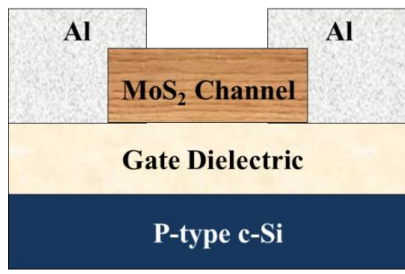

Figure 17 MoS_2 TFT Device Structure

A ~75nm MoS_2 flake was used to fabricate a TFT on bi-layer dielectric and as a reference a ~100nm flake was used to fabricate a TFT on 100nm thermal SiO_2. While thinner MoS_2 layers would be desirable due to decreased interlayer resistance no such flakes were found, in fact most MoS_2 screened by AFM were considerably thicker than those studied here. Optical images of these TFTs are shown in Figure 18 along with AFM measurements confirming the thickness. The bi-layer TFT has a channel length of 7.6μm and width of 3.7μm and the SiO_2 TFT has a length of ~3.5μm and width of ~7.2μm. Raman backscattering spectroscopy was performed using a Renishaw microRamman 1000 spectrometer with a 632nm He-Ne laser as shown in Figure 19. The strong peaks at 383cm^{-1} and 408cm^{-1} are due to the E_{2g} and A_{1g} modes

respectively and show no difference from those of the bulk crystal confirming bulk properties. The raman spectra also confirms that the MoS_2 is the semiconducting 2H polytype.

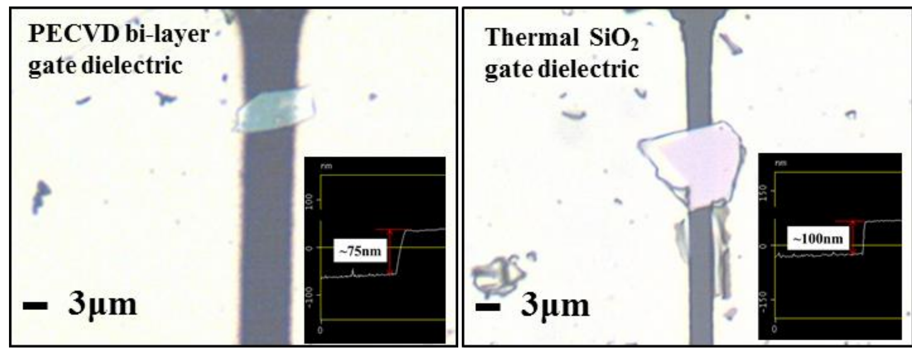

Figure 18 MoS_2 TFT Optical and AFM Micrographs

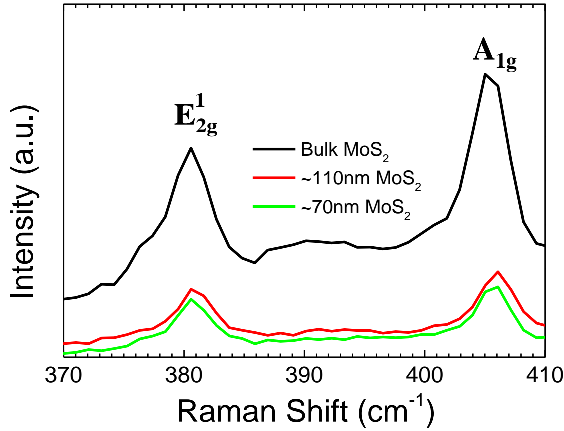

Figure 19 MoS_2 Raman Spectra

Prior to electrical measurements, the TFTs were annealed at 180°C for two hours in order to improve the quality of the Al/MoS_2 electrical contact and the MoS_2/dielectric interface. This is the same procedure used on MIS capacitors before measurement. All measurements were taken in air at room temperature using a Keithley 6430 sub-femtoamp remote source meter at a sweeping speed of 2V/sec. The output curves for these transistors, showing the source-drain current I_{ds} as a function of the drain-source voltage V_{ds} at constant gate source voltage V_{gs} are shown in Figure 20. From the output curves it is apparent that the MoS_2 transistors are operating in the n-type depletion mode because the transistor is normally on at V_{gs}=0V [35]. The

application of positive gate voltages accumulates electrons increasing the drain current and a negative voltage is required to turn the transistor off by depleting the channel.

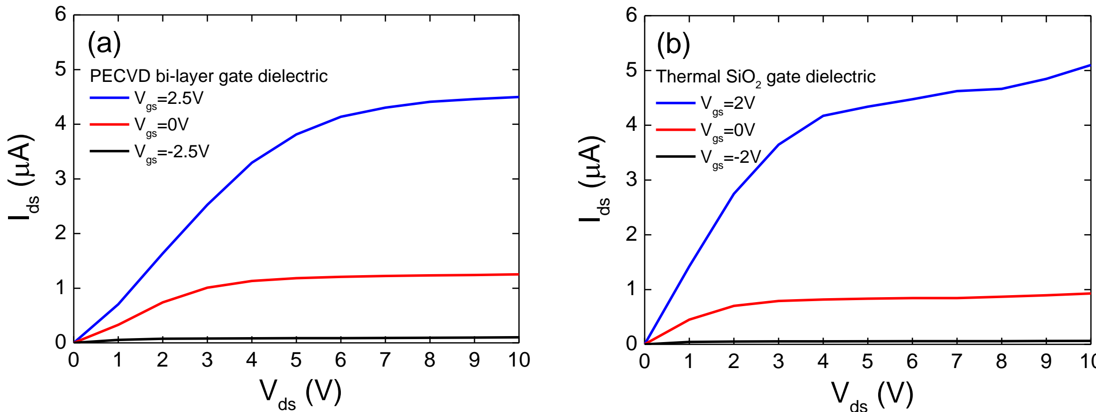

Figure 20 MoS_2 TFT Output Curves

A negative threshold voltage would be expected based on the previous analysis of MIS capacitors made from c-si due to the existence of a large positive trapped charge. The work function of the metal for highly doped p-type silicon is about 5.13eV corresponding to the case where the Fermi level is at the edge of the valence band (any further doping moves the Fermi level very little due to the high density of states in the valence band). Considering multilayer MoS_2 has an electron affinity of 4.0eV and is intrinsically n-type the Fermi level will be somewhere near the conduction band [11]. This would make the work function difference ϕ_{MS} positive. However, a large concentration of trapped charges as already been observed for PECVD dielectrics which serves to negatively shift the flat band voltage. Such positive fixed charge is also expected at the thermal SiO_2 surface [10].

From Figure 20 it can also be seen that I_{ds} appears to increase linearly in the low V_{ds} regime as well as saturation at high V_{ds} due to pinch off of the channel. Good current saturation in MoS_2 transistors is a particular advantage relative to layered graphene which due to the absence of a band gap would become p-type at the drain at high drain bias [4].The use of aluminum ($\phi_M = 4.3eV$) for the source drain contacts gives the appearance of ohmic contacts but they are believed to be Schottky contacts due to the Fermi level pinning effect seen in MoS_2 [11]. Linear behavior is observed due to tunneling through the Schottky Barrier.

The transfer characteristics of the transistors are shown in Figure 21 along with the calculated electron mobility μ_e from Eqn. 11. This confirms the n-type depletion mode behavior and a more negative threshold voltage for the transistor made from PECVD dielectric due to more positive trapped charge. Overall, the TFT fabricated from PECVD gate dielectric shows better electrical performance having a maximum mobility of ~13 $cm^2V^{-1}s^{-1}$,sub theshold swing of 1.05 V/dec and ON/OFF current ratio of ~10^5 compared with 5 $cm^2V^{-1}s^{-1}$, 1.08 V/dec and 10^5 for thermal SiO_2.

A large sub threshold swing can be attributed to interface states at the MoS_2 dielectric interface. Indeed by using eqn.10 neglecting the semiconductor capacitance which is negligible in the deep sub threshold region [12] the trap state density N_{ss} can be calculated to be $2.35\times10^{12}cm^{-2}eV^{-1}$ and $3.9\times10^{12}cm^{-2}eV^{-1}$ for the MoS_2 TFTs employing the PECVD bi-layer and thermal SiO_2 gate dielectrics respectively. This is nearly an order of magnitude higher than reported for other MoS_2 transistors using high-k dielectric [12]. Due to the absence of dangling bonds at the surface of MoS_2 interface traps are expected to be in the dielectric [10].

The maximum mobilities observed here are comparable to other transistors made from MoS_2 on SiO_2 particularly considering the large thickness of MoS_2 used here. In fact, in some cases such thick MoS_2 did not even demonstrate switching behavior [7] It is notable that a μ_e greater than $10cm^2/Vs$ using both a ~75nm thick multi-layered MoS_2 channel and a conventional low-temperature PECVD gate dielectric demonstrates feasibility for large-area electronics application where a-Si:H TFTs (μ_e of $0.5\sim1.0cm^2/Vs$) are used [34]. Reasonably good ON/OFF current ratios of ~10^5 were also observed which is in the suitable range for logic switching applications [4].

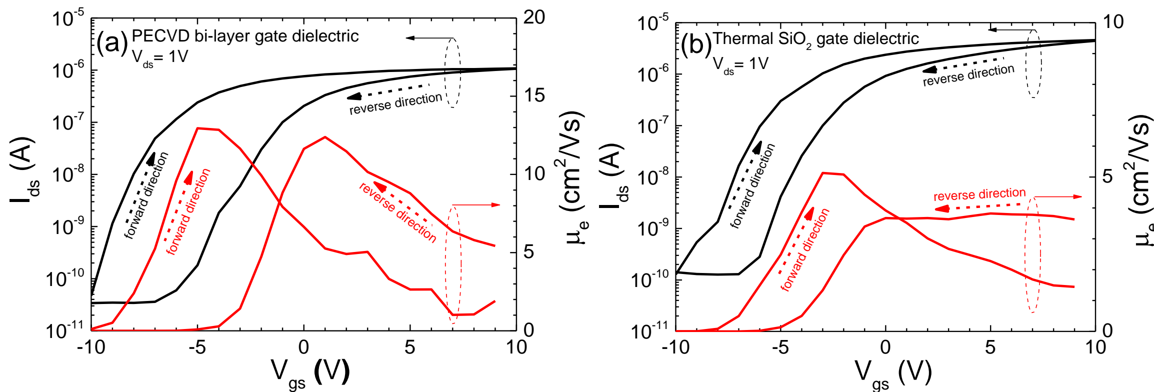

Figure 21 MoS_2 TFT Transfer Curves

Another notable feature of the transfer curves is that they exhibit hysteresis dependent on the sweeping direction of V_{gs}. A positive shift in the threshold voltage V_t of 5V and 3V between the forward and reverse scan direction for PECVD and SiO_2 gate dielectrics, respectively. There is no significant change in the transfer characteristics other than the parallel shifting of the transfer curve which implies that interface states between the semiconductor and dielectric are not significantly being changed over the time scale of this measurement. Additionally, very little hysteresis was seen in CV curves of MIS capacitors using this dielectric. Other MoS_2 transistors have shown to be strongly affected by ambient impurities such as oxygen (O_2) and water (H_2O) on the back channel leading to similar hysteresis effects[40].

A number of potential improvements could be made to the performance of the transistors presented here. Firstly, the contact resistance of the transistor is believed to limit the mobility and so the choice of even lower work function metals like scandium ($\phi_m = 3.5eV$) should result in improved mobility [11]. Since it is believed that hysteresis in these TFTs is being caused by exposure of the back channel to ambient impurities passivation of the TFT with a top dielectric layer should help suppress this effect. Improvements to the recipe used for the dielectric could help reduce the trapped charge and interface states. Finally, and perhaps most importantly the thick flakes used in this study are believed to limit the mobility of the transistors and so thinner multilayer films should show improved performance.

MoS_2 TFTs using PECVD dielectrics show good performance similar to MoS_2 transistors made from thermal SiO_2. High mobilities are observed for MoS_2 relative to a-Si:H and it is expected

that further improvement can be made by using thinner flakes of MoS_2 [10], [11]. In order to aid in the identification of thinner flakes an optical model built based on the theory of optical contrast developed for graphene [23]–[26] will be built and applied to MoS_2 on PECVD dielectrics. These models will be used to make color charts for MoS_2 on PECVD dielectrics, to optimize the dielectric thickness to improve the visibility of MoS_2 and to use color images in order to calculate the thickness of MoS_2. Describing colors requires an understanding of the CIE color system which will be presented in Chapter 4.

Chapter 4 Calculating Color

4.1 CIE Color System

All modern standards of color reproduction are fundamentally based on the perception of color by the human eye. The human eye contains two types of light sensitive cells: rods and cones. Rods are responsible for colorless low light vision and do not play a role in the perception of color [41]. Cones cells are photosensitive and come in three types β, γ and ρ which detect different ranges of light roughly corresponding to blue, green, and red respectively [41]. Experiments on the eye have revealed the spectral sensitivity of cone cells as shown in Figure 22. An important consequence of the cone cells is that color is not an intrinsic property but the perception of a reflected or emitted power distribution by the human eye [42]. As such any stimulus which produces the same response in each of the three types of cone cells cannot be distinguished no matter how different the stimulus is [42].

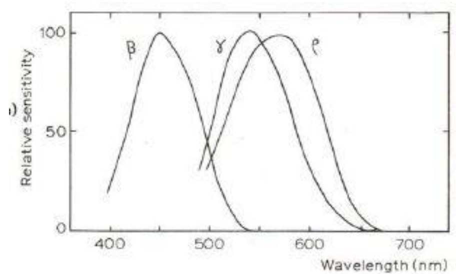

Figure 22 Spectral Sensitivity of Cone Cells [41]

Since the eye has three different types of cone cells any color stimulus can be represented by the combination of three reference primaries. In 1931 the International Commission on Illumination (CIE) established the 1931 CIE color space by defining the reference primaries of the space to be monochromatic light at wavelengths of 700nm (red), 546.1nm (green) and 435.8nm (blue) [42]. By performing experiments on human subjects whereby arbitrary colors were recreated using the defined reference primaries the color matching functions (CMFs) $\bar{r}(\lambda)$ $\bar{g}(\lambda)$ and $\bar{b}(\lambda)$ were obtained as shown in Figure 23 [42]. These CMFs are known as the standard oberserver and give the relative amounts of the reference primaries needed to obtain the same response as the eyes cone cells [42].

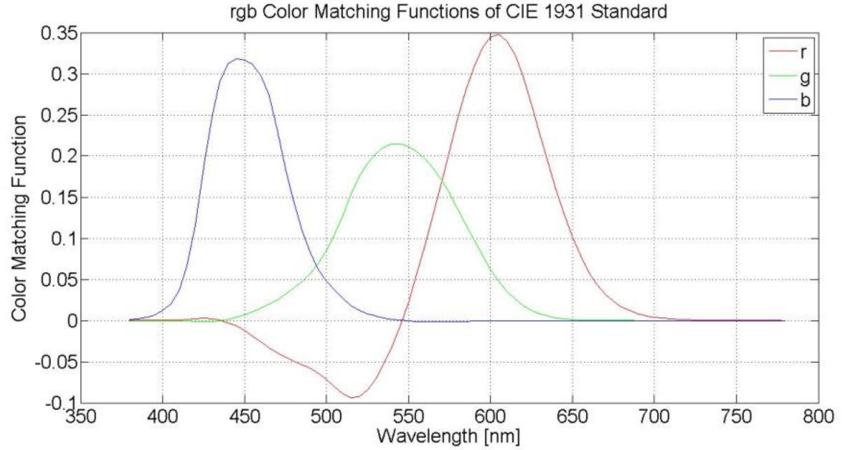

Figure 23 CIE 1931 Standard Observer [43]

4.1.1 XYZ Color Space

The CMFs of the standard observer have negative lobes as a result of the spectral overlap of cone cells. At the time these standards were created the negative lobes in the CMFs made calculations difficult due to the unavailability of computers [42]. For this reason a set of imaginary primaries XYZ were created with corresponding CMFs $\bar{x}(\lambda), \bar{y}(\lambda), \bar{z}(\lambda)$ as shown in Figure 23. The XYZ color space is defined based on the requirement that there are no negative lobes, an equienergy stimulus would produce equal tristimulus values and the Y value represents the luminance of the stimulus [42]. The XYZ color space is a device independent space, it does not consider the influence of a particular display or camera, only the perception of light by the eye.

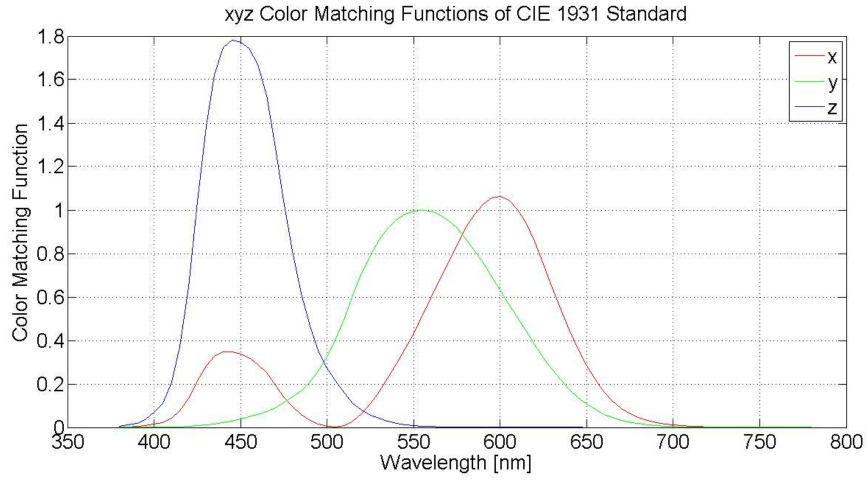

Figure 24 Color Matching Functions of XYZ [43]

Any unknown color stimulus [C] can be represented by a three dimensional vector which can be obtained by vector addition of the reference primaries [X], [Y] and [Z] weighted by the tristimulus values X, Y and Z as described in Eqn. 19 [42]. The tristimulus values can be obtained for reflecting objects using Eqn. 20-23 where $R(\lambda)$is the spectral reflectance, $S(\lambda)$is the relative spectral power distribution(SPD) of the Illuminant, $\bar{x}(\lambda), \bar{y}(\lambda), \bar{z}(\lambda)$are the CMFs and k is a constant chosen so that Y gives a value of 100 when $R = 1$ [42]. For modeling the optical contrast of MoS_2 on dielectric films $R(\lambda)$ will be calculated using a thin film optics approach presented in Chapter 5. The spectral power distribution $S(\lambda)$ is given by the light source used to view the thin films.

$$[\boldsymbol{C}] = \boldsymbol{X}[\boldsymbol{X}] + \boldsymbol{Y}[\boldsymbol{Y}] + \boldsymbol{Z}[\boldsymbol{Z}] \quad \textbf{(19)}$$

$$\boldsymbol{X} = \boldsymbol{k} \int_{380nm}^{780nm} \boldsymbol{R}(\boldsymbol{\lambda}) \boldsymbol{S}(\boldsymbol{\lambda}) \bar{\boldsymbol{x}}(\boldsymbol{\lambda}) \boldsymbol{d\lambda} \quad \textbf{(20)}$$

$$\boldsymbol{Y} = \boldsymbol{k} \int_{380nm}^{780nm} \boldsymbol{R}(\boldsymbol{\lambda}) \boldsymbol{S}(\boldsymbol{\lambda}) \bar{\boldsymbol{y}}(\boldsymbol{\lambda}) \boldsymbol{d\lambda} \quad \textbf{(21)}$$

$$\boldsymbol{Z} = \boldsymbol{k} \int_{380nm}^{780nm} \boldsymbol{R}(\boldsymbol{\lambda}) \boldsymbol{S}(\boldsymbol{\lambda}) \bar{\boldsymbol{z}}(\boldsymbol{\lambda}) \boldsymbol{d\lambda} \quad \textbf{(22)}$$

$$\boldsymbol{k} = \frac{\mathbf{100}}{\int_{380nm}^{780nm} \boldsymbol{S}(\boldsymbol{\lambda}) \bar{\boldsymbol{y}}(\boldsymbol{\lambda}) \boldsymbol{d\lambda}} \quad \textbf{(23)}$$

4.1.2 xyY Color Space

While a color stimulus can be fully described by the tristimulus values X Y and Z it is difficult to imagine what a particular color will look like given these values. This has led to the definition of chromaticity coordinates x, y and z defined by Eqn. 24-26 [42]. The chromaticity coordinates are then related to each other by Eqn. 27 so that the chromaticity can be described by only x and y. This often displayed using a xy chromaticity diagram as shown in Figure 25. The specification of color using xy chromaticity coordinates results in a loss of information regarding light intensity [42]. This can be fully specified using the Y tristimulus value and thus defines the xyY color system [42]. Another notable feature of this chromaticity diagram is that when three reference primaries are used in a device dependent color space (such as RGB) only colors within the triangle formed by the chromaticity coordinates of these three primaries can be recreated [42]. As such not all colors seen by the eye can be recreated on a display.

$$x = \frac{X}{X+Y+Z} \quad (24)$$

$$y = \frac{Y}{X+Y+Z} \quad (25)$$

$$z = \frac{Z}{X+Y+Z} \quad (26)$$

$$x + y + z = 1 \quad (27)$$

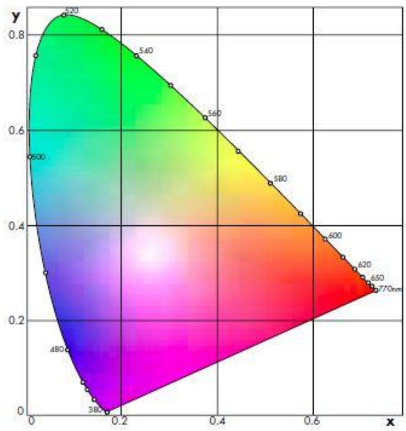

Figure 25 xy Chromaticity Diagram [44]

4.1.3 CIE Lab Color Space

The Lab color space was created to address a problem with xyY color space, namely that it does not represent gradients in color uniformly [44]. The minimum distance between disenable colors is lower at the bottom of Figure 24 and higher at the top. The lab color space seeks to remedy this problem by distorting the xyY color space. Lab values are determined from XYZ values using Eqn. 28-30, here X_N, Y_N, Z_N are the tristimulus values of the reference white (the light source used to calculate XYZ) [44]. In this system L is a measure of the brightness while a* and b* determine the color as illustrated in Figure 26. The advantage of the Lab system is that it can be used to define the color difference ΔE_{ab} defined by Eqn. 31 where $\Delta L, \Delta a^{*}, \Delta b^{*}$ are the differences in the L a* and b* values .The color difference ΔE_{ab} defines how “far” two colors

are from one another [44]. The ΔE_{ab} value is important in this work because it will be used as a quantitative measure of how well MoS_2 can be distinguished from the substrate.

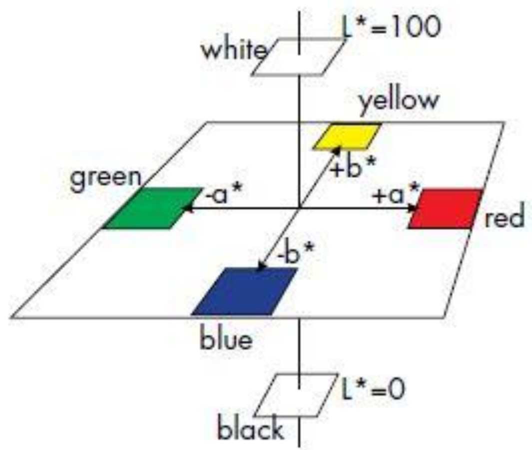

Figure 26 Lab Color Space [44]

$$\boldsymbol{L = 116\left(\frac{Y}{Y_N}\right)^{\frac{1}{3}} - 16} \quad \textbf{(28)}$$

$$\boldsymbol{a^* = 500\left[\left(\frac{X}{X_N}\right)^{\frac{1}{3}} - \left(\frac{Y}{Y_N}\right)^{\frac{1}{3}}\right]} \quad \textbf{(29)}$$

$$\boldsymbol{b^* = 200\left[\left(\frac{Y}{Y_N}\right)^{\frac{1}{3}} - \left(\frac{Z}{Z_N}\right)^{\frac{1}{3}}\right]} \quad \textbf{(30)}$$

$$\boldsymbol{\Delta E_{ab} = \sqrt{\Delta L + \Delta a^* + \Delta b^*}} \quad \textbf{(31)}$$

4.1.4 Standard Illuminants

The tristimulus values obtained from Eqn. 20-22 are dependent on the light source under which the reflecting object is viewed, for this reason several standard illuminants are defined by the CIE [42]. Often the temperature or a correlated color temperature of an illuminant is given which is based on the theory of blackbody radiation. The spectral radiance of a blackbody $B_\lambda$is given by Plank's law in Eqn. 32, here c is the speed of light, h is Plank's constant,k_B is boltzmann's constant, T is temperature and λ is the wavelength [42].

$$B_{\lambda}(\lambda, T) = \frac{2hc^2}{\lambda^5} \frac{1}{e^{\frac{hc}{\lambda k_B T}} - 1} \quad (32)$$

The most important standard illuminants discussed here are A, D65 and E which are shown in Figure 27. Illuminant A is made to approximate a tungsten filament bulb and represents a blackbody at 2856K. Illuminant D65 is made to approximate conditions of daylight and has a correlated color temperature of 6500K. Finally, Illuminant E is an equienergy spectrum representing the ideal of white light. The spectral power distribution of standard illuminants are scaled to be 100 at 560nm, this makes no difference in the calculation of tristimulus values because of the constant k (Eqn. 23).

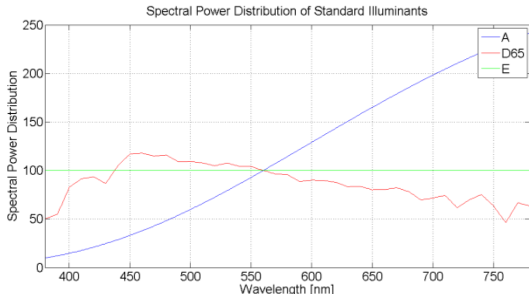

Figure 27 CIE Standard Illuminants [43]

The reference white of the light source (X_N, Y_N, Z_N) is often needed for calculations in device dependent color spaces (RGB) or for the calculation of Lab values. The reference white of a light source is given by the tristimulus values for a perfectly reflecting surface $R(\lambda) = 1$. The reference whites of the common standard illuminants are calculated in Table 2 and are consistent with tabulated values [43].

Table 2 Reference White of Standard Illuminants

Light Source	X_N	Y_N	Z_N
A	109.847	100	35.5928

D65	95.0419	100	108.844
E	99.9977	100	99.986

4.2 Calculating RGB Values

4.2.1 RGB Standards

Displays have three different sub-pixels which are perceived the eye as being red, green, and blue. While the CIE standards are based off of emission from monochromatic sources the pixels in a display are not monochromatic and not consistent from device to device, hence forming a device dependent color space [45]. Additionally, the intensity of light delivered from the sub-pixels is calibrated such that equal values of the R, G, and B tristimulus values will be perceived as white defined by a particular standard. Also, since the RGB values are stored digitally the number of bits which are allocated will also limit the range of colors that can be displayed. An interpretation of images taken by the microscope camera or displaying color charts requires conversion into an RGB color space.

In 1996 HP and Microsoft developed sRGB as a standard color space for the internet. By having various devices such as televisions, scanners, cameras and printers all sRGB compliant the need for computationally intensive color transformations becomes unnecessary. Images taken by a camera in JPEG or TIFF format as well as colors displayed on a computer monitor are based on the sRGB standard. Note that since printing is based on the CYMK color space printed copies of this thesis may not retain color accuracy.

RGB tristimulus values are obtained from XYZ tristimulus values using a transformation matrix M_t as shown in Eqn. 33[46]. The transformation matrix is generated from Eqn. 34-36 using the chromaticity coordinates of the display sub-pixels (x_r,y_r) (x_g,y_g) and (x_b,y_b) as well as the reference white of the light source (X_N,$Y_{N,}$,Z_N) [46].

$$\begin{bmatrix} \boldsymbol{r} \\ \boldsymbol{g} \\ \boldsymbol{b} \end{bmatrix} = [\boldsymbol{M_T}] \begin{bmatrix} \boldsymbol{X} \\ \boldsymbol{Y} \\ \boldsymbol{Z} \end{bmatrix} \quad \textbf{(32)}$$

$$[\boldsymbol{M_T}] = \begin{bmatrix} S_rX_r & S_gX_g & S_bX_b \\ S_rY_r & S_gY_g & S_bY_b \\ S_rZ_r & S_gZ_g & S_bZ_b \end{bmatrix} \quad \textbf{(33)}$$

Where $\boldsymbol{X_l = \frac{x_l}{y_l}}$ $\boldsymbol{Y_l = 1}$ $\boldsymbol{Z_l = \frac{1-x_l-y_l}{y_l}}$ and l=r, g, or b **(34)**

$$\begin{bmatrix} S_r \\ S_g \\ S_b \end{bmatrix} = \begin{bmatrix} X_r & X_g & X_b \\ Y_r & Y_g & Y_b \\ Z_r & Z_g & Z_b \end{bmatrix}^{-1} \begin{bmatrix} X_N \\ Y_N \\ Z_N \end{bmatrix} \quad \textbf{(35)}$$

For the sRGB standard standard phosphor values of x_r=0.64 ,y_r=0.33, x_g =0.3 , y_g=0.6 x_b =0.15 and y_b=0.06 are used with D65 being adopted as the reference white source. The matrix for converting XYZ values to RGB values is then given by Eqn. 37 and is consistent with the result found in [45].

$$[\boldsymbol{M_T}] = \begin{bmatrix} 3.2404 & -1.5371 & -0.4985 \\ -0.9692 & 1.8759 & 0.0416 \\ 0.0557 & -0.2041 & 1.0577 \end{bmatrix} \quad \textbf{(36)}$$

4.2.2 Gamma Correction

The rgb values obtained from the transformation matrix [M_T] will be [0,1]. These values are linear and are often made non-linear through the use of the following gamma function. The gamma function is linear at low light levels to reduce noise and exponential for brighter signals which increases the range (dim colors are made brighter and bright color made dimmer) [45]This procedure mimics the response of the cone cells in the eye are also non-linear except at low light conditions where rod cells are responsible for gathering light.

Gamma correction converts an image luminance $L \in \{r, g, b\}$ into a voltage $V \in \{R, G, B\}$ for the monitor [45]. This is done by linearly scaling values below a transition value and raising values above the threshold to an exponent of γ with an offset as in Eqn.38 [45]. For sRGB the values of these constants are given in the Table 3 below. Following gamma correction any values which are outside the range of [0,1] are clipped to either zero or 1. In the sRGB standard the

RGB values are each represented by 8bit integers which range from [0,255]. Therefore, the result is multiplied by 255 and rounded to the nearest integer.

$$\boldsymbol{V} = \begin{cases} (\mathbf{1} + \boldsymbol{offset})\boldsymbol{L}^{\gamma} - \boldsymbol{offset}, & \mathbf{1} \geq \boldsymbol{L} \geq \boldsymbol{transition} \\ \boldsymbol{slope} \times \boldsymbol{L}, & \boldsymbol{transition} \geq \boldsymbol{L} \geq \mathbf{0} \end{cases} \quad \textbf{(37)}$$

Table 3 sRGB Gamma Parameters [45]

Offset	0.055
γ	0.42
Transition	0.003
Slope	12.92

4.3 Summary

The RGB values for a thin-film of known reflectance can be calculated by first finding the XYZ tristimulus values from Eqn 20-23. XYZ values are then converted to rgb values using Eqn.33 then scaled by the gamma function from Eqn.38. In order to calculate the reflectance spectra $R(\lambda)$ the transfer matrix method will be used as discussed in Chapter 4. All calculations discussed in this chapter have been implemented into MATLAB scripts for further use in Chapter 5.

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Chapter 5 Calculating Reflectance using Transfer Matrix Technique

5.1 Theoretical Background

The solution for the reflectance, transmittance or absorbance of a stack of thin films is derived by considering plane wave solutions to Maxwell's equations incident from a non absorbing medium onto an interface as shown in Figure 28 [47]. By imposing the condition that the electric and magnetic fields of the wave must be continuous across each interface a generalized matrix form of Fresnel's equations can be derived which can be used to solve for an arbitrary stack of thin films [47]. Here the films are assumed to be thin enough that incident and reflected light is coherent and able to interfere. While non-matrix forms of these equations exist they depend on the number of films present and become increasingly complicated as the number of films is increased.

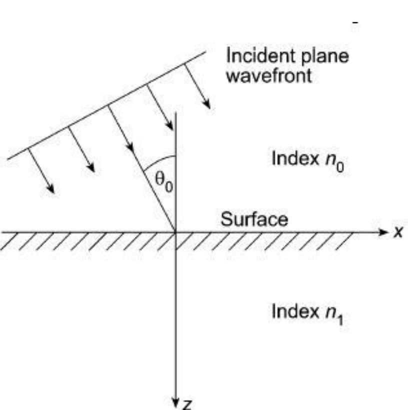

Figure 28 Plane Wave Incident onto Dielectric Interface [47]

The transfer matrix equation is given by Eqn. 39 where B and C are the electric and magnetic field intensities incident on the film stack normalized by the field intensities at the substrate boundary. The calculation is performed by taking the product of q matrices where q is the number of films in the multilayer stack. This product starts from r=1 which is the film closest to the incident medium (air). The index m denotes the substrate which is assumed to be semi-infinite (no light reflects from the back surface).

$$\begin{bmatrix} B \\ C \end{bmatrix} = \left\{ \prod_{r=1}^{q} \begin{bmatrix} \cos \delta_r & i \sin \delta_r / \eta_r \\ i\eta_r \sin \delta_r & \cos \delta_r \end{bmatrix} \right\} \begin{bmatrix} 1 \\ \eta_m \end{bmatrix} \quad \textbf{(38)}$$

Here δ_r (Eqn.40) is the phase factor or phase shift of a wave as it travels through film r and η_r (Eqn. 41 and 42) is the tilted optical admittance of film r, which gives the ratio of field components tangential to a boundary. The tilted optical admittance differs if the electric field is normal to the plane of incidence (s-polarized) or the magnetic field is normal to the plane of incidence (p-polarized). ϒ is the admittance of free space (Eqn.48) and is given by a constant defined by the speed of light c_0 and the vacuum permeability μ_0.

$$\delta_r = \frac{2\pi N_r d_r \cos \theta_r}{\lambda} \quad \textbf{(39)}$$

$$\eta_{rs} = \Upsilon N_r \cos \theta_r \quad \text{(s-polarized)} \quad \textbf{(40)}$$

$$\eta_{rp} = \Upsilon N_r / \cos \theta_r \quad \text{(p-polarized)} \quad \textbf{(41)}$$

$$\Upsilon = \frac{1}{\mu_0 c_0} \quad \textbf{(42)}$$

N_r (Eqn.44) represents the complex refractive index made up of refractive index n which describes the speed of the wave in the medium relative to vacuum and the extinction coefficient k which describes the decay in amplitude of the wave as it propagates through absorbing media. The thickness of each film is given by d_r and light is incident into the film at an angle θ_r relative to the surface normal. For non-normal incidence the angle θ_r into each film can be calculated from Snell's law (Eqn.45).

$$N_r = n_r - ik_r \quad \textbf{(43)}$$

$$N_0 \sin \theta_0 = N_r \sin \theta_r = N_m \sin \theta_m \quad \textbf{(44)}$$

From B and C the reflectance (R), transmittance (T) and absorbance (A) of the film stack can be calculated from Eqn. 46-48 where $\eta_0$is the tilted optical admittance of the incident medium (air). Since the tilted optical admittances depend on the polarization state of the light for the case of random polarization both polarization states must be calculated separately then averaged.

$$\boldsymbol{R} = \left(\frac{\eta_0 B - C}{\eta_0 B + C}\right)\left(\frac{\eta_0 B - C}{\eta_0 B + C}\right)^* \quad \textbf{(45)}$$

$$\boldsymbol{T} = \frac{4\eta_0 Re(\eta_m)}{(\eta_0 B + C)(\eta_0 B + C)^*} \quad \textbf{(46)}$$

$$\boldsymbol{A} = \frac{4\eta_0 Re(BC^* - \eta_m)}{(\eta_0 B + C)(\eta_0 B + C)^*} \quad \textbf{(47)}$$

5.1.1 Implementation into MATLAB

The transfer matrix model was implemented into MATLAB in order to be combined with the scripts written in Chapter 3. The script calculates the reflectance transmittance and absorbance spectra of an arbitrary stack of thin films for randomly polarized light over a specified wavelength range. The incident angle, thickness of each film as well as the refractive index of each film is given as inputs. The correct implementation of this model will be verified in section 5.2.

5.2 Theoretical Verification

5.2.1 Non Absorbing Media at Normal Incidence

The reflectance of light incident from air at normal incidence onto a non-absorbing film of refractive index n_1 coated onto a non-absorbing substrate of refractive index n_m is expected to vary periodically with the film thickness d_r [48]. Light is reflected at both the air/film and film/substrate interfaces and depending on the relative phase shift of these two waves will interfere constructively or destructively [48].

According to Fresnel's equations the light reflected at the air/film interface is undergoing external reflection and will experience a phase shift of π [48]. The remainder of the light is transmitted where it travels to the film/substrate interface and experiences another reflection. The phase shift experienced at the film/substrate interface depends on the relative values of the refractive indices. Provided that $n_1 < n_m$ (external reflection) the phase shift is again π [Wash]. This reflected light then travels back to the film/substrate interface and interferes with the light which was initially reflected.

The interfering light is traveling a distance of twice the film thickness or $2d_f$. In traveling this distance it experiences a phase shift of $\Delta\phi = \left(\frac{2\pi n}{\lambda}\right)(2d_f)$ [48]. When the film thickness is one quarter wave optical thickness ($QWOT = \frac{\lambda}{4n}$) there is an additional phase shift of π traveling through the film. Therefore, reflectance will be a minimum at one QWOT due to constructive interference and will oscillate between minima at odd integer multiples of QWOT and maxima at even integer multiples of the QWOT [48].

The maximum value of reflectance (R_0)will be given by the reflectance of the bare substrate from Eqn. 49 [48]. The minimum value will depend on the refractive index of the film but will be exactly zero when equal to zero when $n_f = \sqrt{n_0 n_m}$ [48]. Figure 29 shows the reflectance output of the transfer matrix model at normal incidence with the substrate index of 1.52 and the film index of $\sqrt{1.52}$ as a function of the film thickness in units of QWOT, the figure displays the expected behavior and oscillates between the predicted maxima and minima values.

$$\boldsymbol{R_0} = \left(\frac{\boldsymbol{n_0 - n_m}}{\boldsymbol{n_0 + n_m}}\right)^2 \quad \textbf{(48)}$$

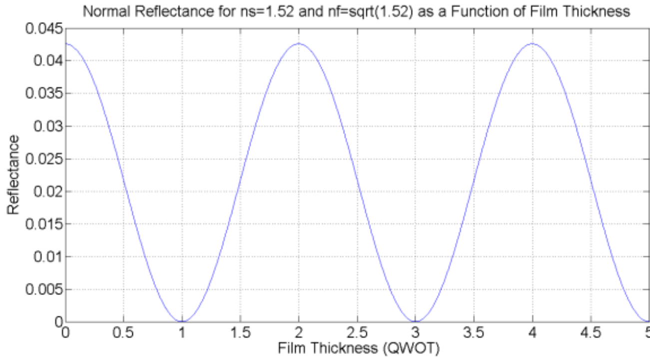

Figure 29 Calculated Reflectance at Normal Incidence

5.2.2 Absorbing Media at Normal Incidence

For an absorbing substrate the extreme points no longer occur at integer values of the QWOT. This is because the phase shift upon reflection at the film substrate interface is now given by Eqn. 50 and so the resulting interference pattern is shifted by an optical thickness of $\frac{\phi}{\pi}$ [48]. Additionally, when the dielectric has a thickness of one half wave optical thickness (HWOT) the phase shift is such that all light passes through it and the reflectance is just that of the metal

substrate given by Eqn. 51 [48]. Figure 30 demonstrates all of the predicted phenomena suggesting that the model is working correctly for absorbing media.

$$\boldsymbol{\phi} = \tan^{-1}\left(\frac{2n_1k_m}{n_1^2 - n_m^2 - k_m^2}\right) \quad (49)$$

$$\boldsymbol{R} = \frac{(n_0 - n_1)^2 + k_1^2}{(n_0 + n_1)^2 + k_1^2} \quad (50)$$

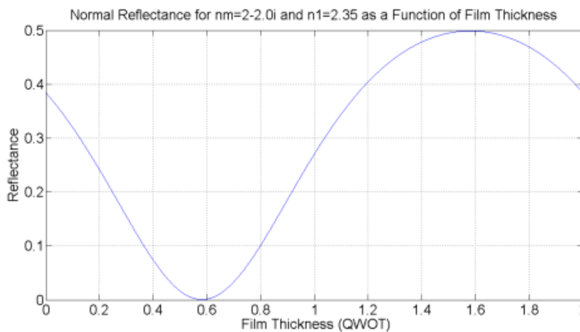

Figure 30 Calculated Reflectance at Normal Incidence for Absorbing Film

5.2.3 Non-Normal Incidence

When examining the effect of changing incident angle on reflectance there are two special angles for which total internal reflection and polarization are observed. When light is moving from a more optically dense medium (n_0) to a less optically dense medium (n_1) at an angle which exceeds the critical angle θ_c (Eqn. 52) total internal reflection is observed where no light will be transmitted through the interface [Wash]. At non-normal incidence the behavior of waves with s and p polarization will differ with the reflectance of p-polarized light going to zero at Brewster's angle θ_p given Eqn. 53 [48]. Figure 31 shows the reflectance as a function of incidence angle for light incident from a medium with refractive index of 1.5 into a medium with refractive index of 1. It can be seen that the reflectance goes to one at the critical angle and goes to zero for p-polarized light at the Brewster's angle as expected.

$$\boldsymbol{\theta_c} = \sin^{-1}\left(\frac{n_0}{n_1}\right) \quad (51)$$

$$\theta_p = \tan^{-1}\left(\frac{n_1}{n_0}\right) \quad (52)$$

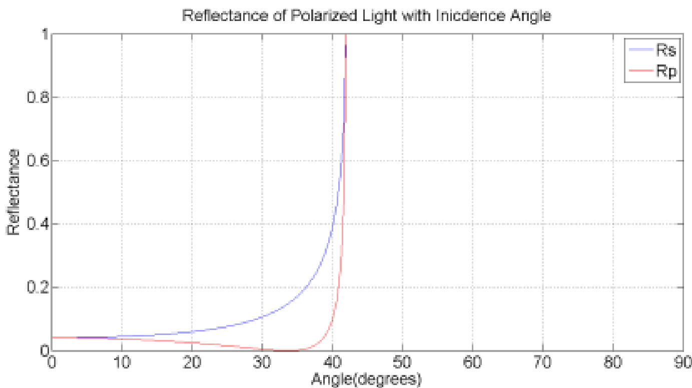

Figure 31 Reflectance of Polarized Light at Non-Normal Incidence

5.3 Experimental Verification

The output reflectance of the transfer matrix model can be directly verified by measuring the reflectance using UV-VIS spectroscopy. Typically UV-VIS is used to measure transmittance or absorbance but using an integrating sphere attachment reflectance can be measured. The transfer matrix model does not consider scattering phenomena and so all reflectance should be specular (the incident and reflected angles being equal). In the specular reflectance configuration of the instrument used the light source is placed at an angle of 9° relative to the surface normal with a detector at an angle of 9° on the opposite side of the substrate. Calibration is performed using a mirror which is assumed to have 100% reflectance giving the magnitude of the incident light. The goal is to accurately calculate the reflectance of the bi-layer, SiN_x, SiO_x and thermal SiO_2 dielectrics used as dielectrics for TFT fabrication in Chapter 3.

5.3.1 Refractive Indices

Thermal SiO_2 or PECVD SiO_x and SiN_x were deposited onto c-Si wafers and the reflectance measured by UV-Vis spectroscopy. A thick film of sputtered aluminum was used as the mirror for the baseline measurement. The refractive indices of silicon and thermal silicon dioxide can be found in [46] and are given in Figure 32 and 33 respectively.

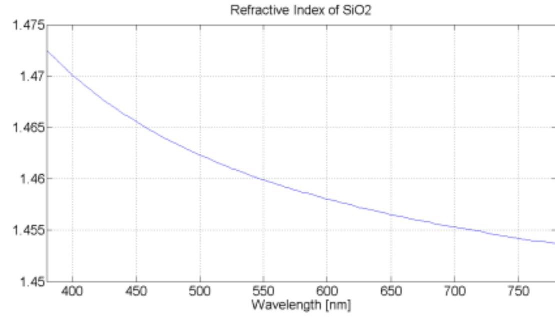

Figure 32 Refractive Index of Thermal SiO2 [46]

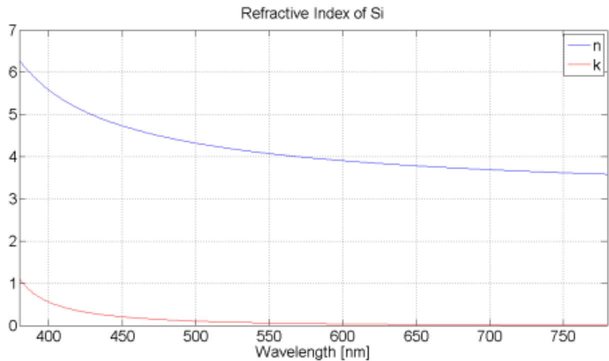

Figure 33 Refractive Index of c-Si [46]

The refractive indices of SiN_x and SiO_x were determined using spectroscopic ellispsometry. Two films of ~300nm of SiO_x and SiN_x were deposited onto silicon and measured to obtain the wavelength dependent refractive indices shown in Figures 34 and 35. The refractive indices found here are consistent with the stoichiometric composition found by FTIR. The refractive index of SiO_x is very close to SiO_2 indicating it is close to stoichiometric while refractive index of SiN_x matches an empirical relation for nitrogen rich films [39]. The refractive index of SiN_x varies significantly with wavelength which makes the measurement of refractive index necessary to obtain accurate calculations.

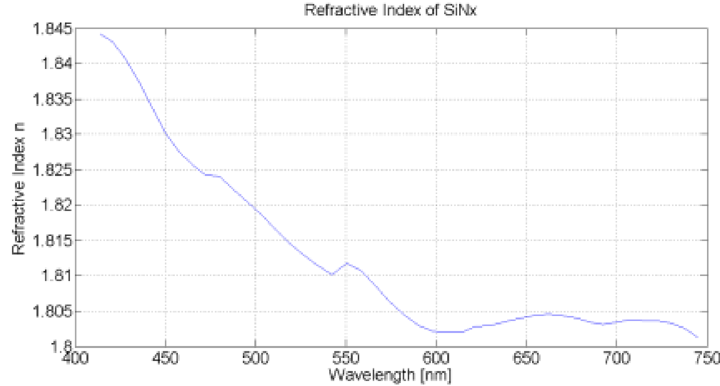

Figure 34 Measured Refractive Index of PECVD SiNx

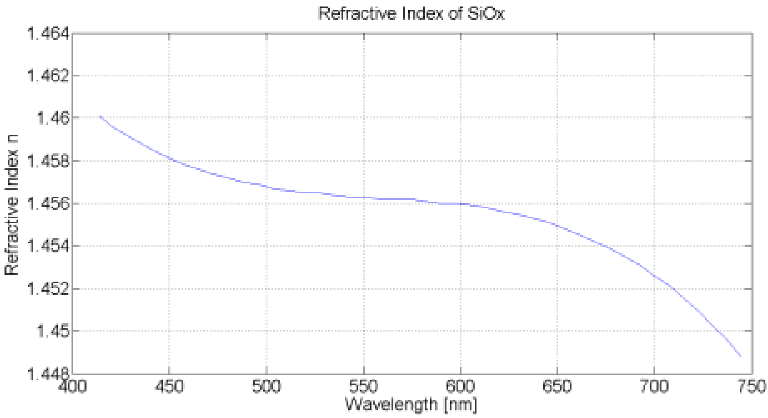

Figure 35 Measured Refractive Index of PECVD SiOx

5.3.2 Reflectance Measurements

A comparison of the calculated reflectance of 100nm SiO2 on silicon using the refractive indices is compared to the reflectance measured by UV-Vis in Figure 36. This deviation is caused by the use of an aluminum mirror for the baseline measurement. Using the refractive index of aluminum [49] in Figure 37 the reflectance of the aluminum mirror is calculated in Figure 38. In order to take the finite reflectance of the mirror into account the UV-VIS measurements should be multiplied by the aluminum reflectance at each wavelength. By adjusting the UV-VIS reflectance measurements and allowing the thickness of the SiO2 to vary slightly the fit from Figure 39 is obtained which closely matches the experimental data.

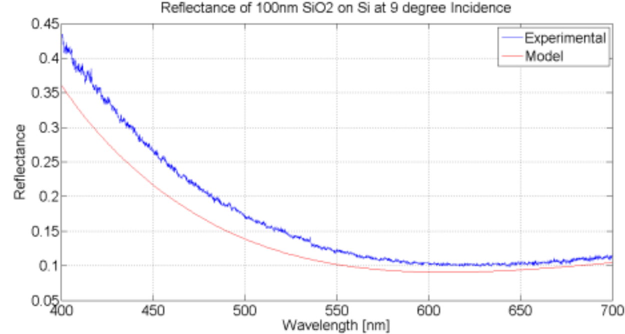

Figure 36 Calculated and Experimental Reflectance of 100nm SiO_2

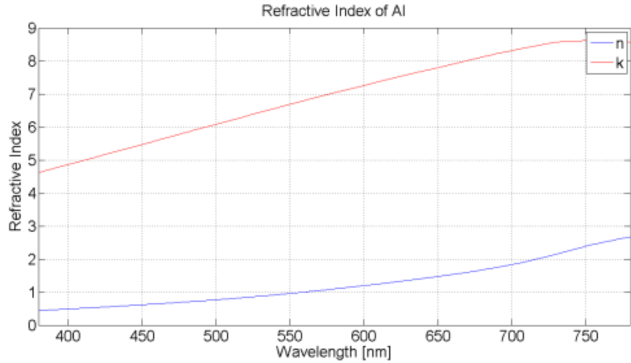

Figure 37 Refractive Index of Aluminum [49]

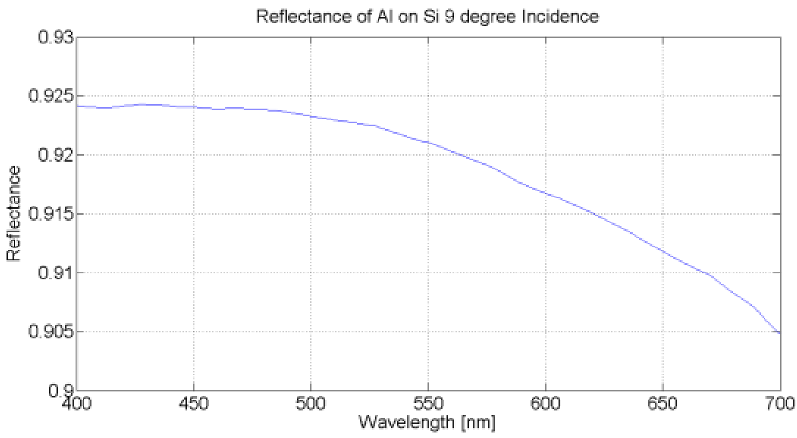

Figure 38 Calculated Reflectance of Aluminum Mirror

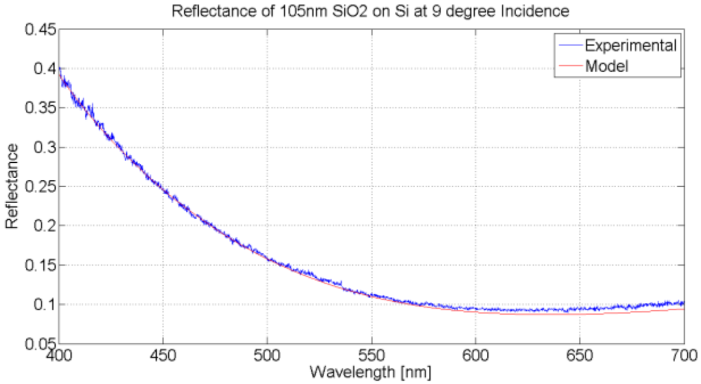

Figure 39 Adjusted Calculated and Experimental Reflectance of SiO_2

UV-Vis reflectance measurements were also taken for the PECVD deposited SiN_x and SiO_x previously measured by spectroscopic ellispsometry. By scaling the UV-Vis reflectance by the reflectance of the aluminum mirror and allowing the thicknesses in the calculation to be a fitting parameter Figures 40 and 41were obtained which again show a very good fit between the experimental and calculated result.

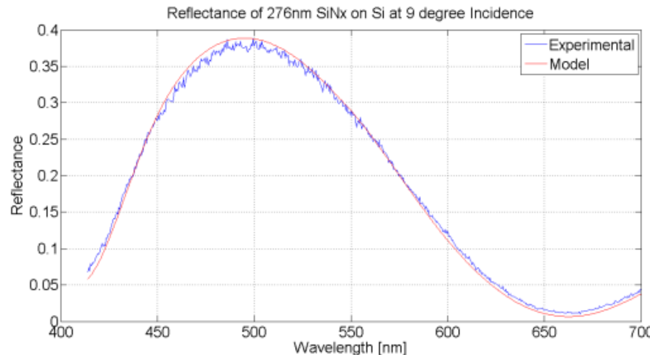

Figure 40 Adjusted Calculated and Experimental Reflectance of SiN_x

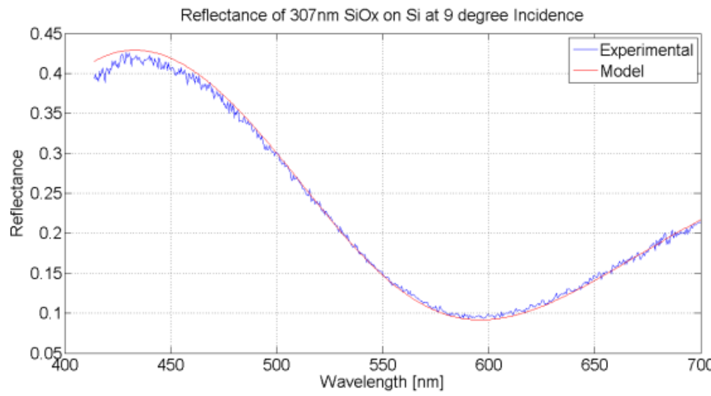

Figure 41 Adjusted Calculated and Experimental Reflectance of SiO_x

As discussed in Chapter 3 a bi-layer of SiNx with a thin film of SiOx produced the best results when used as a gate electrode for MIS capacitors and MoS_2 TFTs. This bi-layer was believed to contain ~200nm of SiNx with ~50nm of SiOx based on the deposition time. After scaling the UV-Vis reflectance by the mirror reflectance and allowing the thicknesses to vary the fit from Figure 42 was obtained. The resulting fit of film thicknesses showed an increased thickness of SiN_x and decreased thickness of SiO_x from what was expected. This is reasonable because the thickness is based on growth rate measurements assumed to be linear which may not be particularly during the early stages of film nucleation and growth. Additionally, this result is consistent with the analysis of the dielectric constant of the bi-layer dielectric presented in Chapter 3. This is a reasonably good fit but results in a small deviation from the calculated result at around 550nm.

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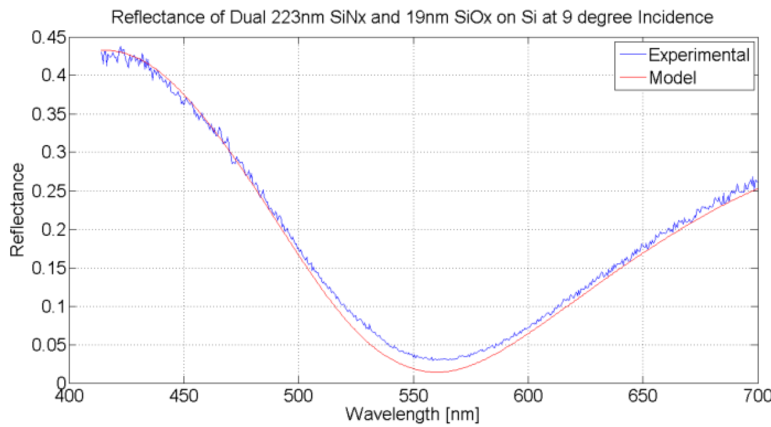

Figure 42 Adjusted Calculated and Experimental Reflectance of SiN_x/SiO_x

The transfer matrix model has been successfully implemented in MATLAB. Combined with the measured refractive indices of PECVD SiN_x and SiO_x this has been used to successfully predict the reflectance spectra of the thermal SiO_2 and bi-layer dielectrics used for TFT fabrication in Chapter 3. It is clear that deposition times are not a reliable way of determining film thicknesses and since the dielectric thickness is a sensitive parameter in the color of dielectric films it is recommended that any different dielectric recipes be measured by UV-VIS and the thicknesses fit using the procedure done above. This guarantees the correct reflectance spectra prior to MoS_2 being placed on the surface. With the accuracy of this model demonstrated it will now be used along with the CIE color calculations presented in Chapter 4 to calculate the color of MoS_2 on SiO_2, SiN_x, SiO_x, and bi-layer SiN_x/SiO_x dielectrics.

Chapter 6 Color and Contrast of MoS_2 on PECVD Dielectrics

6.1 Consideration of Optical System

The microscope used for identification of MoS_2 flakes is a Reichert Polylite 88 microscope with reflected light microscope with a 100W halogen bulb used as the light source. Standard illuminant A is designed to approximate the power distribution of such a halogen bulb. All images were acquired using a MOTICAM CMOS 2.0MP camera in JPEG or TIFF format which follows the sRGB standard.

One factor that needs to be considered is the optical system which due to the numerical aperture (NA) of the lens causes light to arrive at the substrate surface at a range of incident angles. The NA defines the maximum angle θ_{max} light will hit the substrate through Eqn. 54 where n_0 is the refractive index of the incident medium (air) [24]. Since the light source is not coherent the reflected light from different angles will not interfere [46]. Assuming that the light intensity at different angles is given by a Gaussian distribution the reflectance can be calculated at each angle and averaged over the range of angles as in Eqn. 55 where $\phi(x, \mu, \sigma)$ is a Gaussian distribution with a mean μ and standard deviation of σ [46]. The effect of NA is demonstrated by calculating the reflectance of the bi-layer dielectric at normal incidence and comparing it to the reflectance at 100X magnification (NA=0.7) in Figure 43. For lower magnifications such as 20X (NA=0.4) the difference in reflectance is almost negligible. However, at 100X magnification there is a slight deviation in the reflectance spectra which may need to be accounted for although this too appears negligible. Since reflectance averaging significantly increases computation time it is neglected in the proceeding sections.

$$\boldsymbol{NA = n_0 \sin \theta_{max}} \quad \textbf{(53)}$$

$$\boldsymbol{R(\lambda) = \int_{-\theta_{max}}^{\theta_{max}} R(\lambda, \theta_i)\, \phi\left(\theta_i, 0, \frac{\theta_{max}}{3}\right) d\theta_i} \quad \textbf{(54)}$$

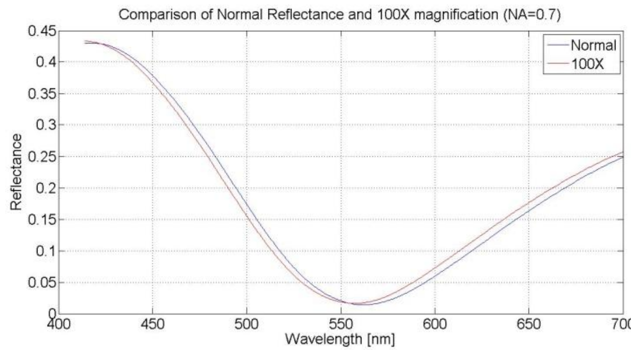

Figure 43 Comparison of Reflectance Calculation with Numerical Aperture

6.2 Color of Dielectric Films

The RGB color values of SiO_2 and bi-layer SiN_x/SiO_x will now be calculated from the reflectance model of Chapter 5 and color model of Chapter 4. Table 4 gives the calculated colors of these films for both illuminant A and D65 without considering the lens numerical aperture. The colors seen for illuminant D65 closely match the visual appearance of these films viewed under office lighting. However, when viewed under the microscope the halogen light source significantly distorts their appearance.

Table 4 Calculated Dielectric RGB Values with Standard Illuminants

Dielectric on Silicon	Illuminant	R	G	B	Preview
105nm SiO2	D65	78	94	139	
	A	109	87	75	
19nm SiOx / 223nm SiNx	D65	79	54	167	
	A	112	48	95	
276nm SiNx	D65	0	154	142	
	A	86	139	77	
307nm SiOx	D65	62	117	175	
	A	111	105	98	

Images of the dielectric films were taken with the attached camera at a magnification of 20X (where the effect of NA is not significant) without the use of a white balance filter. The average pixel intensities from these images rounded to the nearest integer and are shown in Table 5 below. It is clear that the imaging settings are affecting the measured result but adjusting them to match Table 5 is not reasonable as it would involve considerable trial and error. Instead the calculation settings were adjusted to be consistent with the RGB values captured by the camera. The calculation settings that were adjusted are: the spectral power distribution of the light source, the constant k(Eqn. 23) and γ (Eqn.38). The spectral power distribution was adjusted by forcing the function to remain as a blackbody spectrum according to Eqn.32 but allowing the temperature to change. The value of k affects the image brightness while γ(gamma) combines the effects of camera settings such as gain and exposure time. Film thicknesses were also allowed to vary within a small range to reflect thickness non-uniformity across the substrate or variations across different depositions.

Table 5 RGB Values of Microscope Images for Dielectric Films

Dielectric on Silicon	R	G	B	Preview
105nm SiO2	64	52	33	
19nm SiOx/223nm SiNx	68	38	34	
276nm SiNx	70	109	52	
307nm SiOx	73	75	48	

The results of this fit are shown in Table 6 and are very close to the measured values with the exception of the green channel of the bi-layer dielectric. It is believed that the calculation underestimates the green value of the bi-layer dielectric due to the deviation in calculated and measured reflectance in Figure 42 at ~550nm. This is particularly significantly since the photosensitivity to green light is centered on this wavelength as seen in Figure 23. The resulting fitting parameters do not differ significantly from one another. While the effect of k on the RGB values is linear this is not true for temperature and gamma. The effects of changing temperature and gamma within this range are shown in Figure 44 and 45 respectively. This procedure can be

used to insure consistency in imaging and calculation settings if accuracy in RGB values is required.

Table 6 Calculated RGB Using Fitting Parameters

Film	Temperature(K)	k	Gamma	Thickness(nm)	R	G	B	Preview
SiO2	2650	171	0.56	113	62	47	32	
Bi-layer	2400	175	0.55	20/223	69	14	35	
SiNx	2600	199	0.44	276	73	110	51	
SiOx	2500	186	0.52	318	71	73	46	

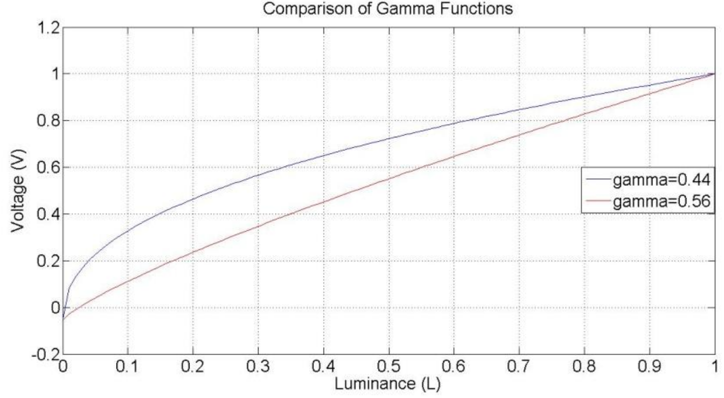

Figure 44 Gamma Functions

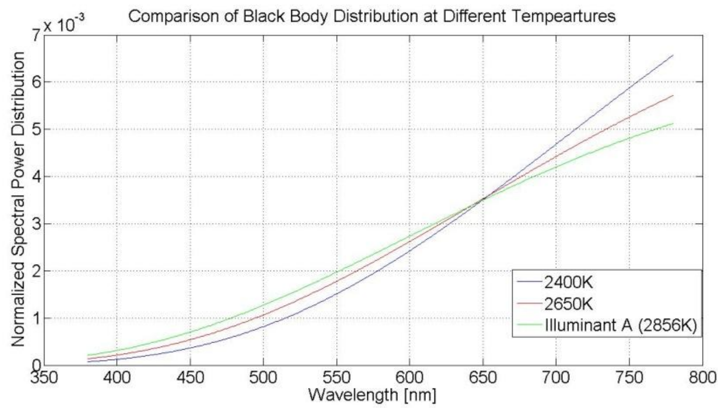

Figure 45 Blackbody Spectral Distribution at different Temperatures

6.2.1 Refractive Index of MoS_2

Using the models presented so far color chart will be created for MoS_2 on the dielectric films used to make TFTs in Chapter 3. In order to calculate the reflectance of MoS_2 the refractive index is also required. Unlike with PECVD dielectrics spectroscopic ellispsometry cannot be used for this purpose because the flakes are much smaller than the spot size used by the light source in the instrument. The bulk crystal used for exfoliation also cannot be used because it is not sufficiently flat to reflect light specularly. Using contrast measurements and a series of filters the refractive index of MoS_2 as a function of wavelength was obtained from [50] as shown in Figure 46.

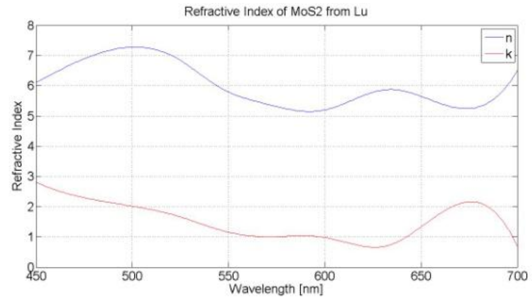

Figure 46 Refractive Index of MoS_2 [50]

6.3 Color Charts for MoS_2

Now that the refractive index of MoS_2 is known color charts can be generated in order to visually identify flakes of different thicknesses based on color. Since auto white balanced was performed on the images of Figure 17 the color charts for 100nm SiO_2 and bi-layer SiN_x/SiO_x were calculated and shown in Figure 47 and 48 for D65 lighting. Note that auto white balance on the camera attempts to remove dependence on the light source which is why D65 is used (the reference white for sRGB). The colors here closely match the optical images of Figure 17 for the thicknesses measured by AFM (75nm on bi-layer and 100nm on SiO_2).

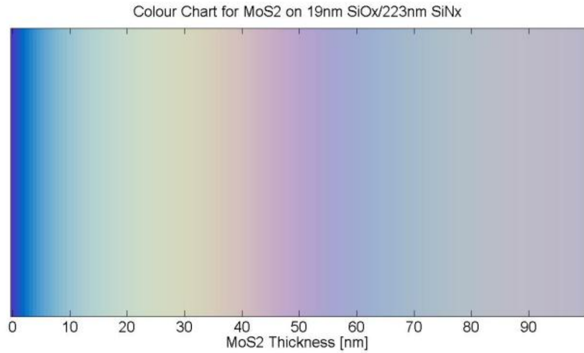

Figure 47 Bi-Layer Color Chart for MoS_2 under D65 Lighting

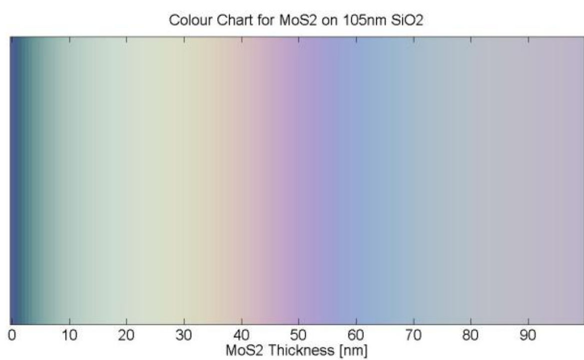

Figure 48 SiO_2 Color Chart for MoS_2 under D65 Lighting

A notable feature of these color charts is that for thick MoS_2 films the color has very little dependence on the substrate. This effect is observed because as the MoS_2 thickness is increased very little light reaches the dielectric interface and so the reflection off the MoS_2 surface governs the color. This can be seen by comparing the reflectance of MoS_2 75nm for both substrates in

Figure 49 which shows only a small difference which is not significant enough to change the perceived color. However, the color of MoS_2 flakes under a thickness of approximately 10nm remains dependent on the substrate as can be seen from the Figure 47 and 48.

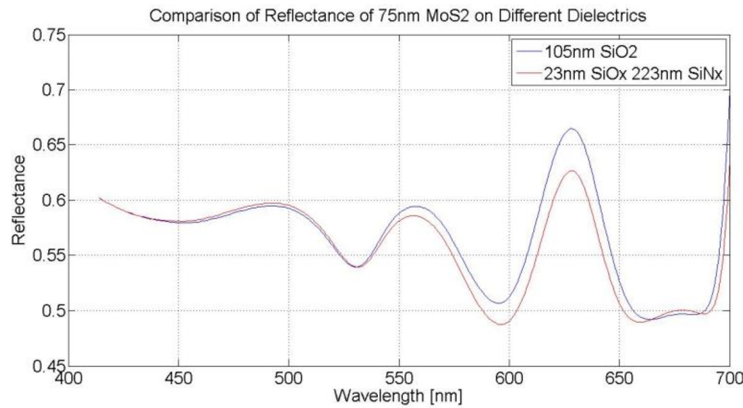

Figure 49 Reflectance of 65nm MoS2 on Different Substrates

When MoS_2 is viewed under halogen light as would be observed under the eyepiece of the microscope without the use of color balance the observed colors are significantly distorted. Using the parameters from Table 6 a color chart for MoS_2 on the bi-layer dielectric was created. This color chart is shown side by side with a microscope image taken of exfoliated MoS_2 flakes in Figure 50. This result closely matches the range of colors seen on MoS_2 flakes from a microscope image.

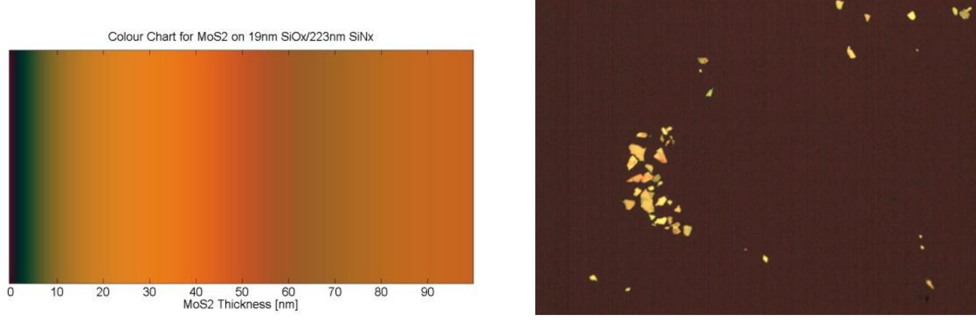

Figure 50 MoS_2 Color Chart and Microscope Image with Halogen Illuminant

6.4 Dielectric Optimization and MoS_2 Thickness Measurement

Several studies on the optical contrast of MoS_2 have been done but most have focused on contrast at monochromatic wavelengths through illumination under band pass filters [29], [30], [32], [33]. Only two studies have considered illumination of MoS_2 under a broadband light source but have either neglected optical calculations [31] or have drastically oversimplified the problem by neglecting to consider the light source and simply averaging over approximate wavelength ranges corresponding to red, green and blue light [27].

Towards the goal of identifying thin layers of MoS_2 the dielectric thicknesses will be optimized to maximize the contrast of monolayer MoS_2 for microscope visibility. A non destructive method of measuring the thickness of MoS_2 using images taken from the camera will also be presented which can be applied in the future to allow devices to be fabricated without the use of AFM to verify the thickness.

6.4.1 Optimizing Visibility using ΔE_{ab}

The goal of this section will be to use the lab color difference ΔE_{ab} to identify the optimal substrate thicknesses for distinguishing ultrathin MoS_2. This will be done by maximizing the color difference ΔE_{ab} between the substrate and a MoS_2 monolayer (0.65nm) for both standard illuminant A and D65. A monolayer was chosen as the target thickness since these are the most difficult to detect but this procedure could be adapted for any MoS_2 thickness provided the thickness is not too large that the color becomes independent of the dielectric thickness. Table 7 shows the ΔE_{ab} color difference between the dielectrics analyzed so far and a monolayer of MoS_2. The contrast difference between monolayer MoS_2 and 276nm SiN_x substrate illustrates well how a poor choice of dielectric makes MoS_2 almost indistinguishable.

Table 7 ΔE_{ab} Color Difference between Dielectrics and Monolayer MoS_2

Dielectric on Silicon	Illuminant	Substrate	MoS2	ΔE_{ab}
105nm SiO2	D65			13.0196
	A			11.2946
19nm SiOx / 223nm SiNx	D65			16.9283
	A			21.0458
276nm SiNx	D65			9.8108
	A			9.8191
307nm SiOx	D65			12.3441
	A			17.6637

The optimal dielectric thicknesses for visibility were found by calculating ΔE_{ab} over a range of thicknesses to find the maximum values shown in Table 8. This analysis was done for both A and D65 light sources because ΔE_{ab} was found to depend on the light source in Table 7. However, the optimal dielectric thickness was found to be independent of the light source. In viewing Table 8 it should be noted that the preview colors are given in sRGB color space and many are outside the range of colors that can be expressed, the real contrast will be even higher when viewed under a microscope.

Table 8 Optimal Dielectric Thicknesses for MoS_2 Visibility

Dielectric on Silicon	Illuminant	Substrate	MoS2	ΔE_{ab}
225nm SiO2	D65			31.1
	A			31.9
75nm SiOx / 240nm SiNx	D65			33.5
	A			34.5
403nm SiNx	D65			21.0
	A			19.3
225nm SiOx	D65			31.1
	A			32.0

A notable feature of Table 8 is that the optimal thickness for SiO_2 and SiO_x is the same; this can be attributed to having very similar refractive indices. Also, it is found that SiN_x has lower contrast than SiO_2/SiO_x which can be attributed to its higher refractive index. This is to be expected since MoS_2 has a large refractive index and so a low index substrate will result in a large difference in surface reflectance (Eqn. 49). The use of a bi-layer film results in a higher contrast than either SiN_x or SiO_x alone. An additional benefit of such a bi-layer film is contrast is far less sensitive to the choice of thickness values. Figure 51 shows ΔE_{ab} as a function of film thickness for SiO_2 under D65 lighting, if the thickness varies from the optimal value of 225nm the contrast drops considerably. However, for a bi-layer of SiOx/SiN_x the contrast remains large over a wide range of thicknesses as shown in Figure 52. This is a considerable advantage for PECVD deposited films which often show thickness deviations across the substrate or from deposition to deposition. This result suggests that a film of 75nm SiO_x and 240nm SiN_x is the optimal substrate for future work in the fabrication of MoS_2 TFTs.

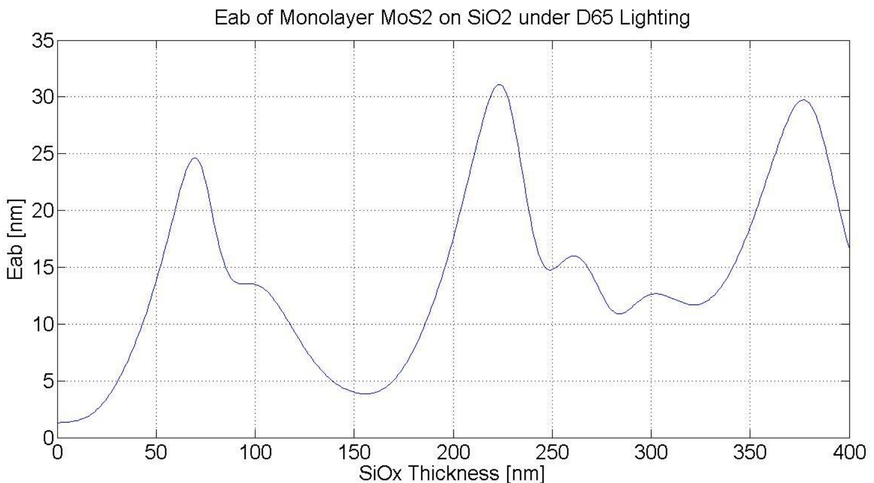

Figure 51 ΔE_{ab} for Varying SiO_2 Thickness

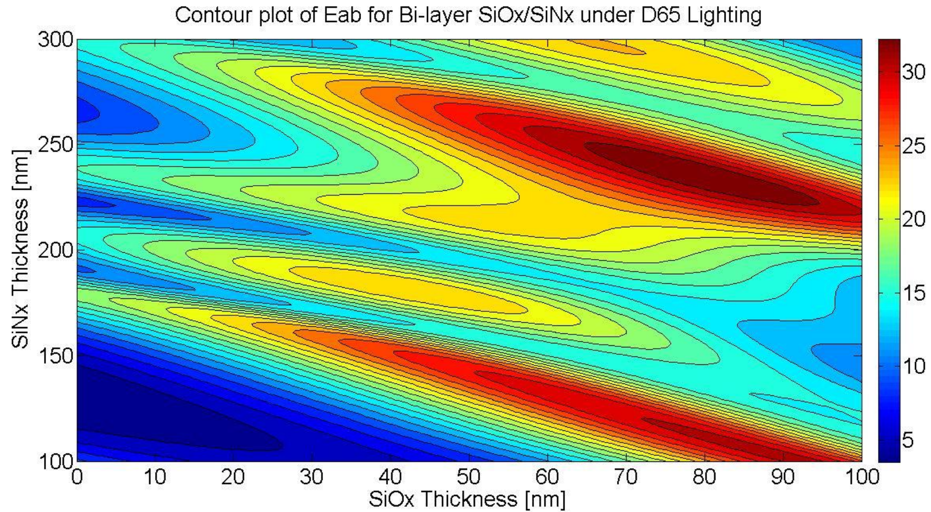

Figure 52 ΔE_{ab} of bi-layer SiN_x /SiO_x for Varying Thicknesses

6.4.2 Thickness Measurement Using Optical Microscopy

While optimizing the dielectric thickness for contrast allows monolayers or bi-layers of MoS_2 to be easily distinguished from the substrate it remains difficult to distinguish MoS_2 flakes from each other to qualitatively determine the thickness based on the visible color alone. A less qualitative way of judging the thickness can be implemented by taking an image and using the magnitude of the RGB values. By measuring the thickness of MoS_2 through analyzing the image the time consuming process of measuring by AFM can be eliminated. Here the contrasts C_R, C_G and C_B can be defined as the normalized difference (Eqn. 56-58) between (R,G,B) and (R_0,G_0,B_0) which are the RGB components of the MoS_2 and dielectric respectively. Images can be taken with the microscope camera and split into separate RGB channels to obtain the required values which can then be compared to those calculated using the models already presented.

$$C_R = \frac{R - R_0}{R_0} \quad (55)$$

$$C_G = \frac{G - G_0}{G_0} \quad (56)$$

$$C_B = \frac{B - B_0}{B_0} \quad (57)$$

An advantage of normalization by the substrate values is that the result is independent of the auto white balance settings used in the capture of the image as well as the scaling constant k used to calculate XYZ. However, other image settings such as the spectral distribution of the light source and the gamma will impact the calculated values of contrast. Gamma is particularly significant because its effect changes with the magnitude of the value being scaled. While gamma can be turned off in the image settings there is no guarantee that gamma is not being executed within the camera hardware. For this reason it is recommended that the fitting of the calculation parameters be adjusted to meet the color of the substrate as was done in Table 6. The calculated contrast for the 19nm/223nm bilayer with optimized calculation parameters is shown in Figure 53 below. Here the blue channel does not provide much useful information but the red and green channels are found to monotonically increase for thicknesses below about 20nm. However, above 20nm the contrast begins to oscillate with increasing MoS_2 thickness so that thickness cannot be identified ambiguously from a single channel alone making this method best applied to thinner MoS_2.

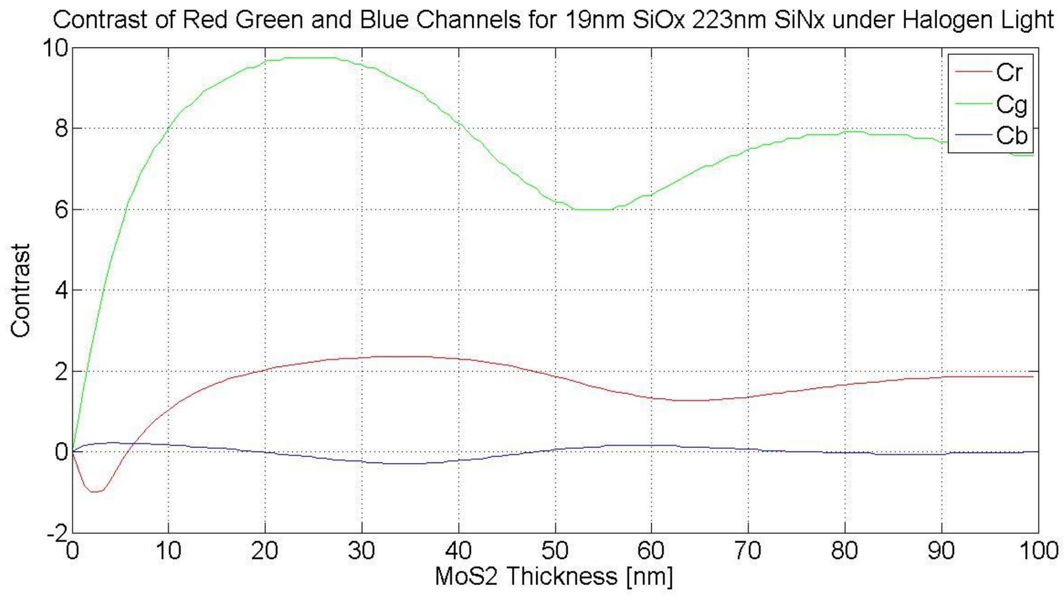

Figure 53 Calculated Contrast for Bi-Layer Film

6.5 Conclusions and Next Steps

MoS_2 should be mechanically exfoliated onto the optimal bi-layer dielectric presented in Table 8. This will allow for thin MoS_2 flakes <20nm to easily be distinguished from the substrate. In order to verify the accuracy of using optical contrast model as a measurement technique microscope images should be captured and the thickness of the thin MoS_2 flakes verified by AFM. This may require adjustment of the calculation of imaging parameters to get a consistent result. Once this has been achieved this technique should be applied to the fabrication of TFTs to further study the promise of using MoS_2 for large area electronics. Additionally, the models presented here could be applied to other substrates to maximize contrast or measure thickness such as glass or flexible PET which are more commonly used in the field of large area electronics.

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