A Hardware/Software Fuel Gauge Analog-to-Digital Converter Solution for Mobile Electronics Applications

by

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Abstract

Power consumption is one of the key considerations in any mobile electronics design. As technology roadmaps advance in the mobile and wearable markets, there will be an evident push for lower power consumption in terms of chipsets and applications. With this in mind, battery technology will have to keep up with higher energy densities, lower cost, and all the while, also reducing the overall dimensions as size is one of the other major constraints in most mobile/wearable designs. Emphasizing a well thought-out power system design is necessary to optimize battery usage. This is especially important as companies creating battery-powered devices will continue to want to maximize the usage of the battery to give its users a high quality user experience.

An important aspect of power system design is the fuel gauge algorithm. A fuel gauge is a measurement and reporting tool that gives a user the ability to understand the status and capacity of the battery. This thesis delivers a full solution which includes a Successive Approximation Register Analog-to-Digital Converter to provide the necessary hardware to collect the measurements of the battery and a fuel gauge algorithm which implements the design in software to report the battery life to the user.

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Chapter 1

Introduction

Power consumption is one of the key considerations in any electronics design. As technology roadmaps advance in the mobile and wearable markets, there will be an evident push for lower power consumption in terms of chipsets and applications. This will be especially true for higher intensity use-case applications like gaming and video streaming / calling. With this in mind, battery technology will have to keep up with higher energy densities, lower cost, and all the while, also reducing the overall dimensions as size is one of the other major constraints in most mobile/wearable designs. Emphasizing a well thought-out power system design is common practice for electronics designers. This will be especially important as companies creating battery-powered devices will continue to want to maximize the usage of the battery to give its users an optimal usage profile and high quality user experience. An important aspect of power system design is the fuel gauge algorithm.

Essentially, a fuel gauge is a tool for reporting capacity to a user. In terms of a battery powered system, it would track and report the battery capacity. Tracking and reporting the battery capacity can be done in hardware (HW) and software (SW), and the following thesis will attempt to define the requirements of this type of design and look at providing possible solutions. HW refers to the physical components that are required to measure variables in order to understand the status of the battery. SW refers to the algorithm which manipulates many variables, both measured and stored values, in order to produce an accurate and useful capacity to report to the user. The combination of these two elements can create a successful fuel gauge. Figure 1.1 is a system block diagram that shows the fuel gauge components and how they fit into an overall system. In summary, the system will operate as is defined by the use case and application and therefore will create a load to be supplied by the battery. The fuel gauge HW will then utilize a combination of Analog-to-Digital Converters (ADCs) to measure the voltage and current. The measurements will be then provided to the SW algorithm for computational analysis. Values will be extracted and reported to the user through some form of display. Full details surrounding the operation and algorithms used by fuel gauges will be discussed in the sections to follow.

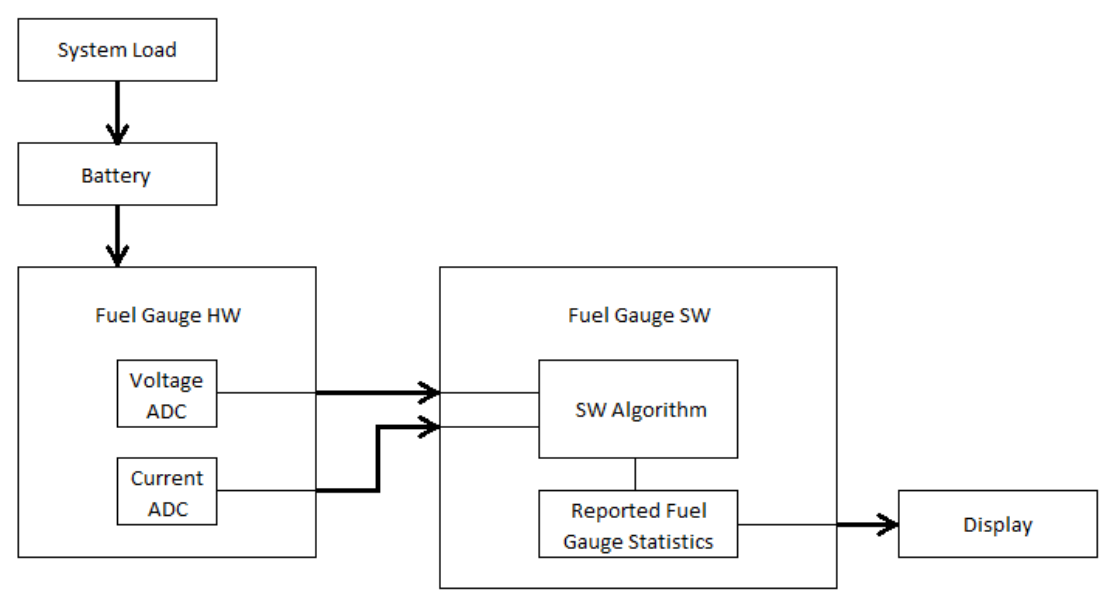

Figure 1.1: Overall Fuel Gauge System Block Diagram

1.1 Thesis Outline

As a general outline for this thesis, the breakdown is as follows. Chapter 2 will give a general overview for fuel gauges, which will include basic concepts, typical HW solutions, and the required SW algorithm variables. It will also cover the specifics of battery models, SW algorithm concepts and simulations. Chapter 3 will discuss Successive Approximation Register ADCs (SAR ADC) in terms of their general concepts and more detailed metrics. Chapter 4 will also delve into the schematic and layout of a 12-bit SAR ADC design and all of the considerations required to create an effective design. Chapter 5 will cover the simulation and testing involved including the schematic and layout simulations as well as the verification test plan, and the test board design. Chapter 6 will review and summarize the project and provide conclusions and recommendations for further advancement.

Chapter 2

Fuel Gauges

In mobile products, battery status is a key concern for most users. For a product to be very successful, it has to add value to the user's daily lifestyle without sacrificing any of the current benefits. It needs to integrate seamlessly with minimal impact to the user's behaviour. For example, a mobile phone that can be used for 16+ hours without re-charging is a benefit seeing as charging can happen during the 7-8 hour sleep period. If the phone requires multiple charges throughout the day, then it starts to become a detriment and will force the user to be conscious of usage and charging locations, and therefore change the user's behaviour. In general, people resist drastic changes, so a product that will require modification of user behaviour may have to be "revolutionary" to generate customer adoption. Most mobile products offer a fuel gauge as a solution to understanding the battery drain and to notify the user of charging requirements. If the user needs the phone to be active for the next 10 hours, and the fuel gauge is reporting less than 20% capacity remaining, then the user might

want to limit their usage, or find a charger to boost the capacity to fit the required runtime. The fuel gauge acts as an indicator and notification tool to influence user behaviour. The fuel gauge has two main functions:

1. Measuring Capacity – HW
2. Reporting Capacity – SW

A complete fuel gauge solution will therefore provide a HW and SW implementation to capture the required functionality. The design of the fuel gauge will depend on the battery characteristics and the type of fuel gauge algorithm selected and of course the application use of the electronic device. The following sections will cover the detailed analysis used to determine an appropriate solution.

2.1 Battery Models

The following section will cover details on batteries, in specific, lithium ion batteries which are very common in portable electronic designs. It will also give an overview of some of the basic circuit models that can be used in simulation and discuss the useful battery parameters required to accurately characterize a battery for the algorithm design. The most common parameters are ESR, load frequency, temperature, aging and self-discharge.

2.1.1 Lithium Ion Batteries

Lithium ion batteries operate on the principle of moving lithium ion charges from the anode to cathode during discharge and cathode to anode during a charge phase. The specifics of the battery chemistry are beyond the scope of this thesis, but

fundamentally, adjusting the materials of the electrolyte, anode, cathode, and external plates, can help optimize the performance and energy density of the cell [1]. The following table shows the advantage of lithium ion over competing chemistries [2].

Table 2.1: Battery Type Density Comparison

Cell Type	Ni-MH	Ni-Cd	Li-Ion
Gravimetric Density [W-hr/kg]	55	50	90
Volumetric Density [W-hr / L]	180	140	210

Beyond the obvious advantage of a higher energy density per volume and per weight, the lithium ion battery offers high flexibility in design as it is rechargeable and can typically be used beyond 500 charge-discharge cycles. However, after a large number of cycles, the overall performance and available capacity will decrease, and this will be clarified in more detail in sections 2.1.3 and 2.3.4.

2.1.2 Equivalent Circuit Models

There are many electrical circuits with varying levels of complexity that can be used to model lithium ion batteries. The most basic being the Rint Model [3]. As seen in Figure 2.1, the circuit is comprised of an ideal voltage source in series with a resistor. The voltage at the battery terminals can be calculated as follows:

$$U_L = U_{oc} - R_o I_L \quad (2.1)$$

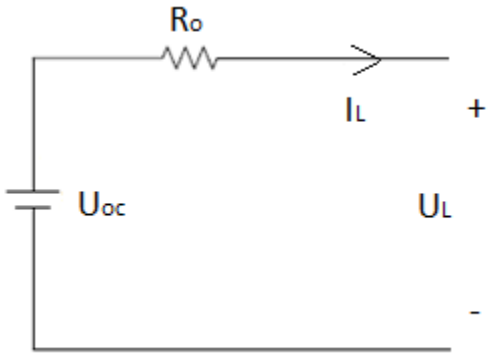

Figure 2.1: Battery Equivalent Circuits – Schematic of the Rint Model

Another useful model is the Thevenin Model. It is similar to the Rint model, with the addition of a parallel resistor-capacitor (RC) component in series with the original resistor [3]. The RC pair is used to represent the transient response of the battery as it is charged / discharged, since the battery will have non-ideal characteristics that will cause timing delays in the battery reaching its expected voltage. The system will draw the required load from the battery but it will not be instantaneous. This is useful information to understand when designing the system.

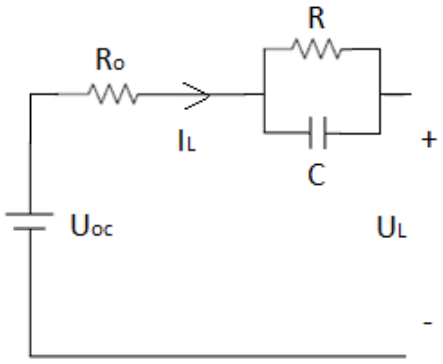

Figure 2.2: Battery Equivalent Circuits – Schematic of the Thevenin Model

2.1.3 ESR

Equivalent series resistance (ESR), i.e. R_o from Figure 2.1, is another critical parameter of fuel gauge measurements. As it was explained in section 2.1.2, the basic battery model (Rint Model) will include a series resistance internal to the "black box" of the battery terminals. Understanding the elements that affect the ESR will help to better predict the value in specific battery scenarios. The main considerations are temperature, aging, and load frequency. Figure 2.3, 2.4 and 2.5 show the typical characteristics of a lithium ion battery ESR. These measurements were taken on a 2800 mAh Lithium Ion Battery, with a nominal voltage of 3.7V and maximum voltage of 4.35V.

Batteries tend to operate differently under different temperature conditions. Typically, the lithium ion battery is best operated under room temperature and lighter loads for both maintaining the health of the battery and for predictability in performance [4]. Higher temperatures improve cycle performance as it will reduce the internal resistance, i.e. ESR. However, it puts more stress on the battery which will have adverse long term effects on the overall health of the battery [4]. Cold temperatures have a rising effect on the ESR which has a direct impact on the available capacity of the battery within the system [4]. The advantage of lower temperatures is that the battery will increase its cycle lifetime. ESR will also increase as the cycle count increases, as can be seen in Figure 2.4.

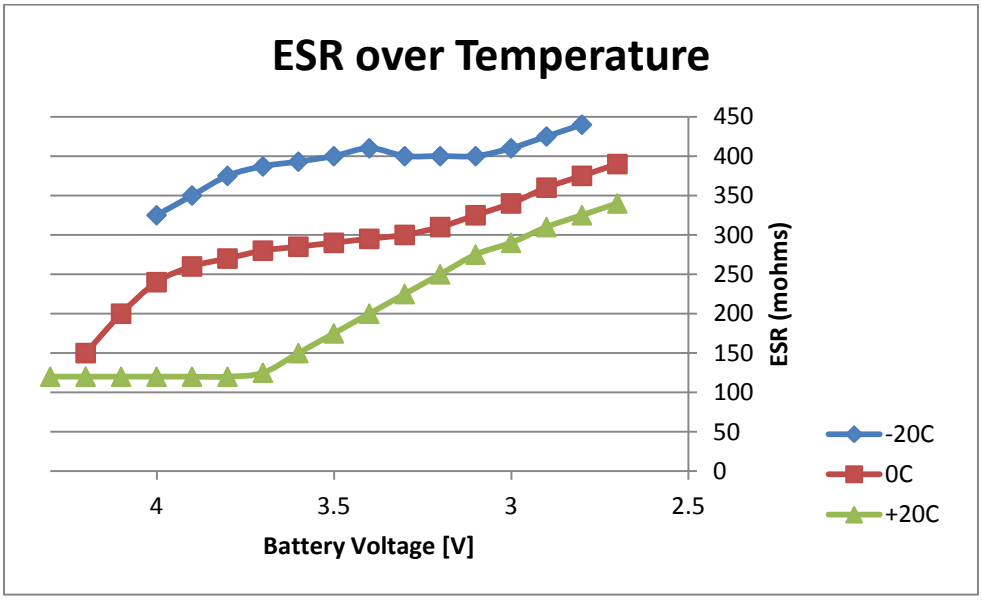

Figure 2.3: Lithium Ion Battery Measured Data – ESR over Multiple Temperatures

(-20deg, 0deg, +20deg)

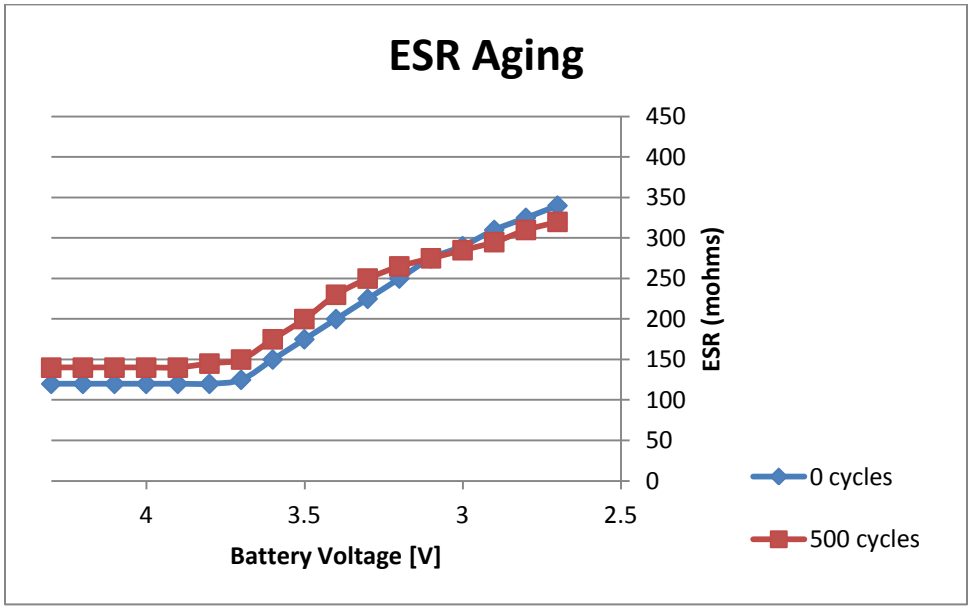

Figure 2.4: Lithium Ion Battery Measured Data – ESR Aging over Multiple Cycles

(0 cycles and 500 cycles)

Load frequency can have a larger effect on the ESR than temperature and aging and it can change in the short term. A higher frequency load will lower ESR as seen in Figure 2.5. Longer pulses tend to drive the ESR higher. The ability to track the ESR is important as it will have a direct effect on the system cut-off voltage, which will be explained in section 2.4.1.

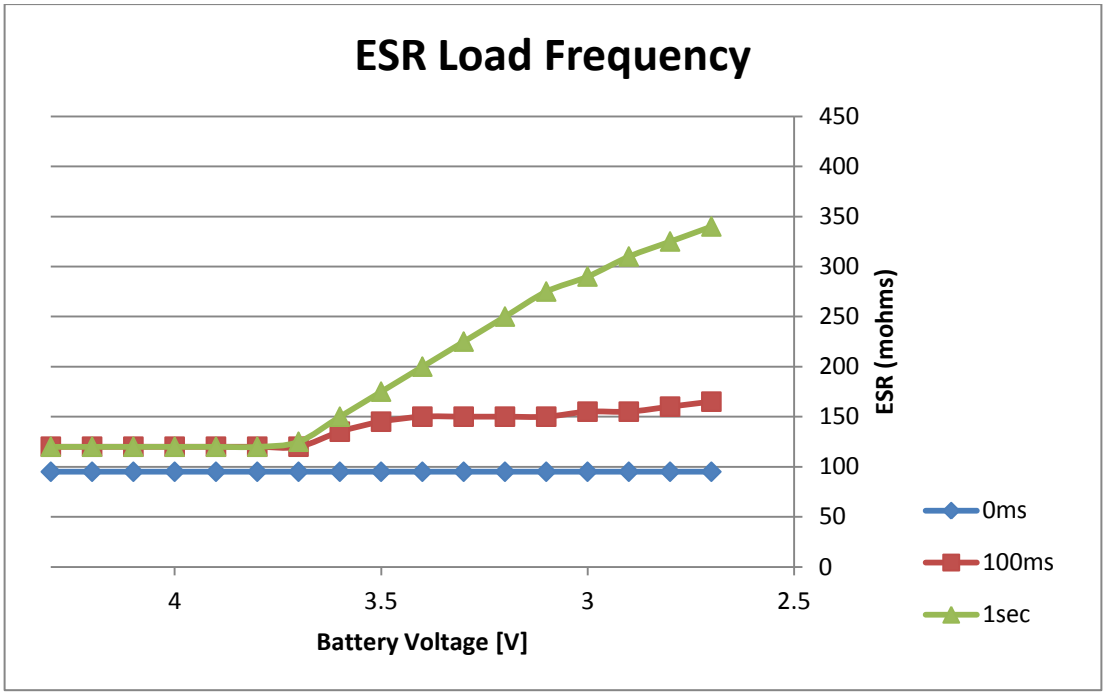

Figure 2.5: Lithium Ion Battery Measured Data – ESR over Multiple Load Frequencies

(0ms, 100ms, 1s)

2.1.4 Self-Discharge

The self-discharge rate of a battery is based on its chemistry. This can be represented by a large value resistor in parallel with the equivalent circuit of the battery. Ideally, the higher the value of the resistor, the smaller the current that is discharged. Equation 2.1 provides an example below that uses the following parameters to determine the amount of time it would take to discharge the battery if not being used:

Battery Current Capacity = 1 Ah

Nominal Voltage = 3.7 V

Self-Discharge Resistance = 50 kohm

$$\text{Time [mths]} = \text{Capacity} / ((\text{Voltage} / \text{Resistance}) * 24\text{hr} * 30 \text{ days}) \quad (2.2)$$

$$= 1 / ((3.7 / 50\text{k}) * 24 * 30)$$

$$= 18.77$$

Depending on the load, when the battery is in use, this typically will not greatly affect the electronics, as the current consumption is below 100uA in this case (i.e. ~74uA). If the normal discharge cycle is ~48hrs, the average discharge rate of the battery in operation is ~20mAh. In comparison, the self-discharge rate is less than 0.5% of the average power consumption.

2.1.5 Open-Circuit Voltage (OCV)

Battery voltage is one of the primary values that is used to compute battery capacity. Section 2.1.2 covered the equivalent electrical circuit models of the battery, and to recap, a battery can be modelled simply by a voltage source in series with a resistor. Therefore, measuring the voltage of a battery at its terminals will report a different value depending on the amount of current that is being sourced. To use the voltage of the battery as a useful parameter in the capacity algorithm, it is best to use the open-circuit voltage. This value should be calculated based on the following equation:

$$OCV = VBAT + (IBAT * ESR) \quad (2.3)$$

where VBAT = Battery Voltage at the Terminals, IBAT = Battery Current, ESR = Equivalent Series Resistance

A purely voltage based fuel gauge will use the OCV and a previously stored table of voltage values to report the capacity.

2.1.6 State of Charge (SOC)

The state of charge (SOC) is the measure that is used to report the capacity of the battery. A 100% SOC refers to a fully-charged battery. There are a number of ways to calculate and report the SOC, and will be discussed in latter sections (2.3.2, 2.3.3). Depending on the algorithm, such as the one in this thesis, multiple SOC variables could be used to determine the overall (user-reported) SOC. Using multiple SOC

calculations allows for higher accuracy since each fuel gauge method has its own strengths and weaknesses that can be optimized and mitigated. Most system designs will require a consistent SOC accuracy over a complete charge/discharge cycle.

2.1.7 Voltage Waveforms (Discharge/Charge)

Different battery chemistries will have different voltage curves. In general, most lithium ion batteries will have a typical voltage curve over its voltage range. The battery curve can be broken down into two segments, sometimes three, depending on the level of accuracy required at the high end of the charge scale. A fully-charged battery will follow a relatively linear discharge curve for the first 60-70% of its available charge. After this point, the voltage drops off exponentially and the voltage per percent increases, i.e. larger voltage gaps between percentages. This is why it is critical to be more accurate at the low end of the battery curve, since the declining voltage will approach the system cut-off voltage more rapidly. The system cut-off voltage will be described in section 2.3.1.

As can be seen in Figure 2.6, one of the factors affecting the voltage curve will be the load. Higher load currents will discharge the battery more quickly and create a steeper voltage curve. Temperature and aging both affect these curves as well; however, it is mostly based on their effects on the ESR as was described in section 2.1.3.

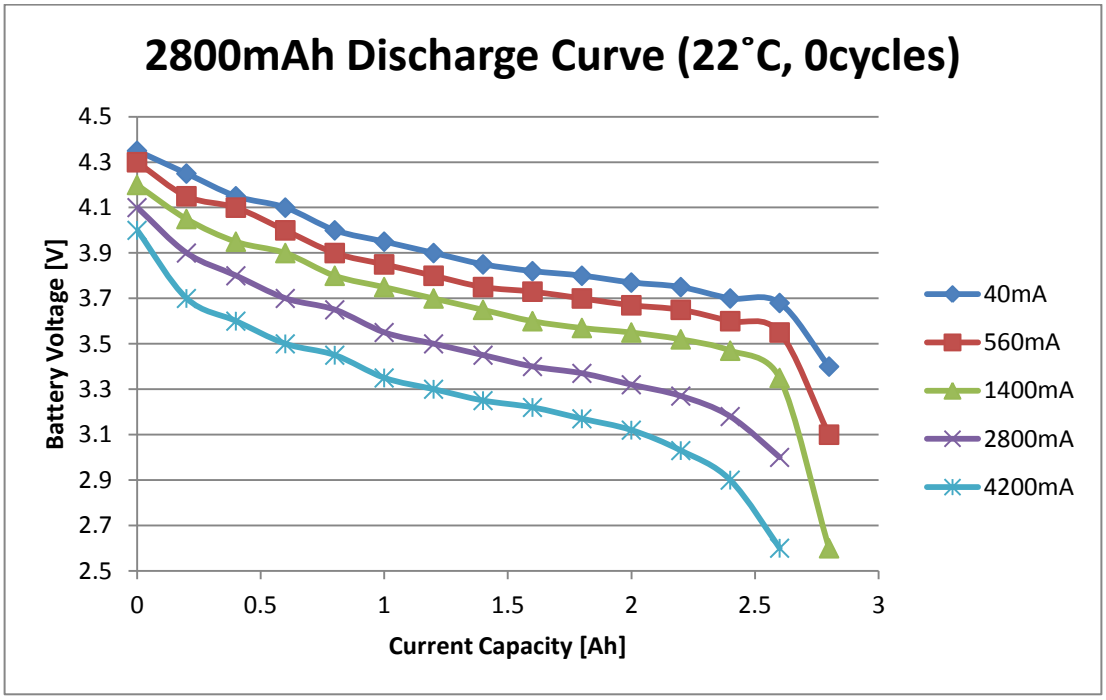

Figure 2.6: Lithium Ion Battery Measured Data - Discharge Voltage Curves Based on Different Discharge Loads

Charging curves will follow a similar trend as the discharge curve, but slightly shifted depending on the charge rate and the type of charging. The two common methods of charging are constant current and constant voltage. Typically, the constant current charging mode will be used for the initial ~80-85% of the charge cycle. The power management solution will usually switch to constant voltage in the higher voltage range of the battery as it will reduce the stress on the battery as the current will slowly reduce as the battery voltage reaches its upper limit. To be clear, the voltage being discussed in the charging mode is the OCV, i.e. the voltage of the battery's internal voltage source. The voltage applied to the terminals will typically be the maximum voltage of the battery. The power management controller (i.e. often

times the PMIC, power management IC) can configure the voltages applied and the charging current limit during the constant current mode.

2.2 Fuel Gauge HW Concepts

There are a few common methods for measuring the capacity of an electronic system. Each technique poses its own advantages and disadvantages and comparisons will be made. The methods below both rely on some form of HW measurement device. The most common device is an ADC. This is a critical piece of the solution and will be described in detail in Chapter 3.

2.2.1 Fuel Gauge Method 1 – Voltage Based

Voltage based gauges rely on the voltage of the battery to map to a capacity level. Typically, most batteries will follow a similar voltage discharge curve. To obtain these curves, the battery will typically be discharged at a constant rate, usually at a light load, over a long period of time to determine the most accurate voltage curve.

Without divulging too many out-of-scope details of battery operated systems, in general, a system will be designed with a maximum operating voltage and a minimum operating voltage. Comparing the voltage level of the battery to these two metrics should give a useful indication of the remaining capacity. The method for measuring the voltage accurately is through the use of an ADC. Depending on the accuracy, resolution and sampling rate of the ADC, the voltage can be tracked over time and can be compared to a table of values to determine the capacity. Details on ADC concepts will be discussed in section 3.1.

An advantage of using a voltage based gauge is that it can be quite accurate when supplying light loads. A light load will allow the measured voltage at the battery terminal to be relatively close to OCV, which will allow the voltage based gauge to be fairly accurate. A disadvantage of using a voltage based gauge on its own is that it does not take into account the load on the battery. This is an important metric to track if the battery is required to support heavy loads, as the voltage measured across the battery terminals will vary based on the load, but the OCV will follow the discharge curve as it was characterized in the data table of the gauge.

2.2.2 Fuel Gauge Method 2 – Current Based

Another common technique is measuring the current draw of the battery, or more commonly known as "Coulomb Counting". The method is self-explanatory in that it relies on counting the load on the battery over time, i.e. counting the coulombs of charge entering / leaving the battery. Again, the measurement HW required is an ADC. There are a number of ways that current can be measured. Using transistors as a current mirror is a possibility as it helps to reduce the voltage drop across the terminals when taking measurements [5]. Process variations and variable temperature conditions as well as component cost make this method ineffective. Designing an active current sensing circuit with transistors and an opamp is also a possibility, but again is not cost effective based on the component count. Typically, the useful application for this solution would be a class-D audio amplifier [6]. It turns out that the simplest and cheapest solution is the optimal path forward for current sensing in battery-powered applications. The current sense resistor is able to reliably drop a voltage across its terminals based on the current flowing in the path. A few design elements need to be considered when implementing this solution. First, the location of the resistor within the circuit path needs to be selected. The

options are the negative terminal or the positive terminal of the battery. The negative terminal isn't the best option as noise from the ground plane could affect the measurement accuracy. The positive side of the battery also has its drawbacks, as it will limit the upper threshold of the output voltage to the system. However, it maintains the stability in the ground plane. Thus, it is a better solution to place the sensing resistor at the positive terminal of the battery. The next design decision is the value of the resistor. This needs to be determined based on the expected loads and the accuracy of the voltage ADC being used for measurements. The resolution of the voltage ADC will be based on the resolution of the current that needs to be realized for the capacity accuracy. Resistor tolerances in terms of values and temperature effects will also need to be reviewed.

2.3 Algorithm Concepts

Once the physical measurements have been made with the appropriate HW, the SW implementation will take over with an algorithm to compute values that are to be reported to the user. The following section will describe the fuel gauge SW algorithm and its major components which can be seen via a system block diagram in Appendix A. Detailed functionality as well as interdependencies will also be shared.

2.3.1 System Cut-Off Voltage

Electronic systems are designed to operate within specific voltage ranges. The system voltage range is usually selected based on the operating voltages of the chipsets, and furthermore, the battery voltage range selected to supply those chipsets. The battery's primary function is to provide a load current to the system. The power

management circuitry has the role of providing a reliable and stable voltage level to each of these chipsets. This is usually done via buck converters, boost converters or low-dropout voltage regulators (LDOs). The efficiency can vary drastically if the load current is fluctuating, and generally it would for a system that is power optimized, as the system designers will want to minimize the power consumption of each individual IC whenever possible to conserve precious battery power. Using a buck converter as an example, Figures 2.7 and 2.8 show the variations in efficiency due to the load current and input voltage. Furthermore, Table 2.2 shows the change in supply current based on a pulsing load current as the battery is operated in a discharge cycle. The data was extracted from Figures 2.7 and 2.8 [7]. The battery input voltage will decline and although the efficiency increases to maintain a constant output voltage, the required battery supply current will increase to support the load.

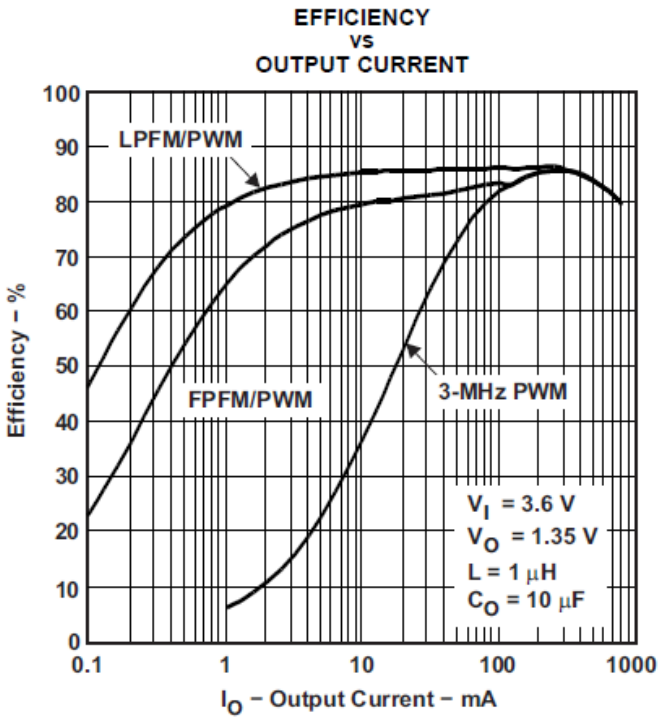

Figure 2.7: TPS62350 Buck Converter Efficiency vs. Output Current [7]

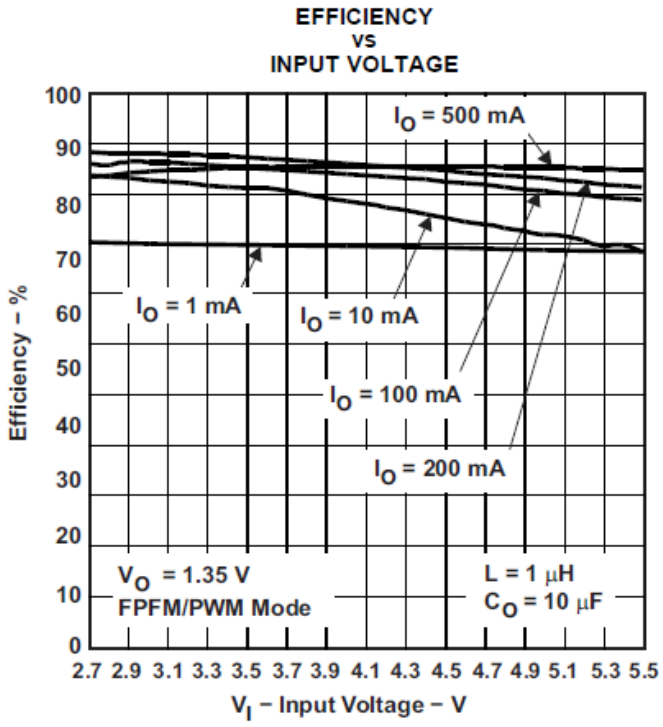

Figure 2.8: TPS62350 Buck Converter Efficiency vs. Input Voltage [7]

The curves show the converter in different operating modes. Pulse width modulation (PWM) uses constant frequency pulse widths to control the output voltage. Pulse frequency modulation (PFM) uses constant pulse times at varying frequencies to control the output voltage. Light PFM (LPFM) and Fast PFM (FPFM) are variations that are optimized for efficiency and transients, respectively [7].

Table 2.2: Battery Input Current During a Discharge Cycle [7]

Supply Voltage [V]	Output Voltage [V]	Load Current [mA]	Buck Efficiency [%]	Input Current [mA]
4.3	1.35	200	84	74.75083
4.3	1.35	1	65	0.483005
4.2	1.35	200	84	76.53061
4.2	1.35	1	65	0.494505
4.1	1.35	200	85	77.47489
4.1	1.35	1	65	0.506567
4.0	1.35	200	86	78.48837
4.0	1.35	1	65	0.519231
3.9	1.35	200	86	80.50089
3.9	1.35	1	65	0.532544
3.8	1.35	200	87	81.66969
3.8	1.35	1	65	0.546559
3.7	1.35	200	87	83.87698
3.7	1.35	1	65	0.561331
3.6	1.35	200	88	85.22727
3.6	1.35	1	65	0.576923

As can be seen in Table 2.2, the lower the supply voltage, the higher the input supply current required to produce the required load current. The input supply current was calculated by re-arranging the basic efficiency formula as seen in Equation 2.3.

$$I_{in} = (V_{out} * I_{out}) / (V_{in} * \text{Efficiency}) \quad (2.4)$$

2.3.2 OCV SOC

The OCV SOC is the state of charge determined based on a voltage based fuel gauge. The voltage method was described in detail in section 2.1.1. This value should be calculated from the measured battery voltage, measured battery current and predicted ESR. This is also relative to the system cut-off voltage. A battery will theoretically be able to deliver charge from its maximum voltage down to its minimum. However, the system cut-off voltage will be selected at a voltage closer to the top of the exponential section of the voltage curve. This provides better accuracy at lower SOC estimations. It also will keep in mind the input voltage range of each of the system chipsets. That being said, the SOC table associated with the OCV, will reflect the selection of the system cut-off voltage as that voltage level will be considered as 0% SOC.

2.3.3 CC SOC

The CC (Coulomb Counting) SOC is the state of charge determined based on a current based fuel gauge. The current method was described in detail in section 2.1.2. This value should be calculated from the measured battery current which will simply keep track of the amount of charge entering or leaving the battery. A battery will theoretically be able to deliver its full rated charge (in mAh) from its maximum voltage down to its minimum voltage. However, initial measurements will have to be taken to determine the amount of usable charge based on the system cut-off voltage selected. Depending on the selection, there may be a small or large amount of charge unavailable for use, which will affect the CC SOC. A sample SOC calculation is provided below.

Parameters:

Maximum Battery Voltage = 4.35V

Maximum Battery Capacity = 1000mAh

System Cut-Off Voltage = 3.4V

Usable Battery Capacity (based on measurements) = 95%

Scenario: Starting from a fully charged battery, 150mAh have been discharged. Therefore:

$$\text{CC SOC} = (((1000 * 95\%) - 150) / (1000 * 95\%)) = \sim 84.2\% \qquad (2.5)$$

2.3.4 Usable Capacity

The usable capacity is based on a calculation of a few different parameters. The concept is that the present load will dictate the potential time to empty and how much capacity will be available if the load is to remain constant and maintained throughout the discharge cycle. The system cut-off voltage is the key to this calculation; however, it is used slightly differently than in the OCV SOC calculation. The OCV calculation assumes that the SOC is based on the voltage of a battery under no-load, i.e. open-circuit. Unfortunately, this is rarely the case when a battery is in operating mode. If a load is placed on the battery, the voltage of the battery at the terminals, is the voltage that the system will see as its input supply voltage. This means that if this voltage drops below the system cut-off level, the designed system should not work.

With this in mind, the OCV will always be higher than the system cut-off voltage, and therefore the system will never allow the battery OCV to reach the

system cut-off voltage as long as the load current is non-zero. The usable capacity is therefore calculated based on the present load assuming that this load would be constant until the battery voltage (at the terminals) reaches system cut-off. This value will constantly be fluctuating as it sees changes in the load, however, it allows the algorithm to predict how much capacity is actually available, as it would be a poor user experience if the reported SOC is much higher than 0% when the system shuts off.

2.3.5 Reference SOC

The reference SOC is used to calculate the associated error of the gauge and to understand whether the accuracy of the reported SOC is meeting the requirements. Essentially the reference SOC is calculated by counting the amount of charge that is exiting or entering the battery and then converted to a percentage based on how much available capacity remains which can be taken from the instantaneous load. From this description, it is simple to see that this is essentially the CCSOC. The reason this can be used as the reference SOC is because it is the theoretical value of the SOC and the amount of charge should be an accurate indicator of the SOC. The concern with using solely the CCSOC as the fuel gauge solution, is that the other effects of the battery conditions and loading state, i.e. ESR, self-discharge, temperature, aging, etc., essentially make the SOC value a best case estimate. In reality, the SOC measurement is a prediction, and thus the OCV SOC is helpful to correlate the overall SOC such that the calculation can be more accurate. It will also be explained in the latter sections that the weighted capacity SOC and the user-reported SOC modify the calculated value, and therefore introduce its own error. Ensuring that the accuracy requirements are met will influence the calculations of the weighted capacity and user reported SOC.

2.3.6 Weighted Capacity SOC

The weighted capacity is a simple formula to optimize the algorithm performance to ensure that the accuracy requirements are being met. Essentially, there are two SOC values that are being derived in this algorithm, OCV SOC and CC SOC, respectively. The simplest equation to utilize these values to produce one value is below:

$$SOC = (OCVSOC * OCV\_Weight) + (CCSOC * CC\_Weight) \quad (2.6)$$

The caveat is that both weightings must add up to a combined total of 100%. That being said, this can be used to customize the SOC value to meet specific accuracy requirements. The OCV SOC can be more accurate at the higher SOC values, therefore, having a higher weighting initially. However, once the battery is discharged below 30-40% SOC, the voltage accuracy decreases and would therefore make sense to increase the weighting on the CC SOC. The advantage of this technique is that many of the other variables (e.g. temperature, aging, etc.) can be used to feedback into this weighting system to optimize many different scenarios.

2.3.7 User Reported SOC

The user reported SOC is the value that the electronic device will share with the user. Typically there are a set of guidelines and requirements surrounding the reporting of this value. For example, it is possible that the usage profile is sporadic and will have bursts of activity followed by limited usage. The reported SOC needs to be accurate and account for all possible scenarios, but can also make some allowances to

simplify the user experience such that it is a “good experience” versus a “poor experience”. One such user experience requirement could be to limit the increase or decrease in SOC % reported to the user, e.g. less than or equal to 1% per minute.

Depending on the device, and maximum allowed power consumption, this may not be an issue. However, there may be some usage periods that surpass this requirement and the fuel gauge will still have to track this. The weighted capacity SOC should keep track of the accurate SOC and then the user reported SOC calculation will report the SOC based on this value, the previously reported SOC and the time since the last update. When the device usage and system load decreases, the gauge should recover the reported value to align with the accurate weighted value that is still being tracked. There are other simple user experience requirements that should be met, e.g. the user should never see an increase in SOC when the device is not being charged. This sounds straightforward, but it is also possible to have the battery voltage “recover” from a loading period based on the change in ESR, and appear to have more charge remaining than what was available when under load. This can also happen in this high load to low load transition period because the available capacity will increase which does make sense. However, these discrepancies shouldn’t be seen by the user, as it should be a seamless transition for them throughout their usage cycle, regardless of how they decide to use the device.

2.3.8 Complex Considerations

Some more advanced concepts can be used when designing a fuel gauging algorithm. These are beyond the scope of this thesis, but it is still important to recognize their impact and how they can be implemented for future revisions of the algorithm. User learning is the most challenging “next step” as the requirements are both SW and HW related. From a HW perspective, this is not so much of a problem as it just

translates to a memory requirement. As far as the SW requirement, the algorithm will have to define segments of a usage profile that it would like to "learn". This could be as simple as dividing the battery usage into 100-50% SOC versus 50-0% SOC, as these could be similar, or it could be broken down by time of the day as it is easy to realize that a user will likely have extended periods of time where usage is limited, e.g. 7-8 hrs of sleep at night.

This can vary by the day of the week, and depending on the capability of the algorithm can be broken down further into daily activities or even individual app usage. For example, the browser app is typically active for no more than 5minutes per use which can help in determining the odds of big SOC drops when operating at lower SOC values, where this knowledge could be critical. There are many iterations that can be designed for, and it is a matter of identifying the most important requirements, defining them and then designing an accurate solution to implement them.

2.4 Algorithm Simulations

Once the algorithm was defined, it was implemented in code in Matlab, which is a useful tool for running complex simulations. The simulations would be run multiple times in various iterations to verify the algorithm and to ensure that the correct variables are being used to meet the requirements of the design.

2.4.1 Use Case Scenarios

The simulations were divided into subsections and various runs to ensure that the design would meet the requirements and will be described below. They were the following:

1. Initial Verification
2. OCV SOC Verification
3. CC SOC Verification
4. Weighting SOC Verification
5. User Reported SOC Verification

The initial verification was the most basic simulation. The settings were defined such that the output could be quickly realized and reviewed to determine the validity of the results. The settings in the following table were used.

Table 2.3: Initial Verification Settings

Parameter	Value	Units
Start SOC	100	%
End SOC	0	%
Discharge Rate	10	mA
Temperature	25	˚C
Sampling Rate	1	/sec
OCV Weight	50	%
CC Weight	50	%

Once the initial operation was validated, the individual base gauges were tested. Starting with the OCV gauge, the OCV weight was set to 100% and the CC weight set to 0%. To easily verify the OCV gauge, a very small load value was placed on the battery and the simulation was run. This helps to eliminate the effects of the ESR, since a light load would have a negligible voltage drop across the resistance. The result should essentially show the voltage curve over time and the SOC should map almost directly to the OCV to SOC table defined in the algorithm. The load value can then be increased to verify the voltage curve under different operating conditions. A constant load should also help to verify the ESR values as the battery terminal voltage and OCV correlate with the load to be reverse-calculated to determine the ESR as can be seen in Equation 2.2.

Introducing a pulsed load with varying frequency will validate the different ESR values based on which load frequencies were characterized. The available capacity should also map to the load value in the sense that a constant load will show how much capacity will be available based on the pre-defined system cut-off voltage.

After the voltage gauge was tested, the CC gauge was verified. This testing required that the CC weight be set to 100% and the OCV weight set to 0%. This verification was simpler and had already been pre-verified with the OCV testing. Varying the load value will reduce the available capacity and the CC SOC should therefore reflect these changes. Again a light load can be applied to verify that the coulomb counting algorithm is working accurately since almost 100% of the capacity will be available for usage. Increasing loads will reduce this value and the discharge time will map accordingly.

During this testing, both gauges were comparing the reported SOC to the reference SOC as described in section 2.3.5. This leads into the next testing section seeing as the SOC error would ideally be minimized. The OCV accuracy is typically better at higher SOC values and poor at low ones. The CC SOC is relatively stable

throughout which gives it a better accuracy relative to the OCV. Load frequency and value also have a direct impact on the accuracy. The weighting can be customized to account for many variables and the more that is tested, the better the weightings can be characterized based on the specific battery.

The final set of testing should be surrounding the SOC that is reported to the user. Essentially, the user experience requirements will dictate the scope of testing, but it should at the very least cover the range of tests that were conducted for the OCV, CC, and weighting tests. The scope should also include any load profiles that would be expected when in real operation. If the user experience requires that the SOC cannot decrease by more than 1%/min then this should be captured in the algorithm. This will also affect the error and ties back into the weighted testing.

Many simulation iterations are required to ensure the overall operation meets the design requirements. The next sections will cover more complexity that is added when factoring in temperature and aging.

2.4.2 Temperature

The effects of temperature are well understood and require verification. Temperature will ultimately affect the ESR, which in turn, affects the available capacity, the discharge curve, the time-to-empty and the weighting for the voltage and current based gauges in the overall SOC estimation. Generally, the battery will be characterized at a few specific temperatures and loads, and the ESR at temperatures in-between will have to be interpolated.

2.4.3 Aging

The effects of aging on battery ESR were described in section 2.1.3. Battery characterization data is collected based on the number of charge/discharge cycles that the battery is placed under. That being said, there is another concept that must be accounted for, i.e. depth of discharge. The depth of discharge refers to the percentage of the battery that is discharged during the loading portion of the cycle. If a battery is discharged from 100% to 60%, the depth of discharge would be 40%. It would therefore be relevant to track the depth of discharge that occurs in each discharge cycle such that a proper cycle count could be kept.

In theory, a full discharge of 100% to 0% for 100 cycles is equivalent to 200 cycles of 100% to 50% discharging. However, this is not fully accurate as the battery does not operate exactly the same in all stages of its charge/discharge. When the battery is being discharged beyond a certain threshold, e.g. below 40%, the battery will be more "stressed" and this will affect the overall long-term health of the battery [3]. This should be also be tracked to provide a more accurate SOC estimation over a large number of cycles. In terms of user experience, it is best to err on the conservative side, as it would be a poor experience to have the battery suddenly drop to low SOCs when a user would potentially be expecting hours more of operation.

2.5 Summary

Fuel gauge algorithms can be complex and can involve many different parameters as seen in the previous sections. Understanding the battery type and expected behaviour is the first step, followed by collecting characterization data for the algorithm. Then the variables can be manipulated to output values that are to be

reported to the user and should be optimized for as many use case scenarios as possible. Simulations help in this regard and should be completed over temperature and many cycles to get a true understanding of the life of the battery. Most of the future work in this area will be to refine the algorithm in terms of accuracy and additional complexity to characterize user-specific behaviour. For the SW to function properly, accurate readings of the battery status are essential. This is done by the HW portion and relies on one or more custom designed ADCs. The following chapter will discuss what is required to design such a HW component.

Chapter 3

Successive Approximation Register Analog to Digital Converters (SAR ADCs)

The main HW component in the fuel gauging solution is an ADC. Different types can be used based on the application, design requirements and configuration, i.e. voltage or current based gauges. For most electronics designs, it is commonplace to use a sigma-delta ADC as it generally can handle higher resolution, and are low power and lower cost [8]. However, they are typically slower speed than some of the other ADC architectures. An alternative architecture is the SAR ADC which will be discussed in sections 3.3. Section 3.1 will cover some of the basic ADC concepts and will lead into some detailed design calculations in section 3.2.

3.1 ADC Concepts

There are many different types of ADCs, but they generally follow the same basic concepts in operation and design. Some of the design factors and elements are discussed below including the sample rate, bandwidth, resolution, SNR and noise.

3.1.1 Resolution

The resolution of an ADC refers to the number of bits. This value can be determined based on the acquisition time plus the conversion time of the ADC [9]. For some ADCs, this means that if the sampling rate is 1Hz (i.e. 1 sample per second) and the ADC can acquire a sampled value and complete a conversion of 4 bits in that time, then the resolution of the ADC is 4 bits. Depending on the type of ADC, multiple conversions could be happening concurrently, which would complicate this understanding [9]. For simplicity as well as pre-emptive understanding of SAR ADC operation, the following example will assume that each consecutive conversion will not start until the previous conversion is complete. Taking 1us as the sampling period, if each the sample can be acquired in 0.2us and each bit can be realized within 0.1us, then the resolution is 8 bits. To calculate the amount of time it takes to convert a single bit, the time constant concept must be understood.

When a signal transitions from one level to another, it never happens immediately in the real world, despite what some plots might misconceive. That being said, the amount of delay will depend on the characteristics of the circuit. This delay is most easily characterized by an RC time constant, where R represents a resistance, and C represents a capacitance. Figure 3.1 shows an equivalent circuit that would be used to conceptualize this effect. The time delay can be calculated as follows based on the R and C parameters:

$$\text{Time [seconds]} = 1 / R \text{ [ohms]} * C \text{ [Farads]} \quad (3.1)$$

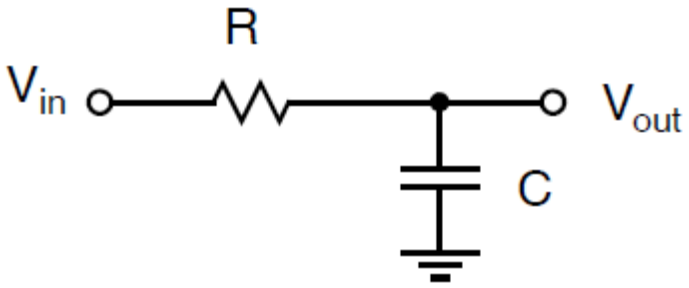

Figure 3.1: RC Time Constant Equivalent Circuit

This time delay needs to be factored into the conversion time of an ADC, and is the primary limitation of the circuit speed.

3.1.2 Sample Rate / Bandwidth

Sampling rate is a universal concept that pertains to signal analysis and measurement techniques. A basic understanding can come from breaking signals down into analog and digital portions, which is not unlike the purpose of an ADC. An analog signal is considered to be continuous whereas a digital signal is formed from discrete steps. The granularity of the discrete steps can potentially show a different signal depending on the frequency of the signal. This is the concept of sampling. The theory developed by Nyquist states that the sampling rate of a signal must be at least two times the period frequency of the signal [10]. That is a minimum value, seeing as the more samples that are taken per period will give a more accurate signal interpretation. Typically, ADCs do not have to follow the Nyquist rate; however, the sample rate should be selected depending on the signal frequencies of interest.

Bandwidth can have many definitions depending on the usage. When viewing the frequency response of a low pass filter circuit in the frequency domain, the response can follow a similar shape to that shown in Figure 3.2. The Y-axis is measured in gain magnitude which is captured in units of dB. Signal frequencies that are within the segment that has a 0dB gain, will appear as full power signals. Once the filter response begins to decay, signals become attenuated and the amplitude of the signal will no longer be what was originally expected. The frequency where a signal is attenuated by 3dB refers to the full power bandwidth of the circuit, as this translates to a 50% decrease in signal amplitude [9].

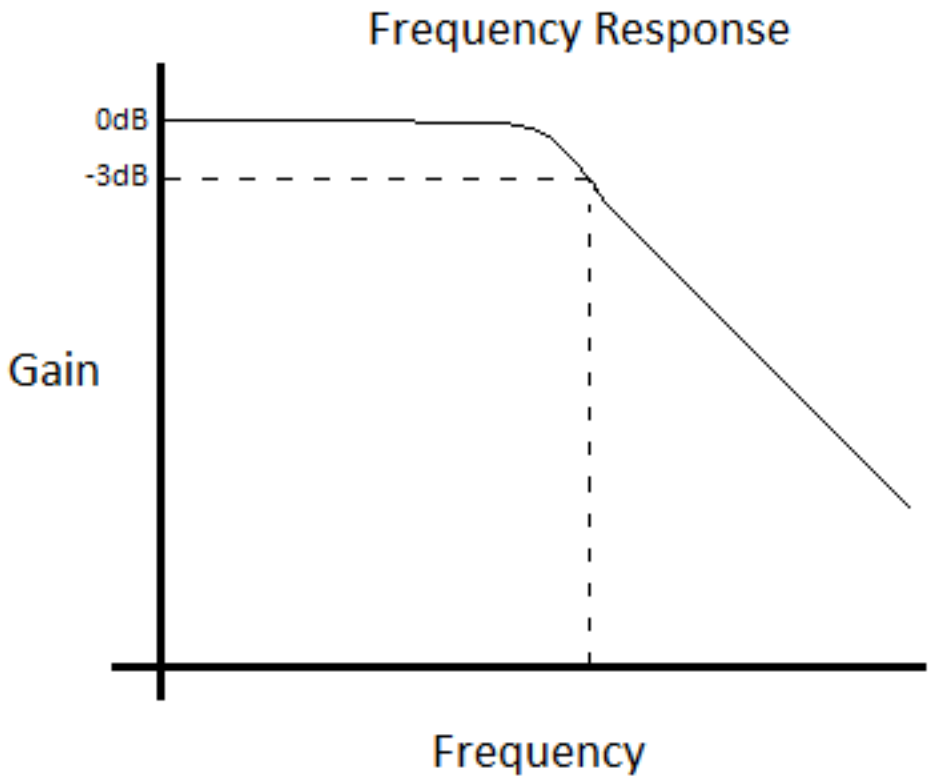

Figure 3.2: Low Pass Filter Frequency Response

3.1.3 Noise

In an ideal environment, a signal would traverse a system without any interference. Unfortunately, in a practical system, noise can be coupled with the signal before it enters the system, once it is being processed, and even as it reaches the output stage. The purpose of performing a noise analysis is to determine which possible noise sources would be the most dominant, and design the system to minimize these sources. Noise is an important, but complex subject and entire chapters have been written to explain the effects on circuits. With respect to ADCs, there are a few possible noise sources and they can be calculated to simplify the design process. The first source is thermal noise. Thermal noise occurs from the movement of charge from the transfer of thermally generated energy [10]. The noise is directly proportional to the temperature of the circuit and is predominant in resistors. Thermal noise can be modelled as a voltage source and its resistor model is presented in Figure 3.3.

$$V^2(f) = 4kTR \tag{3.2}$$

where $k = 1.38 \times 10^{-23}$ [J/K], T = temperature [K], R = resistance [ohm]

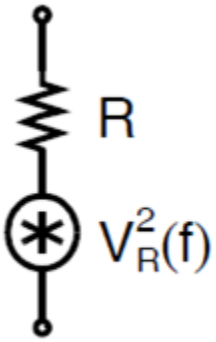

Figure 3.3: Thermal Noise Equivalent Circuit for a Resistor

Flicker noise is another source and it is highly dependent on frequency [10]. This type of noise is more useful in modelling the noise present in MOSFETs. MOSFETs also have thermal noise and are based on the resistance of the current channel. Low frequency applications will be dominated by the flicker noise, and conversely, the flicker noise will be minimized in higher frequency applications. The thermal noise will be dependent on the channel resistance and can be optimized by the area of the gate [10]. Equations 3.3 and 3.4 represent the MOSFET models for thermal and flicker noise, respectively.

$$I_d^2(f) = 8kTg_m/3 \tag{3.3}$$

where $k = 1.38 \times 10^{-23}$ [J/K], T = temperature [K], g_m = transconductance [Siemens]

$$V^2(f) = K/WLC_{ox}f \tag{3.4}$$

where K = device constant, W = gate width [m], L = gate length [m],

C_{ox} = gate capacitance per area [F/m^2], f = frequency [Hz]

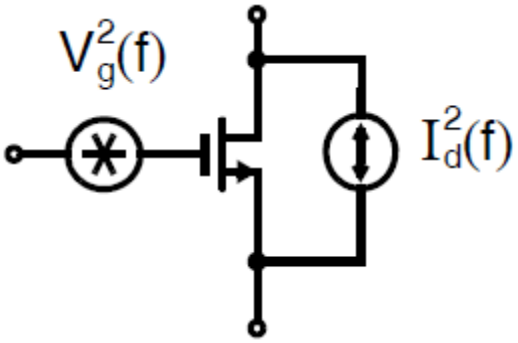

Figure 3.4: Thermal and Flicker Noise Equivalent Circuit for a MOSFET

One more key noise concern for ADCs is quantization noise. When an ADC converts an analog signal to a digital one, the digital value is considered a representation of the analog value. For example if an analog signal is found to be within the voltage range of 0 to 1V, and the ADC will convert this value to a digital representation based on 2-bits, then the digital output will be one of the following values: 0V, 0.25V, 0.5V, 0.75V (or possibly 0.25V, 0.5V, 0.75V, 1V depending on the design). When the ADC is converting the analog value, it will essentially select a digital output based on which digital voltage value it is closest to. This operational flow will be explained in more detail in section 3.3.1. The difference between the analog and digital values is considered the quantization noise or quantization error. The difference between discrete steps is called the lowest significant bit (LSB). Therefore, the maximum possible quantization error will always be +/- 0.5LSB since that is the worst case.

3.1.4 SNR

The signal-to-noise ratio (SNR) is an important metric in an ADC as it will govern the accuracy of the design and can help to identify how much noise can be allowable in the circuit. SQNR (signal-to-quantization-noise ratio) is based on a calculation of the signal voltage/power to the quantization noise voltage/power. The following derivation leads to the final formula used to determine the SQNR:

$$\begin{aligned} SQNR &= 20 \log [\ V_{in\ (rms)} / V_{Qnoise\ (rms)}\ ] \\ &= 20 \log [\ (V_{ref} / \sqrt{12}) / (V_{LSB} / \sqrt{12})\ ] \\ &= 20 \log [\ 2^N\ ] \\ &= 6.02N \end{aligned} \tag{3.5}$$

where N = number of bits of resolution

This calculation is very helpful in understanding the upper bound of noise that can be allowed in the circuit before the design will stop having the desired resolution. Section 3.2.3 will show the calculations that were completed to create the 12-bit ADC design in this thesis.

3.1.5 Power

As with most mobile electronics, power consumption is a large concern when in the design stage as conserving battery life is very important. Understanding the power

requirements can allow the designer to focus on optimization in terms of component selection, system design, and battery sizing. When integrating a fuel gauge in a design, the system designer needs to take into account the power requirement of the fuel gauge itself which includes HW and SW components. The HW aspect is to realize the system load from the ADC as it samples the voltage and/or current, and the SW side is how many instructions the processor must use to process the data and report the values to the user. System optimization can come into effect as early as the feasibility stage of a design, and component selection can be a key factor, which is why the selection of the ADC architecture is important. SAR ADCs offer a unique advantage in that they can be optimized for both speed and low power applications [9]. Section 3.3 will discuss the calculations required to design the appropriate ADC, and will give further insight into why the SAR ADC is the best possible architecture for this application.

3.2 SAR ADC Concepts

The successive approximation register ADC (SAR ADC) is a type of ADC that caters to low power, high accuracy, and short conversion time [10]. The circuitry and operational complexity are also quite low, which makes it a useful design to implement based on the specific application of battery-powered fuel gauging. The following sections will describe its operation and divide the circuit into its major components.

3.2.1 SAR Operation

The operation of the SAR ADC is fairly straightforward in concept. It is essentially a binary search algorithm that divides the full scale range into 2 sections with each bit conversion. The following logical flow diagram will show its operation as it attempts to convert an analog voltage to a digital representation.

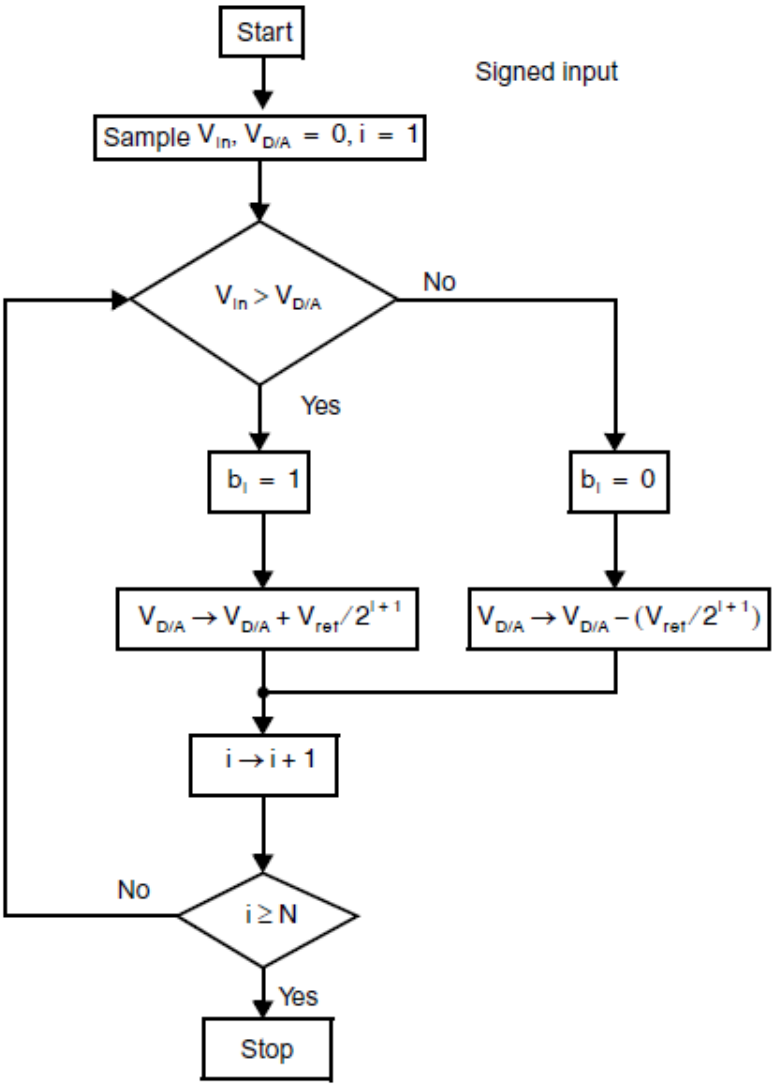

Figure 3.5: SAR ADC Logic Flow

Each successful conversion will be represented in digital format as a 1 or 0, and will be stored. The circuitry to realize this logic is discussed in the following sections. Figure 3.6 shows a block diagram of the circuit sections and the grouping of their parts.

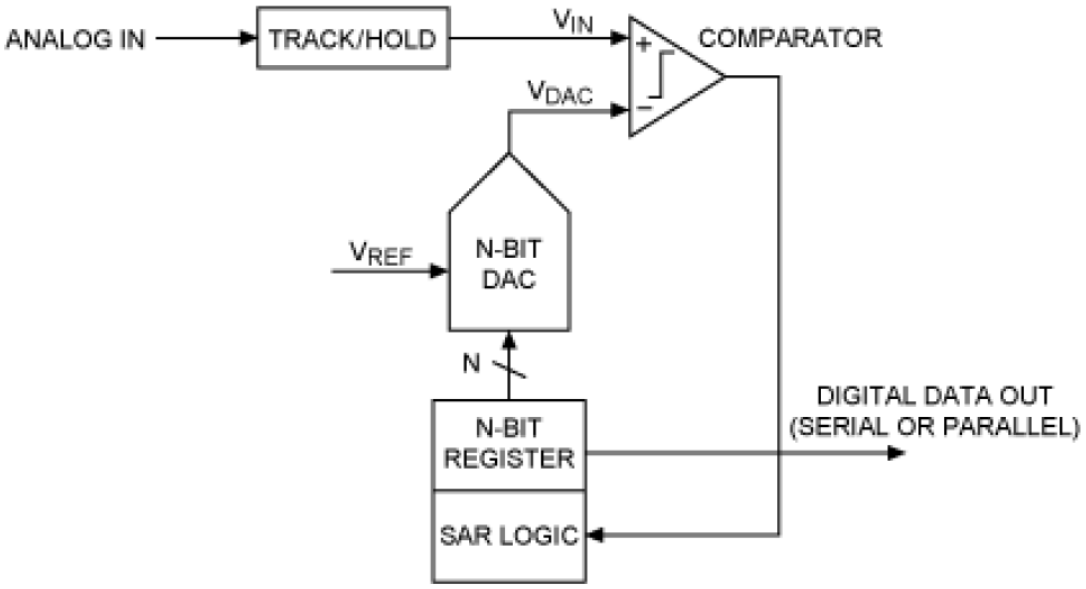

Figure 3.6: SAR ADC System Block Diagram [8]

To break the complete circuit into sections, the ADC can be thought of as the following:

1) Analog Circuit
2) Digital Circuit
3) Comparator

3.2.2 Analog Circuit

For the next 3 sections, a simple SAR ADC example will be walked through to explain the operation of the ADC. A 2-bit ADC example will be used. The analog circuit can be broken up further into 2 separate sections:

1) Sample and Hold Input
2) Digital to Analog Converter (DAC)

The sample and hold input is fairly straightforward, i.e. at the first iteration of the ADC conversion cycle, the analog value that is going to be converted, is stored on a capacitor and the input from the system is disconnected such that this value will not have the opportunity to be changed again until the next cycle. The DAC comes a few steps later in the operation sequence, but can still be considered as part of the analog circuit, thus it will be explained next. The following figure shows a 16-bit version of the switch capacitor array which makes up the DAC. The purpose of the DAC is to take the digital representation of the analog signal that was processed previously and convert it back to an analog signal to be compared again to the input signal for the next bit conversion.

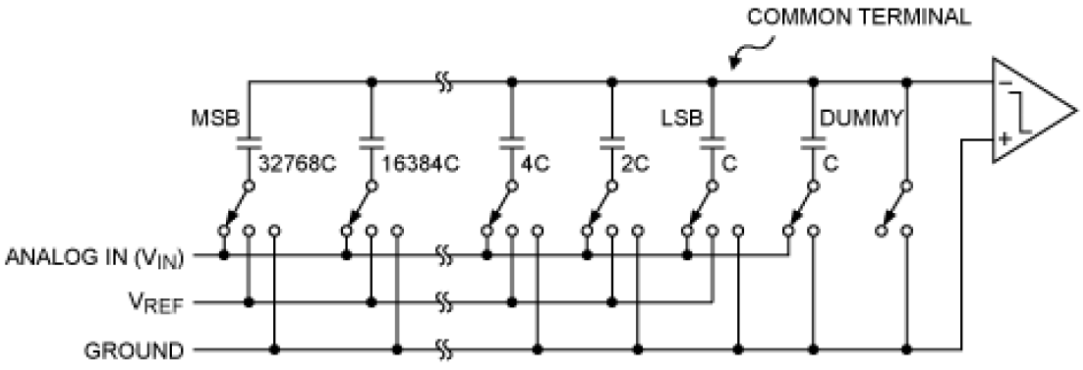

Figure 3.7: 16-Bit DAC Switch Capacitor Circuit [8]

The key factor when designing the switch capacitor array is understanding the fundamental circuit that the DAC is representing, i.e. an RC circuit. Each switch is a MOSFET that is switched on and connected to either of the reference voltage (Vref), input voltage signal (Vin), or ground (GND). The switch will be represented as a small resistance. Connected to the MOSFET is a capacitor whose size is based on the bit value that it is to represent. The voltage that is stored across the capacitor will depend on the connection on its base side and the voltage that is stored on the opposite side of the MOSFET switch. The order of switching is presented below in steps, such that the operation can be understood.

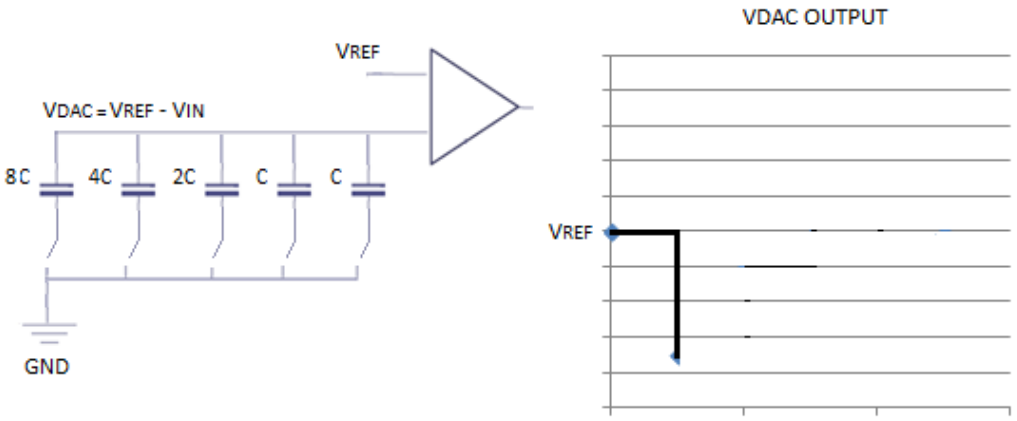

Figure 3.8: Switching Operation Stage 1

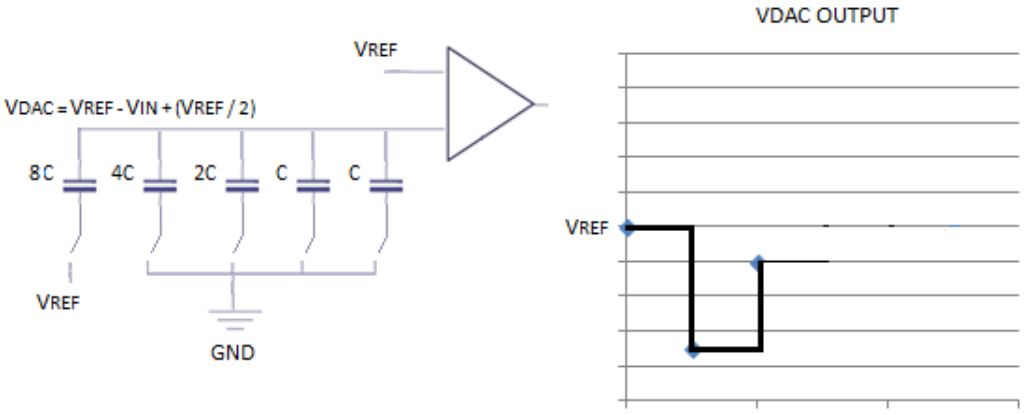

Figure 3.9: Switching Operation Stage 2

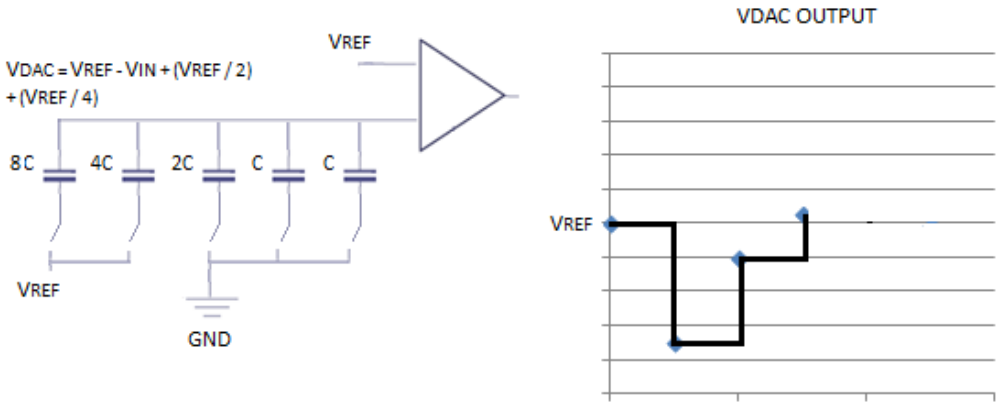

Figure 3.10: Switching Operation Stage 3

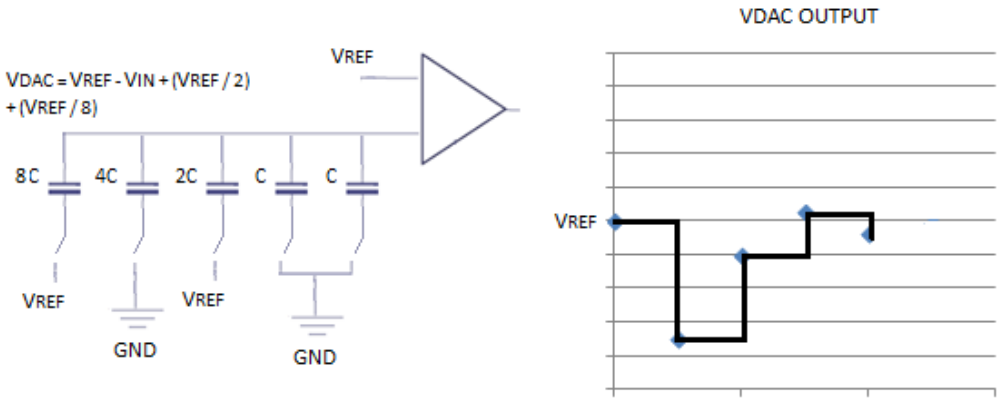

Figure 3.11: Switching Operation Stage 4

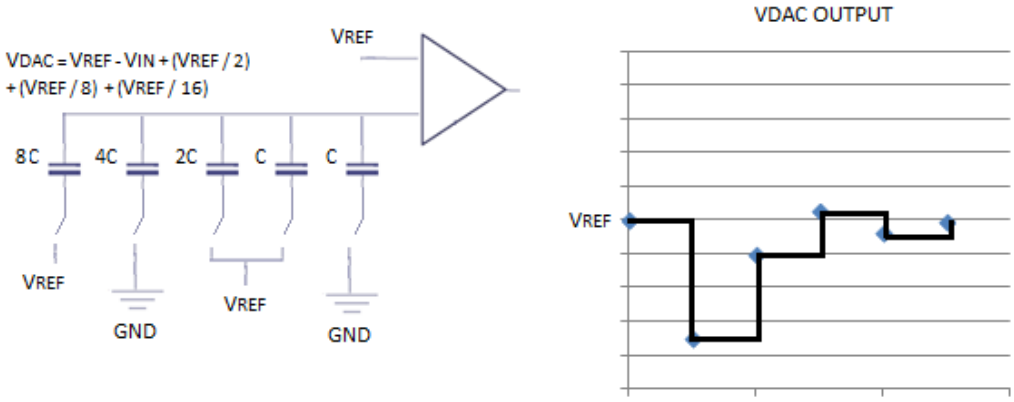

Figure 3.12: Switching Operation Stage 5

The number of iterations of this process scales with the number of bits. The calculations required to design this circuit will be shown in section 3.4.6.

3.2.3 Digital Circuit

The digital circuit is present in the feedback loop as it is required to store the bit values. The overall component used is a binary shift register which controls the configuration of the switches which in turn controls the charge stored in each capacitor in the array. The operation is such that a binary "1" is set at the MSB (most significant bit) first, and all other bits are set to "0". This sets the capacitor array to be charged at half the reference voltage, thus allowing a comparison to the input signal voltage and indicating whether the input is higher or lower. Based on the output of the comparator (discussed in the next section), the MSB register is set to a 1 or 0 and will remain as such for the remainder of the conversion period. The simplest memory register component used is the D flip-flop. The clock signal is also required as an input as it will drive the timing of the registers and the bit conversion comparisons. Figure 3.13 shows the schematic level diagram of the binary shift register for an 8-bit ADC.

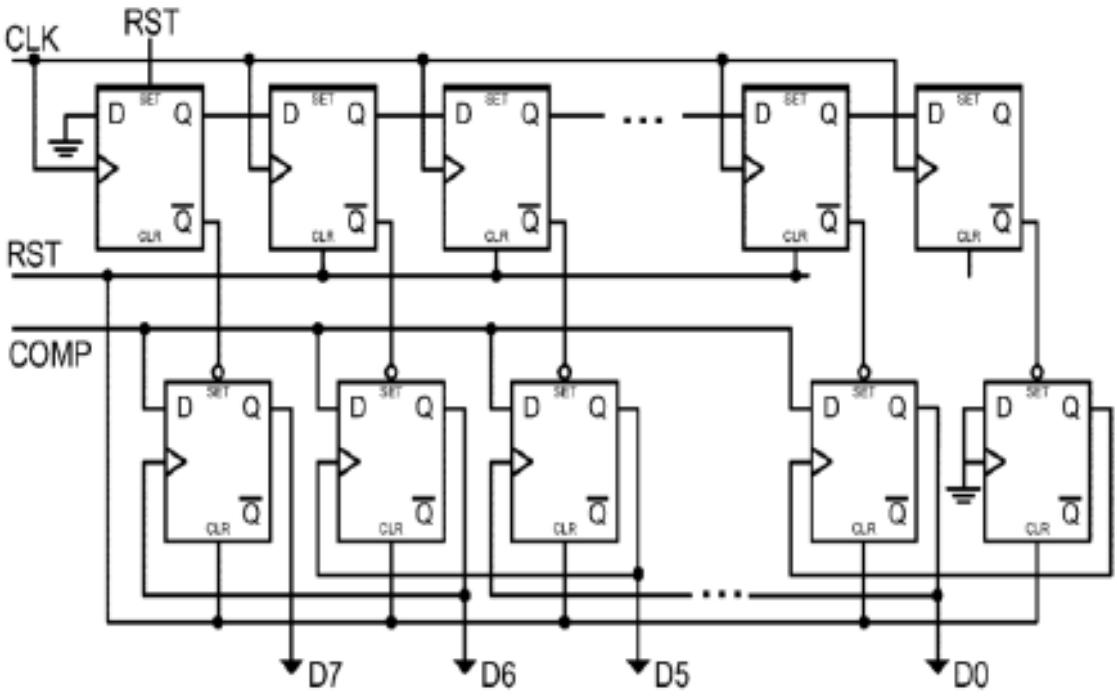

Figure 3.13: 8-bit Binary Shift Register

3.2.4 Comparator

The comparator is the component that will make the decision at each bit conversion as to whether the signal being processed through the ADC is higher or lower than the reference voltage. The comparator will require certain specifications to be met in order to ensure the accuracy and speed of the bit conversion operation. In terms of operation, the comparator needs to be able to take two inputs and based on the delta, drive the output high or low to feed into the digital circuit for processing. That being said, the comparator must have a high gain and low input offset voltage so that very small changes in voltage between the inputs can still be compared with a high accuracy. Noise is also a concern and must be taken into effect for the design. The

comparator design portion of the IC will come at the board level as opposed to the IC level since there were time constraints and a comparator design can be more complex than some other components.

3.3 Voltage ADC Metrics

The following section will describe the process of calculating the parameters that a voltage ADC (VADC) can be designed from. The VADC is simpler to design in comparison to a current ADC, which is why it was chosen to implement the HW portion of the fuel gauging solution. A full fuel gauge solution based on the algorithm in this thesis would require both a voltage and current ADC to properly meet the HW requirements; however, this is beyond the scope of this research project. The design was structured around a 12-bit resolution requirement.

3.3.1 Voltage Range

The range of an ADC refers to the set of input values that can be accurately converted from an analog signal to a digital one. In terms of the VADC, this would require an understanding of the battery being characterized as well as the system design. A lithium ion battery used for low-power electronics will typically have a voltage range between 4.35V and 2.5V when discharging usable current capacity. With that in mind, the system parameters, namely the system cut-off voltage will need to be understood as this will set restrictions on the lower limit of the usable voltage range. Defining the full scale voltage range will affect the later calculations as the resolution, LSB, time constant will be impacted. Even though the required range could only be as high as (4.35V – 2.5V = 1.85V), assuming a worst case full

scale voltage of 2.5V seemed appropriate as it gives room for expansion into future batteries that may have larger voltage range capabilities, as well as system designs that use lower voltages to support operation.

3.3.2 Sampling Frequency

The sampling frequency of the ADC will depend on the application of the system. For most battery-powered mobile electronics platforms, 100kHz could be considered the highest frequency signal as this would also include the filtering of the battery which would attenuate higher frequency signals since the equivalent circuit is essentially a RC low-pass filter (as seen in section 2.1.2). This sample rate is based on the highest frequency of the system load and should be sufficient to maintain the required accuracy. Based on the sample rate discussion in section 3.1.1, the sampling frequency should be at least 2 times the signal frequency, i.e. 200kHz. Thus, based on the requirement of 12-bits, the full conversion must take place within one period, i.e. 5us. Therefore, each bit conversion must happen within ~0.4167us. This translates to an overall clock rate of 2.4MHz. This clock value was adjusted to 2.6MHz for simplifying the design, since 2.6MHz is a more common clock frequency that is used in many lower power electronics IC designs. This also gives some margin in terms of the conversion time.

3.3.3 Resolution and Accuracy

The resolution chosen for this design is 12-bits. This was not arbitrarily chosen, seeing as there is application specific reasoning that was required for the design decision. The first decision that needed to be made was the accuracy of the fuel

gauging solution. Based on the requirements of the system designers, the accuracy required was +/- 0.5%, which is referring to percentage of the SOC. To translate this to a voltage, the smallest voltage drop between 1 percent of an OCV SOC needed to be determined. Based on battery raw data, this was found to be ~2mV. Furthermore, 0.5% would be 1mV accuracy. Using this value, and the full scale voltage range, i.e. 2.5V, the correct bit resolution could be obtained. The calculation below shows the steps required to calculate the minimum required resolution.

Minimum Voltage for 1 Percent OCV delta = 2mV

Accuracy Required = +/- 0.5%

Voltage Accuracy = 2mV/1% * 0.5% = 1mV accuracy

Full Scale Voltage = 2500mV

Minimum # of steps = Full Scale Voltage / Voltage Accuracy = 2500 / 1 = 2500 steps

Table 3.1: Number of Steps in 8-12 Bit ADCs

Bits	Steps
8	256
9	512
10	1024
11	2048
12	4096

Therefore, based on the number of steps available with 12 bits of resolution, the decision was made. The overall accuracy based on having 4096 steps would be ~0.61mV which meets the 1mV requirement.

3.3.4 Specifications

The following details are the consolidated specifications as described in the above chapter.

Table 3.2: 12-Bit Voltage ADC Specifications

Parameter	Value	Units
SOC Accuracy	+/- 0.5	% SOC
Minimum Voltage for 1% SOC	2	mV
Voltage Accuracy	1	mV
Voltage (High)	5	V
Voltage (Low)	2.5	V
Full Scale Voltage Range	2500	mV
Number of Digital Codes	2500	steps
Resolution	12	bits
Largest Signal Input Frequency	100	kHz
Sampling Frequency	200	kHz
Sample + Conversion Period	5	us
Clock Speed	2.6	MHz

Chapter 4

SAR ADC IC Design

The overall IC design of a SAR ADC can be complex and has many integrated components. To lighten the scope of the design, the comparator was removed from the IC design and moved to the PCB board design section seeing as it would have added extra space requirements and complexity from the integrated circuit design and routing perspective. The analog and digital circuit sections remain integrated and their circuit schematic derivation will be described in the following sections.

4.1 Schematic Design

The overall schematic design was straightforward once the different blocks and components were understood. However, the simplest way to tackle the design was to break up the components into modular blocks. Each schematic can be used in higher

level schematics and thus can model the entire system without having hundreds of transistors placed on the same schematic page.

4.1.1 Inverter

The inverter is one of the simplest digital circuits and serves the function of changing a digital input of low or high to a digital output of a high or low, respectively. One of the key considerations to developing the inverter circuit is the sizing of the PMOS and NMOS transistors. The first step is to determine the drive strength differences between the PMOS and NMOS. With the technology parameters given by the design house, this was estimated to be about 3:1 ratio for PMOS:NMOS sizing. The sizing pertains to the width to length ratio. The length of the transistor is ideally maintained at the minimum of the design technology, and seeing as the inverter is one of the fundamental building blocks of the larger circuit components, the smaller the inverter component, the smaller the overall design will be. However, due to design constraints, the length parameter was set to 190nm. The final concern is the overall worst-case delay that the inverter will introduce when switched either to VDD (high) or to GND (low). Figure 4.1 shows the schematic circuit for the inverter. The number next to the transistor indicates the W:L ratio of the transistor with L being 190nm as suggested above.

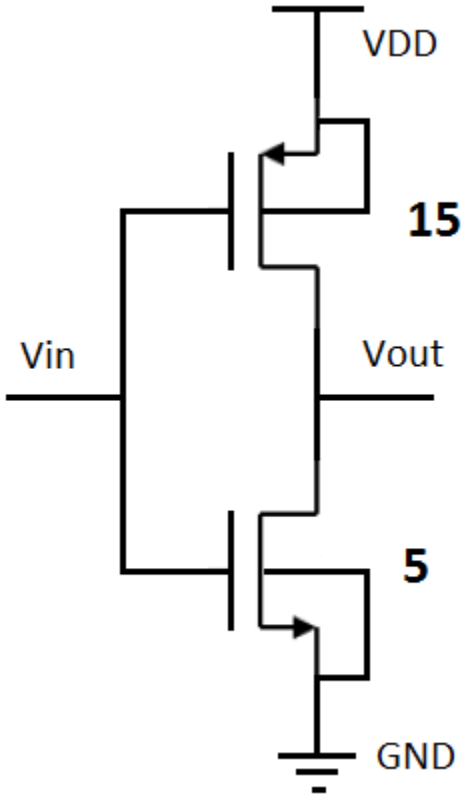

Figure 4.1: Inverter Circuit Schematic

4.1.2 Transmission Gate

The transmission gate is the circuit being used as the switch for the majority of the capacitor arrays. The idea is that it will maintain a low ON resistance and not introduce a lot of delay as to slow down the circuit. Figure 4.2 shows the basic circuit and it can be seen that it uses both a PMOS and NMOS transistor, but not at the same time. The input control signal will be used to turn on either the PMOS or the NMOS depending on the polarity of the signal that is being transmitted. High signals tend to be more strongly driven by PMOS transistors and vice-versa for low

signals and NMOS transistors. The transmission gate also makes use of an inverter component which also needs to be factored into the total delay. Again, sizing the transistors should be done such that it will not impact the overall delay to a point where the bit conversion time will be affected. This will be easier to realize further into the schematic design when the full worst-case circuit delay chain is developed.

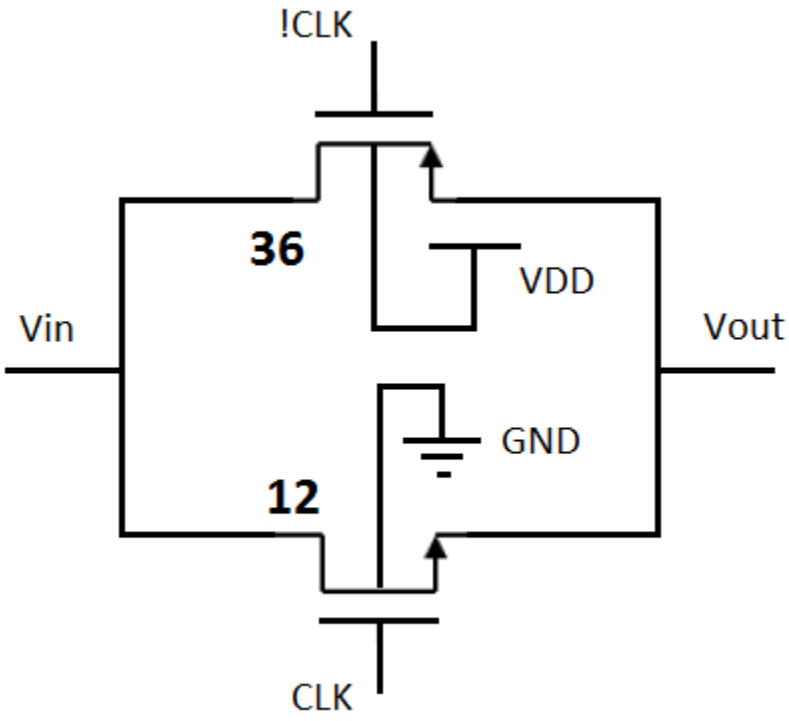

Figure 4.2: Transmission Gate Circuit Schematic

4.1.3 NOR Gate

The NOR gate is based on two fundamental digital circuits, the NOT circuit and the OR gate circuit. The NOT circuit is essentially an inverter as it reverses the output from high to low and low to high depending on the input. The 2-input OR and 2-input NOR circuit truth tables are showcased in the tables below.

Table 4.1: OR Gate Truth Table

Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	1

Table 4.2: NOR Gate Truth Table

Input 1	Input 2	Output
0	0	1
0	1	0
1	0	0
1	1	0

The outputs are straightforward and the circuit implementation is derived below. It can be seen in Figure 4.3 that the number of transistor components used is now at 4, and thus proves further why it is imperative to maintain small sized

transistors for all of the basic circuits. This will be more apparent in the following circuits as they will make use of multiple NOR, transmission gates, and inverters.

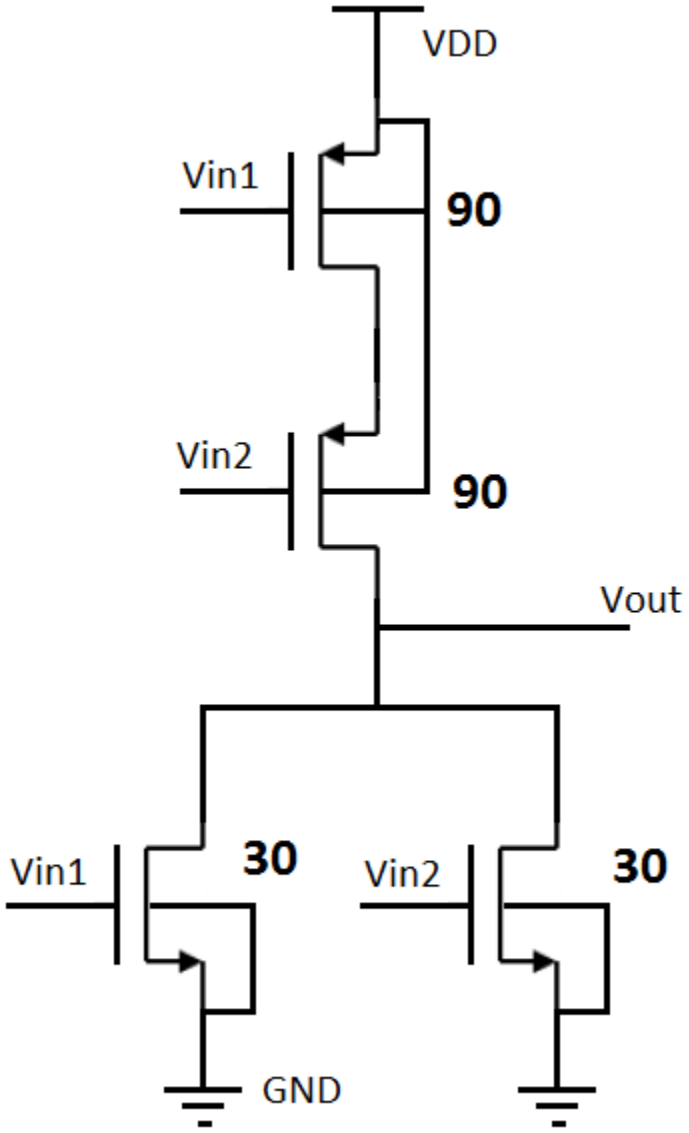

Figure 4.3: NOR Gate Circuit Schematic

4.1.4 D Flip-Flop (DFF)

The D flip-flop is the memory storage component used to maintain each bit during the conversion cycle. The component circuit as seen in Figure 4.4 is made up of NOR gates and inverters. The basic DFF will have 1 input connection, as well as an input clock. A more complex version, like the one used for this design, has a set and reset feature as well. The component symbol looks like the following image in Figure 4.5. The operating principle of the DFF is that the input signal is passed to the output when a rising edge is seen at the clock input. At any other instant, the output will remain static and independent of any variance on the input. The set and reset features add a method to force the output to either a 1 (set) or 0 (reset), regardless of the input signal. Adding multiple DFFs in a specific configuration can produce the binary shift register which is required to create the digital portion of the circuit.

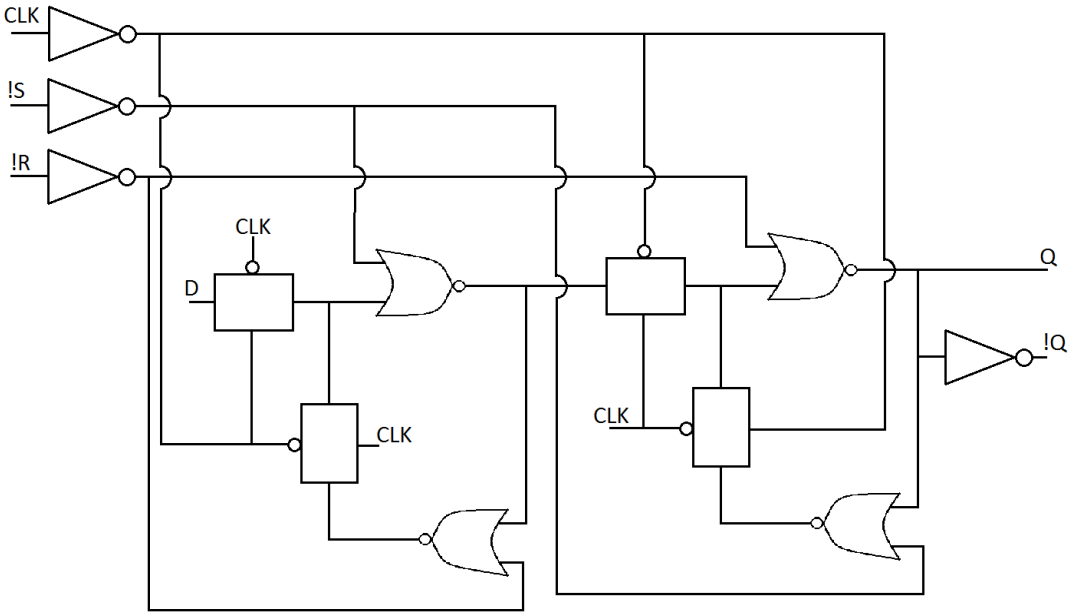

Figure 4.4: DFF Circuit Schematic

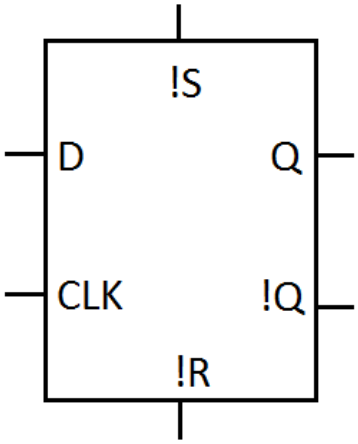

Figure 4.5: DFF Schematic Symbol Diagram

4.1.5 Resistor –Capacitor (RC) Unit Cell

The capacitor array and associated switching circuitry is shown in Figure 4.6. Each capacitor in the array has a value that is a multiple of a base capacitor.

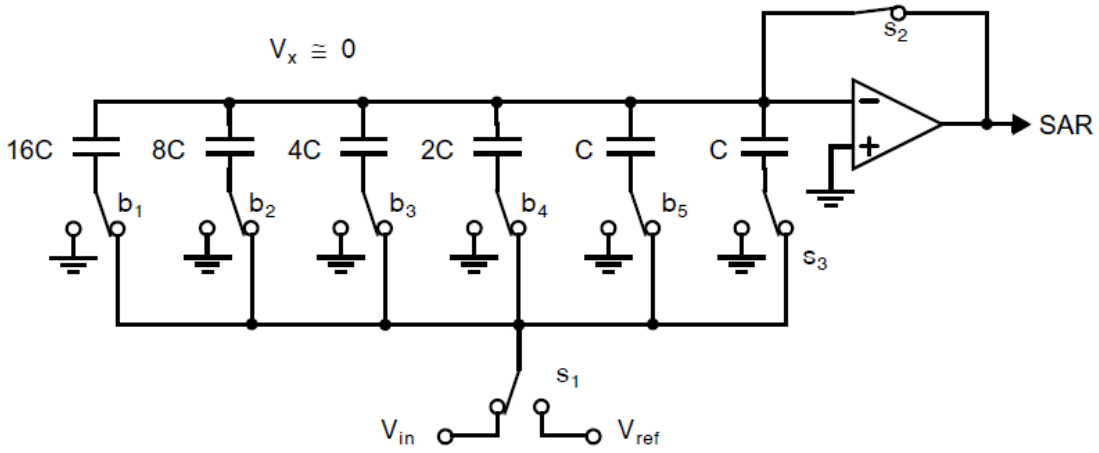

Figure 4.6: 5-Bit Capacitor Array and Switching Circuitry

Thus instead of creating a different switch and capacitor for each string in the array, it made more sense to create a unit cell that could be replicated for each string. The value of the resistor and capacitor was the next step for the circuit design and it needed to be figured out based on the design requirements. As seen in section 3.1.3, noise in resistors is primarily generated through thermal effects. A concept that was not discussed was how to derive the noise element associated with a capacitor. Fortunately, it is a simple concept in that a capacitor alone does not generate any noise of its own [10]. However, the noise from a resistor will couple with the capacitor and will be calculated based on the following formula in Equation 4.1.

$$V_n = kT / C \quad (4.1)$$

Although the noise on the capacitor is derived from the resistor, it is actually independent of the resistor value, such that a capacitor connected in any practical circuit will have this noise associated with it, and this is true because any conductor or wire that connects a capacitor will have some resistance. Using this formula in combination with the SNR formula from section 3.1.4, the maximum allowable noise can be used to determine the worst case capacitor value. After the capacitor value is set, then using the bit conversion period derived in section 3.2.2, the resistance value can be calculated. Finally, using that resistance value, the switching FET can be sized to align with this value.

The unit cell incorporates a number of switching options based on whether the input signal is VDD, GND, or the input signal itself. Figure 4.7 shows the circuit schematic for the RC unit cell.

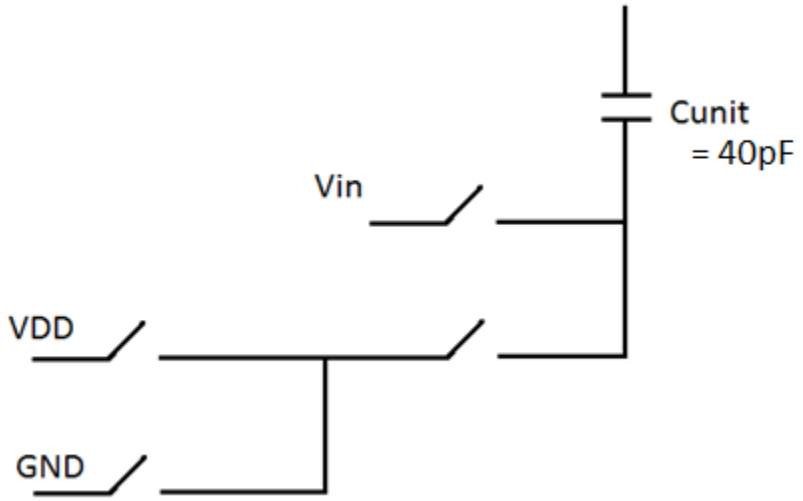

Figure 4.7: RC Unit Cell Circuit Schematic

4.1.6 Analog Circuit

The analog circuit combines the sample and hold input circuit, the capacitor DAC, and the output to the comparator. For a 12-bit ADC, the amount of required RC unit cells is proportional to the number of bits. In order to reduce the total number of capacitors in the circuit, a capacitor bank splitting technique was used. Figure 4.8 shows the basic concept for a 4-bit capacitor array and it is clear that the number of capacitors is greatly reduced. For a 12-bit array, this concept can be used to split the array into 2 sections or even 4 sections. For simplicity, this design breaks the array into 2x 6-bit halves.

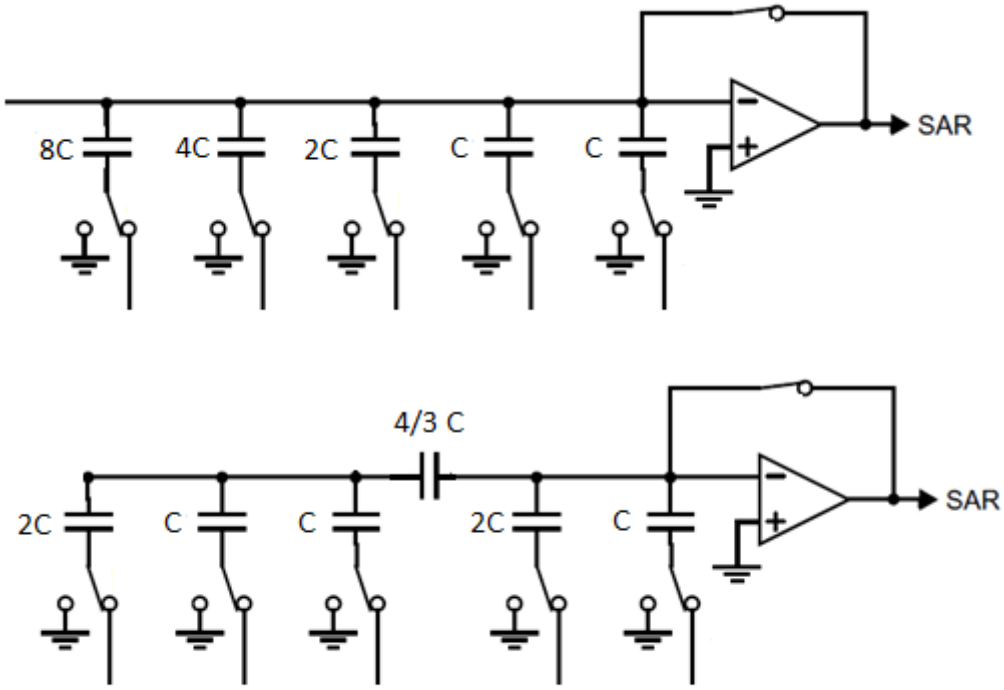

Figure 4.8: 4-Bit Split Capacitor Array Example Circuit

4.1.7 Digital Circuit

The digital circuit takes the comparator output and translates it into a bit pattern such that it will represent the analog value. As seen in section 3.3.3, Figure 3.14 shows the schematic circuit diagram of the binary shift register that stores the bit information. The circuit makes use of a number of D flip-flops chained together with some common inputs and then an output for each digital bit. Each digital output gets fed back into the switching circuitry of the capacitor array for each consecutive bit conversion cycle.

This was simpler to design relative to the analog circuit since this circuit is mostly made up of pre-designed component blocks. The main evaluation that was needed at the schematic simulation level was to ensure that the circuit was operationally functional. The simulation details will be provided in Chapter 5.

4.2 Layout Design

The layout design is similar to the schematic design in that it follows a modular block approach. Each single component was designed individually which laid the ground work for the more complicated block designs. The complication from a layout perspective was of course the routing and space limitations. The following sections will uncover the design aspects related to each of the blocks as well as the initial planning phase that was used to ensure a smoother design process.

4.2.1 Floor Planning

At a high level, the floor planning was approached from a top-down perspective. The sizes of components were estimated based on some quick preliminary design decisions. The overall design was commissioned to fit within a 1mm x 1mm limitation. This was to include the pad layout, analog and digital circuitry as well as the ESD circuits. The overall floor plan was an estimate and became an iterative process as the layout design progressed. Once some of the initial component blocks were laid out, it became easier to determine whether they would fit within the overall restriction once they were scaled up to the required amount of circuits. The layout also had to be thought of from a 3-dimensional view since multiple metal layers were available for the design. Restrictions also needed to be set in terms of the layers used

such that there would be budgeted space and layers for wiring connections between blocks.

4.2.2 Capacitor Array Planning

The capacitor array needed to be planned as well. This was required for a couple reasons. Firstly, the amount of space required for each capacitor would limit the size based on how many had to be fit into the circuit area. Second and more importantly, the fabrication design process variations needed to be mitigated such that the placement of capacitors wouldn't affect the overall output once the device was fully functional. Process variations can affect measurement results since the process is not guaranteed to be 100% uniform. Knowledge of this helped in setting the priority level of having a well planned out capacitor layout. Figure 4.9 shows the technique used to mitigate the process variations.

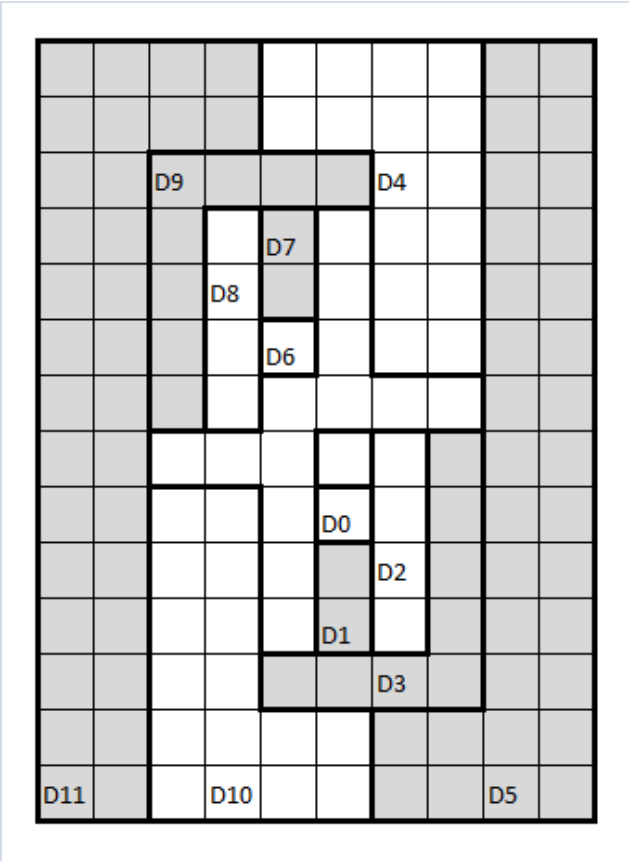

Figure 4.9: 12-Bit Capacitor Array Floor Plan

4.2.3 Pad Layout

The pad layout was fairly straightforward in terms of placement. The overall die package was based on the number of pads that were required for output pins. One of the more common packages was the DIP-28, which has 7 pads on each of the 4 outside limits of the die. Each pad would then be connected internally through bond wires to each of the pins available on the external package, such that measurements and testing can be undertaken when the design is fabricated. Unfortunately, the DIP28 package was not available when the fabrication was being completed so a

CQFP44 pin package was used instead. The wire bonding was mapped as shown in Figure 4.10. Any unused pads were left open, and were not used when designing the test board.

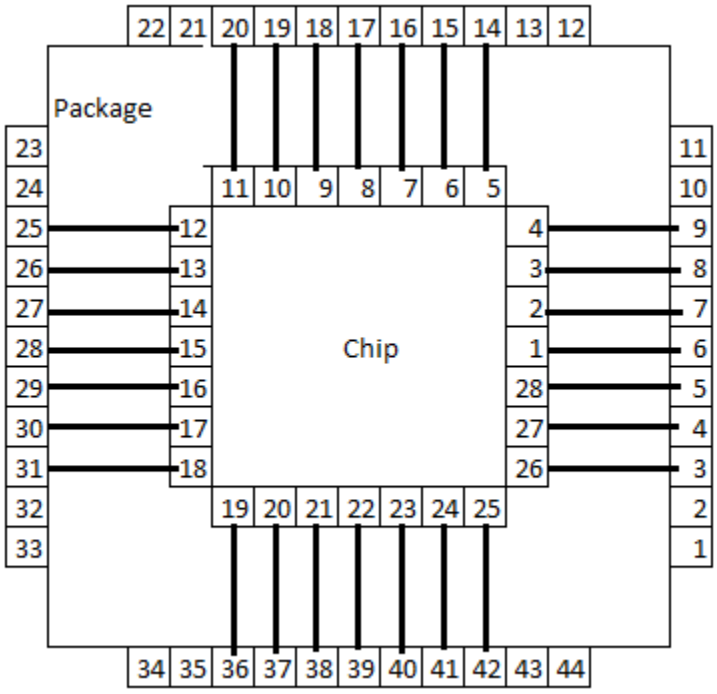

Figure 4.10: CQFP44 Wire Bond Mapping

4.2.4 Overall Layout and Fabrication

The design was approved by CMC Microsystems and fabricated in the 130nm process. The space commissioned for the design was 1mm x 1mm. The IC layout followed the same approach as the schematic in that hierarchical levels were created to integrate modular blocks into the final design. Figure 4.11 shows the overall IC

layout including the pad layouts, analog and digital circuitry and ESD circuits. The ESD circuits were necessary to prevent the device from being damaged by static sources when being handled and/or tested. The routing was completed with 3 thin metal layers and 2 thick metal layers. VDD and GND were allocated as much metal as possible within the constraints of the design to minimize the effects of different voltage levels around the IC. Routing was not overly complicated and the space constraints were not a huge concern either, which allowed for routing thicknesses to be maximized in most cases. The important consideration was to not have the routing limit the design in terms of adding parasitic resistance or capacitance. Overall test plan and PCB board design are discussed in the next chapter in order to ensure a suitable verification plan to test the IC.

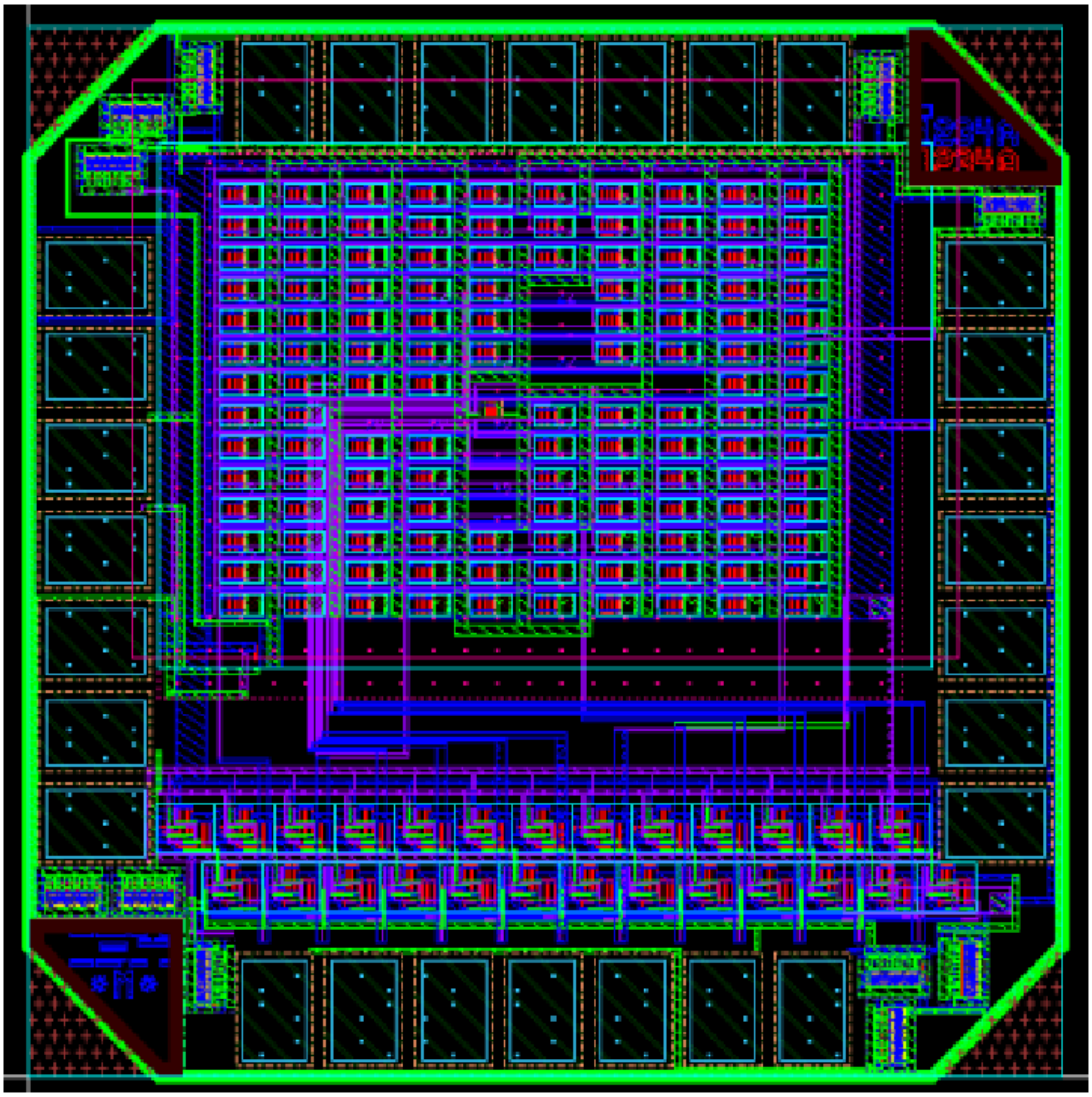

Figure 4.11: Complete 12-Bit ADC IC Layout

Chapter 5

Simulation and Testing Details

The following chapter discusses the requirements for simulation and verification testing surrounding the fuel gauge design. Some SW design simulations were already provided and described in section 2.4. These were performed in Matlab in the theoretical simulation domain. The following design simulations will focus more on the HW design in terms of the IC itself. Once the design has been simulated and the results are sufficient to prove that the design will have a high chance of operating correctly, the IC is submitted for fabrication and the next phase of the design is commenced. In order to properly design a test board for verification, a test plan should be designed such that the testing requirements are identified. Once these requirements are clear, the PCB board can be designed such that it meets the testing requirements.

The test board design is a critical requirement for verification as it will allow for a real-world implementation and gives the designer a practical way of measuring the performance of the design.

5.1 IC Design Simulations

The IC design simulations were taking place throughout the complete design phase. The purpose being twofold, firstly, so that the functional operation is verified, and secondly, so that the design is meeting the requirements based on specific inputs and parameters set in the system. Simulations were performed at the schematic stage, layout stage and after the parasitic components were extracted.

Functional operation was verified at each of the hierarchical levels. To be more specific, the simulations were broken up as follows:

1. Functional Simulations:
    a. Level 1
        i. Inverter
        ii. Transmission Gate
        iii. NOR Gate
    b. Level 2
        i. DFF
        ii. RC Unit Cell
    c. Level 3
        i. Analog Circuit
        ii. Digital Circuit
    d. Level 4
        i. Complete 12-Bit ADC

The functional operation is important at each stage and especially starting at Level 1, because if something was not working, it would enable a shorter debugging process. Using the inverter as an example, with a clear understanding of the inverter operation, simple tests can be performed to complete the verification. The following tests were completed with the corresponding outputs:

Test 1:

Input = High Voltage (VDD)

Expected Output = Low Voltage (GND)

This test is required for a very basic verification of the correct output level.

Test 2:

Input = Low Voltage (GND)

Expected Output = High Voltage (VDD)

This test is required for a very basic verification of the correct output level.

Test 3:

Input = Small Incremental Voltage Sweep (GND to VDD and VDD to GND with 1% voltage increments)

Expected Output = Consistent Transition (VDD to GND and GND to VDD)

This test is required to verify at which point do the transistors drive the signal low or high as this may affect the output transitions when integrating into higher level blocks.

Test 4:

Input = Fast Transient (GND to VDD and VDD to GND)

Expected Output = Consistent Transition (VDD to GND and GND to VDD)

This test is required to verify fast operation and to characterize the delay.

Using these tests for an inverter would be able to properly identify whether the design was successful. This set of tests would be repeated at the schematic, layout and parasitic layout stages to ensure consistency and validity of the design. For each of the remaining blocks, more complex tests would be added to this list to verify functionality and would be performed at each level in consecutive order to ensure that debugging time would be minimal.

The functional tests could be performed at any input value such that the operation itself was verified, meaning that the most stringent clock speed or period was not used. Moving forward to the performance tests, the required parameters would need to be used to ensure that the design criteria was being met. The reason this wasn't utilized in the first round of tests, was because it was more useful in terms of a systematic approach in creating a successful design. If the design parameters were used from the start of the simulations, it would be more difficult to ascertain whether an incorrect result was because of the designed components, or because there was a circuit implementation issue. Once the functionality is verified, then the design components (i.e. transistor widths) could be optimized to produce the best performance.

5.2 HW Verification Test Plan

The HW verification test plan is defined by the requirements of the design. It is important to start a design by understanding high-level features and use cases and then defining the requirements based on these. Then an appropriate design implementation can be selected. The test plan below should be used to verify the majority of requirements.

5.2.1 Use Case Scenarios

In terms of defining the use cases, the requirements must be reviewed to ensure appropriate tests can be designed to cover each of the scenarios. A number of tests need to be performed, similar to the matlab simulations that were performed at the preliminary design stage. They were the following:

1. Initial Bring-Up Verification
2. Functional Operation Measurements
3. Optimized Performance Measurements
4. Power Consumption Measurements

Starting with the initial chip bring-up, is the basic testing to ensure that the design powers up and that there is a stable voltages at the output nodes. Once this is performed, functional operation measurements can be completed. This covers the range of testing that includes input voltage variations to verify the entire range of 12-bit ADC values. The purpose of this test would be to ensure that there are no missing digital codes, as this would be problematic. An input voltage sweep could also be used to verify accuracy in terms of the voltage outputs. After testing the functional operation, the design can be tested at extreme limits to understand the upper and

lower bounds on some of the requirements. For example, the input clock frequency can be increased from the specified value until chip doesn't perform as expected, or starts outputting erroneous results. Similar testing can be performed while changing the voltage reference value. Last and possibly most important, the power consumption needs to be quantified. The power would want to be tested based on varying the input voltage, reference voltage, and clock frequency.

5.3 Test Board Design

The test board design is fairly straightforward from a design perspective. The overall component count is minimal, the power is low so there are no requirements for high load traces, and the signals would not be considered high frequency signals, so trace lengths are also not a concern. The following sections describe the main design contributors and the decision process that was implemented.

5.3.1 Comparator

The comparator is the one critical component that was left out of the IC design due to the reduced scope. It was more imperative to prove out the operational functionality of the ADC vs. designing a full IC from scratch. It also made more sense to focus time and effort into the overall solution in terms of the SW algorithm in combination with the HW ADC. Designing a comparator relative to the other components of the ADC would be much more time-consuming and thus was left to the test board design.

That being said, the comparator component was chosen based on the ability to not gate the rise and fall time of the IC design. This value is called the

propogation delay. As was seen in the earlier design section, each bit conversion needed to finish within < 400ns. Therefore, choosing a part that was well above this value in terms of speed was a good idea. The TS3022IDT part from STMicroelectronics fit this specification. The other important factors to consider were the input voltage, which was in the range of 1.8-5V. The input bias and quiescent currents were not so much of a concern at this point because these are external to the chip. The size of the part was also not critical as the test board was not meant to be designed for any size restriction.

5.3.2 External Component Selection

There were very few external components required for this design. The majority were bypass capacitors. 3 capacitors were added for each IC that had a VDD pin, i.e. the ADC IC and the comparator. These 6 capacitors varied in value and dimension, such that they could easily be swapped out for other parts in the case of a more suitable part becoming available.

Some connectors were also added such that probing and adding supply voltages and values would be a simple exercise. Table 5.1 provides the mapping of component to signal and/or pin.

Table 5.1: Component / Signal Nets

Designator	Component	Signal Net Name
J1	ADC IC	n/a
J2	2-Pin Connector	Vin_CLK
J3	2-Pin Connector	Vin
J4	2-Pin Connector	GND
J5	2-Pin Connector	GND
J6	2-Pin Connector	!Reset
J7	2-Pin Connector	CLK
J8	2-Pin Connector	Vnode_Gnd
J9	Comparator	n/a
J10	2-Pin Connector	VDD
C1	Bypass Capacitor	VDD
C2	Bypass Capacitor	VDD
C3	Bypass Capacitor	VDD
C4	Bypass Capacitor	VDD
C5	Bypass Capacitor	VDD
C6	Bypass Capacitor	VDD

5.3.3 Schematic Design

The schematic design was just a matter of connecting the chosen components in such a way that the necessary pins could be accessed, and that the pcb layout could be mapped to it. As seen in Figure 5.1, the design is fairly simple.

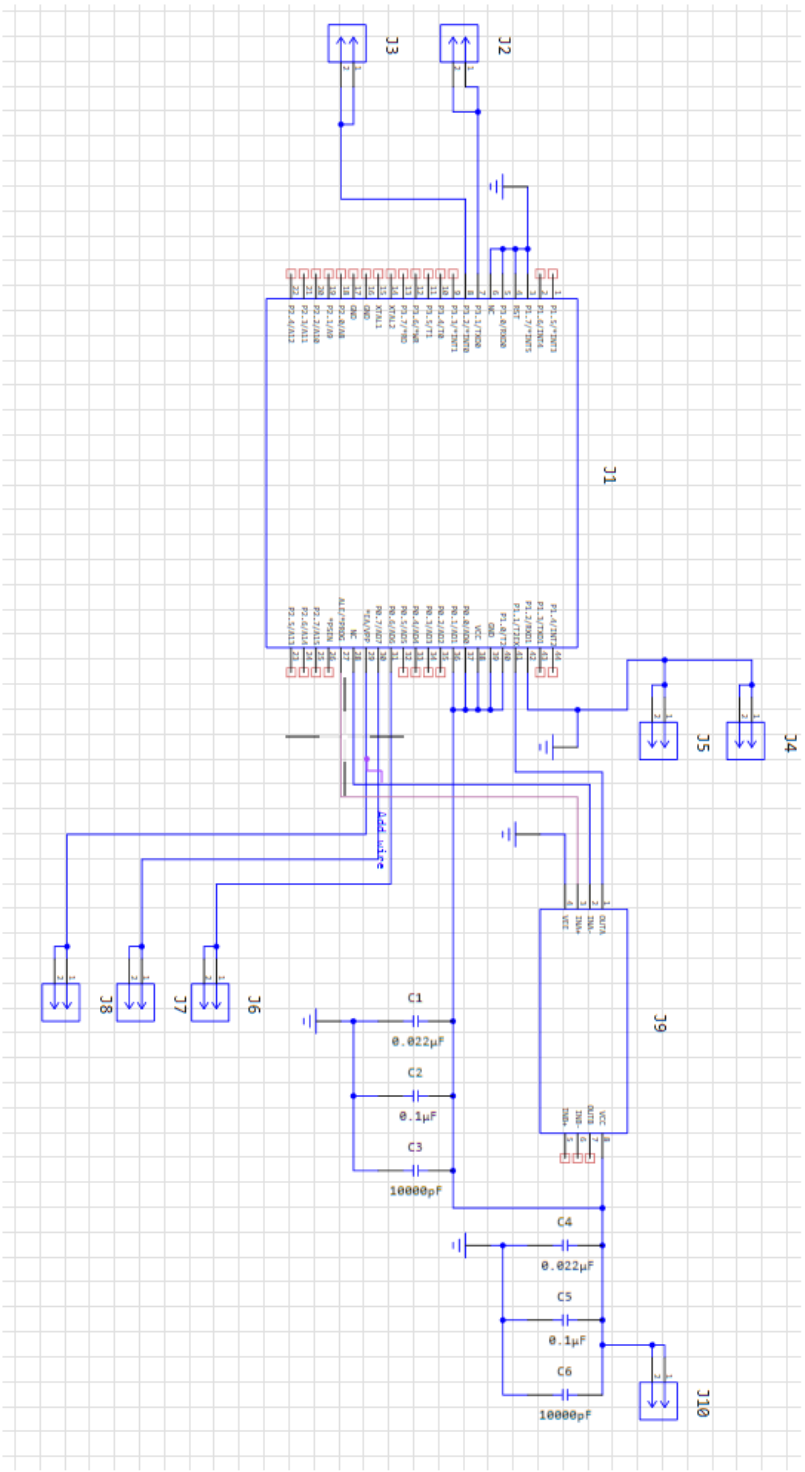

Figure 5.1: Test Board Schematic Design

5.3.4 PCB Component Placement and Routing

Once the schematic design is reviewed and approved, the PCB layout design can be started. The first step is to identify the placement of the parts. Since there are very few parts and board space is not critical, the spacing between parts can be selected based on ease of use versus sizing constraints. From practical experience, fitting too many small connectors close to each other can be problematic when connecting signal probes. The more space between them, the easier the actual testing will proceed. With a simple design, all components can be placed on a single side of the board.

The critical components for placement are the bypass capacitors. The closer the capacitors are to the pins of the chip, the better opportunity there is for filtering out higher frequency signals that could couple into the inputs and affect the measurements.

Routing is another simple step. The first thing to determine is the number of layers required in the board. For most simple designs, 2 layers is sufficient. When routing high power signals, an increase in signal trace width will improve performance as there will be less resistance between the incoming signal at the connector, and the resulting signal after passing through the trace to the device pin. As mentioned previously, based on the lower power requirements, this shouldn't be a concern. All other traces can be routed systematically, and if required, can be passed through plated vias to the 2^{nd} layer to avoid crossing two different signal paths. Figures 5.2 and 5.3 show the component placement and routing of both side of the board.

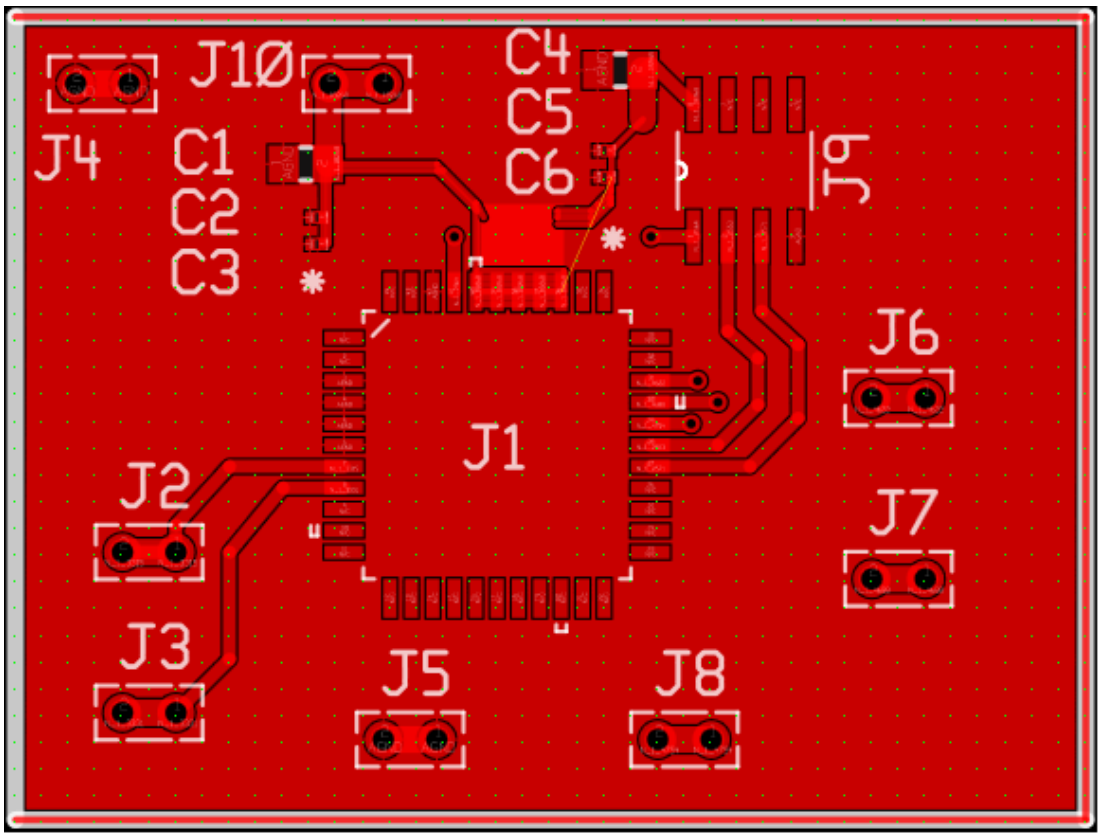

Figure 5.2: Test Board Layout Top Layer

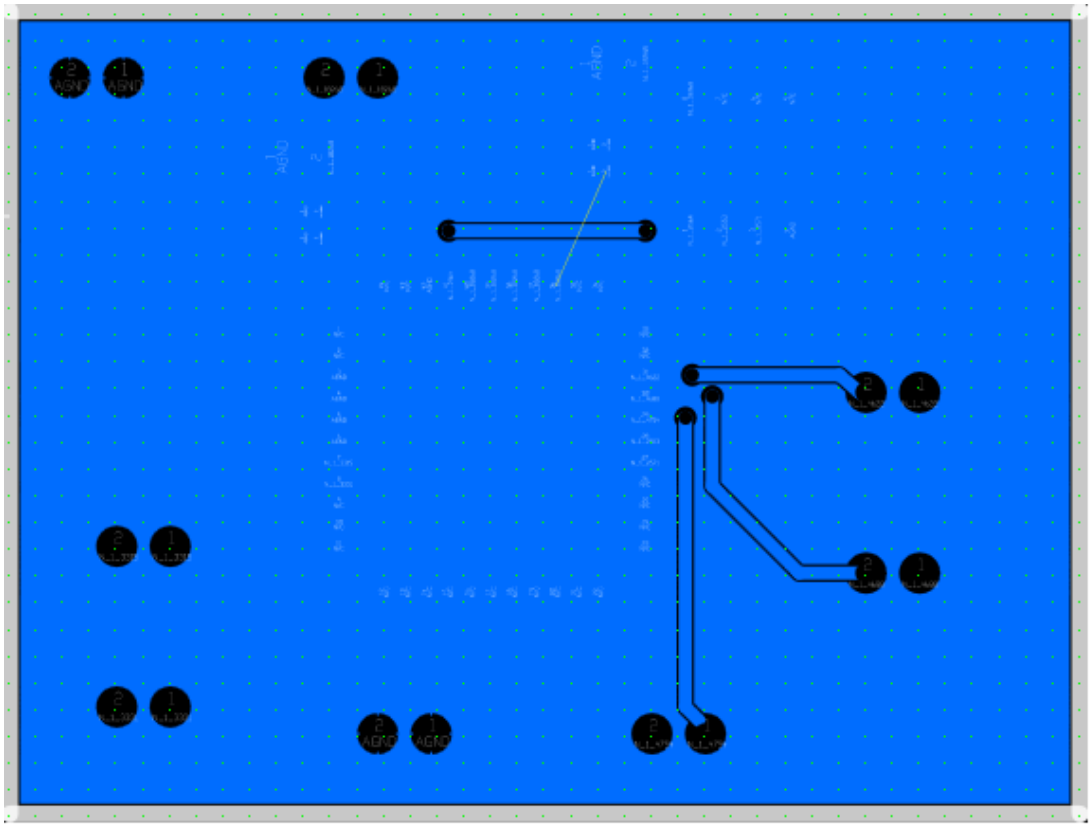

Figure 5.3: Test Board Layout Bottom Layer

5.4 Testing Next Steps

Unfortunately, due to time constraints, and a mix-up with the fabrication plant, the CQFP44 pin packaged parts were not available for testing before the submission of this thesis. However, based on the verification test plan and the created test board design, the chip will be able to be tested in the future.

Chapter 6

Summary and Future Work

When designing a fuel gauge solution, it is important to understand the specifications and defined requirements. In terms of HW, these are based on the possible system loads, the battery type, expected usage, the battery lifetime per cycle, the expected total number of cycles and the battery operating conditions in terms of temperature. Once these factors can be identified, then the overall architecture can be selected and the ADC parameters can be defined. These will also need to be defined in conjunction with the SW requirements, which can be defined based on the projected user experience. This essentially boils down to the accuracy of the reported battery capacity. Once this value is understood, the ADC accuracy can be defined and the SW algorithm can be created to ensure that this requirement is met.

Having this high-level understanding of the fuel gauge design is important as it laid the background for Chapters 2-5 which went into detail about the overall

design solution. In Chapter 2 the battery type and HW methods were explained to give context into what is required from a HW perspective. The necessary variables and calculations were also provided from a SW perspective to give a better understanding of the algorithm. The main parameters that needed to be collected were the battery terminal voltage, battery current and temperature. The rest of the parameters such as aging, i.e. cycle count, and ESR were inherently calculated based on battery characterization data and the state of the battery in terms of charging and discharging.

Chapter 3 went into details of the ADC architecture and what made the SAR ADC an appropriate solution for this application. Design parameters and calculations were explained and it was seen that a 12-bit SAR ADC could meet the requirements in terms of speed and accuracy.

Chapter 4 described the IC design and how the SAR ADC was implemented in a small 1mm x 1mm die. Based on timelines and overall scope, it made sense to remove the comparator from the IC design and implement it through an external component in the test board design.

Chapter 5 showcased the IC design simulations and the process required to ensure proper functionality and performance metrics. The HW verification test plan was also identified and outlined in terms of what needed to be validated for the chip to be deemed successful. It also gave details of the test board design and which design parameters needed to be accounted for.

Overall, the purpose of the thesis was to ensure that the designed solution was a valid fit for the requirements. In industry, it is important to have clearly defined requirements and metrics to determine whether they are being met. In terms of this design, the combination of the HW and SW components was critical in achieving a positive user experience which is the major point of the fuel gauge as an electronic

component. When electronics companies are deciding what their next product will be, it is important for them to understand what the customer wants from that product. A positive user experience is almost always a necessity. Having an accurate fuel gauge can help tremendously in this area as users usually want to know how much battery they have left. They also are interested in ensuring that they can use their devices as much as they would like to without having it impact their behaviour, especially in terms of re-routing their lives to find a charger. Power is a critical component in most wearable and mobile applications, and keeping track of the available power (from a battery) is an important feature.

In terms of future work, it would be useful to continue with the verification of the fabricated IC. Due to time constraints, this was not achieved, and could be critical to determine whether the design was successful or whether iteration would be required to solve any issues in terms of accuracy or functionality. It would also be useful to implement the SW algorithm into an existing design to better understand the impacts of different operating conditions especially temperature, aging, and depth of discharge. The complex considerations section (2.3.8) touched on a few points that could be added to the algorithm such as user-learning. Characterizing user data into usable metrics for reporting battery capacity could be a huge improvement to the way the user responds to notifications from the fuel gauge. Further work could definitely add value to this research and possibly allow for new insights for designers as they develop newer technology with tighter constraints on power.

Appendix A

The fuel gauge algorithm system block diagram is shown in Figure A.1.

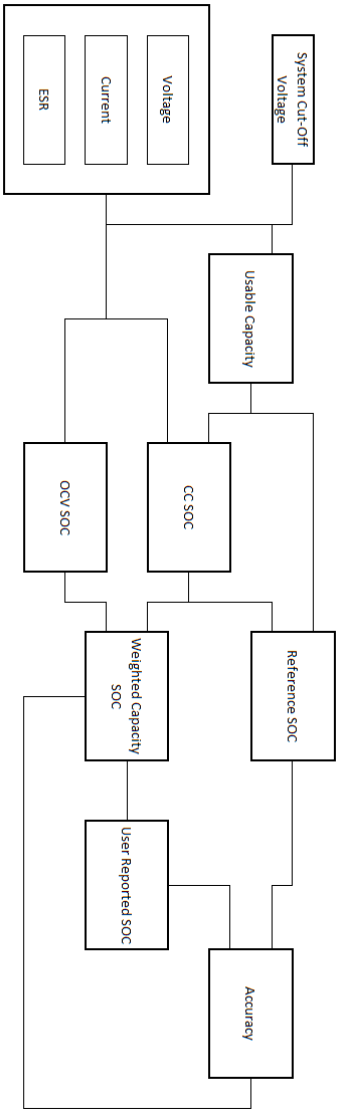

Figure A.1: Fuel Gauge Algorithm System Block Diagram

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